



SANYO Semiconductors

DATA SHEET

LA5315M — Monolithic Linear IC For LCD Use Variable Divided Voltage Generator

Overview

The LA5315M is a variable divided voltage generator IC for multiple drive of LCD matrix.

Features

- Power supply for variable bias LCD drive (1/5 to 1/13 bias available by internal resistances).
- 5 voltage outputs.
- Low current drain (1.5mA max).
- Miniflat package.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$	GND- V_{CC}	-35 to 0	V
Maximum output current	$I_{OUT\ max}$	V1, V2, V3, V4, V5	15	mA
Allowable power dissipation	$P_d\ max$		370	mW
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

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51408 MS PC/31500TN (KT)/9279TA TS No.3246-1/6

LA5315M

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	$\text{GND}-V_{CC}$: (When $V_1 > -1\text{V}$, I_{IN} is needed.)*	-30 to -10	V
Recommended input voltage	V_{REF}	$\text{GND}-V_{REF}$: $V_{REF} \geq V_{CC}$ *	-30 to -6	V
Recommended input current	I_{IN}	V_{IN} : $V_1 > -1\text{V}$, current source of I_{IN} : 1V or greater relative to GND	0.2 to 3	mA
Recommended output current	I_{OUT1}	V_1	-0.1 to +5	mA
	$I_{OUT2, 3}$	V_2, V_3	-5 to +5	mA
	$I_{OUT4, 5}$	V_4, V_5	-10 to +0.1	mA

note * Set V_{CC} , V_{REF} so that $|V_2|$, $|V_{CC}-V_5|$ become 1V or greater.

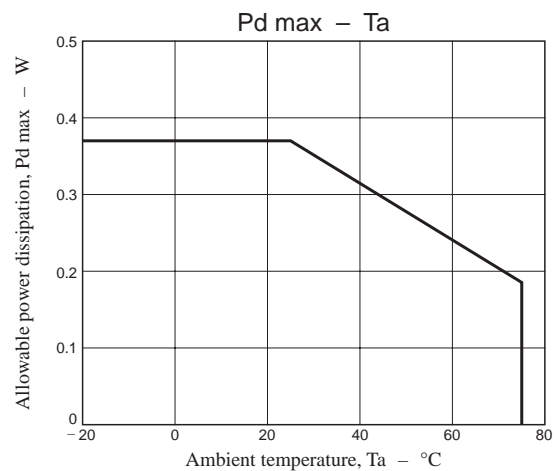
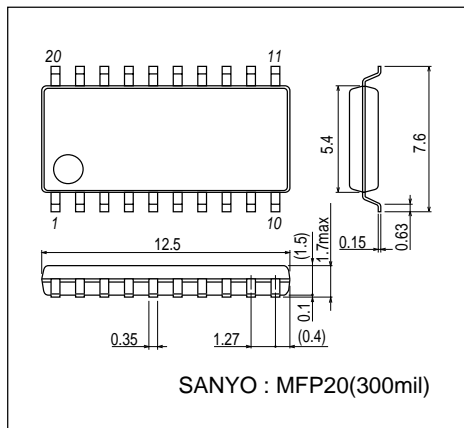
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = -16\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	$V_{IN}, \text{GND}-V_{CC}, V_{REF} : V_{CC} = V_{REF} = -16\text{V}$, $V_{IN} = \text{GND}, R_X = 5\text{R}$			1.5	mA
Output voltage ratio 1	R_{a1}	V_2/V_1	1.96	2.00	2.04	
Output voltage ratio 2	R_{a2}	$(V_5-V_3)/(V_5-V_4)$	1.96 2.00 2.04 8.73 9.00 9.27 4.37 4.50 4.63 4.37 4.50 4.63 8.73 9.00 9.27	2.00 2.00 2.04 9.00 9.00 9.27 4.50 4.50 4.63 4.50 4.50 4.63 9.00 9.00 9.27	2.04 2.04 9.27 4.63 4.63 9.27	
Output voltage ratio 3	R_{b1}	V_5/V_1				
Output voltage ratio 4	R_{b2}	V_5/V_2				
Output voltage ratio 5	R_{b3}	$V_5/(V_5-V_3)$				
Output voltage ratio 6	R_{b4}	$V_5/(V_5-V_4)$				
Internal resistance ratio 1	4R	$V_{IN3}-R_X1$				
Internal resistance ratio 2	5R	$V_{IN3}-R_X2$			5	
Internal resistance ratio 3	6R	$V_{IN3}-R_X3$			6	
Internal resistance ratio 4	7R	$V_{IN3}-R_X4$			7	
Internal resistance ratio 5	8R	$V_{IN3}-R_X5$			8	
Internal resistance ratio 6	9R	$V_{IN3}-R_X6$			9	
Resistance	R	$R_{X1}-R_{X2}$: R value when 0.5V is applied across pins 5 and 6		20		k Ω
Load regulation 1	ΔV_1	$V_1 : +100\mu\text{A} < I_{OUT1} < +5\text{mA}$			20	mV
Load regulation 2	ΔV_2	$V_2 : +100\mu\text{A} < I_{OUT2} < +5\text{mA}$			20	mV
Load regulation 3	ΔV_3	$V_3 : +100\mu\text{A} < I_{OUT3} < +5\text{mA}$			20	mV
Load regulation 4	$-\Delta V_2$	$V_2 : -5\text{mA} < I_{OUT2} < -100\mu\text{A}$			20	mV
Load regulation 5	$-\Delta V_3$	$V_3 : -5\text{mA} < I_{OUT3} < -100\mu\text{A}$			20	mV
Load regulation 6	$-\Delta V_4$	$V_4 : -10\text{mA} < I_{OUT4} < -100\mu\text{A}$			20	mV
Load regulation 7	$-\Delta V_5$	$V_5 : -10\text{mA} < I_{OUT5} < -100\mu\text{A}$			20	mV

Package Dimensions

unit : mm (typ)

3036C



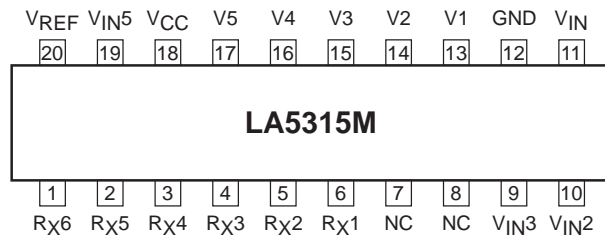
LA5315M

Pin Functions

Pin No.	Pin Name	Description	Remarks
1	R _X 6	R _X pin	Pin 10 shorted R _X = 9R
2	R _X 5	R _X pin	Pin 10 shorted R _X = 8R
3	R _X 4	R _X pin	Pin 10 shorted R _X = 7R
4	R _X 3	R _X pin	Pin 10 shorted R _X = 6R
5	R _X 2	R _X pin	Pin 10 shorted R _X = 5R
6	R _X 1	R _X pin	Pin 10 shorted R _X = 4R
7		NC	
8		NC	
9	V _{IN} 3	V3 input	
10	V _{IN} 2	V2 input	
11	V _{IN}	V1 supply (+ supply)	When V1 > -1.0V, V _{IN} is applied. When V1 < -1.0V, this pin is shorted to GND.
12	GND	GND	
13	V1	V1 output	
14	V2	V2 output	
15	V3	V3 output	
16	V4	V4 output	
17	V5	V5 output	
18	V _{CC}	V _{CC} supply (- supply)	
19	V _{IN} 5	V5 input	
20	V _{REF}	V _{REF} supply (- supply)	

Note) Do not use the NC pin.

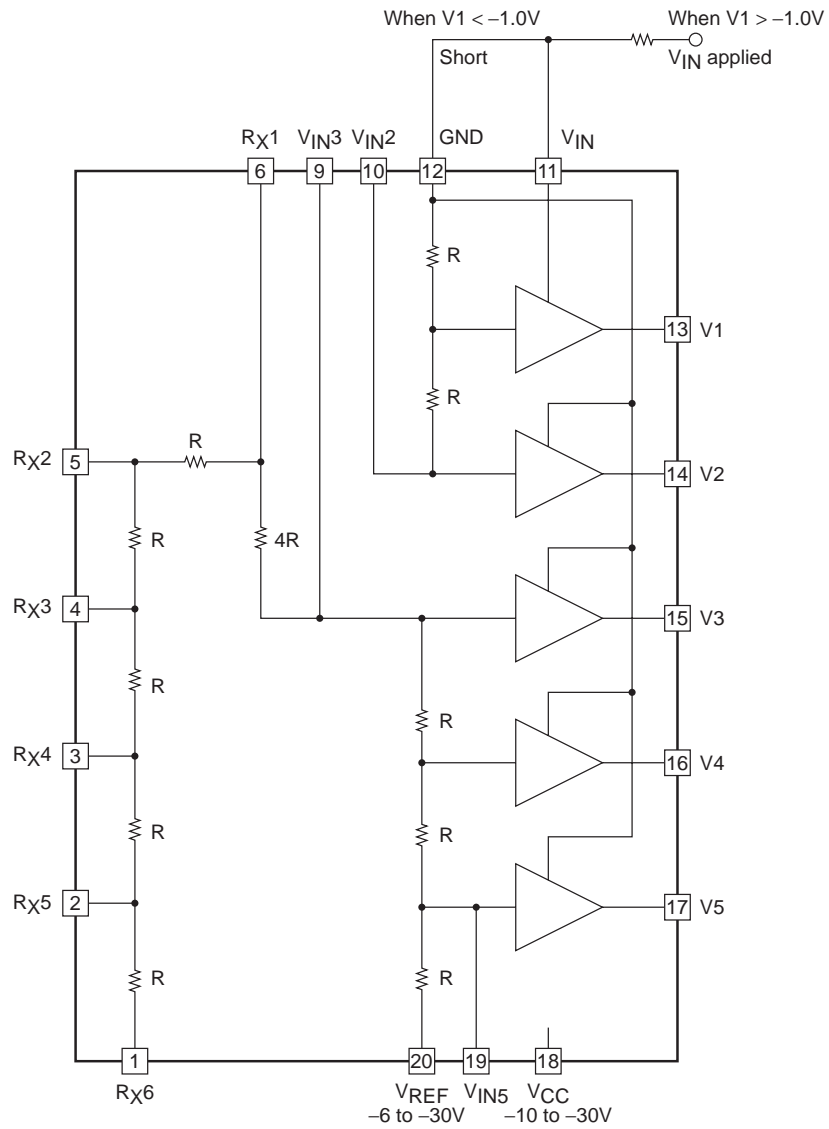
Pin Assingment



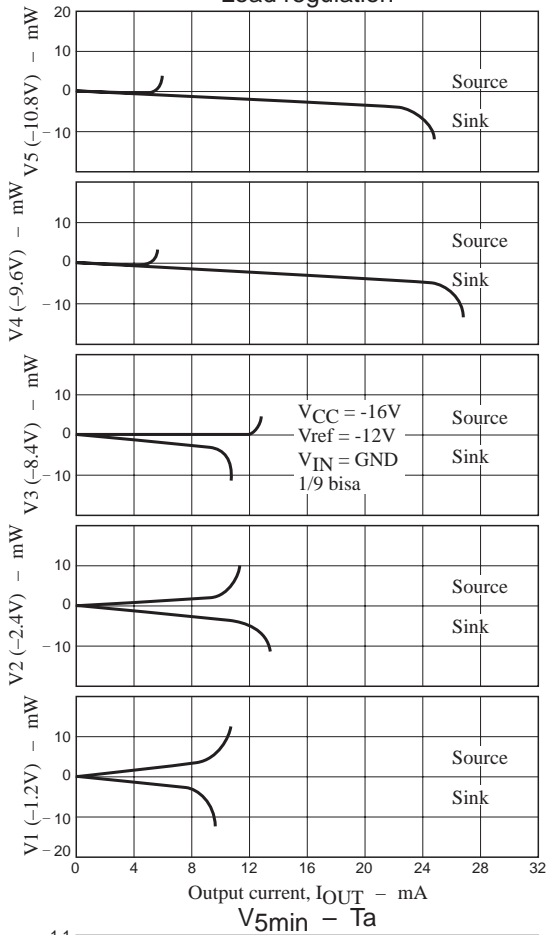
Top view

LA5315M

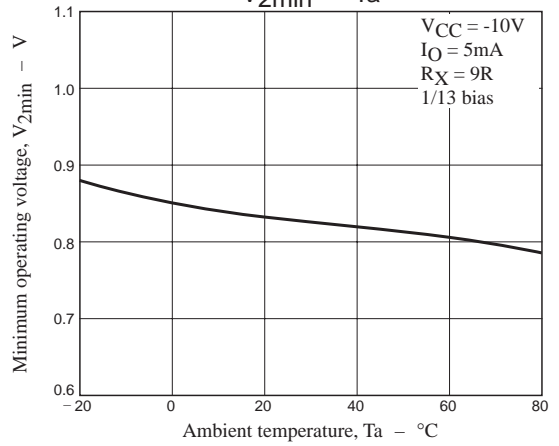
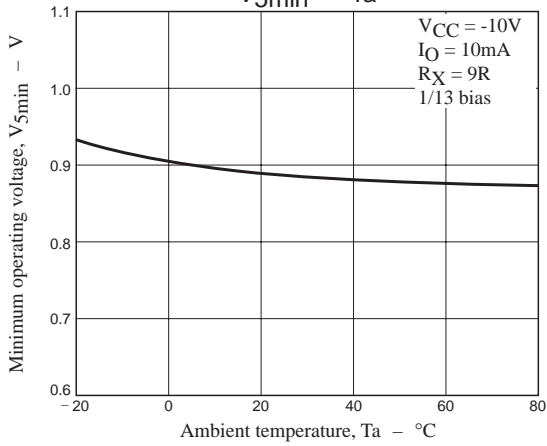
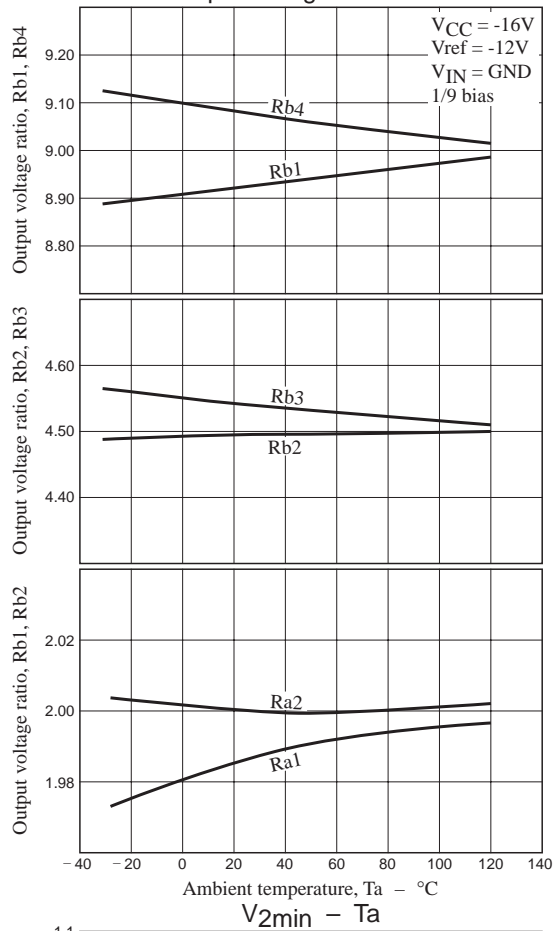
Block Diagram



Load regulation



Output voltage ratio - T_a



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