No. 4326

SANYO

LC3664BL, BML-70/85/10/12

64 K (8192 words x 8 bits) SRAM

Overview

The LC3664BL, BML-70/85/10/12 are fully asynchronous silicon gate CMOS static RAMs with an 8192 words x 8 bits.

This series has $\overline{CE1}$ and CE2 chip enable pins for device select/nonselect control and an $\overline{OE}$ output enable pin for output control, and features high speed as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

Features

* Access time
  70 ns (max.) : LC3664BL-70, LC3664BML-70
  85 ns (max.) : LC3664BL-85, LC3664BML-85
  100 ns (max.) : LC3664BL-10, LC3664BML-10
  120 ns (max.) : LC3664BL-12, LC3664BML-12
* Low current dissipation
  During standby
     0.5 µA (max.) /Ta = 25°C
     1 µA (max.)   /Ta = 0 to 40°C
     6 µA (max.)   /Ta = 0 to 70°C

  During data retention
     0.2 µA (max.) /Ta = 25°C
     0.5 µA (max.) /Ta = 0 to 40°C
   2.5 µA (max.) /Ta = 0 to 70°C

  During operation (DC)
     10 mA (max.)
* Single 5 V power supply: 5 V ±10%
* Data retention power supply voltage: 2.0 to 5.5 V
* No clock required (Fully static memory)
* All input/output levels are TTL compatible
* Common input/output pins, with three output states
* Packages
  DIP 28-pin plastic package (600 mil) : LC3664BL
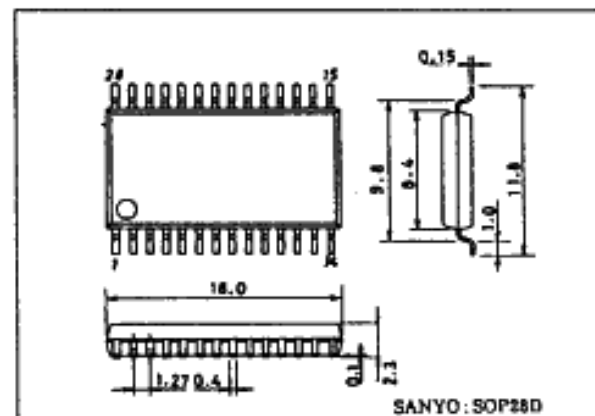 SOP 28-pin plastic package (450 mil) : LC3664BML

Package Dimensions

unit : mm

3012A - DIP28
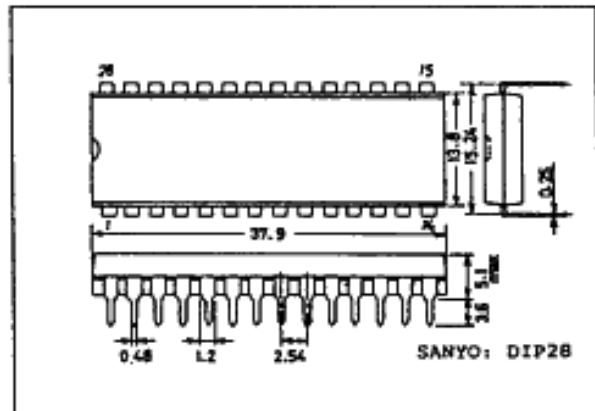
SANYO: DIP28

3187 - SOP28D

SANYO: SOP28D

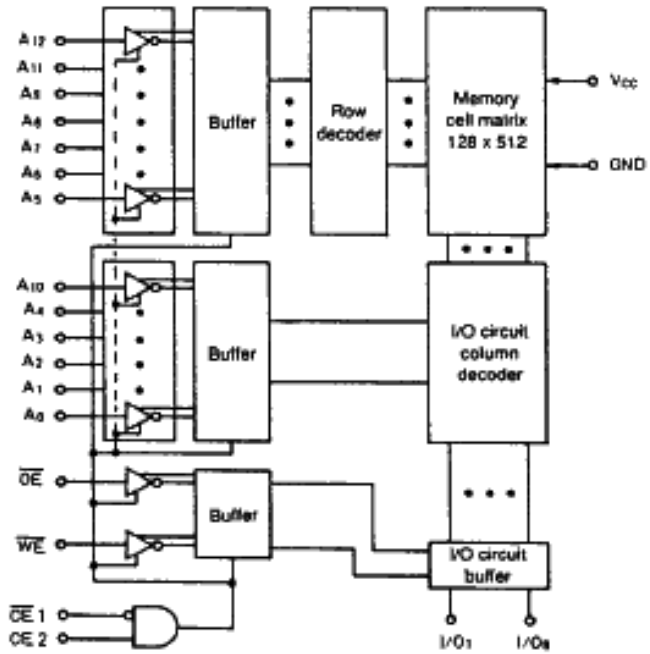## SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO JAPAN

Pin Assignment

TOP VIEW

```
     NC  1            28  Vcc
    A12  2            27  WE
     A7  3            26  CE 2
     A6  4            25  A8
     A5  5            24  A9
     A4  6            23  A11
     A3  7            22  OE
     A2  8            21  A10
     A1  9            20  CE 1
     A0 10            19  I/O8
    I/O1 11           18  I/O7
    I/O2 12           17  I/O6
    I/O3 13           16  I/O5
     GND 14           15  I/O4
```

Block Diagram

A0 to A12 : Address input
WE   : Read/write control input
OE   : Output enable input
CE1, CE2   : Chip enable input
I/O1 to I/O8 : Data input/output
Vcc, GND   : Power supply pins

Functions

Mode	$\overline{CE1}$	CE 2	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	ICCA
Write cycle	L	H	X	L	Data input	ICCA
Output disable	L	H	H	H	High impedance	ICCA
Nonselect	H	X	X	X	High impedance	ICCS
	X	L	X	X	High impedance	ICCS

X : H or L

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Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Condition	Rating	unit
Maximum supply voltage	Vcc max		7.0	V
Input pin voltage	VIN		−0.5* to Vcc+0.5	V
I/O pin voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	Pd max	LC3664BL	1.0	W
		LC3664BML	0.7	W
Operating temperature range	Topg		0 to 70	°C
Storage temperature range	Tstg		−55 to +150	°C

* −3.0 V when pulse width is less than 50 ns

DC Allowable Operating Ranges at Ta = 0 to 70°C

Parameter	Symbol	min	typ	max	unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input "H" level voltage	VIH	2.2		Vcc+0.3	V
Input "L" level voltage	VIL	−0.3*		+0.8	V

* −3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to 70°C, VCC = 5 V ±10%

Parameter	Symbol	Condition			min	typ*	max	unit
Input leakage current	ILI	VIN = 0 to Vcc			−0.5		+0.5	μA
I/O leakage current	ILO	VCE1 = VIH or VCE2 = VIL or VOE = VIH or VWE = VIL, VI/O = 0 to Vcc			−0.5		+0.5	μA
Output "H" level voltage	VOH	IOH = −1.0mA			2.4			V
Output "L" level voltage	VOL	IOL = 2.1mA					0.4	V
Operating supply current (DC)	ICCA1	VCE1≤0.2V, VCE2≥Vcc−0.2V, VIN≤0.2V or VIN≥Vcc−0.2V, II/O = 0mA				1	5	mA
	ICCA2	VCE1 = VIL, VCE2 = VIH, II/O=0mA, VIN = VIH or VIL				3	10	mA
Average operating supply current	ICCA3	VCE1 = VIL, VCE2 = VIH, II/O = 0mA, min cycle	Access time	70ns		30	50	mA
				85ns		25	50	
				100ns		23	50	
				120ns		20	50	
Standby supply current	ICCS1	{VCE2≤0.2V} or {VCE1≥Vcc−0.2V, (VCE2≥Vcc−0.2V or VCE2≤0.2V)}		0 to 70°C		0.2	6	μA
				0 to 40°C			1	
				25°C			0.5	
	ICCS2	VCE2 = VIL or VCE1 = VIH, VIN = 0 to Vcc				0.4	2	mA

* Reference values at VCC = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Condition	min	typ	max	unit
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0V$			8	pF
Input capacitance	C_{IN}	$V_{IN} = 0V$			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to 70°C, Vcc = 5 V ±10%

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + C_L = 100 pF (85 ns/100 ns/120 ns)
		1 TTL gate + C_L = 30 pF (70 ns)
		(including scope and jig capacitance)

Read Cycle

Parameter	Symbol	LC3664BL-70 LC3664BML-70 min	max	LC3664BL-85 LC3664BML-85 min	max	LC3664BL-10 LC3664BML-10 min	max	LC3664BL-12 LC3664BML-12 min	max	unit
Read cycle time	tRC	70		85		100		120		ns
Address access time	tAA		70		85		100		120	ns
CE1 access time	tCA1		70		85		100		120	ns
CE2 access time	tCA2		70		85		100		120	ns
OE access time	tOA		35		45		50		60	ns
Output hold time	tOH	20		20		20		20		ns
CE1 output enable time	tCOE1	10		10		10		10		ns
CE2 output enable time	tCOE2	10		10		10		10		ns
OE output enable time	tOOE	5		5		5		5		ns
CE1 output disable time	tCOD1	0	30	0	30	0	30	0	30	ns
CE2 output disable time	tCOD2	0	30	0	30	0	30	0	30	ns
OE output disable time	tOOD	0	30	0	30	0	30	0	30	ns

Write Cycle

| Parameter	Symbol	LC3664BL-70 LC3664BML-70 min	max	LC3664BL-85 LC3664BML-85 min	max	LC3664BL-10 LC3664BML-10 min	max	LC3664BL-12 LC3664BML-12 min	max	unit
Write cycle time	tWC	70		85		100		120		ns
Address valid to end of write	tAW	60		60		75		85		ns
Address setup time	tAS	0		0		0		0		ns
Write pulse width	tWP	50		50		60		70		ns
CE1 setup time	tCW1	60		60		75		85		ns
CE2 setup time	tCW2	60		60		75		85		ns
Write recovery time	tWR	0		0		0		0		ns
CE1 Write recovery time	tWR1	0		0		0		0		ns
CE2 Write recovery time	tWR2	0		0		0		0		ns
Data setup time	tDS	30		30		35		40		ns
Data hold time	tDH	0		0		0		0		ns
CE1 Data hold time	tDH1	0		0		0		0		ns
CE2 Data hold time	tDH2	0		0		0		0		ns
WE output enable time	tWOE	10		10		10		10		ns
WE output disable time	tWOD	0	25	0	25	0	25	0	25	ns

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Timing Charts

• Read Cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$
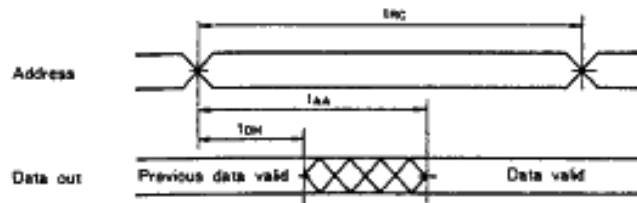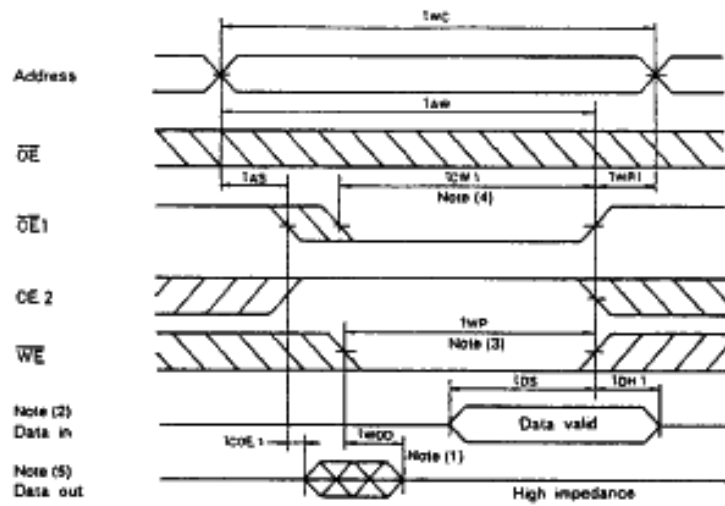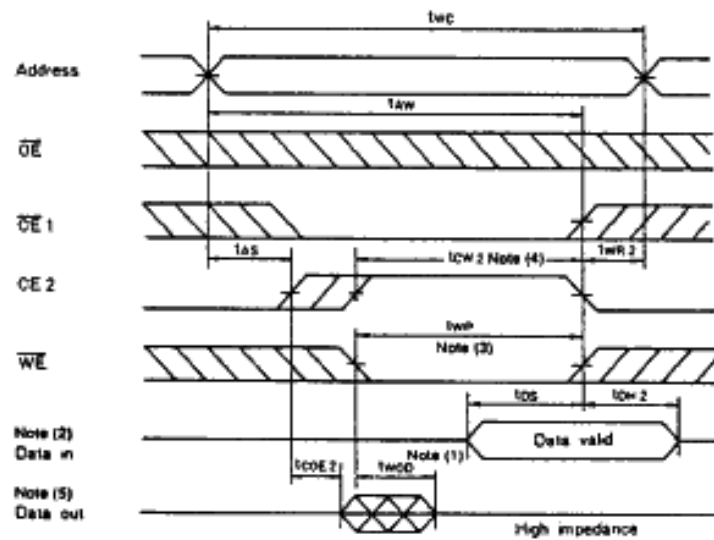

• Read Cycle (2): $\overline{WE} = V_{IH}$
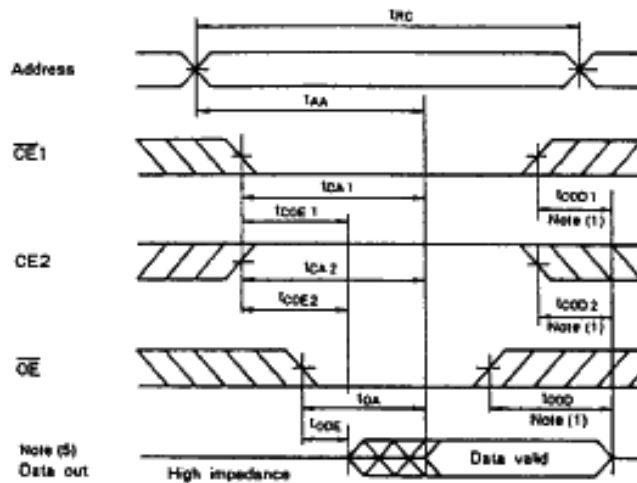
• Write Cycle (1): $\overline{WE}$ Control   Note (6)
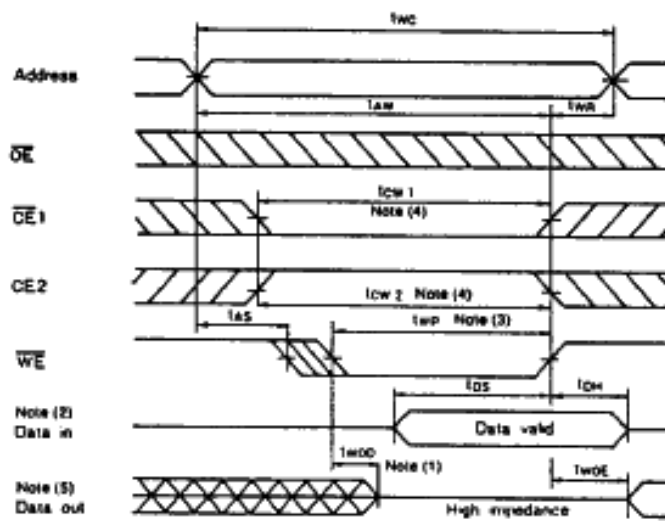
• Write Cycle (2): CE1 Control   Note (6)


• Write Cycle (3): CE2 Control   Note (6)

Notes (1) t_{COD1}, t_{COD2}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.

(2) An external antiphase signal must not be applied when DOUT is in the output state.

(3) t_{WP} is the time interval that $\overline{CE1}$ and $\overline{WE}$ are low-level and CE2 is high-level, and is defined as the interval from the falling of $\overline{WE}$ to the rising of $\overline{CE1}$ or $\overline{WE}$, or the falling of CE2, whichever is earlier.

(4) t_{CW1} and t_{CW2} are the time interval that $\overline{CE1}$ and $\overline{WE}$ are low-level and CE2 is high-level, and is defined as the time from the falling of $\overline{CE1}$ or the rising of CE2 to the rising of $\overline{CE1}$ or $\overline{WE}$, or the falling of CE2, whichever is earlier.

(5) DOUT goes to the high-impedance state when either $\overline{OE}$ is high-level, $\overline{CE1}$ is high-level, CE2 is low-level, or $\overline{WE}$ is low-level.

(6) When $\overline{OE}$ is high-level during the write cycle, DOUT goes to the high-impedance state.

Data Retention Characteristics at Ta = 0 to 70°C

Parameter	Symbol	Condition		min	typ	max	unit
Data retention supply voltage	V_{DR1}	$V_{\overline{CE1}} \geq V_{CC}-0.2V$, $V_{CE2} \geq V_{CC}-0.2V$ or $V_{CE2} \leq 0.2V$		2.0		5.5	V
	V_{DR2}	$V_{CE2} \leq 0.2V$		2.0		5.5	V
Data retention supply current	I_{CCDR1}	$V_{CC} = 3.0V$ $V_{\overline{CE1}} \geq V_{CC}-0.2V$, $V_{CE2} \geq V_{CC}-0.2V$ or $V_{CE2} \leq 0.2V$	0 to 70°C			2.5	µA
			0 to 40°C			0.5	
			25°C			0.2	
	I_{CCDR2}	$V_{CC} = 3.0V$, $V_{CE2} \leq 0.2V$	0 to 70°C			2.5	µA
			0 to 40°C			0.5	
			25°C			0.2	
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			t_{RC}*			ns

* t_{RC} = Read Cycle time

Data Retention Waveform (1) ($\overline{CE1}$ control)
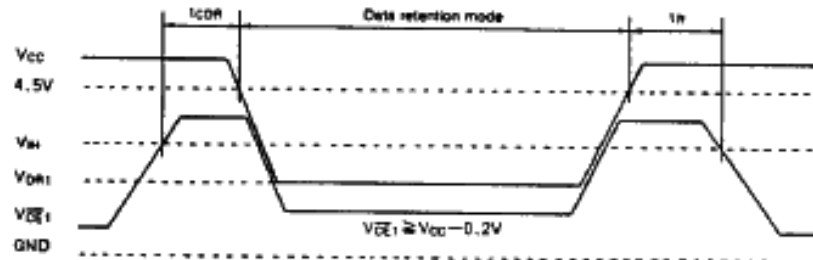
Data Retention Waveform (2) (CE2 control)