EM78P447S

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.5

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	-
1.1	Changed the Power-on reset contents	2003/06/25
1.2	Added device characteristic at Section 6.3	2004/11/05
1.3	Added new package type	2006/04/19
1.4	Added EM78P447SFK and EM78P447SBM package type on the Features section and other related sections, as well as on the Appendix section.	2006/07/25
1.5	EM78P447SAK update P54 description	2006/10/26

1 General Description

The EM78P447S is an 8-bit microprocessor with low-power and high-speed CMOS technology. It has a built-in 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Seven option bits are also available to meet user's requirements.

With its enhanced OTP-ROM features, the EM78P447S provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- Operating voltage: 2.3V~5.5V
- Operating temperature: -40°C~85°C
- Operating frequency range (base on 2 clocks)
  - Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V
  - RC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V
- Low power consumption:
  - Less than 2.2 mA at 5V/4MHz
  - 30 μA Typical at 3V/32kHz
  - 1 μA Typical, during sleep mode
- 4K×13 bits on-chip ROM
- One security register to prevent intrusion of OTP memory codes
- One configuration register to accommodate user's requirements
- 148×8 bits on-chip registers (SRAM, general purpose register)
- 3 bidirectional I/O ports
- 5-level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Two clocks per instruction cycle
- Power down (Sleep) mode

- Two available interrupts
  - TCC overflow interrupt
  - External interrupt
- Programmable free running watchdog timer
- 10 programmable pull-high pins
- 2 programmable open-drain pins
- 2 programmable R-option pins
- Package types:
  - 24-pin Skinny DIP 300 mil : EM78P447SCK
  - 24-pin SOP 300 mil : EM78P447SCM
  - 28-pin DIP 600 mil : EM78P447SAP
  - 28-pin Skinny DIP 300 mil : EM78P447SAK
  - 28-pin Skinny DIP 400 mil : EM78P447SFK
  - 28-pin SOP 300 mil : EM78P447SAM
  - 28-pin SSOP 209 mil : EM78P447SAS
  - 32-pin DIP 600 mil : EM78P447SBP
  - 32-pin SOP 450 mil : EM78P447SBWM
  - 32-pin SOP 300 mil : EM78P447SBM
- Single instruction cycle commands
- Transient point of system frequency between HXT and LXT is 400kHz

3 Pin Assignment

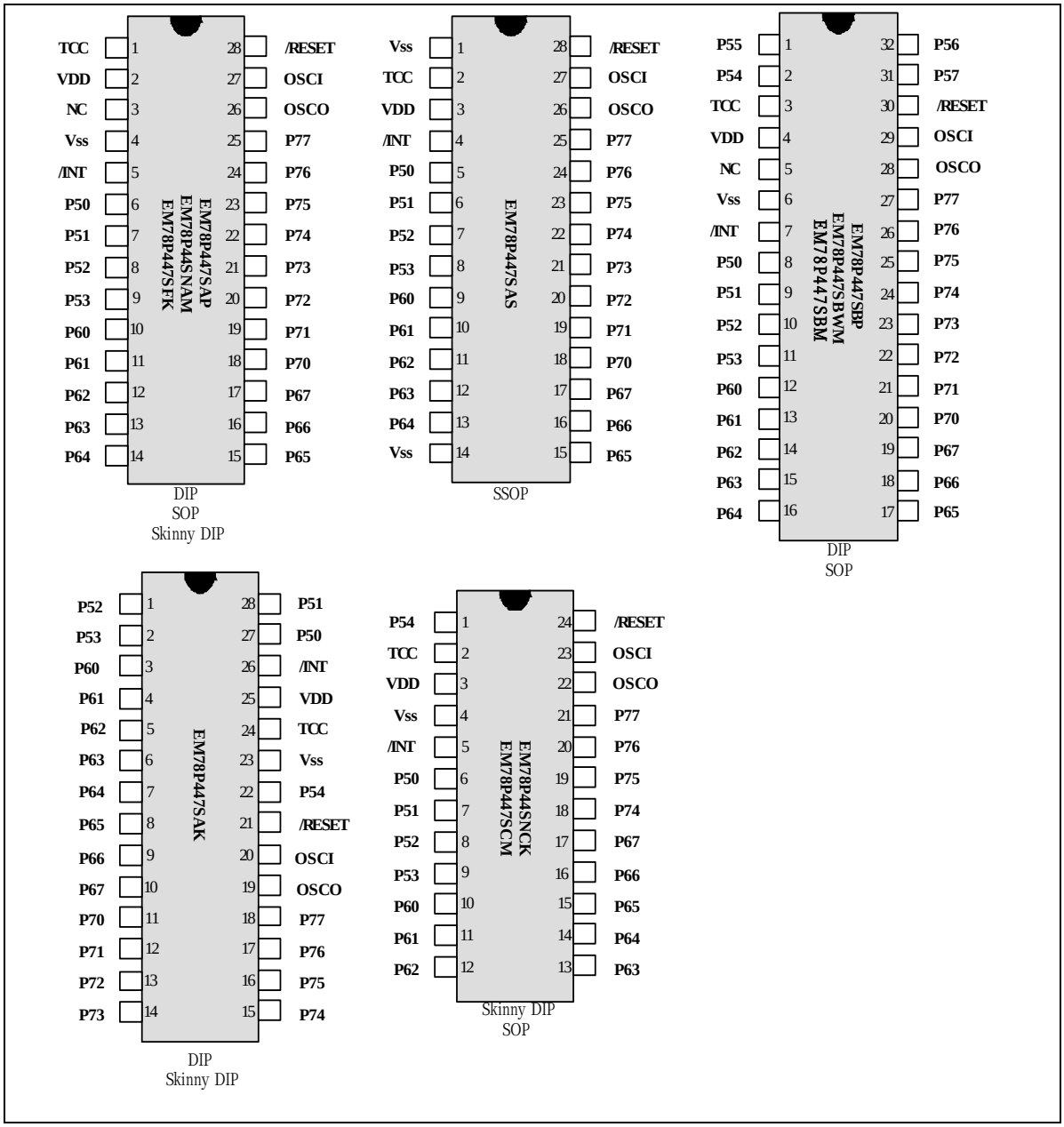


Fig. 1 Pin Assignment

Table 1 EM78P447SAP, EM78P447SAM and EM78P447SFK Pin Description

Symbol	Pin No.	Type	Function
VDD	2	-	Power supply
OSCI	27	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	26	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	1	I	Real time clock/counter (with Schmitt Trigger input pin) must be tied to VDD or VSS if not in use.
/RESET	28	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	6~9	I/O	Bidirectional 4-bit input/output pins
P60~P67	10~17	I/O	Bidirectional 8-bit input/output pins. These can be pulled-high internally by software control.
P70~P77	18~25	I/O	Bidirectional 8-bit input/output pins. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control. P70 and P71 can also be defined as R-option pins.
/INT	5	I	External interrupt pin triggered by a falling edge.
VSS	4	-	Ground
NC	3	-	No connection

Table 2 EM78P447SAS Pin Description

Symbol	Pin No.	Type	Function
VDD	3	-	Power supply
OSCI	27	I	Crystal type: Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	26	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	2	I	Real time clock/counter (with Schmitt trigger input pin) must be tied to VDD or VSS if not in use.
/RESET	28	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	5~8	I/O	Bidirectional 4-bit input/output pins
P60~P67	9~13, 15~17	I/O	Bidirectional 8-bit input/output pins. These can be pulled -high internally by software control.
P70~P77	18~25	I/O	Bidirectional 8-bit input/output pins. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control. P70 and P71 can also be defined as R-option pins.
/INT	4	I	External interrupt pin triggered by a falling edge.
VSS	1, 14	-	Ground

Table 3 EM78P447SAK Pin Description

Symbol	Pin No.	Type	Function
VDD	25	-	Power supply
OSCI	20	I	Crystal type: Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	19	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	24	I	Real time clock/counter (with Schmitt trigger input pin) must be tied to VDD or VSS if not in use.
/RESET	21	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P54	27~28 1~2 22	I/O	Bidirectional 5-bit input/output pins.
P60~P67	3~10	I/O	Bidirectional 8-bit input/output pins. These can be pulled -high internally by software control.
P70~P77	11~18	I/O	Bidirectional 8-bit input/output pins. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control. P70 and P71 can also be defined as R-option pins.
/INT	26	I	External interrupt pin triggered by a falling edge.
VSS	23	-	Ground

Table 4 EM78P447SBP, EM78P447SBWM and EM78P447SBM Pin Description

Symbol	Pin No.	Type	Function
VDD	4	-	Power supply
OSCI	29	I	Crystal type: Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	28	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	3	I	Real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	30	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P57	8~11, 2~1, 32~31	I/O	Bidirectional 8-bit input/output pins.
P60~P67	12~19	I/O	Bidirectional 8-bit input/output pins. These can be pulled -high internally by software control.
P70~P77	20~27	I/O	Bidirectional 8-bit input/output pins. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control. P70 and P71 can also be defined as R-option pins.
/INT	7	I	External interrupt pin triggered by a falling edge.
VSS	6	-	Ground

NC	5	-	No connection

Table 5 EM78P447SCK and EM78P447SCM Pin Description

Symbol	Pin No.	Type	Function
VDD	3	-	Power supply
OSCI	23	I	Crystal type: Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	22	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	2	I	Real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	24	I	Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P54	6~9, 1	I/O	Bidirectional 5-bit input/output pins.
P60~P67	10~17	I/O	Bidirectional 8-bit input/output pins. These can be pulled -high internally by software control.
P74~P77	18~21	I/O	Bidirectional 4-bit input/output pins. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control.
/INT	5	I	External interrupt pin triggered by a falling edge.
VSS	4	-	Ground

4 Function Description

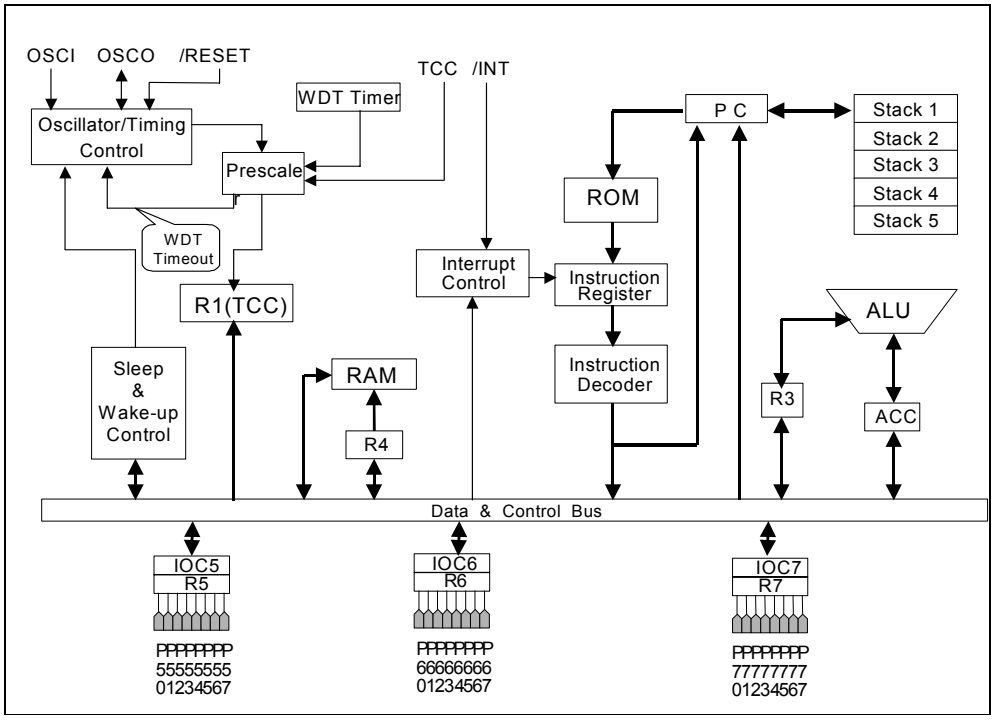


Fig. 2 Functional Block Diagram

4.1 Operational Registers

4.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to act as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

4.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge, which is defined by the TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

4.1.3 R2 (Program Counter) and Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.3.
- The configuration structure generates 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2,A" allows the contents of 'A' to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2,A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6", etc.) will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

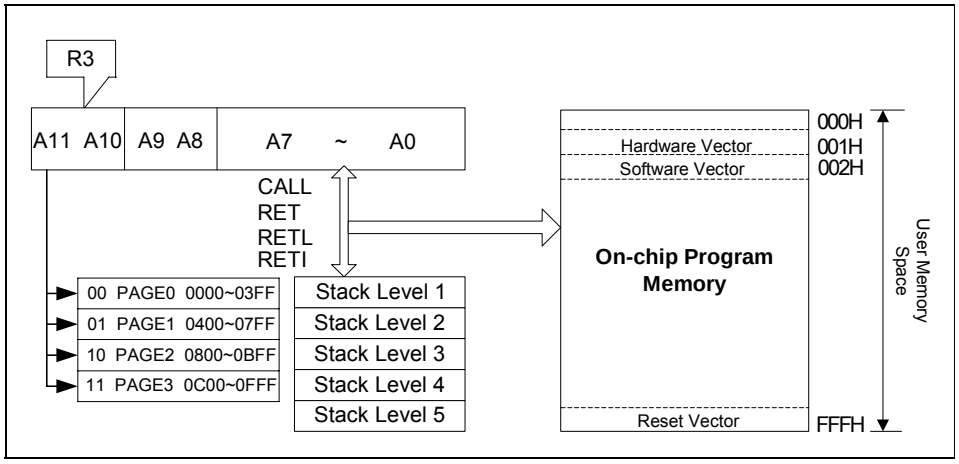


Fig. 3 Program Counter Organization

Aaddress	R PAGE Registers	IOC PAGE Registers
00	**R0** (Indirect Addressing Register)	Reserve
01	**R1** (Time Clock Counter)	**CONT** (Control Register)
02	**R2** (Program Counter)	Reserve
03	**R3** (Status Register)	Reserve
04	**R4** (RAM Select Register)	Reserve
05	**R5** (Port 5)	**IOC5** (I/O Port Control Register)
06	**R6** (Port 6)	**IOC6** (I/O Port Control Register)
07	**R7** (Port 7)	**IOC7** (I/O Port Control Register)
08	General Register	Reserve
09	General Register	Reserve
0A	General Register	Reserve
0B	General Register	**IOCB** Wake-up Control Register for Port 6)
0C	General Register	Reverse
0D	General Register	Reverse
0E	General Register	**IOCE** (WDT, SLEEP2, Open Drain, R Option Control Register)
0F	General Register	**IOCF** (Interrupt Mask Register)
10 : 1F	General Registers	
20 : 3E	Bank 0 / Bank 1 / Bank 2 / Bank 3	
3F	**R3F** (Interrupt Status Register)	

Fig. 4 Data Memory Configuration

4.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	PS1	PS0	T	P	Z	DC	C

Bit 7 (GP): General read/write bit.

Bits 6 (PS1) ~ 5 (PS0): Page select bits. PS1~PS0 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to change (e.g. MOV R2, A), PS1~PS0 are loaded into the 11th and 12th bits of the program counter and select one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the program will always return to the page from where the subroutine was called, regardless of the PS1~PS0 bits current setting.

PS1	PS0	Program Memory Page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

Bit 4 (T): Time-out bit. Set to 1 with the "SLEP" and "WDTC" commands, or during power up, and reset to 0 with the WDT time-out.

Bit 3 (P): Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag.

Bit 0 (C): Carry flag

4.1.5 R4 (RAM Select Register)

Bits 7~6: determine which bank is activated among the 4 banks.

Bits 5~0: are used to select the registers (address: 00~3F) in the indirect addressing mode.

If no indirect addressing is used, the RSR can be used as an 8-bit general-purpose read/writer register.

See the data memory configuration in Fig. 4.

4.1.6 R5~R7 (Port 5 ~ Port 7)

R5, R6 and R7 are I/O registers

4.1.7 R8~R1F and R20~R3E (General Purpose Registers)

R8~R1F, and R20~R3E (including Banks 0~3) are general-purpose registers.

4.1.8 R3F (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXIF	-	-	TCIF

Bit 3 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, the flag is cleared by software

Bits 1, 2, 4~7: not implemented and read are as "0".

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows; the flag is cleared by software.

"**0**" : non-interrupt

"**1**" : interrupt request

R3F can be cleared by instruction, but cannot be set by instruction.

IOCF is the interrupt mask register.

Note that reading R3F obtains the result of the R3F "logic AND" and IOCF.

4.2 Special Purpose Registers

4.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

4.2.2 CONT (Control Register)

The CONT register is both readable and writable.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PHEN	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (/PHEN): Control bit used to enable the pull-high of P60~P67, P74 and P75 pins

"**0**" : Enable internal pull-high

"**1**" : Disable internal pull-high

Bit 6 (/INT): Interrupt enable flag

"**0**" : masked by DISI or hardware interrupt

"**1**" : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

"**0**" : internal instruction cycle clock

"**1**" : transition on TCC pin

Bit 4 (TE): TCC signal edge

"**0**" : increment if a transition from low to high takes place on TCC pin

"**1**" : increment if a transition from high to low takes place on TCC pin

Bit 3 (PAB) Prescaler assignment bit

"**0**" : TCC

"**1**" : WDT

Bit 2 (PSR2) ~ Bit 0 (PSR0) TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

4.2.3 IOC5 ~ IOC7 (I/O Port Control Register)

"**0**" : defines the relative I/O pin as output

"**1**" : put the relative I/O pin into high impedance

IOC5 and IOC7 registers are both readable and writable.

4.2.4 IOCB (Wake-up Control Register for Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/WUE7	/WUE6	/WUE5	/WUE4	/WUE3	/WUE2	/WUE1	/WUE0

Bit 7 (/WUE7): Control bit used to enable the wake-up function of P67 pin.

Bit 6 (/WUE6): Control bit used to enable the wake-up function of P66 pin.

Bit 5 (/WUE5): Control bit used to enable the wake-up function of P65 pin.

Bit 4 (/WUE4): Control bit used to enable the wake-up function of P64 pin.

Bit 3 (/WUE3): Control bit used to enable the wake-up function of P63 pin.

Bit 2 (/WUE2): Control bit used to enable the wake-up function of P62 pin.

Bit 1 (/WUE1): Control bit used to enable the wake-up function of P61 pin.

Bit 0 (/WUE0): Control bit used to enable the wake-up function of P60 pin.

"**0**" : Enable internal wake-up

"**1**" : Disable internal wake-up

IOCB Register is both readable and writable.

4.2.5 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ODE	WDTE	SLPC	ROC	-	-	/WUE

Bit 6 (ODE): Control bit used to enable the open-drain function of P76 and P77 pins

"**0**" : Disable open-drain output

"**1**" : Enable open-drain output

The ODE bit can be read and written to.

Bit 5 (WDTE): Control bit used to enable Watchdog timer

The WDTE bit is used only when ENWDT, the CODE Option bit, is "0". It is only when the ENWDT bit is "0" that WDTE bit is able to disable/ enable the WDT.

"**0**" : Disable WDT

"**1**" : Enable WDT

The WDTE bit is not used if ENWDT, the CODE Option bit ENWDT, is "1". That is, if the ENWDT bit is "1", WDT is always disabled no matter what the WDTE bit status is.

The WDTE bit can be read and written.

Bit 4 (SLPC): This bit is set by hardware at the low level trigger of the wake-up signal and is cleared by software. SLPC is used to control the oscillator operation. The oscillator is disabled (oscillator is stopped, and the controller enters into Sleep 2 mode) on the high-to-low transition and is enabled (controller is awakened from Sleep 2 mode) on the low-to-high transition. In order to ensure having a stable oscillator output, once the oscillator is enabled again, there should be a delay for approximately 18ms[1] (oscillator start-up timer, OST) before the next instruction of the program is executed. The OST is always activated by a wake-up event from sleep mode regardless whether the Code Option bit ENWDT status is "0" or otherwise. After waking up, the WDT is enabled if the Code Option ENWDT is "1". The block diagram of Sleep 2 mode and wake-up invoked by an input trigger is depicted in Fig. 5. The SLPC bit can be read and written to.

[1] Vdd = 5V, set up time period = 16.2ms ± 30%
Vdd = 3V, set up time period = 19.6ms ± 30%

Bit 3 (ROC): ROC is used for the R-option. Setting ROC to "1" enables the status of the R-option pins (P70, P71) for the controller to read. Clearing ROC disables the R-option function. Otherwise, the R-option function is introduced. Users must connect the P71 pin and/or P70 pin to VSS with a 430KΩ external resistor (Rex). If Rex is connected/disconnected to VDD, the status of P70 (P71) will be read as "0"/"1" (refer to Fig. 7b). The ROC bit can be read and written to.

Bits 1~2, and 7: Not used

Bit 0 (/WUE): Control bit used to enable the wake-up function of P74 and P75.

"**0**" : Enable the wake-up function

"**1**" : Disable the wake-up function

The /WUE bit can be read and written to.

4.2.6 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXIE	-	-	TCIE

Bit 3 (EXIE): EXIF interrupt enable bit

"**0**" : Disable EXIF interrupt

"**1**" : Enable EXIF interrupt

Bits 1, 2 and 4~7 Not used.

Bit 0 (TCIE) TCIF interrupt enable bit.

"**0**" : Disable TCIF interrupt

"**1**" : Enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction (refer to Fig. 9).

IOCF register is both readable and writable.

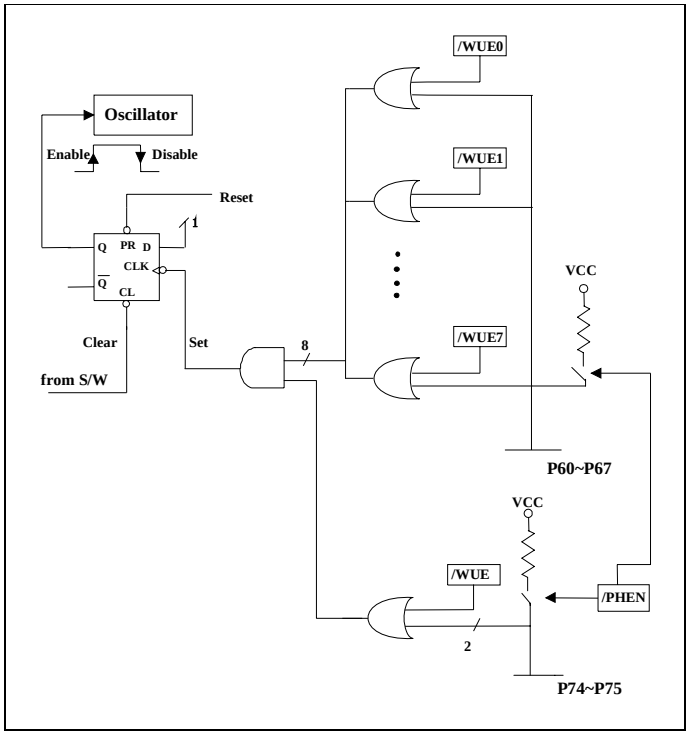


Fig. 5 Sleep Mode and Wake-up Circuits on I/O Ports Block Diagram

4.3 TCC/WDT and Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC in TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If the TCC signal source is from the internal clock, TCC is incremented by 1 every time an instruction cycle is executed (without prescaler). Referring to Fig. 6, CLK=Fosc/2 or CLK=Fosc/4 selection is determined by the Code Option bit CLK status. CLK=Fosc/2 is used if CLK bit is "0", and CLK=Fosc/4 is used if CLK bit is "1". If the TCC signal source comes from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT keeps on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[2] (default).

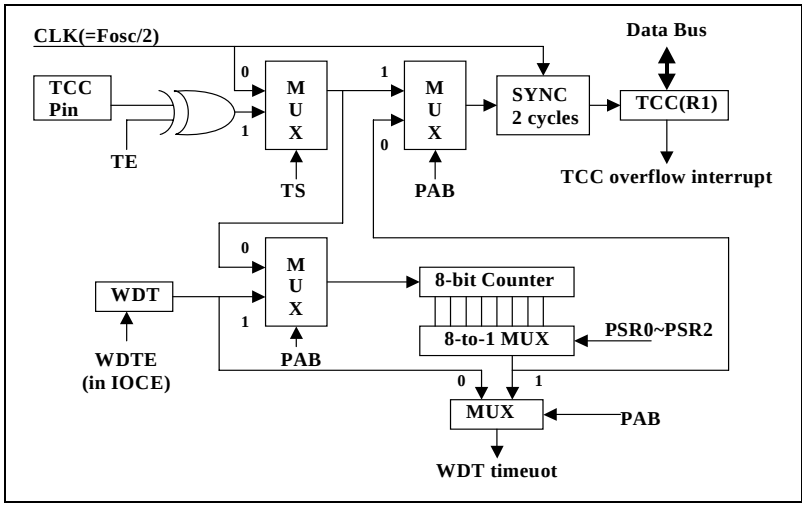


Fig. 6 TCC and WDT Block Diagram

[2] Vdd = 5V, set up time period = 16.2ms ± 30%
Vdd = 3V, set up time period = 19.6ms ± 30%

4.4 I/O Ports

The I/O registers, Port 5, Port 6, and Port 7, are bidirectional tri-state I/O ports. The Pull-high, R-option, and Open-drain functions can be performed internally by CONT and IOCE respectively. There is input status change wake-up function on Port 6, P74, and P75. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are shown in Figures. 7(a) and (b) respectively.

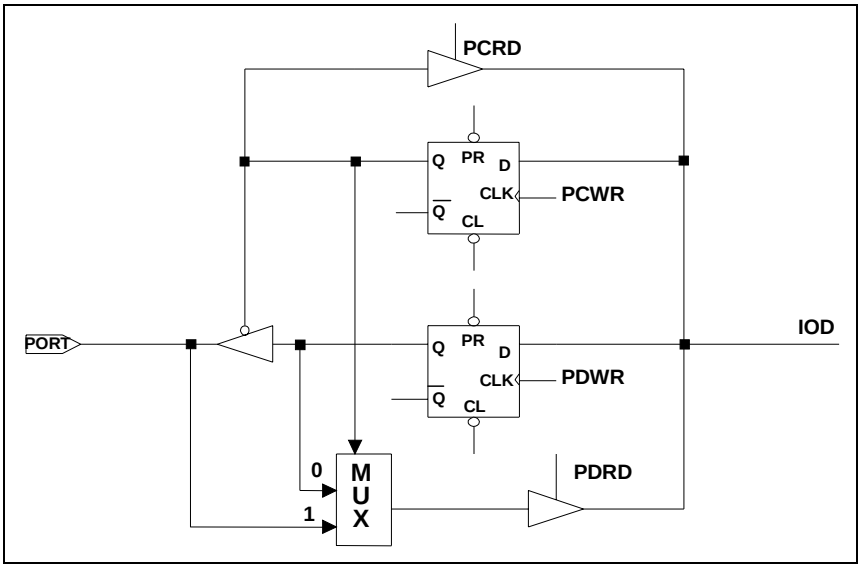


Fig. 7 (a) I/O Port and I/O Control Register Circuit

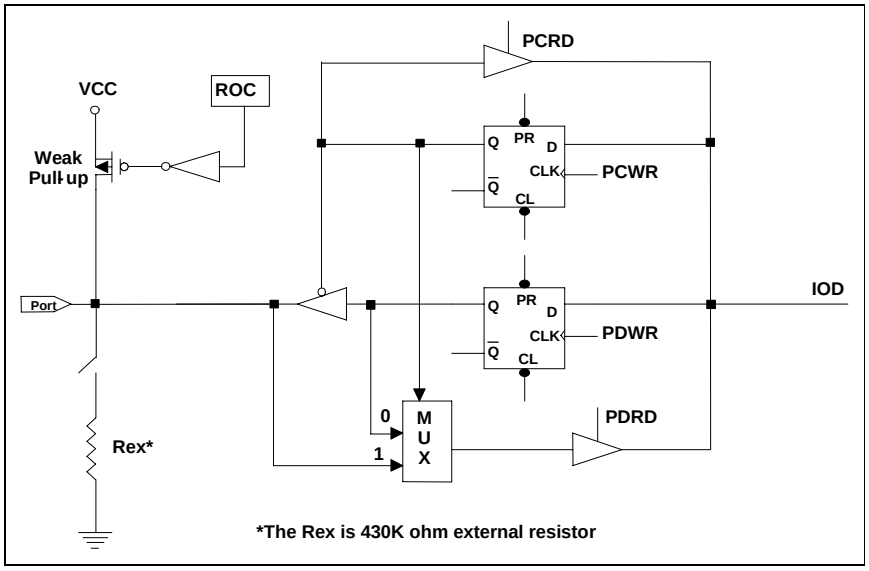


Fig.7(b) I/O Port with R-Option (P70, P71) Circuit

4.5 Reset and Wake-up

4.5.1 Reset

A Reset is initiated by one of the following conditions:

(1) Power on reset, or

(2) /RESET pin input “low”, or

(3) WDT timeout (if enabled)

The device is kept in a Reset condition for a period of approx. 18ms[3] (one oscillator start-up timer period) after the reset is detected. Once a Reset occurs, the following functions are performed (refer to Fig. 8).

- The oscillator starts or is running
- The Program Counter (R2) is set to all "1"
- When power is switched on, Bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- Upon power on, Bits 5~6 of R3 are cleared.
- Upon power on, the upper 2 bits of R4 are cleared.
- The bits of CONT register are set to all "1" except Bit 6 (INT flag).
- IOCB register is set to ”1” (disable P60 ~ P67 wake-up function).
- Bits 3 and 6 of IOCE register are cleared, and Bits 0, 4, and 5 are set to "1".
- Bits 0 and 3 of R3F register and Bits 0 and 3 of IOCF registers are cleared.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by:

(1) External reset input on /RESET pin;

(2) WDT time-out (if enabled)

The above two cases will cause the controller EM78P447S to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

[3] Vdd = 5V, set up time period = 16.2ms ± 30%
Vdd = 3V, set up time period = 19.6ms ± 30%

In addition to the basic Sleep 1 Mode, EM78P447S has another sleep mode (designated as Sleep 2 Mode and is invoked by clearing the IOCE register "SLPC" bit). In the Sleep 2 Mode, the controller can be awakened by:

(A) Any of the wake-up pins is "0" as illustrated in Figure. 5. Upon waking, the controller will continue to execute the succeeding address. In this case, before entering Sleep2 Mode, the wake-up function of the trigger sources (P60~P67 and P74~P75) should be selected (e.g., input pin) and enabled (e.g., pull-high, wake-up control). It should be noted that after waking up, the WDT is enabled if the Code Option bit ENWDT is "0". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(B) WDT time-out (if enabled) or external reset input on /RESET pin will trigger a controller reset.

Table 6 Usage of Sleep1 and Sleep2 Mode

Usage of Sleep 1 and Sleep 2 Mode	
Sleep 2	Sleep 1
(a) Before Sleep 1. Set Port 6 or P74 or P75 Input 2. Enable Pull-high and set WDT prescaler over 1:1 (Set CONT.7 and CONT.3 ~ CONT.0) 3. Enable Wake-up (Set IOCB or IOCE.0) 4. Execute Sleep 2 (Set IOCE.4)	(a) Before Sleep 1. Execute SLEP instruction
(b) After Wake-up 1. Next instruction 2. Disable Wake-up 3. Disable WDT (Set IOCE.5)	(b) After Wake-up 1. Reset

If Port 6 Input Status Changed Wake-up is used to wake-up the EM78P447S (Case [a] above), the following instructions must be executed before entering Sleep 2 mode:

```
MOV             A, @11111111b   ;Set Port6 input
IOW             R6
MOV             A, @0xxx1010b   ;Set Port 6 pull-high, WDT prescaler,
                                ;prescaler must be set at 1:1
CONTW
MOV             A, @00000000b   ;Enable Port 6 wake-up function
IOW             RB
MOV             A, @xx00xxx1b   ;Enable SLEEP 2
IOW             RE
After Wake-up
NOP
MOV             A, @11111111b   ;Disable Port 6 wake-up function
IOW             RB
MOV             A, @
                xx01xxx1b       ;Disable WDT
IOW             RE
```

NOTE

- *After waking up from Sleep 2 mode, WDT is automatically enabled. The WDT enabled/disabled operation after waking up from Sleep 2 mode should be appropriately defined in the software.*
- *To avoid reset from occurring when the Port 6 status changed interrupt enters into interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above 1:1 ratio.*

Table 7 Summary of the Initialized Register Values

Address	Name	Reset Type	Bit 7		Bit 6		Bit 5		Bit 4		Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57		C56		C55		C54		C53	C52	C51	C50
		Type	A	B	A	B	A	B	A	B	-	-	-	-
		Power-On	0	1	0	1	0	1	0	1	1	1	1	1
		/RESET and WDT	0	1	0	1	0	1	0	1	1	1	1	1
		Wake-Up from Pin Change	0	P	0	P	0	P	0	P	P	P	P	P
N/A	IOC6	Bit Name	C67		C66		C65		C64		C63	C62	C61	C60
		Power-On	1		1		1		1		1	1	1	1
		/RESET and WDT	1		1		1		1		1	1	1	1
		Wake-Up from Pin Change	P		P		P		P		P	P	P	P
N/A	IOC7	Bit Name	C77		C76		C75		C74		C73	C72	C71	C70
		Power-On	1		1		1		1		1	1	1	1
		/RESET and WDT	1		1		1		1		1	1	1	1
		Wake-Up from Pin Change	P		P		P		P		P	P	P	P
N/A	CONT	Bit Name	/PHEN		/INT		TS		TE		PAB	PSR2	PSR1	PSR0
		Power-On	1		0		1		1		1	1	1	1
		/RESET and WDT	1		P		1		1		1	1	1	1
		Wake-Up from Pin Change	P		P		P		P		P	P	P	P
0x00		Bit Name	-		-		-		-		-	-	-	-
		Power-On	U		U		U		U		U	U	U	U
		/RESET and WDT	P		P		P		P		P	P	P	P
		Wake-Up from Pin Change	P		P		P		P		P	P	P	P
0x01	R1(TCC)	Bit Name	-		-		-		-		-	-	-	-
		Power-On	0		0		0		0		0	0	0	0
		/RESET and WDT	0		0		0		0		0	0	0	0
		Wake-Up from Pin Change	P		P		P		P		P	P	P	P
0x02	R2(PC)	Bit Name	-		-		-		-		-	-	-	-
		Power-On	1		1		1		1		1	1	1	1
		/RESET and WDT	1		1		1		1		1	1	1	1
		Wake-Up from Pin Change	**0/P		**0/P		**0/P		**0/P		**0/P	**0/P	**0/P	**0/P
0x03	R3(SR)	Bit Name	GP		PS1		PS0		T		P	Z	DC	C
		Power-On	0		0		0		1		1	U	U	U
		/RESET and WDT	0		0		0		t		t	P	P	P
		Wake-Up from Pin Change	P		P		P		t		t	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	R4 (RSR)	Bit Name	RSR.1	RSR.0	-	-	-	-	-	-
		Power-On	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5 (P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6 (P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7 (P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x3F	R3F (ISR)	Bit Name	X	X	X	X	EXIF	X	X	TCIF
		Power-On	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-Up from Pin Change	U	U	U	U	P	U	U	P
0x0B	IOCB	Bit Name	/WUE7	/WUE6	/WUE5	/WUE4	/WUE3	/WUE2	/WUE1	/WUE0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	X	ODE	WDTE	SLPC	ROC	X	X	/WUE
		Power-On	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-Up from Pin Change	U	P	1	1	P	U	U	P
0x0F	IOCF	Bit Name	X	X	X	X	EXIE	X	X	TCIE
		Power-On	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-Up from Pin Change	U	U	U	U	P	U	U	P
0x08	R8	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09~ 0x3E	R9~R 3E	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

** Execute the next instruction after "SLPC" bit status of the IOCE register goes on high-to-low transition.

×: Not used. **U**: Unknown or don't care. **-**: not defined. **P**: Previous value before reset. **t**: Check Table 8

4.5.2 The Status of RST, T, and P of Status Register

A Reset condition is initiated by one of the following occurrence:

1. A power-on condition,

2. A high-low-high pulse on the /RESET pin, and

3. Watchdog timer time-out

The values of T and P (listed in Table 8 below) are used to verify the event that triggered the processor to wake up.

The following table shows the events that may affect the status of T and P.

Table 8 Values of RST, T and P after RESET

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep 1 mode	1	0
/RESET wake-up during Sleep 2 mode	*P	*P
WDT during Operating mode	0	*P
WDT wake-up during Sleep 1 mode	0	0
WDT wake-up during Sleep 2 mode	0	*P
Wake-up on pin change during Sleep 2 mode	*P	*P

*P: Previous status before reset

Table 9 Events that may Affect the T and P Status

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep 2 mode	*P	*P

*P: Previous value before reset

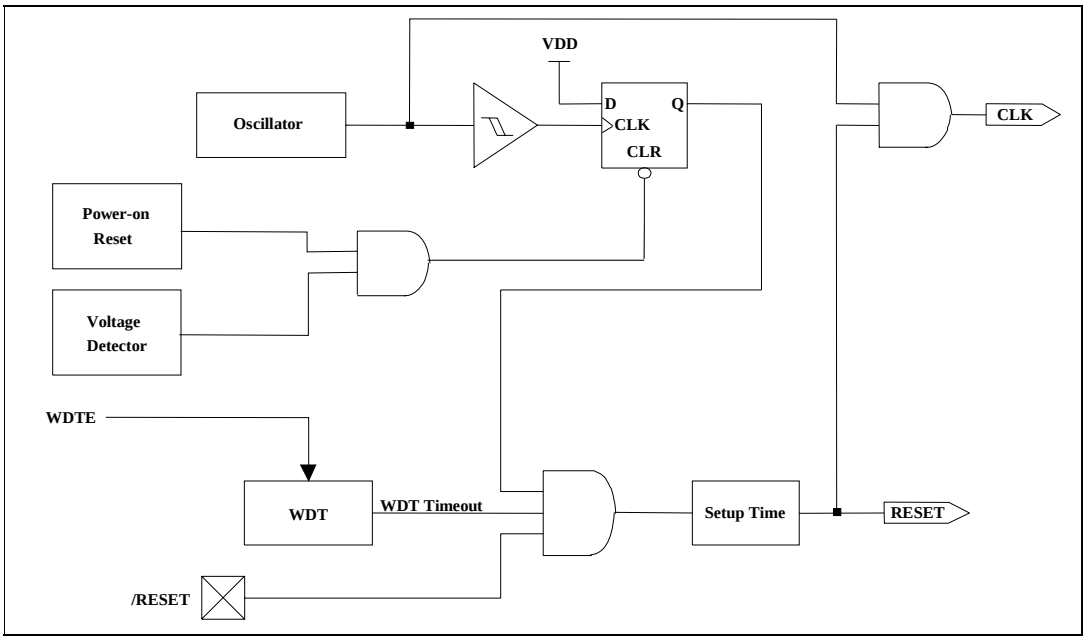


Fig. 8 Controller Reset Block Diagram

4.6 Interrupt

The EM78P447S has two interrupts as listed below:

(1) TCC overflow interrupt

(2) External interrupt (/INT pin)

R3F is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 001H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in R3F. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of R3F is the logic AND of R3F and IOCF (refer to Fig. 9). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from address 002H.

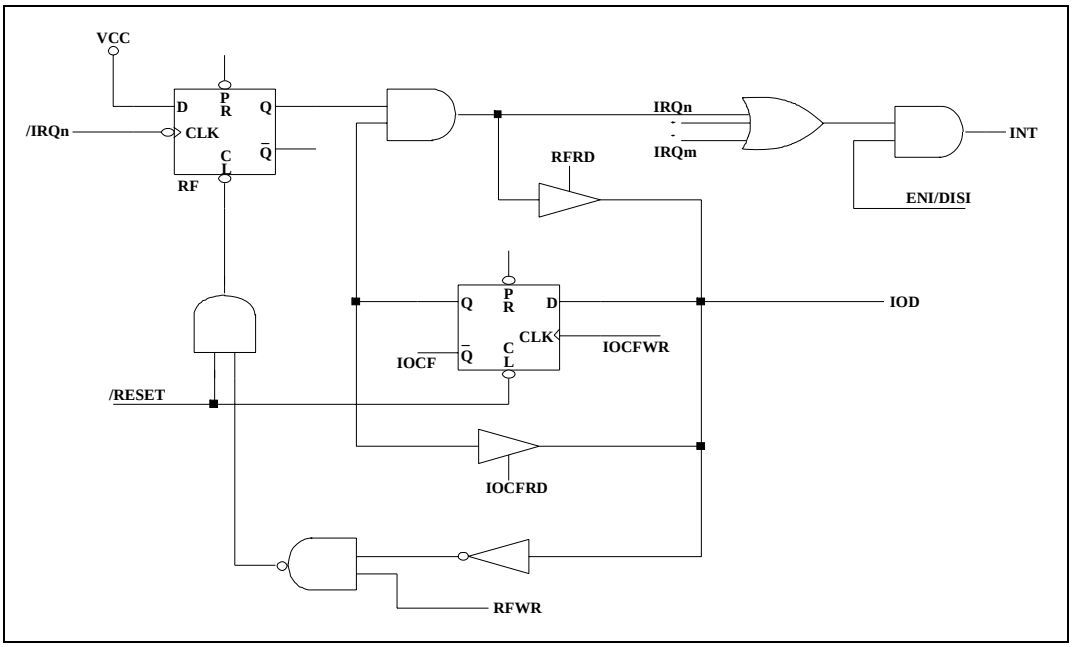


Fig. 9 Interrupt Input Circuit

4.7 Oscillator

4.7.1 Oscillator Modes

The EM78P447S can operate in three different oscillator modes, i.e., high Crystal (HXT) oscillator mode, low Crystal (LXT) oscillator mode, and External RC oscillator mode (ERC) oscillator mode. User can select one of them by programming MS, HLF and HLP in the Code Option Register. Table 10 shows how these three modes are defined.

The maximum limit for operational frequencies of crystal/resonator under different VDDs is listed in Table 11.

Table 10 Oscillator Modes Defined by MS and HLP

Mode	MS	HLF	HLP
ERC External RC oscillator mode)	0	*x	*x
HXT (High Crystal oscillator mode)	1	1	*x
LXT (Low Crystal oscillator mode)	1	0	0

Note: *x: Don't care

The transient point of the system frequency between HXT and LXY is 400kHz.

Table 11 Summary of the Maximum Operating Speeds

Conditions	VDD	Fxt Max. (MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

4.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P447S can be driven by an external clock signal through the OSCI pin as shown in Fig. 10 below.

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation, as shown in Fig. 11. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 12 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS which is a serial resistor may be necessary for AT strip cut crystal or low frequency mode.

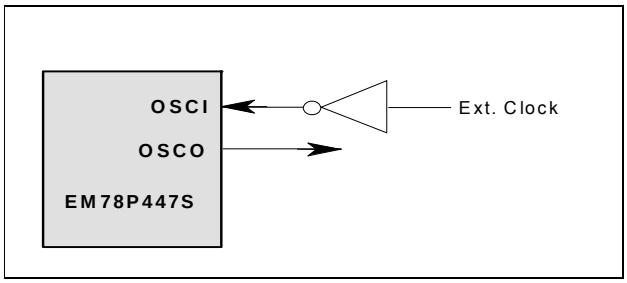


Fig. 10 Crystal/Resonator Circuit

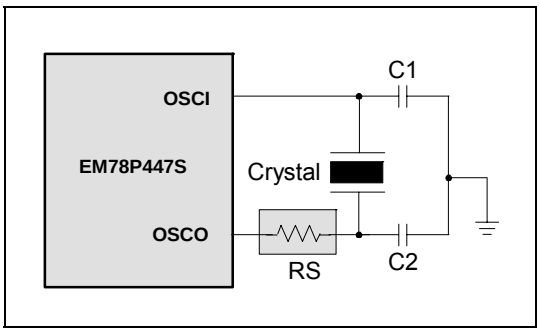


Fig. 11 Crystal/Resonator Circuit

Table 12 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768 kHz	25	15
		100 kHz	25	25
		200 kHz	25	25
	HXT	455 kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig. 15) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the PCB is layout, will affect the system frequency.

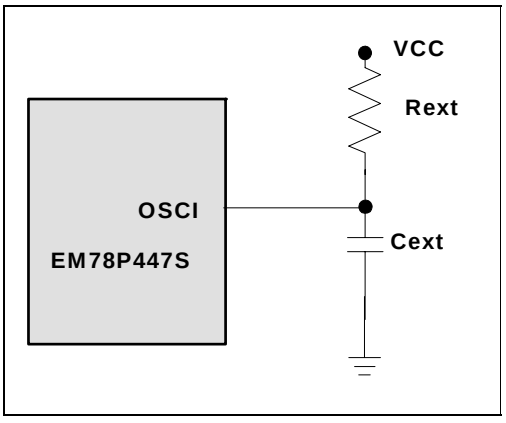


Fig. 12 External RC Oscillator Mode Circuit

Table 13 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	4.32 MHz	3.56 MHz
	5.1k	2.83 MHz	2.8 MHz
	10k	1.62 MHz	1.57 MHz
	100k	184 kHz	187 kHz
100 pF	3.3k	1.39 MHz	1.35 MHz
	5.1k	950 kHz	930 kHz
	10k	500 kHz	490 kHz
	100k	54 kHz	55 kHz
300 pF	3.3k	580 kHz	550 kHz
	5.1k	390 kHz	380 kHz
	10k	200 kHz	200 kHz
	100k	21 kHz	21 kHz

Note: 1. Measured on DIP packages
2. This is for design reference only
3. The frequency drift is ± 30%

4.8 Code Option Register

The EM78P447S has one Code option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MS	/ENWDT	CLK	CS	HLP	HLP	TYPE	-	-	-	-	-	-

Bit 12 (MS): Oscillator type selection

"**0**" : RC type

"**1**" : Crystal type (Crystal 1 and Crystal 2)

Bit 11 (/ENWDT): Watchdog timer enable bit

"**0**" : Enable

"**1**" : Disable

Bit 10 (CLK): Instruction period option bit.

"**0**" : two oscillator periods

"**1**" : four oscillator periods

Refer to the Instruction Set section.

Bit 9 (CS): Code Security Bit

"**0**" : Security On

"**1**" : Security Off

Bit 8 (HLF): Crystal frequency selection

"**0**" : Crystal 2 type (low frequency, 32.768kHz)

"**1**" : Crystal 1 type (high frequency)

This bit will affect the system oscillation only when Bit 12 (MS) is "1". When MS is"0", HLF must be "0".

NOTE

The transient point of the system frequency between HXT and LXY is 400 kHz.

Bit 7 (HLP): Power selection

"**0**" : Low power

"**1**" : High power

Bit 6 (TYPE): Type selection for EM78P447SA or B

"**0**" : EM78P447SB

"**1**" : EM78P447SA

Bit 5 and Bit 4: Reserved.

"**0**" : Bit 5 is set to "1" all the time

"**1**" : Bit 4 is set to "0" all the time

Bits 3~0 : Customer's ID code

4.9 Power-on Considerations

Any microcontroller is not guaranteed to start and operate properly before the power supply remains at its steady state.

The EM78P447S POR voltage range is 1.2V~1.8V. For customer applications, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10µs before power can be switched ON again. This way, the EM78P447S will reset and work normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, in most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

4.10 External Power-on Reset Circuit

The circuit shown in Fig.13 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 KΩ. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

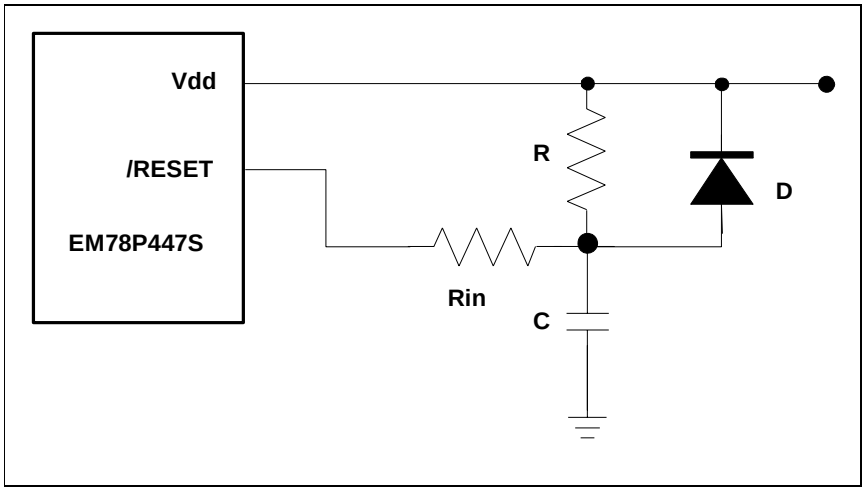


Fig. 13 External Power-Up Reset Circuit

4.11 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Fig.14 and Fig.15 show how to build the residue-voltage protection circuit.

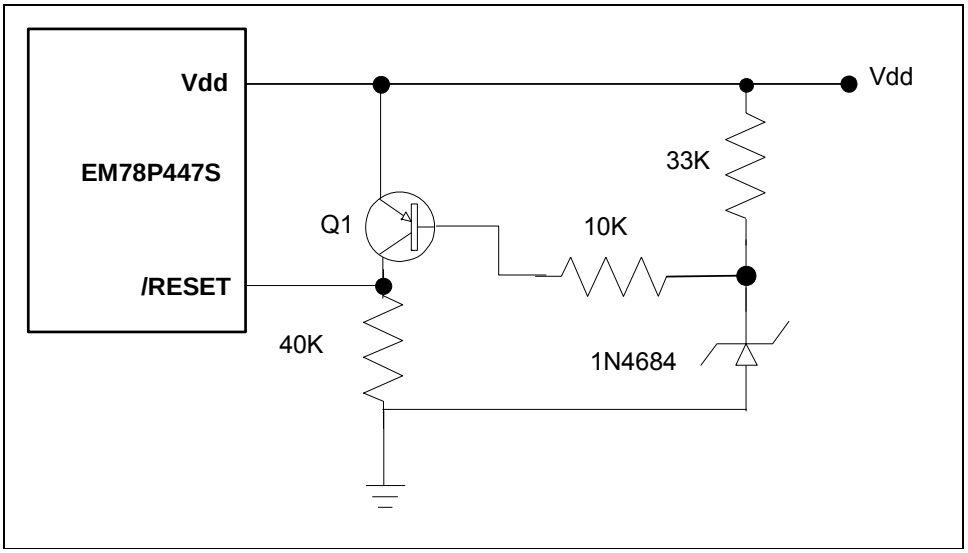


Fig.14 Residue Voltage Protection Circuit 1

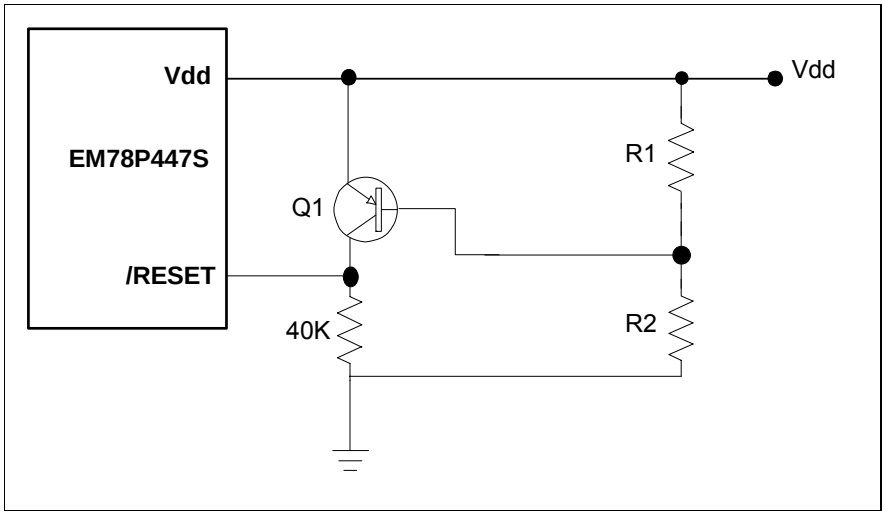


Fig.15 Residue Voltage Protection Circuit 2

4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS (C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of four oscillator periods.

(B) Executed within two instruction cycles, "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") instructions which were tested to be true. Also execute within two instruction cycles, the instructions that are written to the program counter.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, not Fosc / 2 as indicated in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

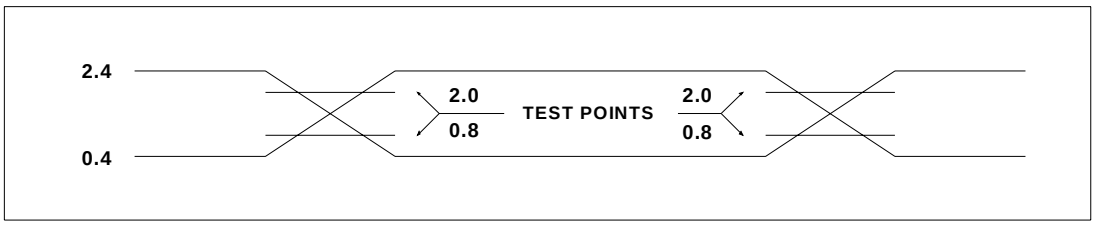
Note: [1] This instruction is applicable to IOC5~IOC7, IOCB, IOCE and IOCF only.

[2] This instruction is not recommended for R3F operation.

[3] This instruction cannot operate under R3F.

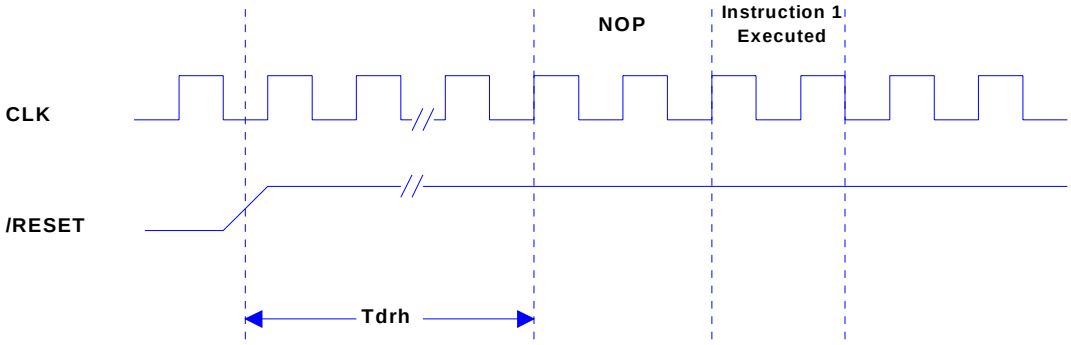
4.13 Timing Diagram

AC Test Input/Output Waveform

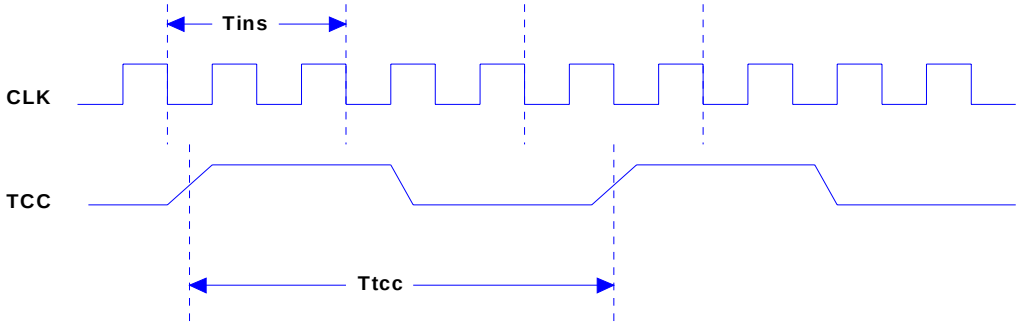


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	20 MHz

6 Electrical Characteristics

6.1 DC Electrical Characteristic

Ta= -40°C ~ 85 °C, VDD= 5.0V±5%, VSS= 0V

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
FXT	Crystal: VDD to 3V	Two cycles with two clocks	DC	-	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	-	20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	950	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	µA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0	-		V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6	-	-	0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC	2.0	-	-	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC	-	-	0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	3.5	-		V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI	-	-	1.5	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5	-	-	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6	-	-	0.4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC	1.5	-	-	V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC	-	-	0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	2.1	-		V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI	-	-	0.9	V
VOH1	Output High Voltage (Ports 5, 6, 7)	IOH = -10.0 mA	2.4	-	-	V
VOL1	Output Low Voltage (Ports 5, 6)	IOL = 9.0 mA	-	-	0.4	V
VOL2	Output Low Voltage (Port 7)	IOL = 14.0 mA	-	-	0.4	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	-50	-100	-240	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	-	-	1	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	-	-	7	µA

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
ICC1	Operating supply current (VDD=3V) Two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	15	25	30	µA
ICC2	Operating supply current (VDD=3V) Two cycles/four clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	-	30	35	µA
ICC3	Operating supply current (VDD=5V) Two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	-	-	2.2	mA
ICC4	Operating supply current (VDD=5V) Two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	-	-	5.0	mA

6.2 AC Electrical Characteristic

Ta=-40°C ~ 85 °C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	-	-	0	-	ns
Thold	Input pin hold time	-	-	20	-	ns
Tdelay	Output pin delay time	C_{load}=20pF	-	50	-	ns

* N = selected prescaler ratio

6.3 Device Characteristic

The graphic provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphics, the data maybe out of the specified warranted operating range.

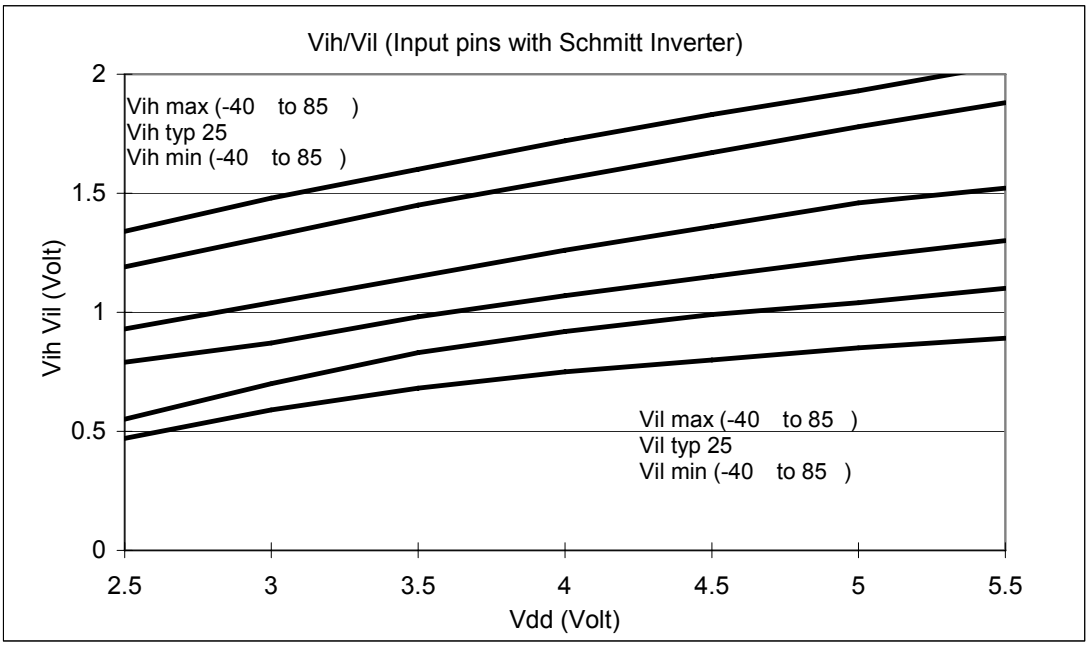


Fig. 16 Vih, Vil of TCC, /INT, /RESET Pin

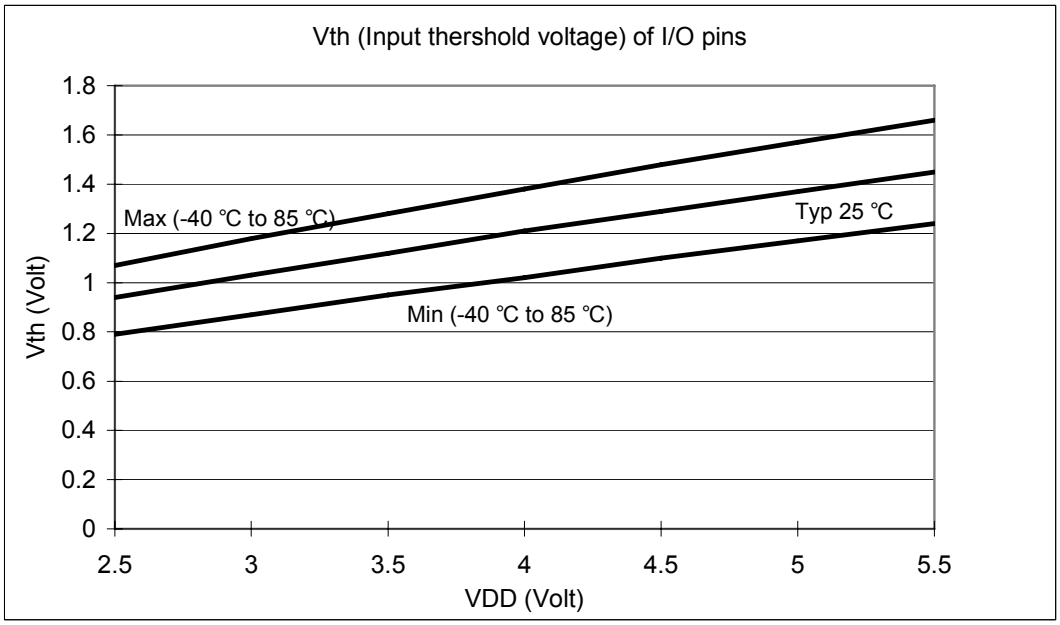


Fig. 17 Vth (Threshold Voltage) of P60~P67, P70~P77 vs. VDD

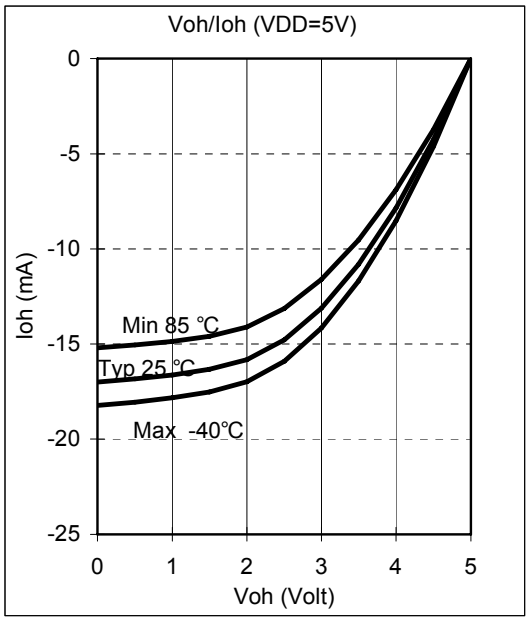


Fig.18 Port 5, Port 6, and Port 7

Voh vs. Ioh, VDD=5V

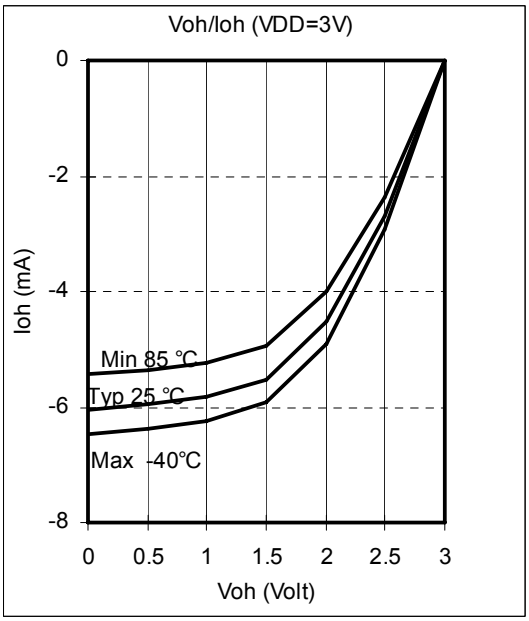


Fig.19 Port 5, Port 6, and Port 7

Voh vs. Ioh, VDD=3V

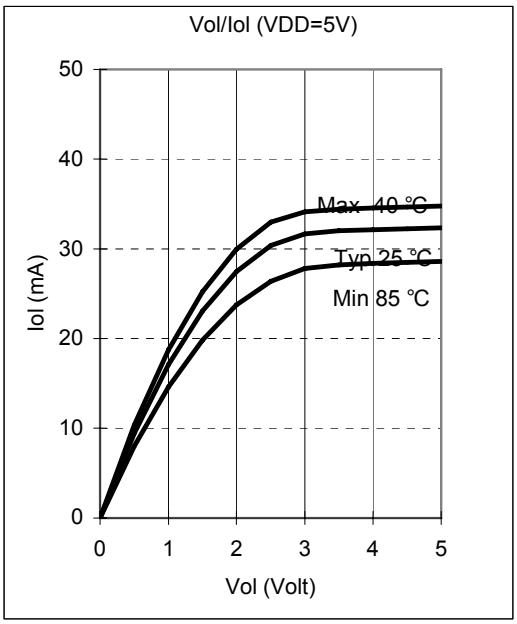


Fig. 20 Port 5, and Port 6 Vol vs, Iol, VDD=5V

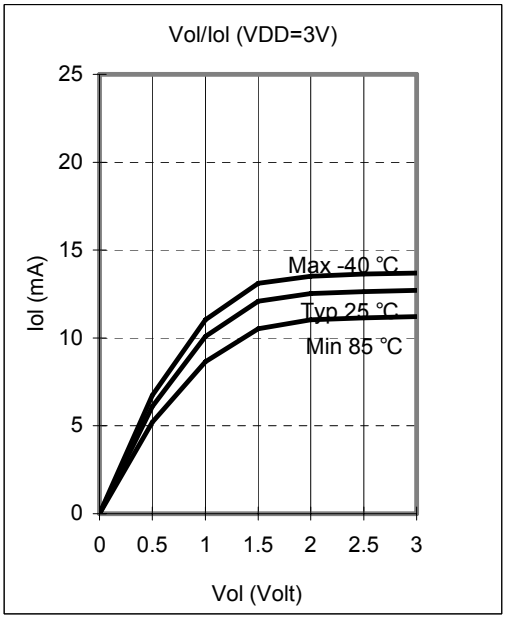


Fig. 21 Port 5, and Port 6 Vol vs. Iol, VDD=3V

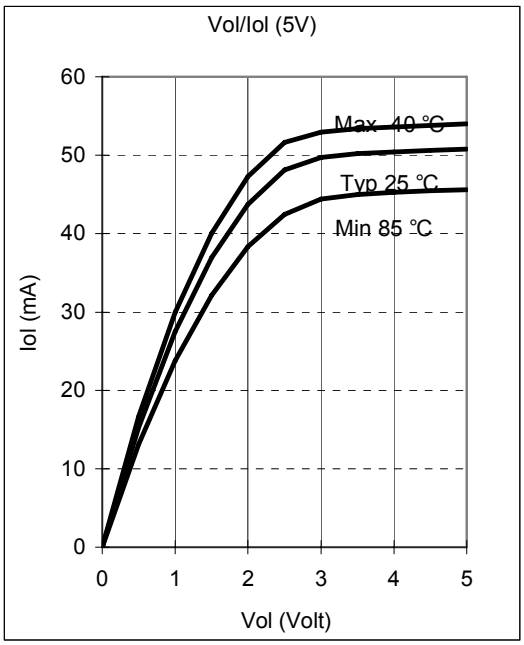


Fig. 22 Port 7 Vol vs. Iol, VDD=5V

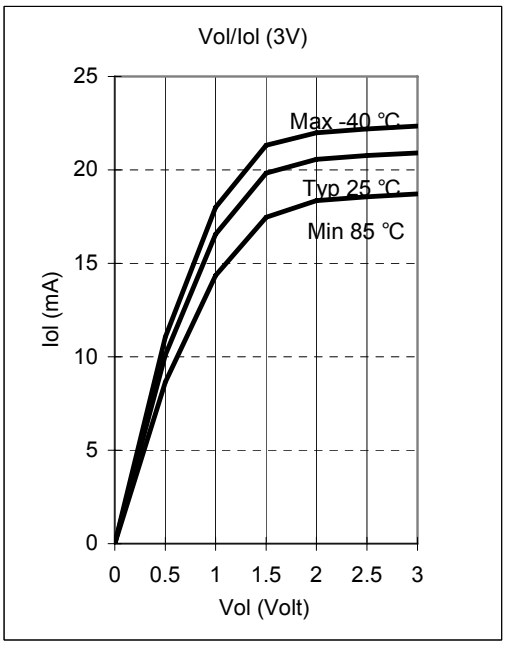


Fig. 23 Port 7 Vol vs. Iol, VDD=3V

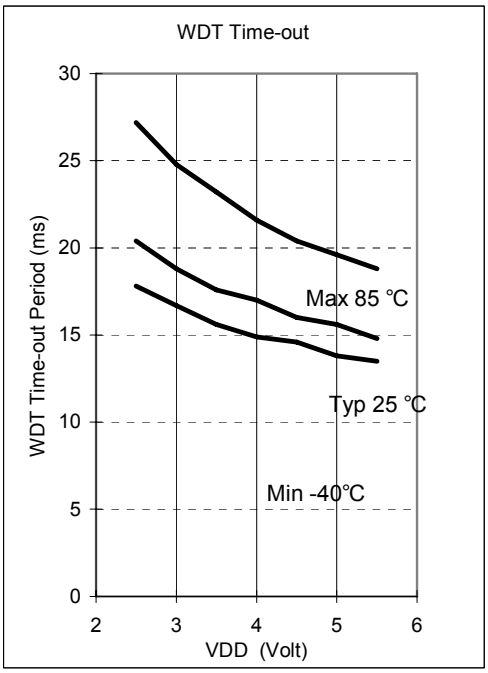


Fig. 24 WDT Time-out Period vs. VDD, Prescaler Set to 1 : 1

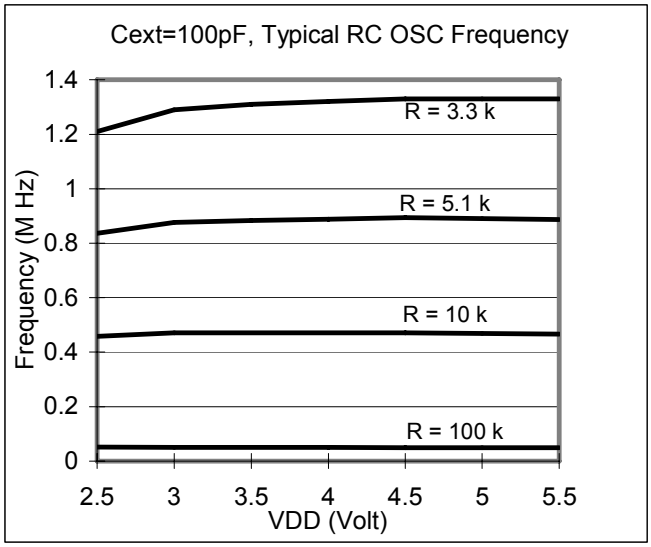


Fig. 25 Typical RC OSC Frequency vs. VDD (Cext=100pF, Temperature at 25℃)

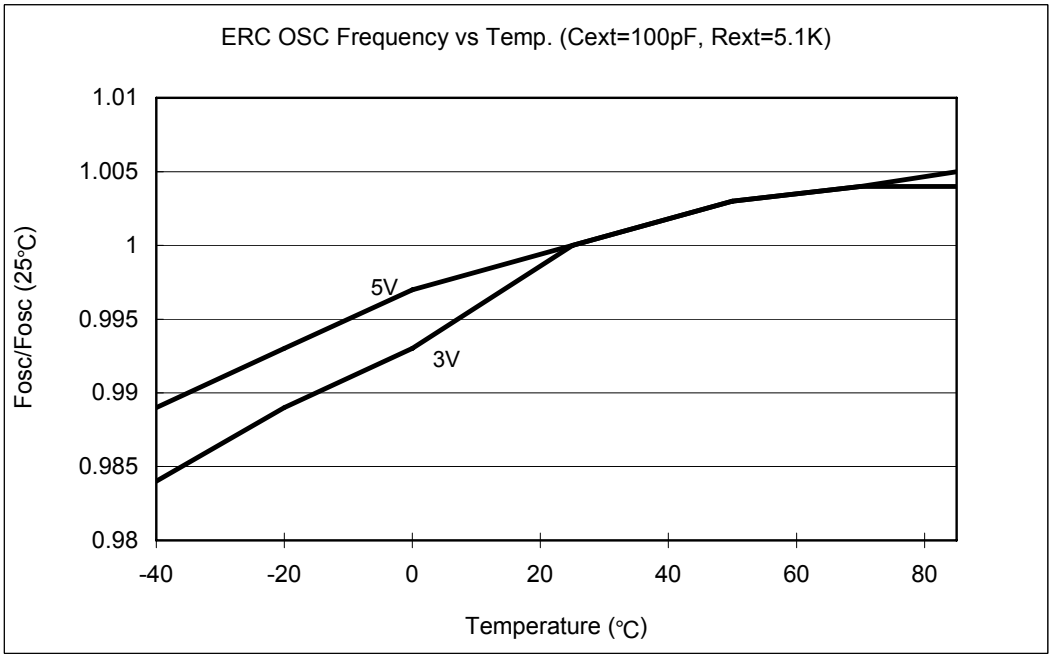


Fig. 26 Typical RC OSC Frequency vs. Temperature (R and C are Ideal Components)

Four conditions exist with the operating current ICC1 to ICC4. These conditions are as follows：

ICC1：VDD=3V, Fosc=32 kHz, 2clocks, WDT disable

ICC2：VDD=3V, Fosc=32 kHz, 2clocks, WDT enable

ICC3：VDD=5V, Fosc=4 MHz, 2clocks, WDT enable

ICC4：VDD=5V, Fosc=10 MHz, 2clocks, WDT enable

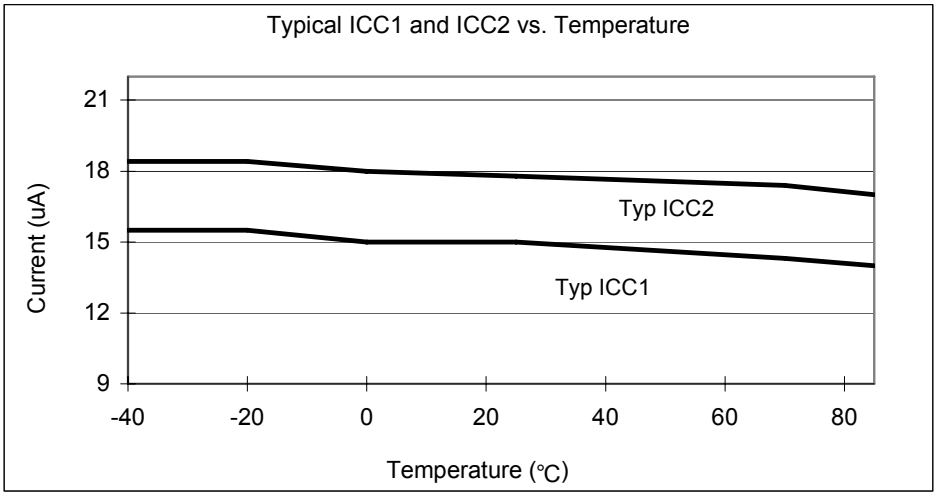


Fig. 27 Typical Operating Current (ICC1 and ICC2) vs. Temperature

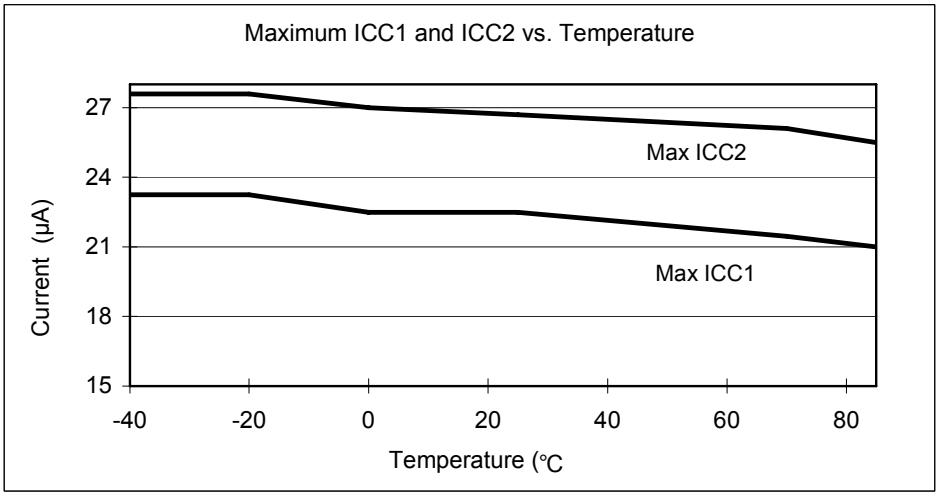


Fig. 28 Maximum Operating Current (ICC1 and ICC2) vs. Temperature

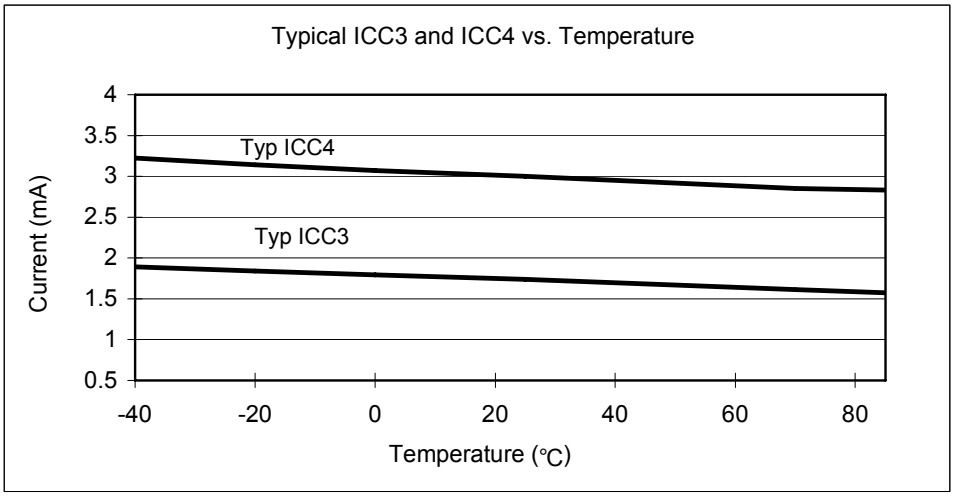


Fig. 29 Typical Operating Current (ICC3 and ICC4) vs. Temperature

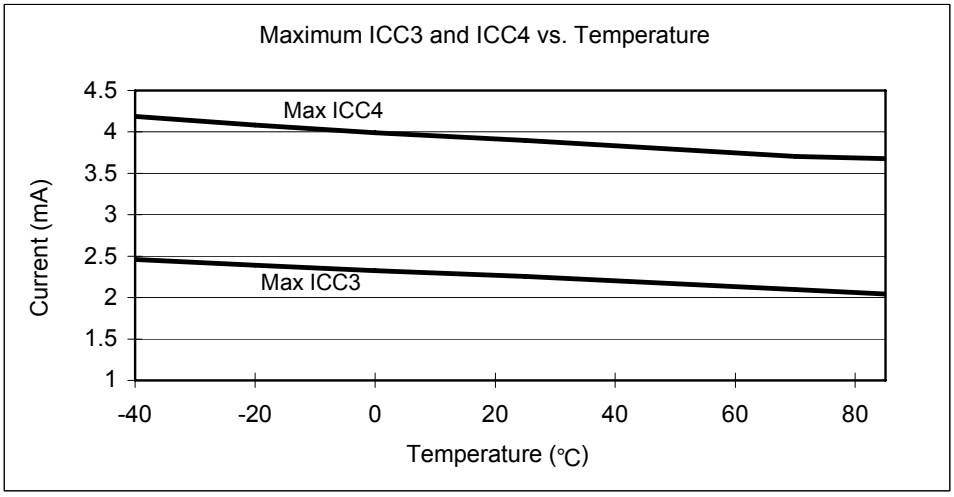


Fig. 30 Maximum Operating Current (ICC3 and ICC4) vs. Temperature

Two conditions exist with the standby current ISB1 and ISB2. These conditions are as follows:

ISB1：VDD=5V, WDT disable

ISB2：VDD=5V, WDT enable

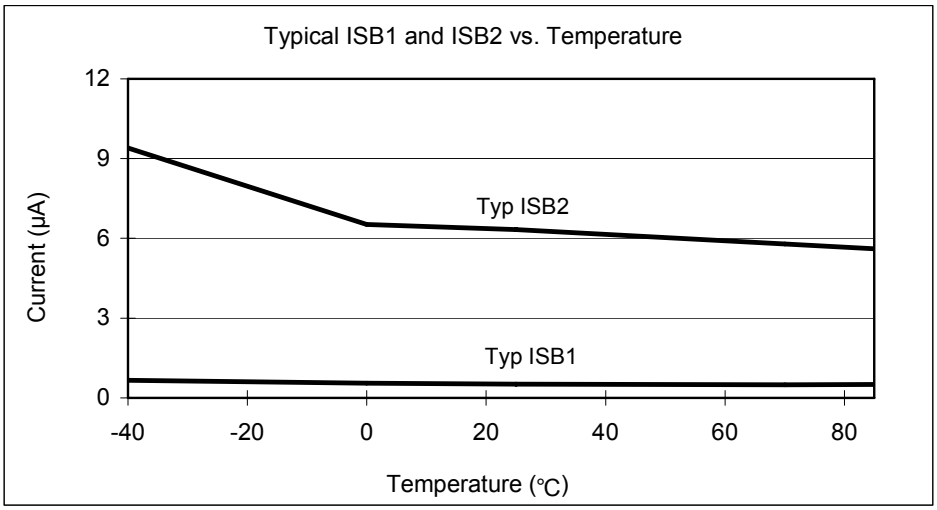


Fig. 31 Typical Standby Current (ISB1 and ISB2) vs. Temperature

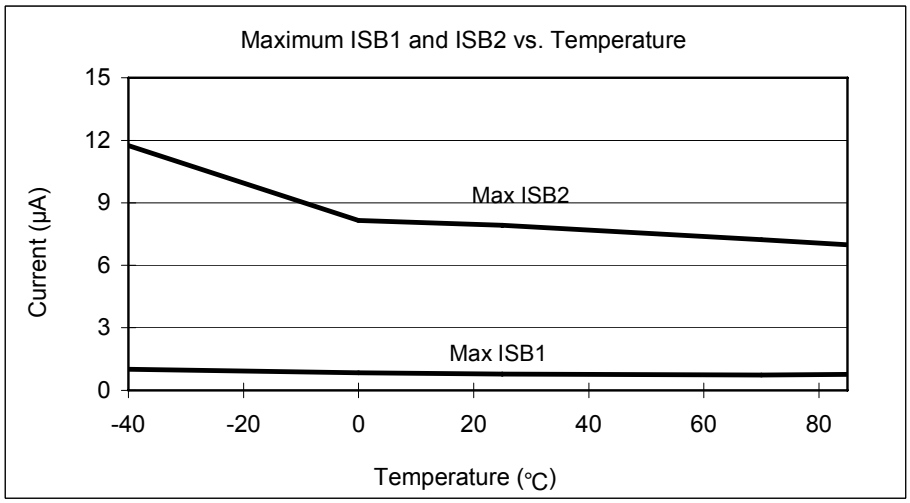


Fig. 32 Maximum Standby Current (ISB1 and ISB2) vs. Temperature

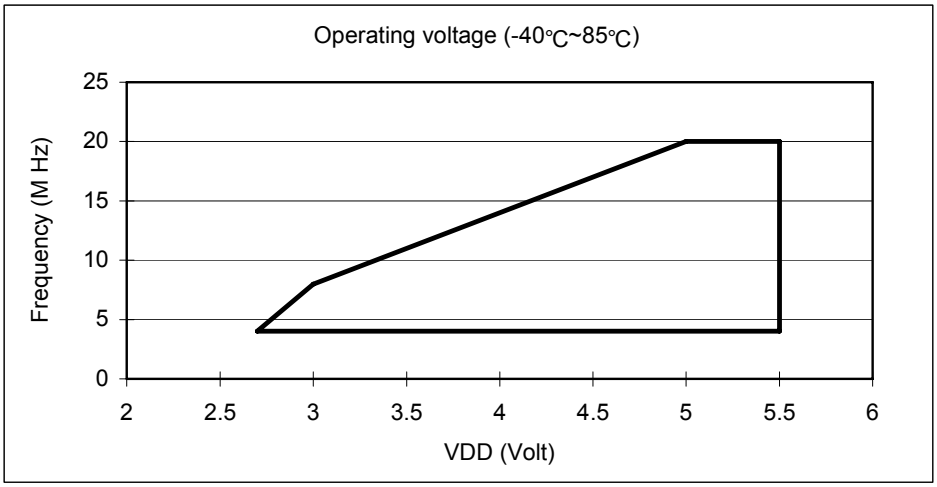


Fig. 33 Operating Voltage and Temperature Range from -40 ℃ to 85 ℃

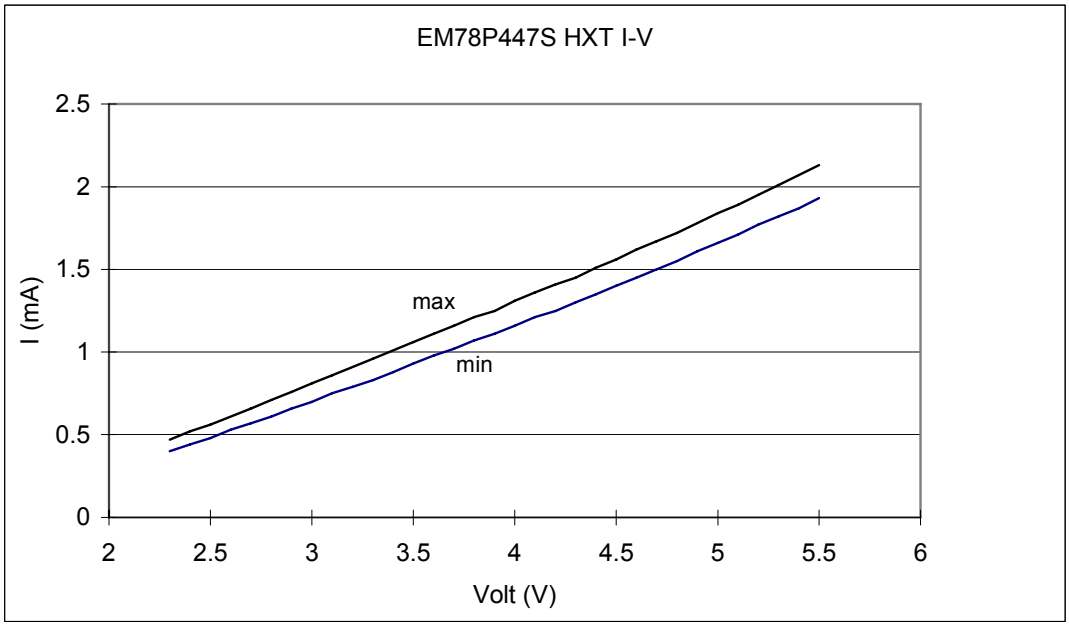


Fig. 34 EM78P447S I-V Curve Operating at 4 MHz

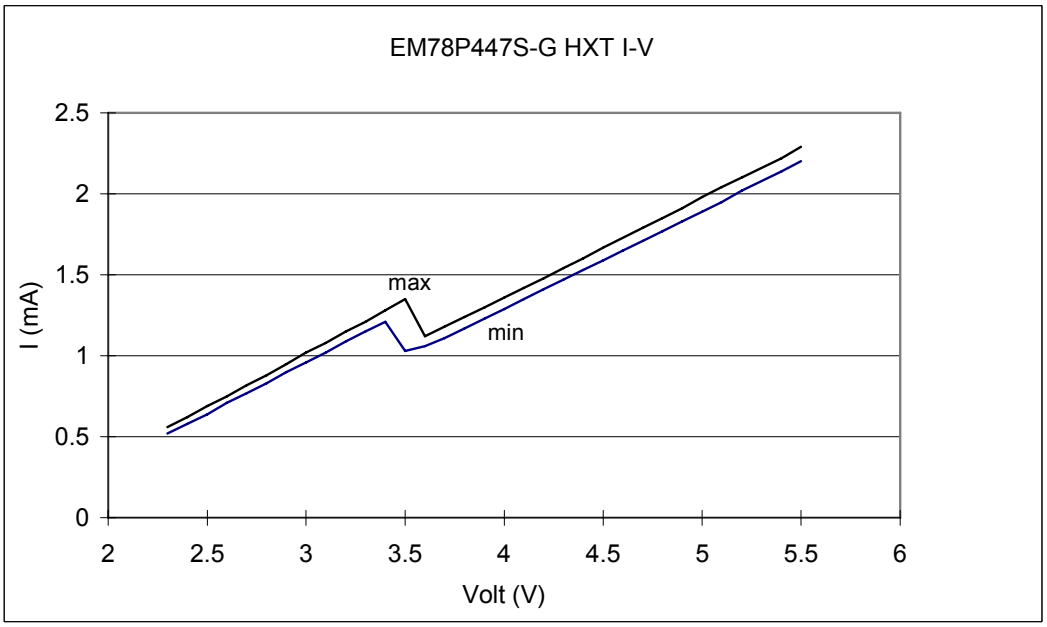


Fig. 35 EM78P447S-G I-V Curve Operating at 4 MHz

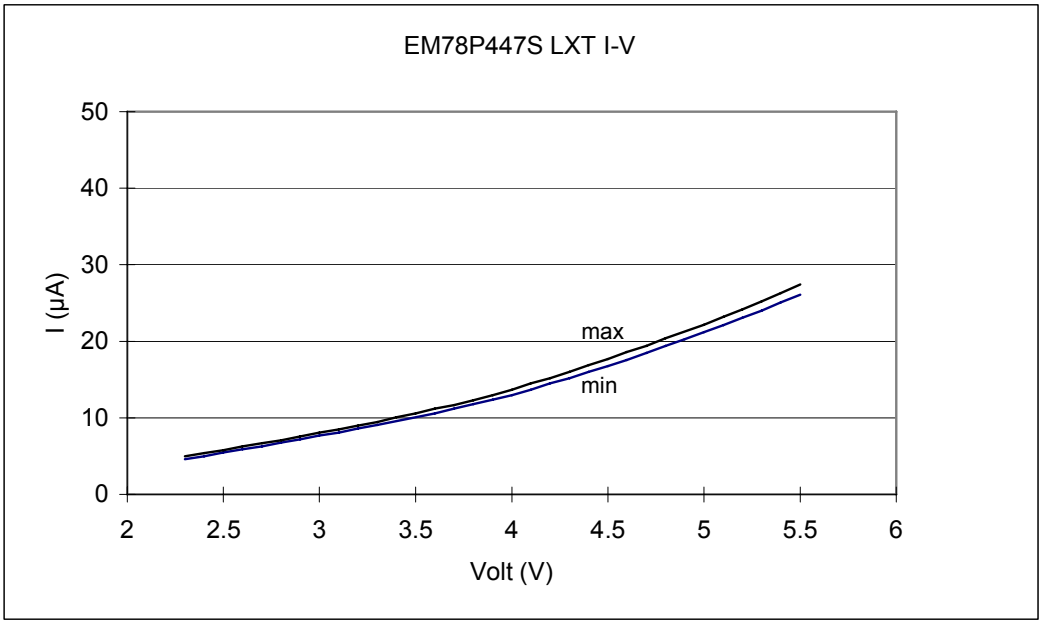


Fig. 36 EM78P447S I-V Curve Operating at 32.768 kHz

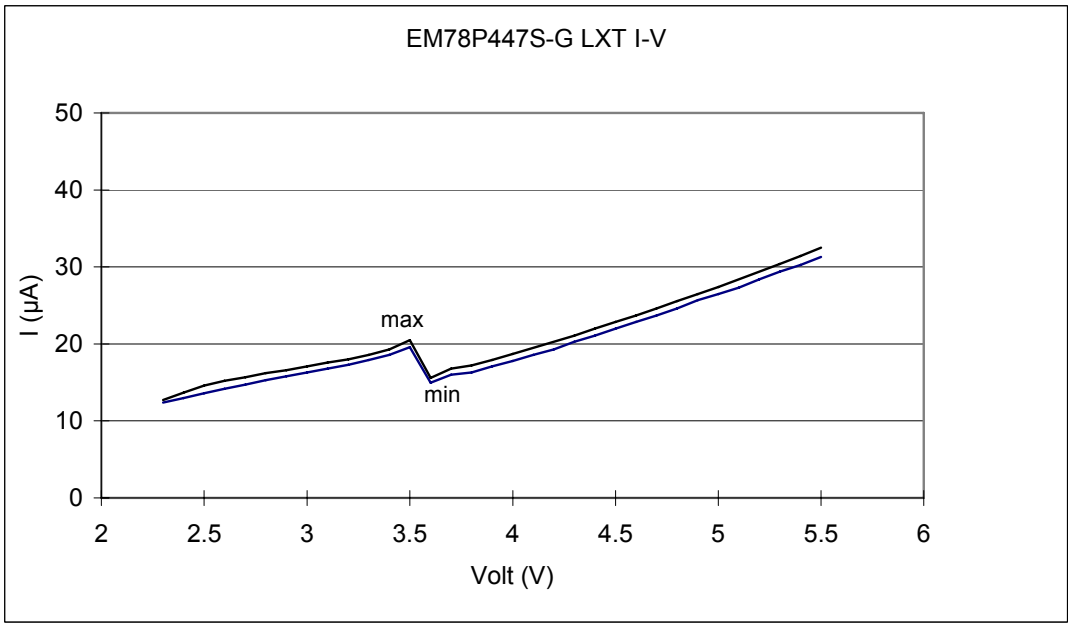


Fig. 37 EM78P447S-G I-V Curve Operating at 32.768 kHz

APPENDIX

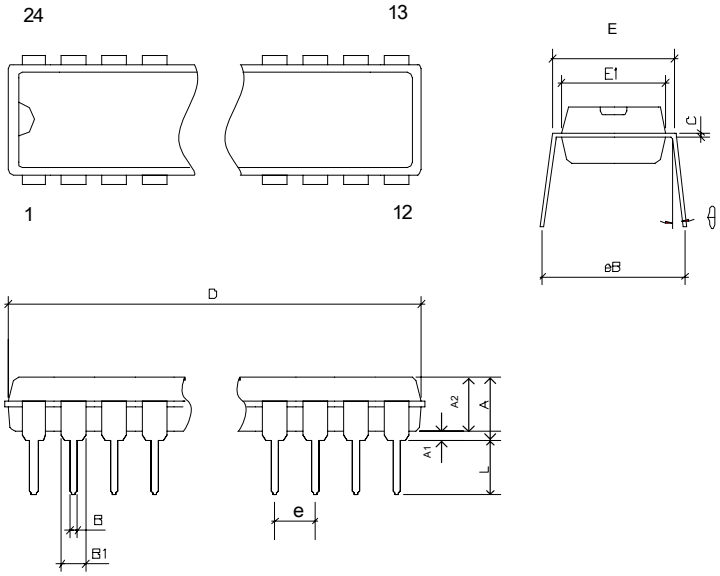
A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P447SAP	DIP	28	600 mil
EM78P447SAM	SOP	28	300 mil
EM78P447SAK	Skinny DIP	28	300 mil
EM78P447SFK	Skinny DIP	28	400 mil
EM78P447SAS	SSOP	28	209 mil
EM78P447SBP	DIP	32	600 mil
EM78P447SBWM	SOP	32	450 mil
EM78P447SBM	SOP	32	300 mil
EM78P447SCK	Skinny DIP	24	300 mil
EM78P447SAPS	DIP	28	600 mil
EM78P447SAMS	SOP	28	300 mil
EM78P447SAKS	Skinny DIP	28	300 mil
EM78P447SFKS	Skinny DIP	28	400 mil
EM78P447SASS	SSOP	28	209 mil
EM78P447SBPS	DIP	32	600 mil
EM78P447SBWMS	SOP	32	450 mil
EM78P447SBMS	SOP	32	300 mil
EM78P447SCKS	Skinny DIP	24	300 mil
EM78P447SCMS	SOP	24	300 mil
EM78P447SAPJ	DIP	28	600 mil
EM78P447SAMJ	SOP	28	300 mil
EM78P447SAKJ	Skinny DIP	28	300 mil
EM78P447SFKJ	Skinny DIP	28	400 mil
EM78P447SASJ	SSOP	28	209 mil
EM78P447SBPJ	DIP	32	600 mil
EM78P447SBWMJ	SOP	32	450 mil
EM78P447SBMJ	SOP	32	300 mil
EM78P447SCKJ	Skinny DIP	24	300 mil
EM78P447SCMJ	SOP	24	300 mil

Note: Part Numbers including “S” or “J” are Green products and do not contain hazardous substances.
These are the third edition of Sony SS-00259 standard.
The Pb content should comply with Sony specs which should be less than 100ppm.

B Package Information

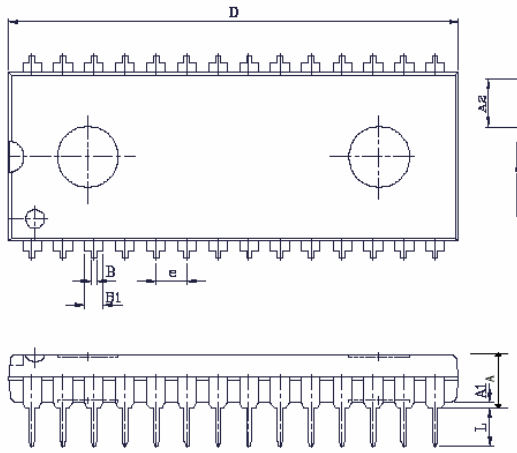
24-Lead Plastic Dual Inline Skinny Package (SDIP) - 300 mil



Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
e_B	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE: PDIP-24L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

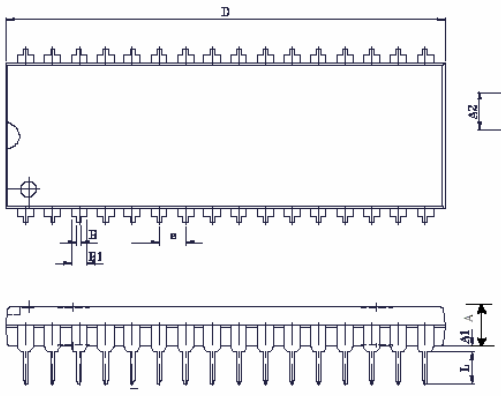
28-Lead Plastic Dual Inline Package (DIP) - 600 mil



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	36.830	37.084	37.338
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

TITLE: PDIP-28L 600MIL PACKAGE OUTLINE DIMENSION	
File : D28	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

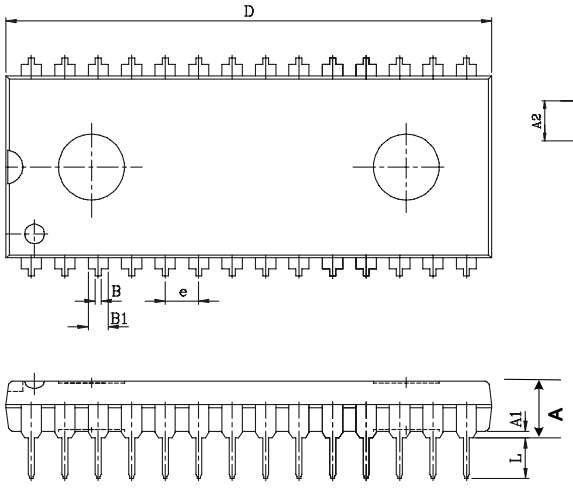
32-Lead Plastic Dual Inline Package (DIP) - 600 mil



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.175	3.937	4.953
c		0.254(TYP)	
D	41.783	41.910	42.164
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.330	0.457	0.584
B1	1.143	1.270	1.397
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

TITLE: PDIP-32L 600MIL PACKAGE OUTLINE DIMENSION	
File : D32	Edition: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

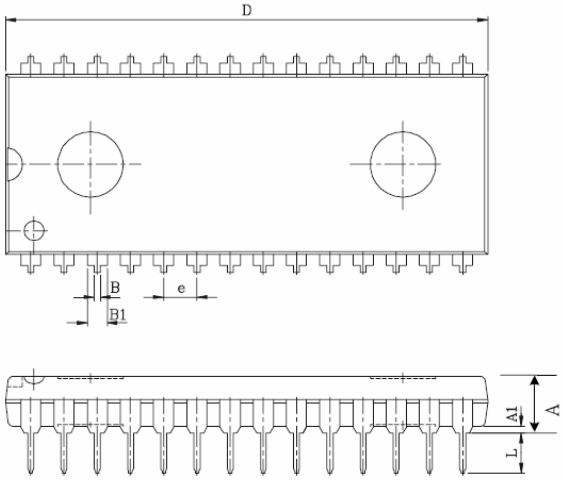
28-Lead Skinny Plastic Dual Inline Package (Skinny DIP) - 300 mil



Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e		2.540(TYP)	
θ°	0		10

TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edition: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

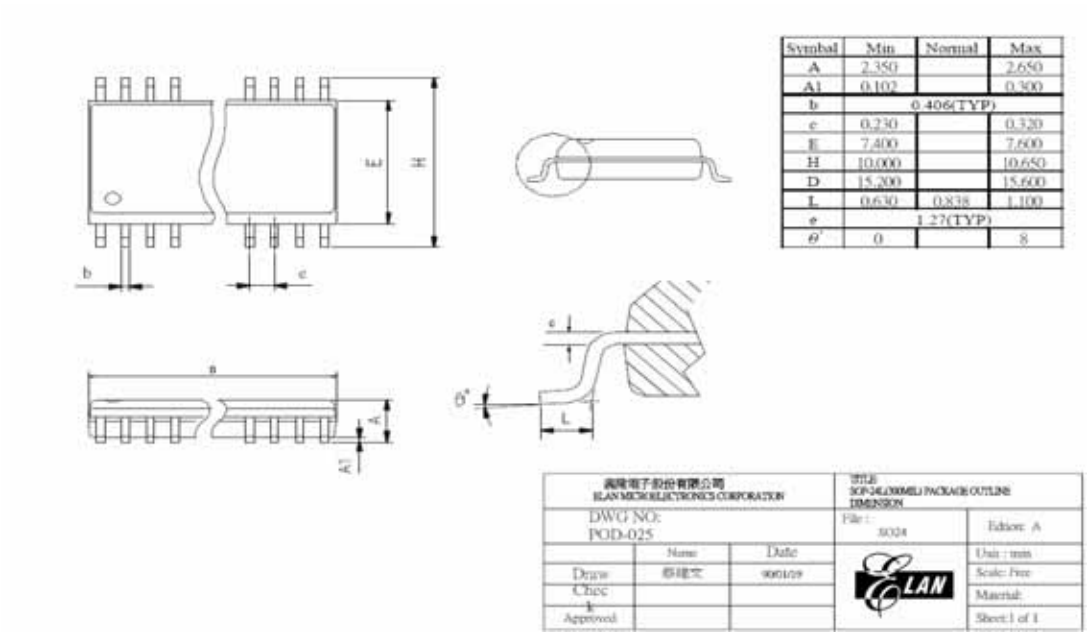
28-Lead Skinny Plastic Dual Inline Package (Skinny DIP) - 400 mil



Symbal	Min	Normal	Max
A			4.360
A1	0.500		
B	0.380	0.460	0.540
B1	0.920	1.000	1.080
c	0.200	0.250	0.300
E		10.160	
E1	8.640	8.890	9.140
L	3.000		
e		1.778	
θ	0		10

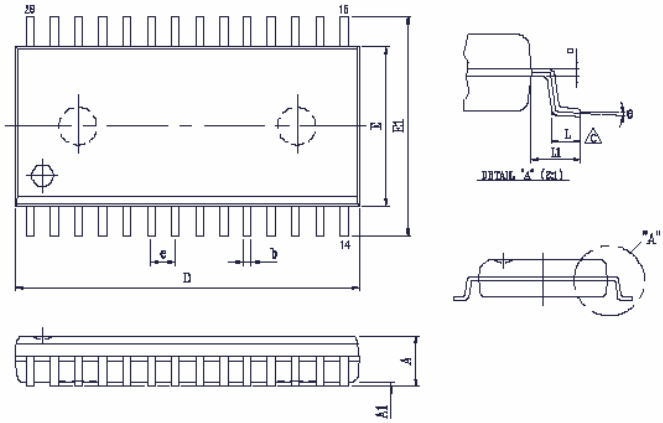
義隆電子股份有限公司 ELAN MICROELECTRONICS CORPORATION			TITLE: PDIP-28L SKINNY 40 0MIL PACKAGE OUTLINE DIME NSION	
DWG NO: POD-079			File : K28A	Edtion: A
	Name	Date		Unit : mm
Draw	鍾玉真	96/5/24		Scale: Free
Check	何明龍	96/5/24		Material:
Approved				Sheet:1 of 1

24-Lead Plastic Small Outline Package (SOP) - 300 mil



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e		1.27(TYP)	
θ	0		8

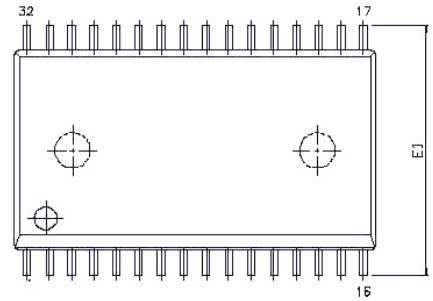
28-Lead Plastic Small Outline Package (SOP) - 300 mil



Symbol	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ	0		8

TITLE:
SOP-28L(300MIL) PACKAGE OUTLINE
DIMENSION
File : SO28
Edition: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

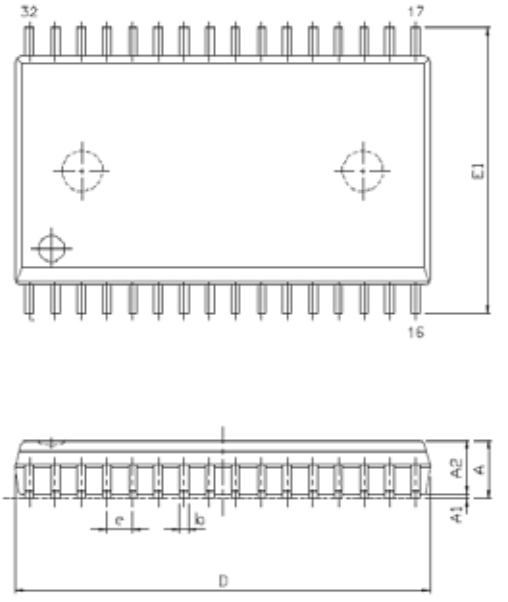
32-Lead Plastic Small Outline Package (SOP) - 300 mil



Symbal	Min	Normal	Max
A	2.540		3.048
A1	0.102		0.350
A2	2.540	2.642	2.744
b	0.350		0.500
c	0.254(TYP)		
E	11.176	11.303	11.430
E1	13.692	14.097	14.502
D	20.300	20.500	20.700
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-32L(450MIL) PACKAGE OUTLINE DIMENSION	
File : SO32	Edition: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

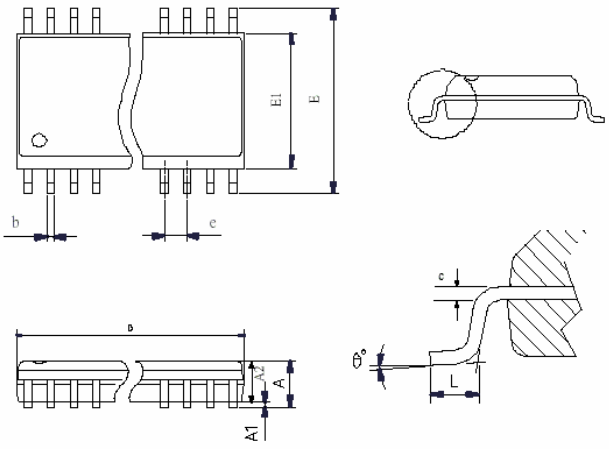
32-Lead Plastic Small Outline Package (SOP) - 450 mil



Symbal	Min	Normal	Max
A	2.540		3.048
A1	0.102		0.350
A2	2.540	2.642	2.744
b	0.350		0.500
c	0.254(TYP)		
E	11.176	11.303	11.430
E1	13.692	14.097	14.502
D	20.300	20.500	20.700
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e	1.27(TYP)		
θ°	0		8

義隆電子股份有限公司 ELAN MICROELECTRONICS CORPORATION			TITLE: SOP-32L(450MIL) PACKAGE OUTLINE DIMENSION
DWG NO: POD-028			File : SO32 / Edition: A
	Name	Date	Unit : mm
Draw	蔡建文	99/12/20	Scale: Free
Chec k			Material:
Approved			Sheet:1 of 1

28-Lead Shrink Small Outline Package (SSOP) - 209 mil



Symbal	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	9.900	10.200	10.500
L	0.630	0.900	1.030
e	0.650(TYP)		
θ°	0	4	8

TITLE: SSOP-28L(209MIL) OUTLINE PACKAGE PACKA OUTLINE DIMENSION	
File : SSO28	Edition: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

C EM78P447S Program Pin List

DWTR is used to program the EM78P447S IC's. The connector of DWTR is selected by CON3 (EM78P447S). The software is selected by EM78P447S.

Program Pin Name	IC Pin Name	28-DIP Pin No.	32-DIP Pin No.
VPP	/RESET	28	30
ACLK	OSCO	26	28
DINCK	P77	25	27
DATAIN	P76	24	26
/PGMB	P75	23	25
/OEB	P74	22	24
VDD	VDD	2	4
VSS	VSS	4	6

Wiring Diagram for ELAN DWTR