

## Document Title

128K x8 bit Low Power and Low Voltage CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	August 12, 1995	Preliminary
1.0	Finalize	April 12, 1996	Final
2.0	Revise - Change datasheet format	March 7, 1998	Final

---

The attached datasheets are provided by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications and products. SAMSUNG Electronics will answer to your questions about device. If you have any questions, please contact the SAMSUNG branch offices.

---



Revision 2.0  
March 1998

## 128K x8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology : Poly Load
- Organization : 128Kx8
- Power Supply Voltage :
  - KM68V1000B family : 3.0~3.6V
  - KM68U1000B family : 2.7~3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP, 32-TSOP1-0820F/R

### GENERAL DESCRIPTION

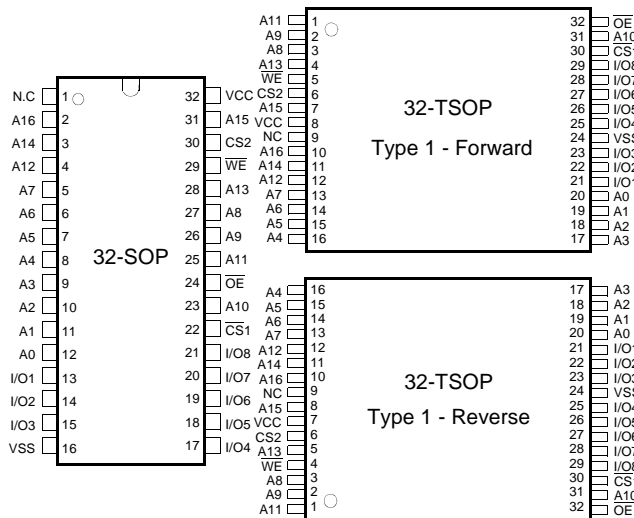
The KM68V1000B and KM68U1000B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I <sub>sb1</sub> , Max)	Operating (I <sub>cc2</sub> , Max)	
KM68V1000BL/L-L KM68U1000BL/L-L	Commercial(0~70°C)	3.0~3.6V 2.7~3.3V	70 <sup>1)</sup> /100 100	50/15μA 50/15μA	40mA	32-SOP 32-TSOP1- R/F
KM68V1000BLE/LE-L KM68U1000BLE/LE-L	Extended(-25~85°C)	3.0~3.6V 2.7~3.3V	70 <sup>1)</sup> /100 100	100/20μA 50/15μA		
KM68V1000BLI/LI-L KM68U1000BLI/LI-L	Industrial(-40~85°C)	3.0~3.6V 2.7~3.3V	70 <sup>1)</sup> /100 100	100/20μA 50/15μA		

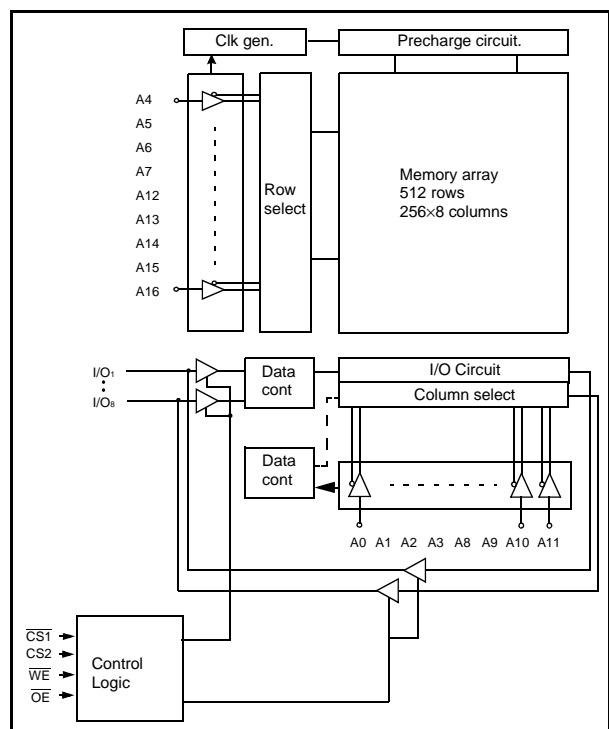
1. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function
CS <sub>1</sub> , CS <sub>2</sub>	Chip Select Inputs
OE	Output Enable Input
WE	Write Enable Input
A <sub>0</sub> -A <sub>16</sub>	Address Inputs
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

### FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

## PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000BLG-7	32-SOP,70ns,3.3V,L	KM68V1000BLGE-7	32-SOP,70ns,3.3V,L	KM68V1000BLGI-7	32-SOP,70ns,3.3V,L
KM68V1000BLG-10	32-SOP,100ns,3.3V,L	KM68V1000BLGE-10	32-SOP,100ns,3.3V,L	KM68V1000BLGI-10	32-SOP,100ns,3.3V,L
KM68V1000BLT-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTE-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTI-7	32-TSOP F,70ns,3.3V,L
KM68V1000BLT-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTE-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTI-10	32-TSOP F,100ns,3.3V,L
KM68V1000BLR-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRE-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRI-7	32-TSOP R,70ns,3.3V,L
KM68V1000BLR-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRE-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRI-10	32-TSOP R,100ns,3.3V,L
KM68V1000BLG-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGE-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGI-7L	32-SOP,70ns,3.3V,LL
KM68V1000BLG-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGE-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGI-10L	32-SOP,100ns,3.3V,LL
KM68V1000BLT-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTE-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTI-7L	32-TSOP F,70ns,3.3V,LL
KM68V1000BLT-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTE-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTI-10L	32-TSOP F,100ns,3.3V,LL
KM68V1000BLR-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRE-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRI-7L	32-TSOP R,70ns,3.3V,LL
KM68V1000BLR-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRE-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRI-10L	32-TSOP R,100ns,3.3V,LL
KM68U1000BLG-10	32-SOP,100ns,3.0V,L	KM68U1000BLGE-10	32-SOP,100ns,3.0V,L	KM68U1000BLGI-10	32-SOP,100ns,3.0V,L
KM68U1000BLT-10	32-TSOP F,100ns,3.0V,L	KM68U1000BLTE-10	32-TSOP F,100ns,3.0V,L	KM68U1000BLTI-10	32-TSOP F,100ns,3.0V,L
KM68U1000BLR-10	32-TSOP R,100ns,3.0V,L	KM68U1000BLRE-10	32-TSOP R,100ns,3.0V,L	KM68U1000BLRI-10	32-TSOP R,100ns,3.0V,L
KM68U1000BLG-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLGE-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLGI-10L	32-SOP,100ns,3.0V,LL
KM68U1000BLT-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000BLTE-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000BLTI-10L	32-TSOP F,100ns,3.0V,LL
KM68U1000BLR-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000BLRE-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000BLRI-10L	32-TSOP R,100ns,3.0V,LL

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low status.)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OU</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on V <sub>CC</sub> supply relative to Vss	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	0.7	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM68V1000BL, KM68U1000BL
		-25 to 85	°C	KM68V1000BLE, KM68U1000BLE
		-40 to 85	°C	KM68V1000BLI, KM68U1000BLI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	KM68V1000B Family	3.0	3.3	3.6	V
		KM68U1000B Family	2.7	3.0	3.3	
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	KM68V1000B, KM68U1000B Family	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	KM68V1000B, KM68U1000B Family	-0.3 <sup>3)</sup>	-	0.4	V

Note:

- Commercial Product : TA=0 to 70°C, unless otherwise specified  
Extended Product : TA=-25 to 85°C, unless otherwise specified  
Industrial Product : TA=-40 to 85°C, unless otherwise specified
- Overshoot : V<sub>CC</sub>+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested

## CAPACITANCE<sup>1)</sup> (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

- Capacitance is sampled not, 100% tested

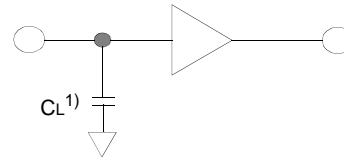
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	$\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>IO</sub> =0mA	-	2	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1\leq 0.2V$ , $CS_2\geq V_{CC}-0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	3	5	mA	
	I <sub>CC2</sub>	Min cycle, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$	-	30	40	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , $CS_2=V_{IL}$	-	-	0.3	mA	
Standby Current (CMOS)	KM68V1000BL/L-L	I <sub>SB1</sub> $\overline{CS}_1\geq V_{CC}-0.2V$ $CS_2\geq V_{CC}-0.2V$ or $CS_2\leq 0.2V$ Other input =0~V <sub>CC</sub>	Low Power	-	1.0	50	μA
	Low Low Power		-	0.5	15		
	KM68V1000BLE/LE-L KM68V1000BLI/LI-L		Low Power	-	1.0	100	μA
	Low Low Power		-	0.5	20		
KM68U1000BL/L-L	Low Power	-	1.0	50	μA		
Low Low Power	-	0.5	15				
KM68U1000BLE/LE-L KM68U1000BLI/LI-L	Low Power	-	1.0	50	μA		
Low Low Power	-	0.5	15				

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load(see right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS (Commercial product : $T_A=0$ to $70^\circ\text{C}$ , Extended product : $T_A=-25$ to $85^\circ\text{C}$ , Industrial product : $T_A=-40$ to $85^\circ\text{C}$ )

KM68V1000B Family:  $V_{CC}=3.0\sim 3.6\text{V}$ , KM68U1000B Family:  $V_{CC}=2.7\sim 3.3\text{V}$ )

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	70	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	70	-	100	ns
	Chip select to output	t <sub>CO</sub>	-	70	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	35	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	70	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	60	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	60	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	55	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	30	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

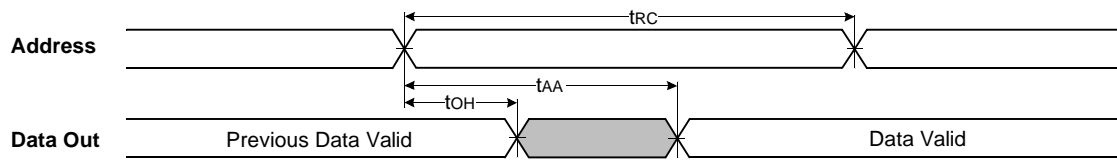
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V	
Data retention current	I <sub>DR</sub>	V <sub>CC</sub> =3.0V $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ $CS_2 \geq V_{CC}-0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	Low Power	-	1	30	$\mu\text{A}$
			Low Low Power	-	0.5	15	
			Low Power	-	-	50	
			Low Low Power	-	-	20	
			Low Power	-	-	25	
			Low Low Power	-	-	10	
			Low Power	-	-	25	
			Low Low Power	-	-	15	
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms	
Recovery time	t <sub>RDR</sub>		5	-	-		

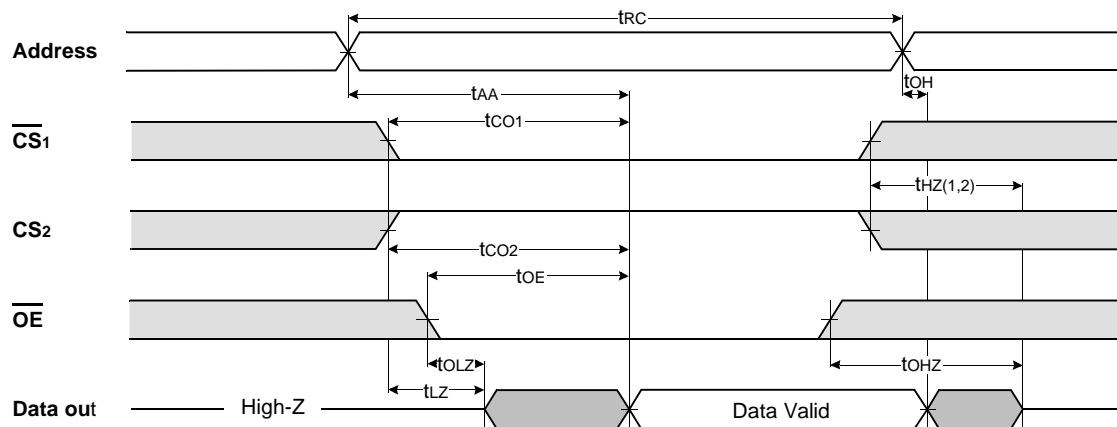
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $CS_2 \geq V_{CC}-0.2\text{V}$  ( $\overline{CS}_1$  controlled) or  $CS_2 \leq 0.2\text{V}$  ( $CS_2$  controlled)

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



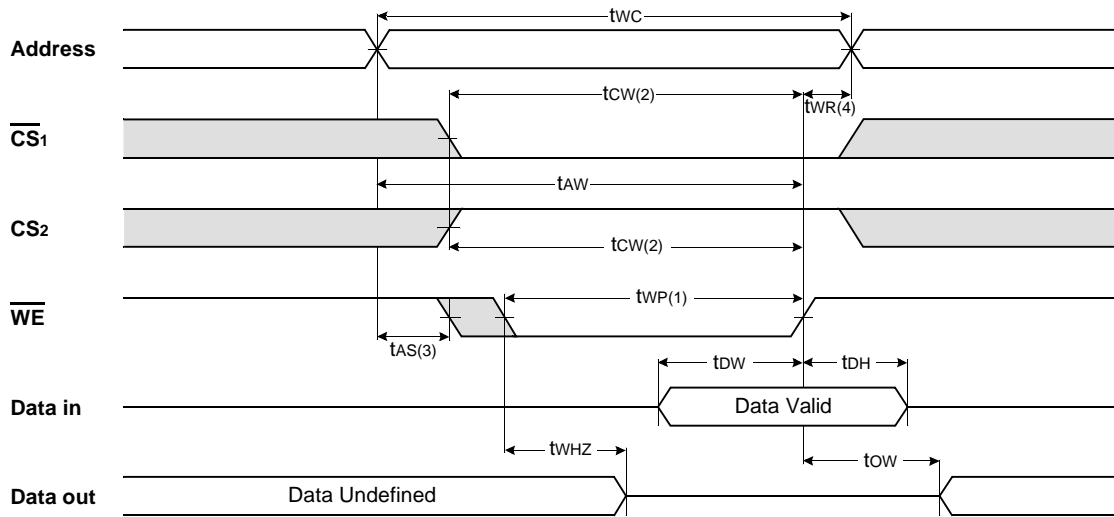
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



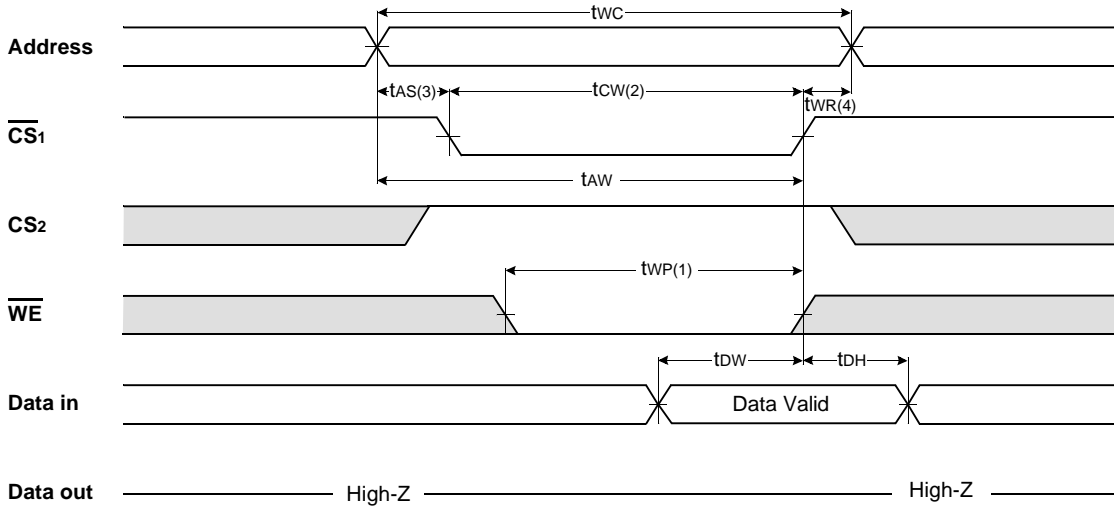
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

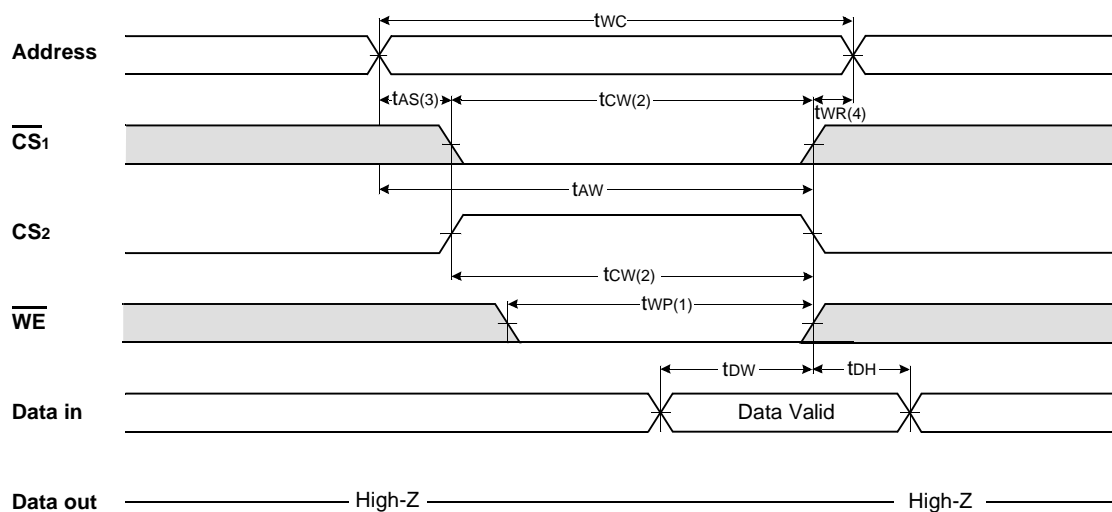
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}_1$  Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}_1$ Controlled)

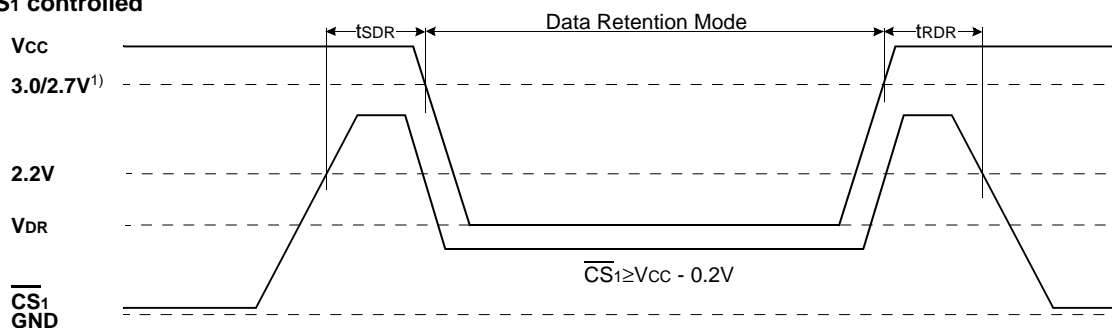


### NOTES (WRITE CYCLE)

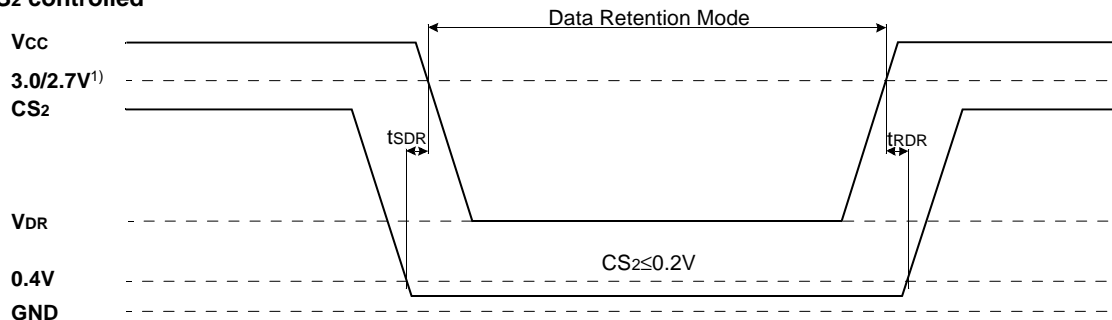
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low : A write end at the earliest transition among  $CS_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR(2)}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### $CS_2$ controlled



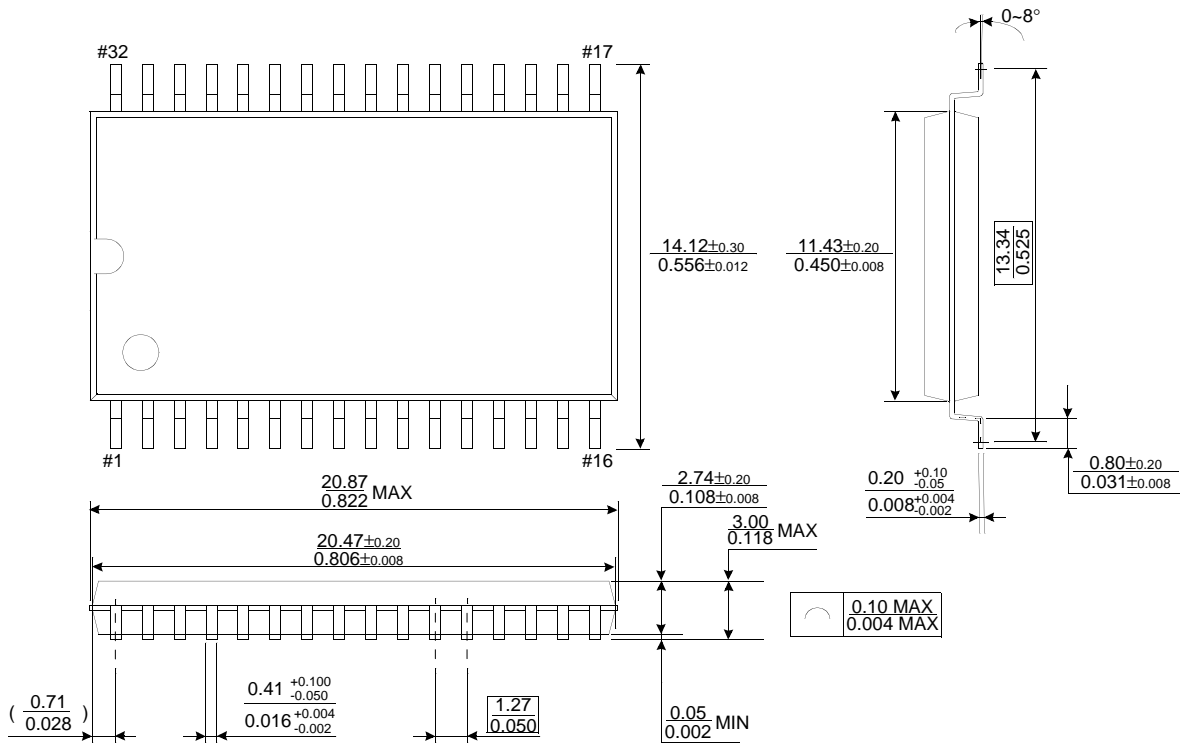
1. 3.0V for KM68V1000B Family , 2.7V for KM68U1000B Family



## PACKAGE DIMENSIONS

Units : millimeter(inch)

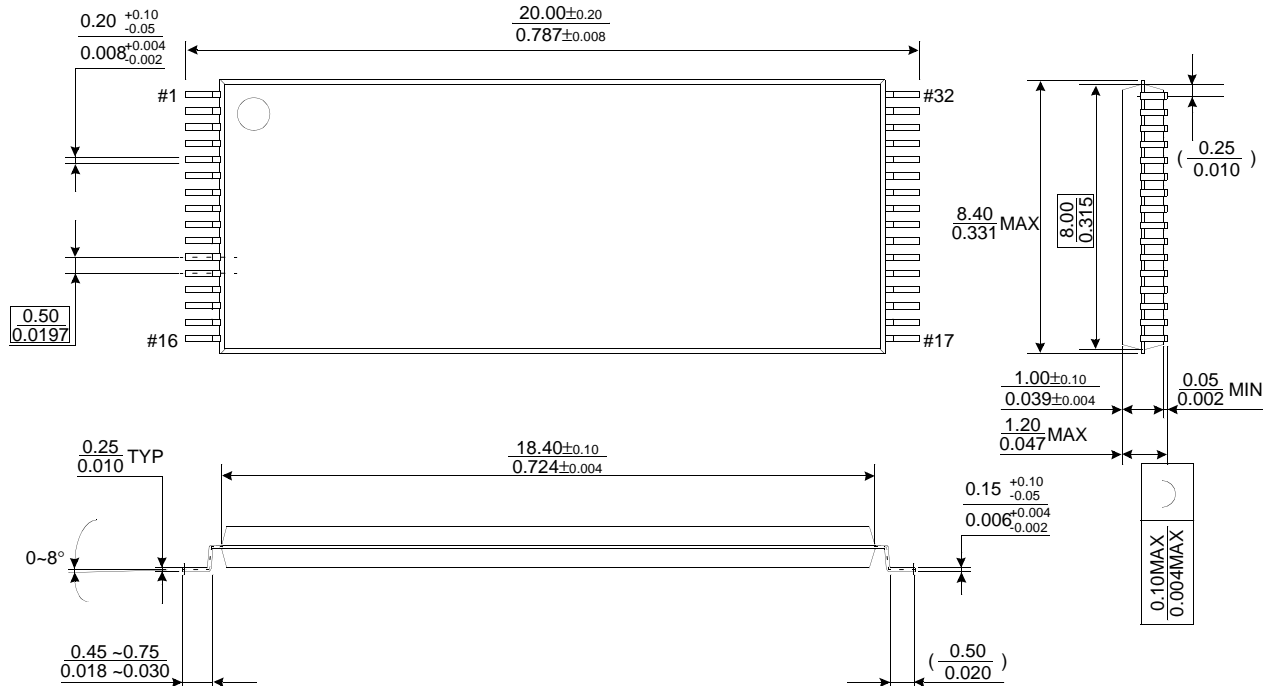
### 32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



## PACKAGE DIMENSIONS

Units : millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820R)

