64Mb H-die (x32) SDRAM Specification

Revision 1.4

August 2004

*Samsung Electronics reserves the right to change products or specification without notice.

Revision History

Revision 0.0 (June, 2003)
- Target spec First release.

Revision 0.1 (July, 2003)
- Delete speed 4.5ns.

Revision 0.2 (September, 2003)
- Preliminary spec release.

Revision 1.0 (November, 2003)
- Final spec release.

Revision 1.1 (December, 2003)
- Corrected typo.

Revision 1.2 (December, 2003)
- Modified load cap 50pF -> 30pF & Typo.

Revision 1.3 (February, 2004)
- Corrected typo.

Revision 1.4 (August, 2004)
- Corrected typo.

512K x 32Bit x 4 Banks SDRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period(4K Cycle)

GENERAL DESCRIPTION

The K4S643232H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

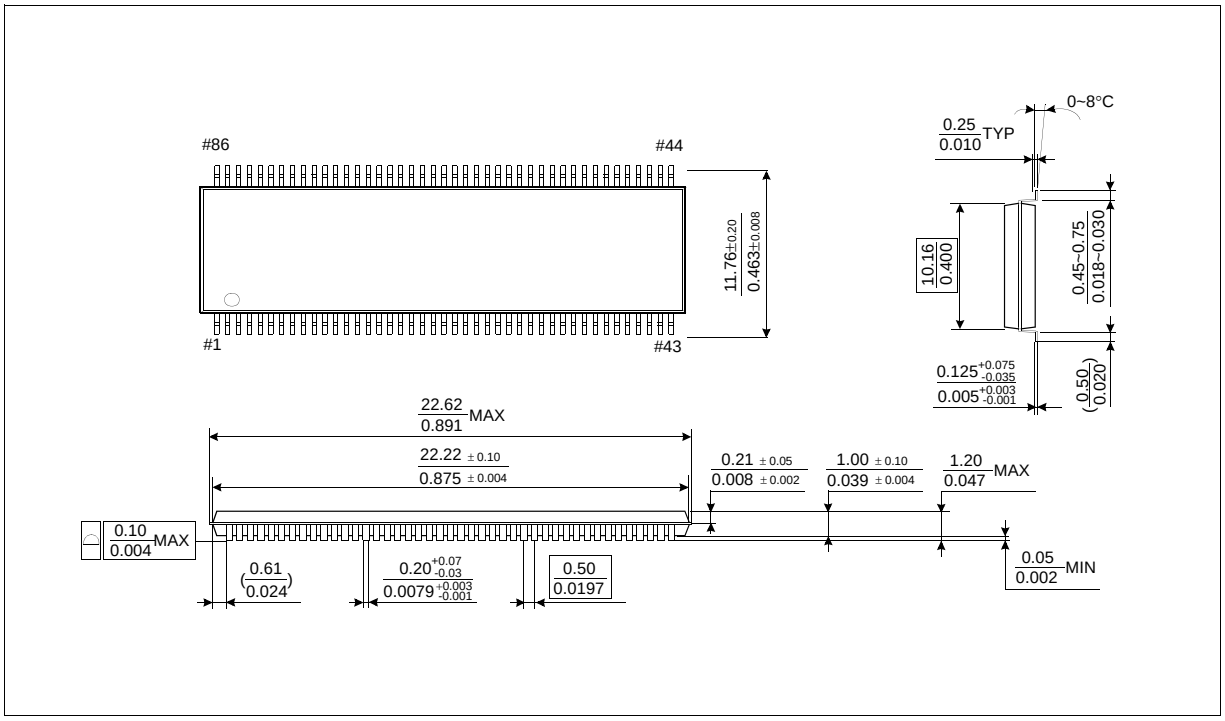
Ordering Information

Part No.	Orgainization	Max Freq.	Interface	Package
K4S643232H-TC/L70	2Mb x 32	143MHz(CL=3)	LVTTL	86pin TSOP(II)
K4S643232H-TC/L60		166MHz(CL=3)		
K4S643232H-TC/L55		183MHz(CL=3)		
K4S643232H-TC/L50		200MHz(CL=3)		

Organization	Row Address	Column Address
2Mx32	A0~A10	A0-A7

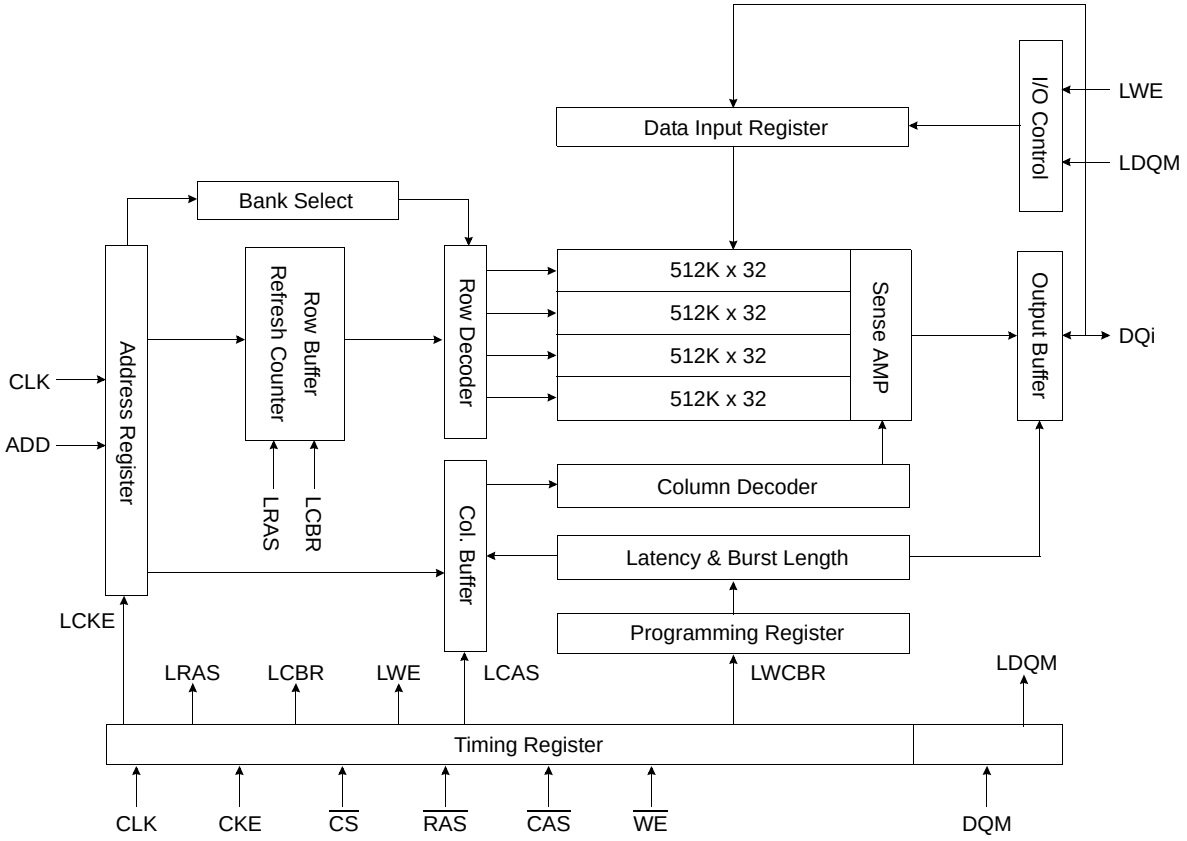
Row & Column address configuration

Package Physical Dimension

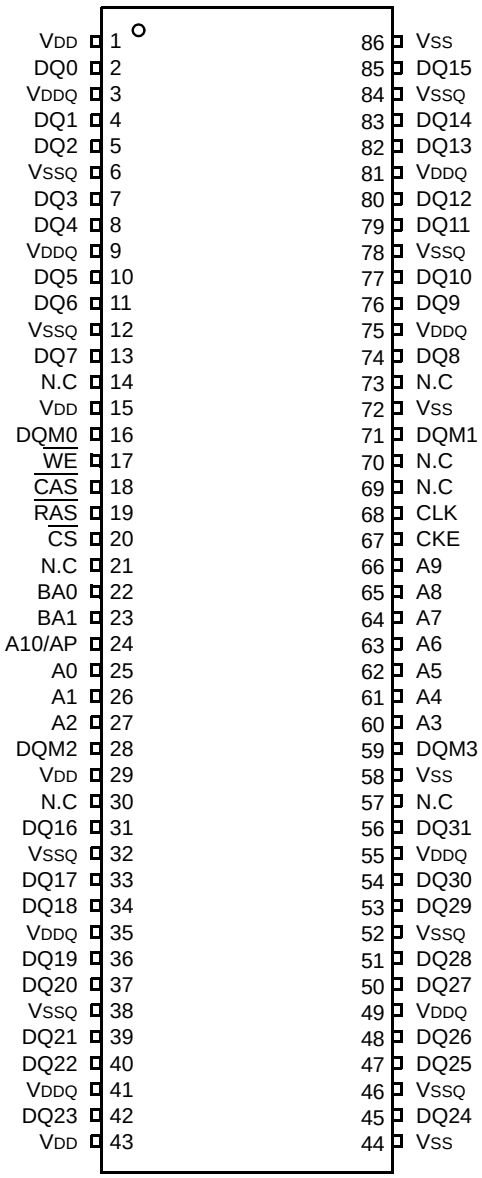


86Pin TSOP(II) Package Dimension

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top view)



86Pin TSOP (II)
(400mil x 875mil)
(0.5 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode.
A_0 ~ A_{10}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
BA0,1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 3	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 31}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	*No Connection*	This pin is recommended to be left No connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	-	4	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	-	4.5	pF
Address	C_{ADD}	-	4.5	pF
DQ_0 ~ DQ_{31}	C_{OUT}	-	6.5	pF

DC CHARACTERISTICS

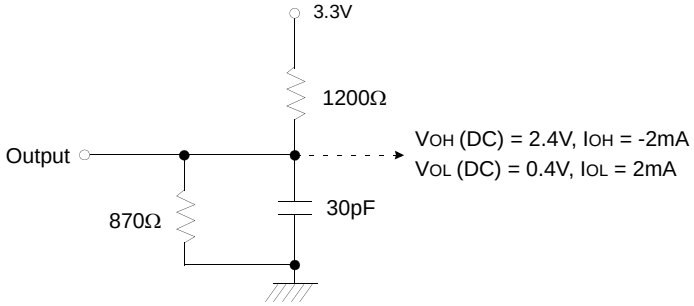
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C

Parameter	Symbol	Test Condition	CAS Latency	Speed				Unit	Note
				50	55	60	70		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min), $t_{CC} \geq t_{CC}$(min), I_O = 0mA	3	140	140	130	130	mA	2
			2	110					
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2				mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2					
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 30ns		12				mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		7					
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		4				mA	
	I_{CC3PS}	CKE ≤ V_{IL}(max), t_{CC} = ∞		4					
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 30ns		40				mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		35					
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA, Page Burst All bank Activated, t_{CCD} = t_{CCD}(min)	3	170	160	150	140	mA	2
			2	120					
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	150	150	140	120	mA	3
			2	120					
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	C	2				mA	4
			L	450				uA	5

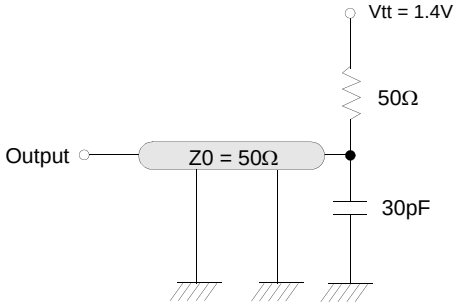
Notes : 1. Unless otherwise notes, Input level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}) in LVTTL.
2. Measured with outputs open.
3. Refresh period is 64ms.
4. K4S643232H-TC
5. K4S643232H-TL

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	50		55		60		70		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS	tCC	5	1000	5.5	1000	6	1000	7	1000	ns	1
	CAS		10		10		10		10			
Row active to row active delay		tRRD(min)	2								CLK	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	3	2	3	2	3	2	3	2	CLK	1
Row precharge time		tRP(min)	3	2	3	2	3	2	3	2	CLK	1
Row active time		tRAS(min)	8	5	7	5	7	5	7	5	CLK	1
		tRAS(max)	100								us	
Row cycle time		tRC(min)	11	7	10	7	10	7	10	7	CLK	1
Last data in to row precharge		tRDL(min)	2								CLK	2
Last data in to new col.address delay		tCDL(min)	1								CLK	2
Last data in to burst stop		tBDL(min)	1								CLK	2
Col. address to col. address delay		tCCD(min)	1								CLK	3
Mode Register Set cycle time		tMRS(min)	2								CLK	
Number of valid output data	CAS Latency=3		2								ea	4
	CAS Latency=2		1									

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	50		55		60		70		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	tCC	5	1000	5.5	1000	6	1000	7	1000	ns	1
	CAS Latency=2		10		10		10		10			
CLK to valid output delay	CAS Latency=3	tSAC	-	4.5	-	5.0	-	5.5	-	5.5	ns	1, 2
	CAS Latency=2		-	6	-	6	-	6	-	6		
Output data hold time		tOH	2	-	2	-	2	-	2	-	ns	2
CLK high pulse width	CAS Latency=3	tCH	2	-	2	-	2.5	-	3	-	ns	3
	CAS Latency=2		3	-	3	-	3	-	3	-		
CLK low pulse width	CAS Latency=3	tCL	2	-	2	-	2.5	-	3	-	ns	3
	CAS Latency=2		3	-	3	-	3	-	3	-		
Input setup time	CAS Latency=3	tSS	1.5	-	1.5	-	1.5	-	1.75	-	ns	3
	CAS Latency=2		2.5	-	2.5	-	2.5	-	2.5	-		
Input hold time		tSH	1	-	1	-	1	-	1	-	ns	3
CLK to output in Low-Z		tSLZ	1	-	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	4.5	-	5.0	-	5.5	-	5.5	ns	-
	CAS latency=2		-	6	-	6	-	6	-	6		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)