LH52258A

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25 ns
- Low-Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- JEDEC Standard Pinout
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52258A is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

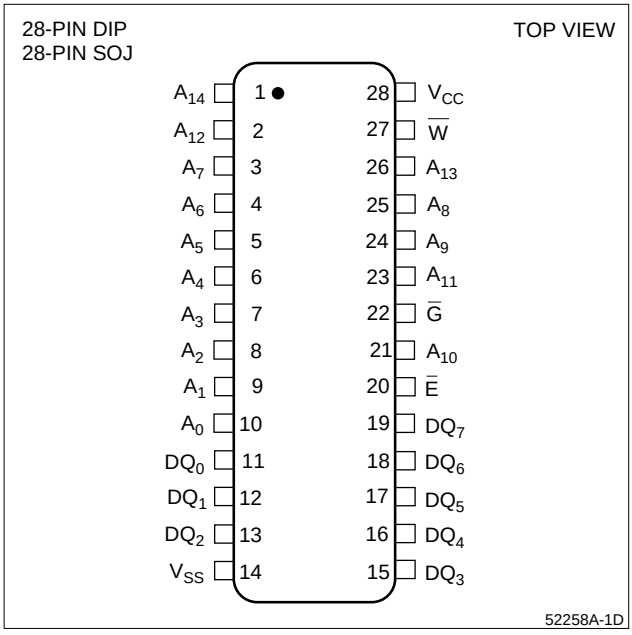


Figure 1. Pin Connections for DIP and SOJ Packages

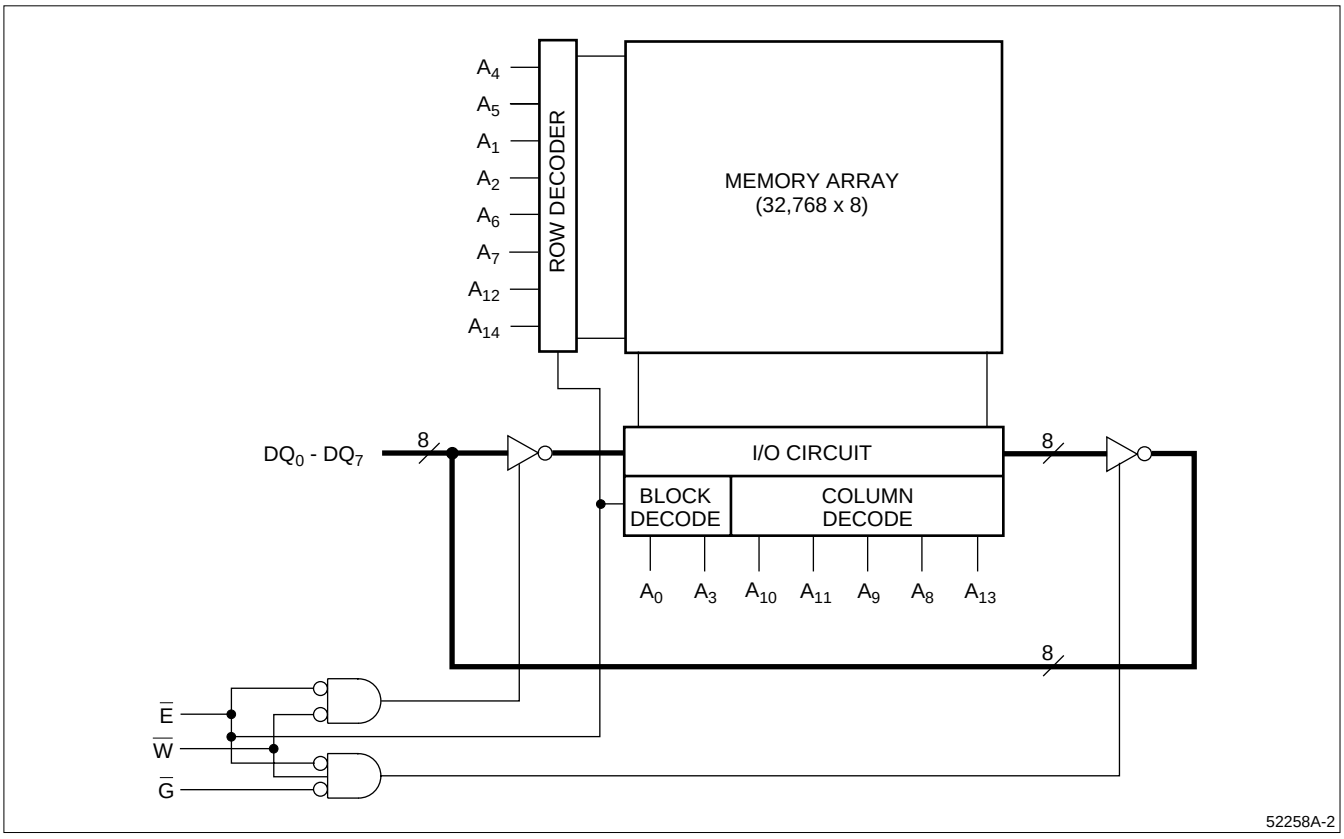


Figure 2. LH52258A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 – A_{14}$	Address Inputs
$DQ_0 – DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	–0.5 V to 7 V
Input Voltage Range	–0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	–65° to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	–0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{RC} = 20 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 20 ns		95	150	mA
I_{CC1}	Operating Current [2]	t_{RC} = 25 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 25 ns		90	140	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$ – 0.2 V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		6	15	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	–2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	–2		2	µA
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 m A			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$ – 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC}$ – 0.2 V			250	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

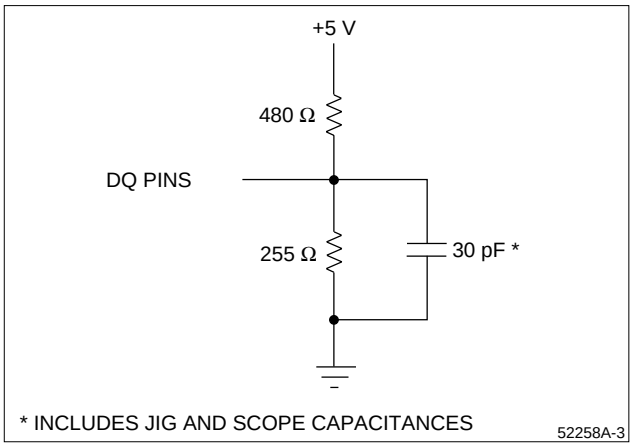


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

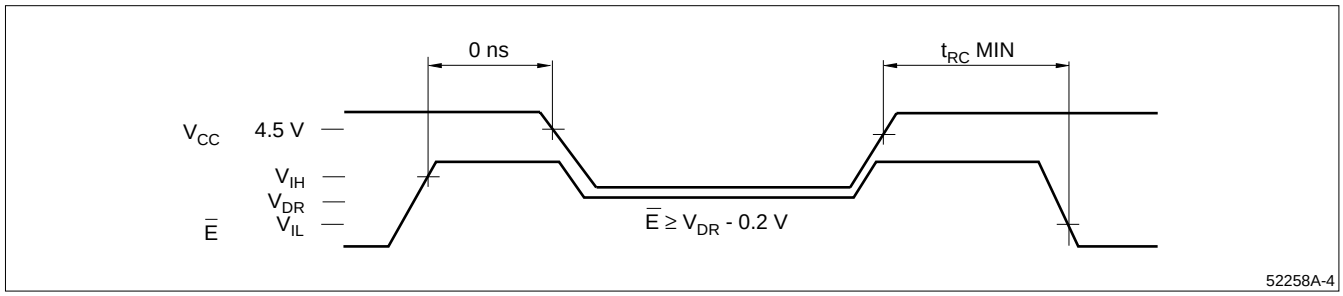


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	–20		–25		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address Access Time		20		25	ns
t_{OH}	Output Hold from Address Change	4		4		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	10	0	12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	9	0	10	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	20		25		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Setup	0		0		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		ns
t_{DW}	Input Data Setup Time	10		12		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Guaranteed by design but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

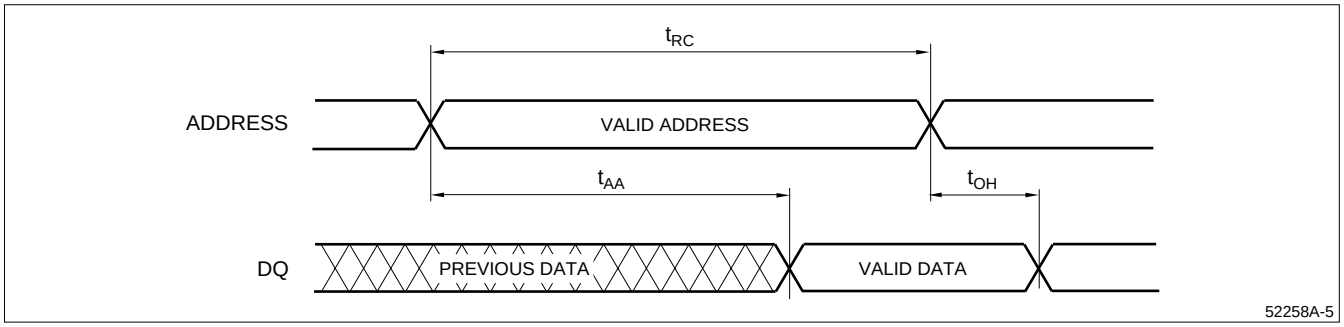


Figure 5. Read Cycle No. 1

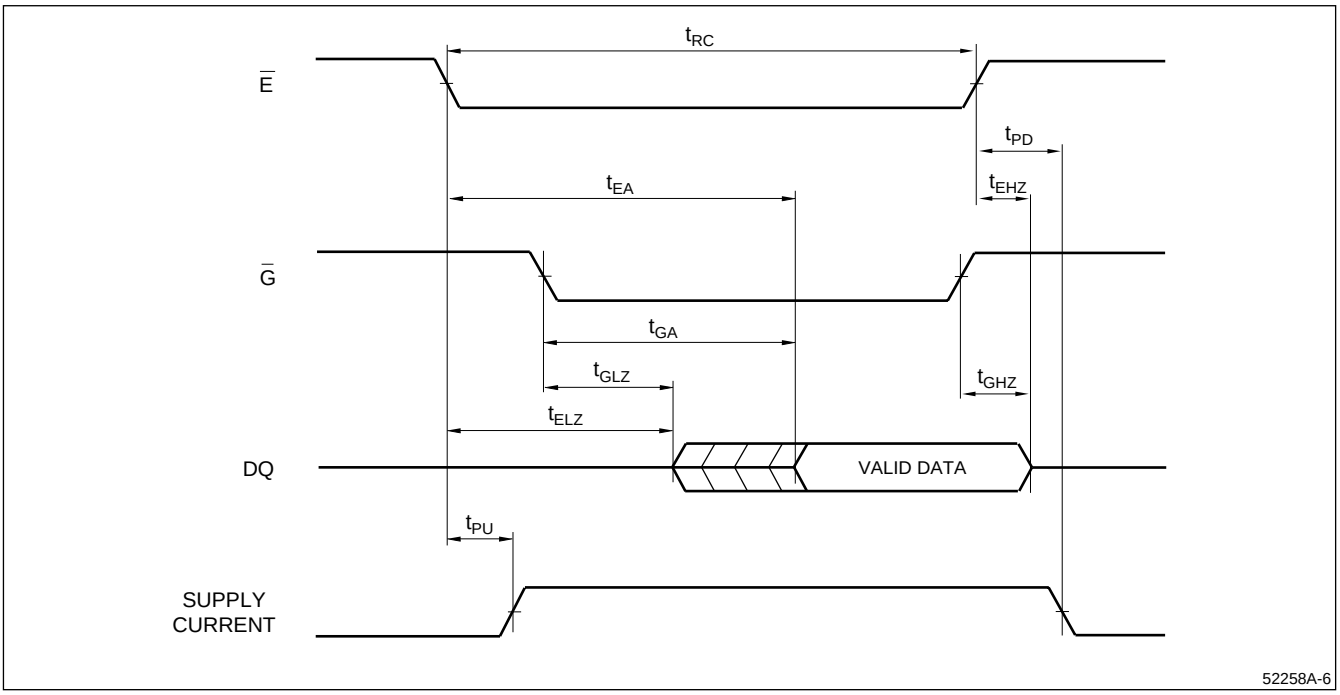


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258A's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

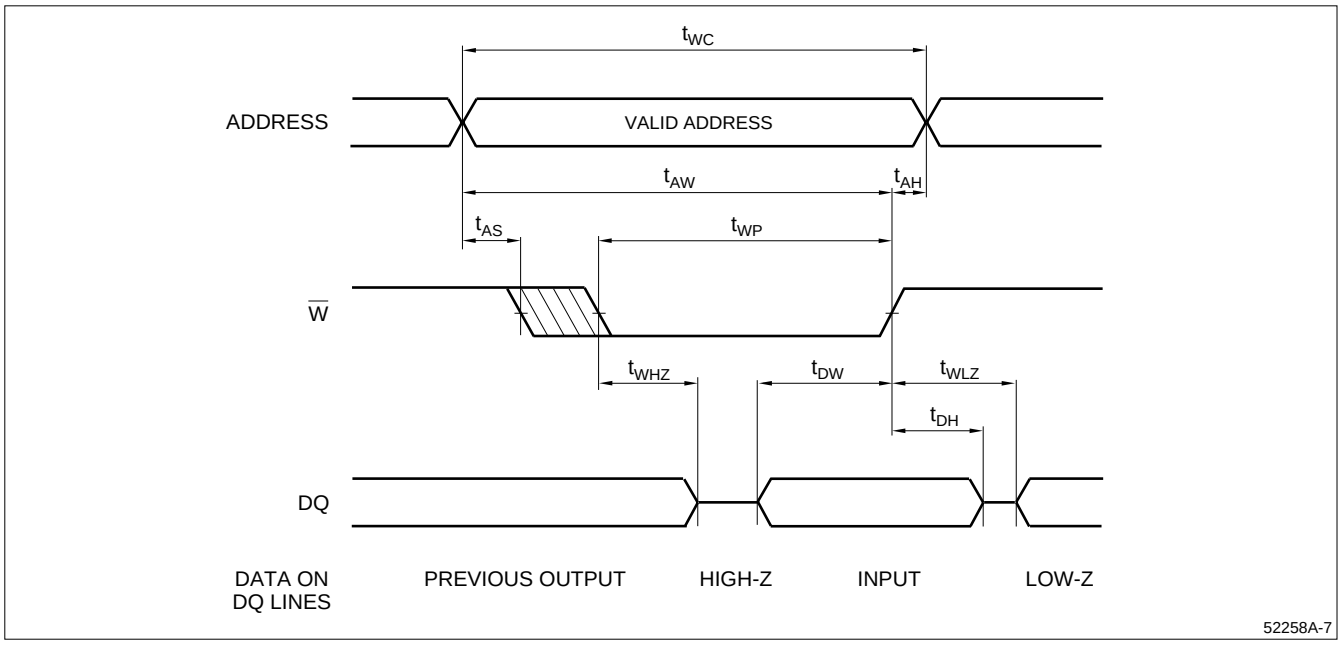


Figure 7. Write Cycle No. 1

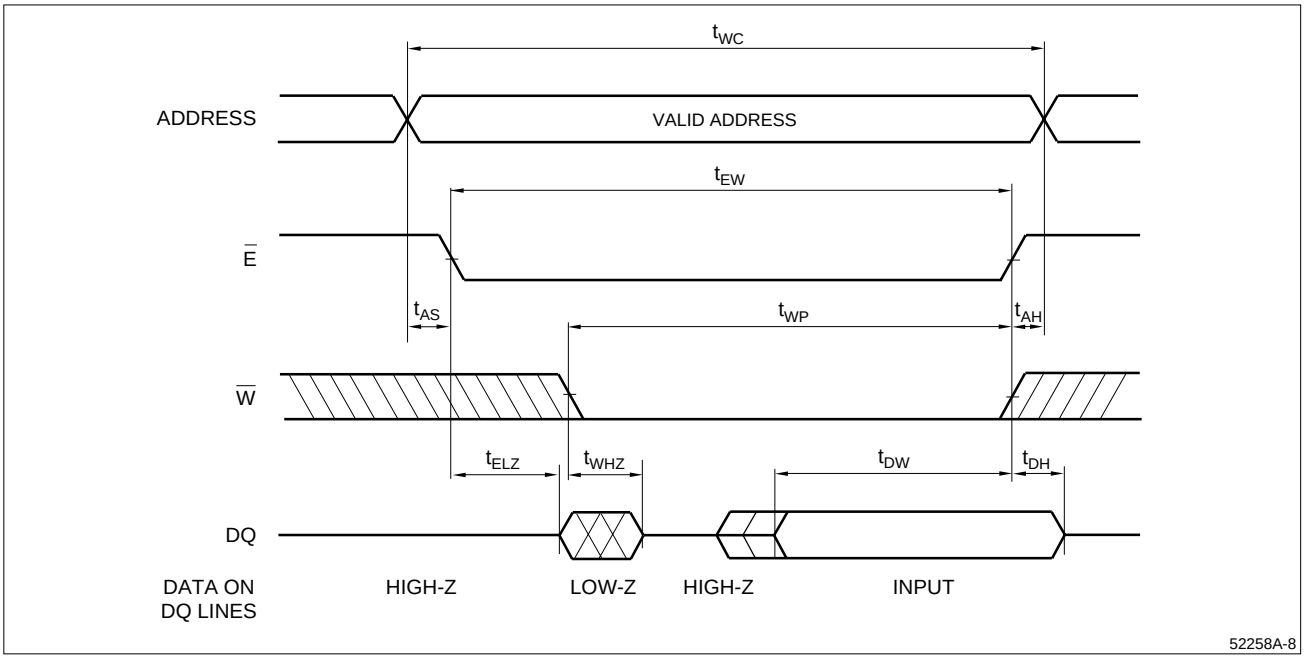
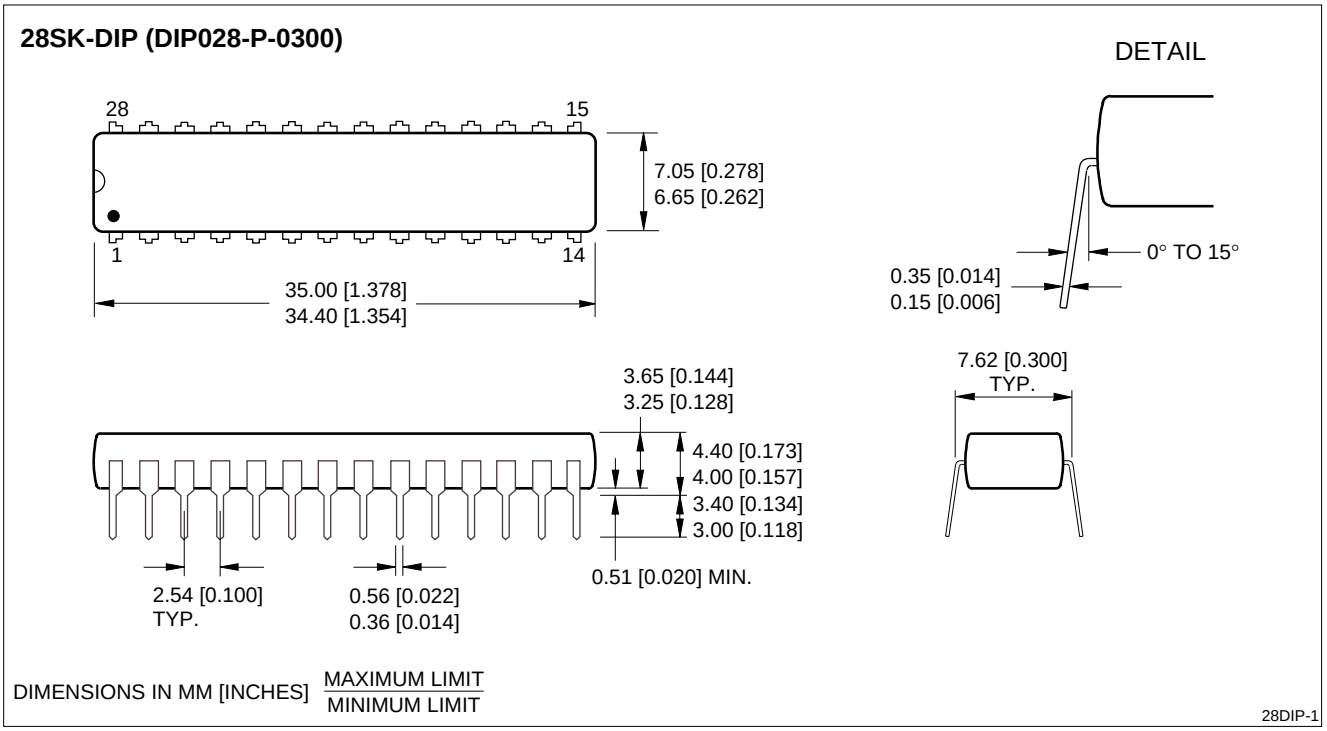


Figure 8. Write Cycle No. 2

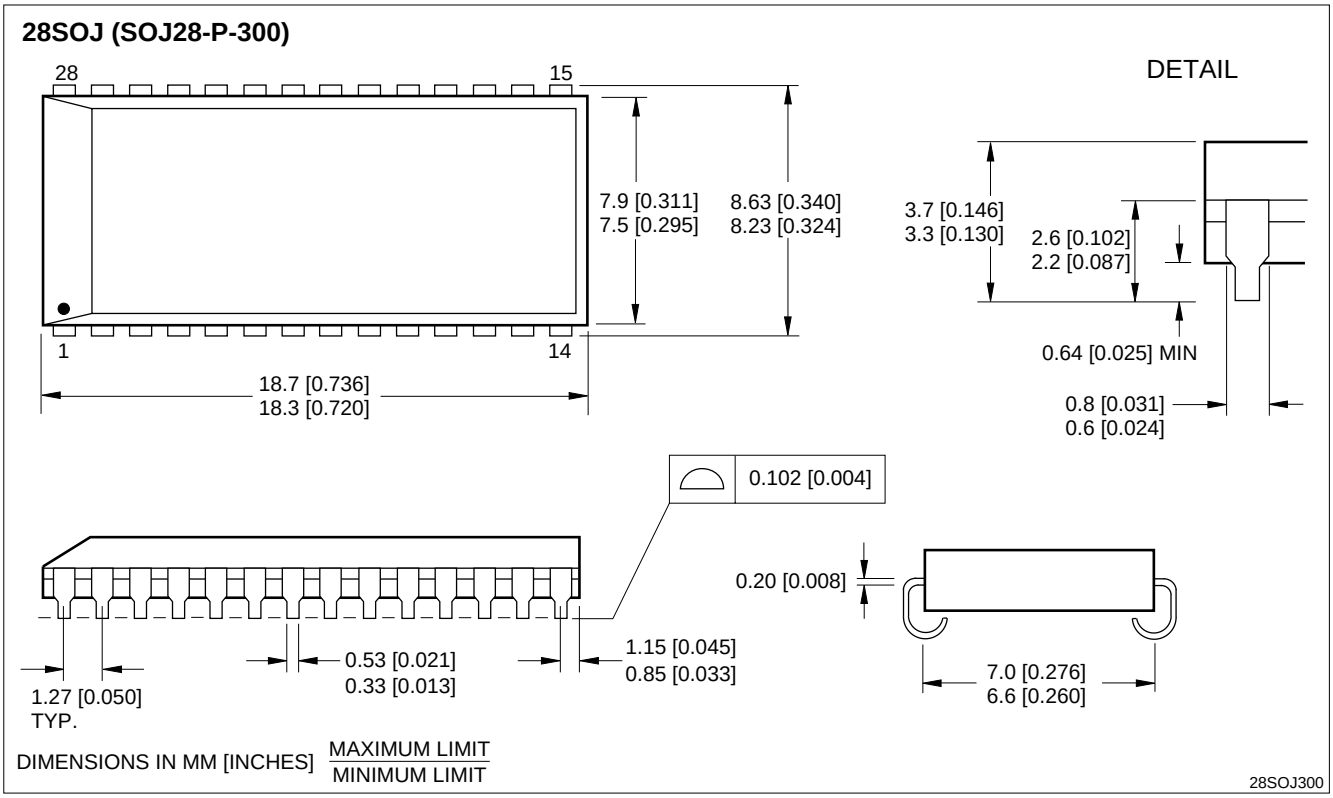
PACKAGE DIAGRAMS

28SK-DIP (DIP028-P-0300)



28-pin, 300-mil DIP

28SOJ (SOJ28-P-300)



28-pin, 300-mil SOJ

ORDERING INFORMATION