M52347SP/FP

Sync Signal Processor

REJ03F0190-0200
Rev.2.00
Sep 14, 2006

Description

The M52347 automatically selects three types of synchronous signals containing separate sync (positive and negative polarities of 0.5 to 2.5 V_{p-p}), composite sync (positive and negative polarities of 0.5 to 2.5 V_{p-p}) and sync-on-video (sync negative polarity), and performs waveform shaping. The IC is optimum to synchronous signal processing for multi-scan type display monitor.

Features

- Low power consumption with supply voltage of 5 V
- Capable of obtaining output information on whether to input synchronous signal, and on polarity
- Output of clamp pulse
- Equipped with V TIME GATE SW that enables selecting whether or not VD portion pulse is output from pin 14/15.
- Equipped with CLAMP SW that enables switching the clamp pulse output position.

Application

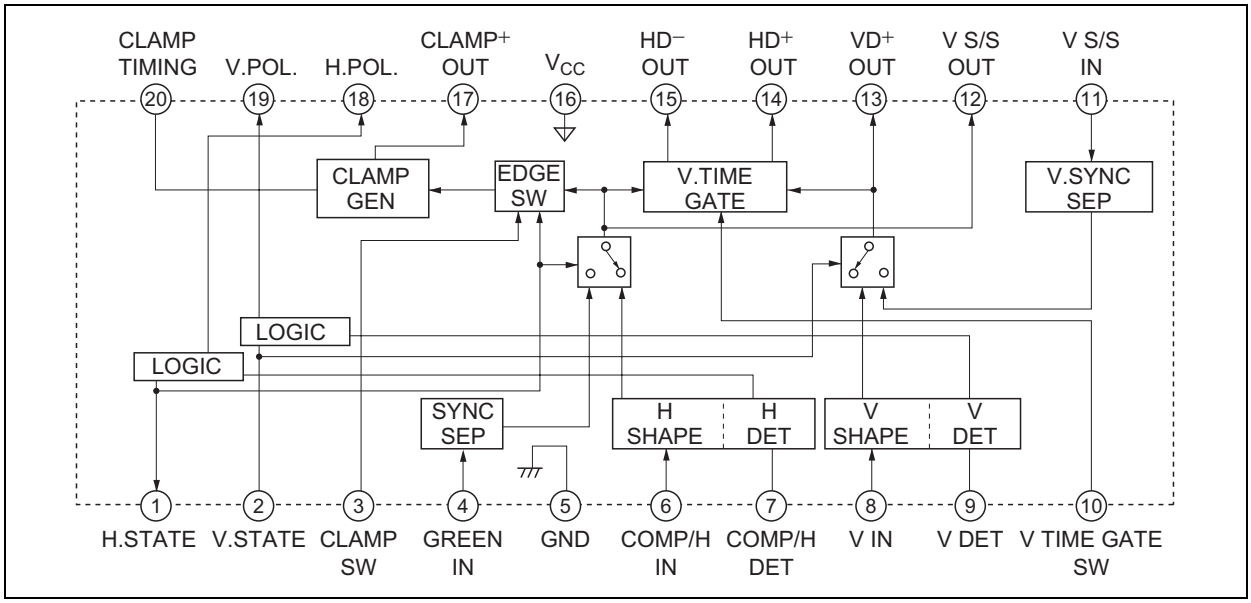
Display monitor

Recommended Operating Condition

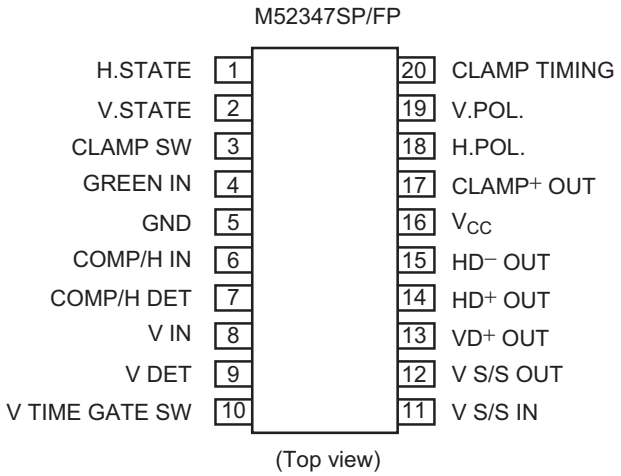
Supply voltage range: V_{CC} = 4.5 to 5.5 V

Rated supply voltage: V_{CC} = 5 V

Block Diagram



Pin Arrangement



Outline: PRDP0020BA-A (20P4B) [SP]
PRSP0020DA-A (20P2N-A) [FP]

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	6.0	V
Power dissipation	Pd	1237.6 (SP), 827.8 (FP)	mW
Electrostatic discharge	Surge	±200	V
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +150	°C

Electrical Characteristics

(Ta = 25°C, V_{CC} = 12 V, unless otherwise noted)

Item	Symbol	Limits			Unit	Relay Condition				TP Condition		Input Pin	Input Condition	Output pin	Output waveform	Note
		Min.	Typ.	Max.		4	6	8	16	3	10					
Circuit current	I_{CC}	40	53	66	mA	2	2	2	2	5 V	5 V	16	—	A	—	
Pin 1 output Hi level	1 OH	4.0	5.0	5.0	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	1	DC	*1
Pin 1 output Low level	1 OL	0	0.04	0.5	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 0.2 V_{P-P} 1 µs 50 kHz 1.0 V_{P-P}	1	DC	*1, *2
Pin 2 output Hi level	2 OH	4.0	5.0	5.0	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	2	DC	*1
Pin 2 output Low level	2 OL	0	0.04	0.5	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1.0 V_{P-P} 1 µs 50 kHz 0.2 V_{P-P}	2	DC	*1, *2
Pin 18 output Hi level	18 OH	4.0	5.0	5.0	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	18	DC	*1
Pin 18 output Low level	18 OL	0	0.04	0.5	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	18	DC	*1
Pin 19 output Hi level	19 OH	4.0	5.0	5.0	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	19	DC	*1
Pin 19 output Low level	19 OL	0	0.04	0.5	V	2	1	1	1	0 V 2.5 V 5 V	5 V	6 8	1 µs 50 kHz 1 V_{P-P} 1 µs 50 kHz 1 V_{P-P}	19	DC	*1
Pin 14 output Hi level	14 OH	4.0	5.0	5.0	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	V Meas	
Pin 14 output Low level	14 OL	0	0.25	0.5	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	V Meas	

Notes: 1. The true value table depends on Table 1

2. 0.2 V_{P-P} of input signal is equivalent to NON SYNC.

Electrical Characteristics (cont.)

Item	Symbol	Limits Min.	Typ.	Max.	Unit	Relay Condition 4	6	8	16	TP Condition 3	10	Input Pin	Input Condition	Output pin	Output waveform	Note
Pin 15 output Hi level	15 OH	4.0	5.0	5.0	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	V Meas	
Pin 15 output Low level	15 OL	0	0.25	0.5	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	V Meas	
Pin 17 output Hi level	17 OH	4.0	5.0	5.0	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	V Meas	
Pin 17 output Low level	17 OL	0	0.25	0.5	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	V Meas	
Pin 13 output Hi level	13 OH	4.0	5.0	5.0	V	2	2	1	1	0 V 2.5 V 5 V	5 V	8	1 µs 50 kHz 2 V_{P-P}	13	V Meas	
Pin 13 output Low level	13 OL	0	0.25	0.5	V	2	2	1	1	0 V 2.5 V 5 V	5 V	8	1 µs 50 kHz 2 V_{P-P}	13	V Meas	
Pin 12 output Hi level	12 OH	4.0	5.0	5.0	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	12	V Meas	
Pin 12 output Low level	12 OL	0	0.25	0.5	V	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	12	V Meas	
Sync-Sep Sync input signal Max. noise amplitude voltage	SS-NV	—	—	0.05	V_{P-P}	1	2	2	1	0 V 2.5 V 5 V	5 V	4	1 µs 50 kHz 0.05 V_{P-P}	14 15 17	No pulse must be output.	*3
Sync-Sep Sync input signal Min. amplitude voltage	SS-LV	0.2	—	—	V_{P-P}	1	2	2	1	0 V 2.5 V 5 V	5 V	4	1 µs 50 kHz 0.2 V_{P-P}	14 17	50 kHz No pulse must be output in this portion.	*4
CLAMP SW threshold voltage H	V3H	2.8	3.1	3.4	V	2	1	2	1	Vari-able	5 V	3 6	DC voltage must be applied. 1 µs 50 kHz 2 V_{P-P}	14, 17 15		*5
CLAMP SW threshold voltage H variable	V3L	1.0	1.3	1.6	V	2	1	2	1	Vari-able	5 V	3 6	DC voltage must be applied. 1 µs 50 kHz 2 V_{P-P}	14, 17 15		*6
V TIME GATE SW threshold voltage variable	V10	2.0	2.5	3.0	V	2	1	1	1	0 V 5 V	Vari-able	6 8 10	1 µs 50 kHz 2 V_{P-P} 1 µs 50 kHz 2 V_{P-P} DC voltage must be applied.	14 15		*7

Notes: 3. Must not operate when input amplitude is 0.05 V_{P-P} or less. (Pseudo noise signal)
4. Must operate when the input amplitude is 0.2 V_{P-P} or more.
5. Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse is not output.
6. Checking output pulse for output with a voltage of 0 VDC applied, increase the DC voltage and then measure the voltage when the output pulse is not output.
7. Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse becomes narrow.

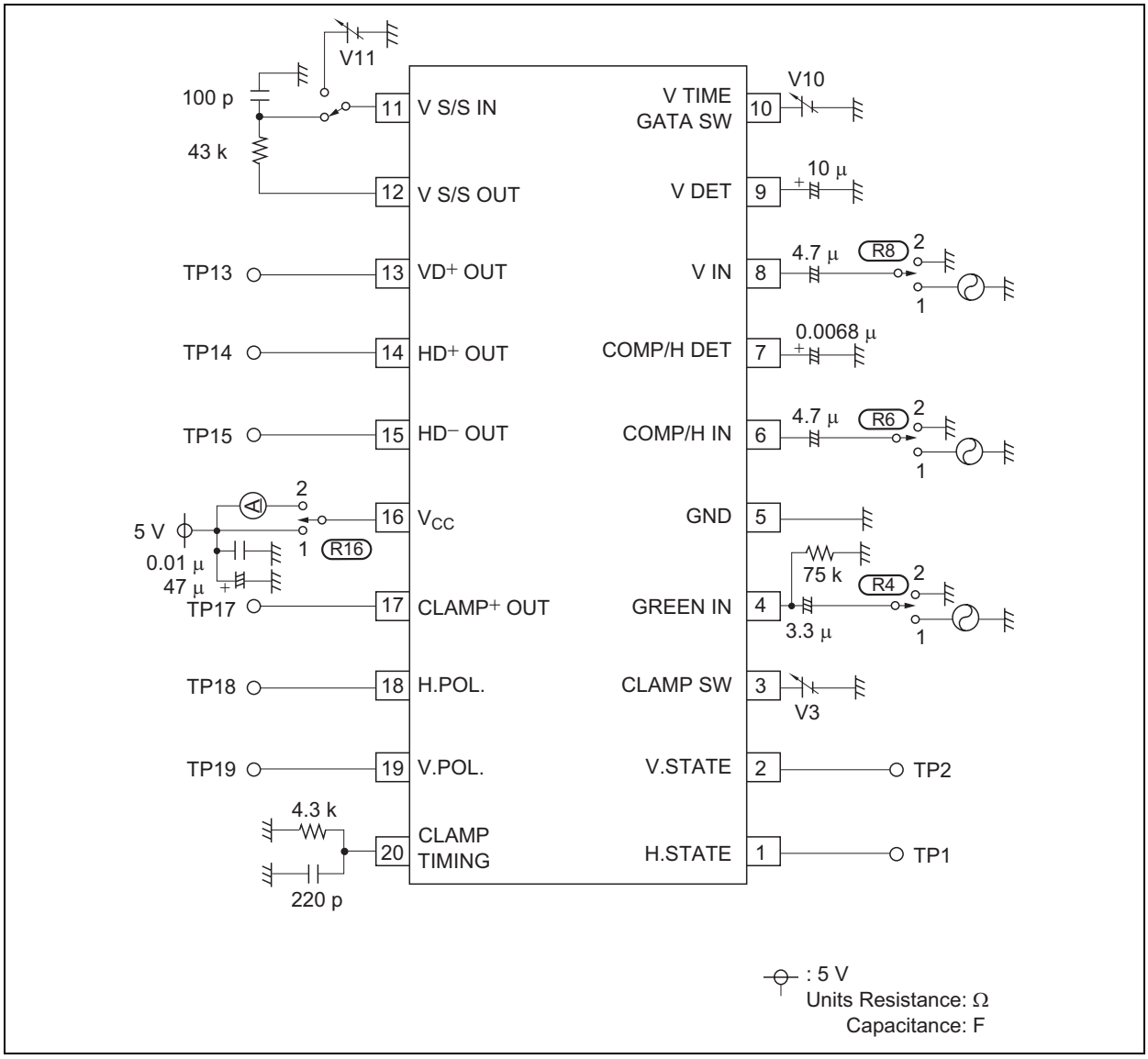
Electrical Characteristics (cont.)

Item	Symbol	Limits Min.	Typ.	Max.	Unit	Relay Condition 4	6	8	16	TP Condition 3	10	Input Pin	Input Condition	Output pin	Output waveform	Note
HD+-delay time (A)	HD+-DA	—	120	350	ns	1	1	2	1	0 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	Input 6 (50%) Time Meas Output 14 (50%)	
HD+-delay time (B)	HD+-DB	—	80	350	ns	1	1	2	1	0 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	Input 6 (50%) Time Meas Output 14 (50%)	
HD+-delay time (C)	HD+-DC	—	140	350	ns	1	1	2	1	2.5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	Input 4 (50%) Time Meas Output 14 (50%)	
HD+-delay time (D)	HD+-DD	—	120	350	ns	1	1	2	1	2.5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	14	Input 4 (50%) Time Meas Output 14 (50%)	
HD−-delay time (A)	HD−-DA	—	70	350	ns	1	1	2	1	0 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	Input 6 (50%) Time Meas Output 15 (50%)	
HD−-delay time (B)	HD−-DB	—	120	350	ns	1	1	2	1	0 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	Input 6 (50%) Time Meas Output 15 (50%)	
HD−-delay time (C)	HD−-DC	—	100	350	ns	1	1	2	1	2.5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	Input 4 (50%) Time Meas Output 15 (50%)	
HD−-delay time (D)	HD−-DD	—	150	350	ns	1	1	2	1	2.5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	15	Input 4 (50%) Time Meas Output 15 (50%)	
CP+-delay time (A)	CP+-DA	—	90	350	ns	1	1	2	1	0 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	Input 6 (50%) Time Meas Output 17 (50%)	
CP+-delay time (B)	CP+-DB	—	130	350	ns	1	1	2	1	2.5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	Input 4 (50%) Time Meas Output 17 (50%)	
CP+-delay time (C)	CP+-DC	—	90	350	ns	1	1	2	1	5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	Input 6 (50%) Time Meas Output 17 (50%)	
CP+-PULSE-WIDTH	CP+-PW	250	400	550	ns	1	1	2	1	0 V 2.5 V 5 V	5 V	4 6	1 µs 50 kHz 0.6 V_{P-P} 1 µs 50 kHz 2 V_{P-P}	17	Time Meas Output 17 (50%)	
VD+-delay time (A)	VD+-DA	—	100	350	ns	2	2	1	1	0 V 2.5 V 5 V	5 V	8	1 µs 50 kHz 2 V_{P-P}	13	Input 8 (50%) Time Meas Output 13 (50%)	
VD+-delay time (B)	VD+-DB	—	70	350	ns	2	2	1	1	0 V 2.5 V 5 V	5 V	8	1 µs 50 kHz 2 V_{P-P}	13	Input 8 (50%) Time Meas Output 13 (50%)	
V Sync-Sep threshold voltage H	V11H	3.0	3.5	4.0	V	2	1	2	1	0 V 5 V	0 V	6 11	1 µs 50 kHz 2 V_{P-P} DC voltage must be applied.	14 15		*8
V Sync-Sep threshold voltage L	V11L	1.3	1.8	2.3	V	2	1	2	1	0 V 5 V	0 V	6 11	1 µs 50 kHz 2 V_{P-P} DC voltage must be applied.	14 15		*9

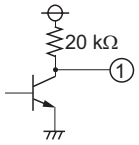
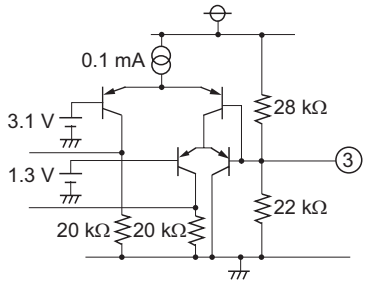
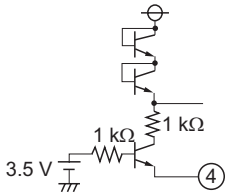
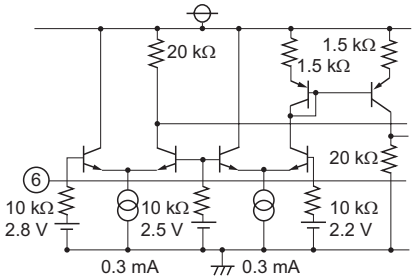
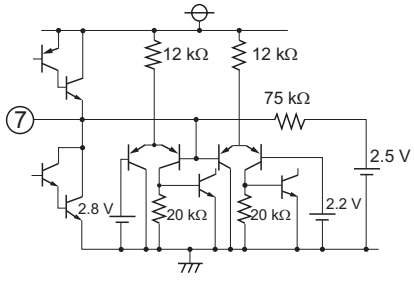
Notes: 8. Checking output pulse for output with a voltage of 0 VDC applied, increase the DC voltage and then measure the voltage when the output pulse is not output.

9. Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse is output.

Test Circuit



Pin Description

Pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
1	H.STATE	0 V_{DC} or 5 V_{DC}		Logic output pin for horizontal synchronous signal When pin 6 input signal is POSI, outputs "H"; when NON, outputs "L"; and when NEG, outputs "H".
2	V.STATE	0 V_{DC} or 5 V_{DC}	Same as pin 1	Logic output pin for vertical synchronous signal When pin 8 input signal is POSI, outputs "H"; when NON, outputs "L"; and when NEG, outputs "H".
3	CLAMP SW	2.2 V when open		This SW is available to change the generating position of clamp pulse for input signal. (See Table 2.) V_{TH} L = 0 to 1 V V_{TH} M = 1.6 to 2.8 V V_{TH} H = 3.4 to 5 V
4	GREEN IN	2.8 V when open		GREEN (SYNC ON VIDEO) input pin Input with negative sync. Comparison of pin 4 input signal and reference voltage within the IC performs synchronous separation.
5	GND	—	—	Grounding
6	COMP/H IN	2.5 V when open		Composite sync/H sync input pin. Bias is approx. 2.5 V and impedance is 10 kΩ. The internal double threshold comparator is used for shaping waveform and detecting polarity. Optimum input amplitude is 0.6 V_{P-P} at pin 6. Up to approx. 50% of duty, waveform shaping and polarity detection can be done.
7	COMP/H DET	2.5 V when open (no signal)		External capacitance is required as a filter pin for detecting polarity and detecting non-input. As the value is larger, the ripple is smaller and less malfunction occurs. However, this lowers the response speed of detection.
8	V IN	2.5 V when open	Same as pin 6	V sync input pin Same as pin 6
9	V DET	2.5 V when open (no signal)	Same as pin 7	Same as pin 7

Pin Description (cont.)

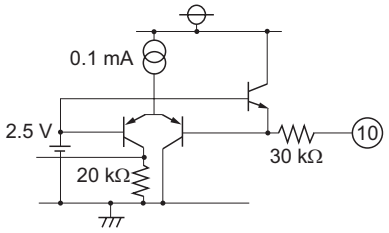
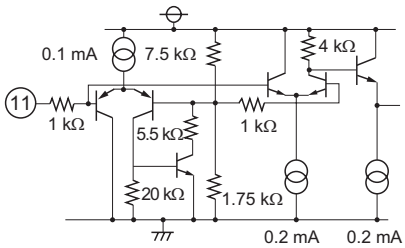
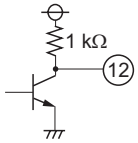
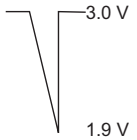
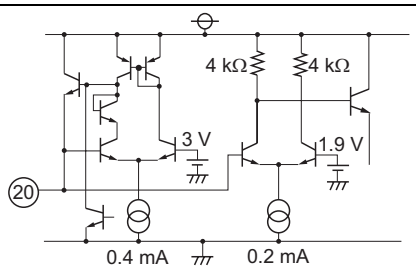
Pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
10	V.TIME GATE SW	3.2 V when open		V TIME GATE SW pin Can select whether to output the pulse of VD portion from pin 14, 15 output pulse. The threshold voltage is approx. 2.5 V. V_{TH} L = 0 to 2 V V_{TH} H = 3 to 5 V
11	V S/S IN	—		V S/S IN pin Inputs a signal of having externally integrated composite sync for V sync separation.
12	V S/S OUT	—		V S/S pulse output pin No problem occurs when current of approx. 6 mA flows to internal part of the IC. To improve the rising speed, connect a resistance between power supplies.
13	VD^+OUT	—	Same as pin 12	VD^+ pulse output pin Same as pin 12
14	HD^+OUT	—	Same as pin 12	HD^+ pulse output pin Same as pin 12
15	HD^-OUT	—	Same as pin 12	HD^- pulse output pin Same as pin 12
16	V_{CC}	5 V	—	Power supply
17	$CLAMP^+$ OUT	—	Same as pin 12	$CLAMP^+$ pulse output pin Same as pin 12
18	H.POL.	0 V_{DC} or 5 V_{DC}	Same as pin 1	Logic output pin for horizontal synchronous signal When pin 6 input signal is POSI, outputs "L"; when NON, outputs "L"; and when NEG, outputs "H".
19	V.POL.	0 V_{DC} or 5 V_{DC}	Same as pin 1	Logic output pin for vertical synchronous signal When pin 8 input signal is POSI, outputs "L"; when NON, outputs "L"; and when NEG, outputs "H".
20	CLAMP TIMING			CLAMP TIMING pin The clamp pulse width is determined depending on the external resistance and capacitance. As the resistance value and capacitance value are larger, the clamp pulse width is wider.

Table 1 Decorder Logic Output

Pin 6 Input COMP/H	Pin 8 Input V	Output Pin 1	2	18	19
POSI.	NON	H	L	L	L
	POSI.	H	H	L	L
	NEG.	H	H	L	H
NEG.	NON	H	L	H	L
	POSI.	H	H	H	L
	NEG.	H	H	H	H
NON.	NON	L	L	L	L
	POSI.	L	H	L	L
	NEG.	L	H	L	H

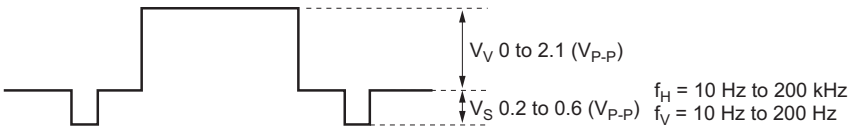
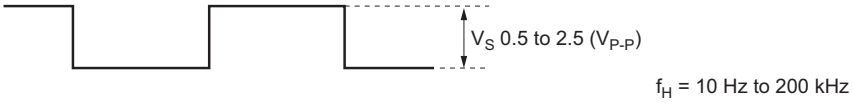
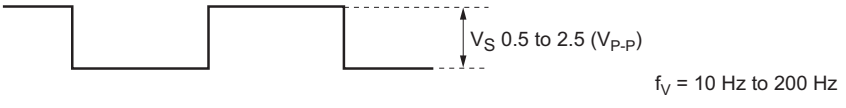
Table 2 Clamp Pulse Position

Input Signal		Pin 17 Output Signal		
Pin 4	Pin 6	Pin 3 "H"	Pin 3 "M"	Pin 3 "L"
O	X	4 trailing edge	4 trailing edge	4 trailing edge
O	O	6 leading edge	4 trailing edge	6 trailing edge
X	O	6 leading edge	X	6 trailing edge

Table 3 Output Priority Order

Input Signal			Output Signal			
			Pin 3 "H" "L"		Pin 3 "M"	
Pin 4	Pin 6	Pin 8	Pins 12, 14, 15, 17	Pin 13	Pins 12, 14, 15, 17	Pin 13
O	X	X	4	11	4	11
O	O	X	6	11	4	11
O	X	O	4	8	4	8
O	O	O	6	8	4	8
X	X	X	X	X	X	X
X	O	X	6	11	X	X
X	X	O	X	8	X	8
X	O	O	6	8	X	8

Table 4 Allowable Input Amplitude Voltage

Pin 4 input amplitude	
Pin 6 input amplitude	
Pin 8 input amplitude	

Application Method

1. Input Block

1) GREEN (SYNC ON VIDEO) IN (Pin 4)

Input with sync negative polarity.

Comparison of pin 4 input signal and the reference voltage of the inside of the IC performs the synchronous separation. When the input at pin 4 is less than or equal to the reference voltage (2.8 V) and the flowing current is more than or equal to the input sensitivity current (200 μA or more), the signal is separated.

When only a synchronous signal is input into pin 4, the operatable amplitude and the duty are as shown in Figure 1.

If the IC does not operate normally with the video signal input, change the value of external resistance R to make the current optimum.

But, when capacity value is too big, output response becomes bad.

2) COMP/H IN, VIN (pins 6 and 8)

The composite sync input is connected to pin 6. H and V of the separate sync input are connected to pins 6 and 8, respectively. For each of pins 6 and 8, the bias is 2.5 V and the impedance is 10 k. The internal double threshold converter is used for shaping waveform and for detecting polarity.

Average DC voltage of input signal is 2.5 V. Each threshold voltage is set at a voltage 0.3 V away from this voltage.

If the duty ratio at pin 6 is small as shown in Figure 2, the optimum value is approx. 0.3 V_{P-P}. If the duty ratio is large, the optimum value is approx. 0.6 V_{P-P}. Figure 3 shows the allowable input amplitude and the reference value of duty test.

Only 5 V TTL input, decrease the amplitude by resistor splitting.

In addition, Figure 4 shows an example for improving the capability of the allowable duty when the input amplitude is 0.7 V_{P-P} or more.

To use the IC out of the standard value, remove the filter from pins 7 and 9, observe the waveform and check for a match with the waveform shown in Figure 5.

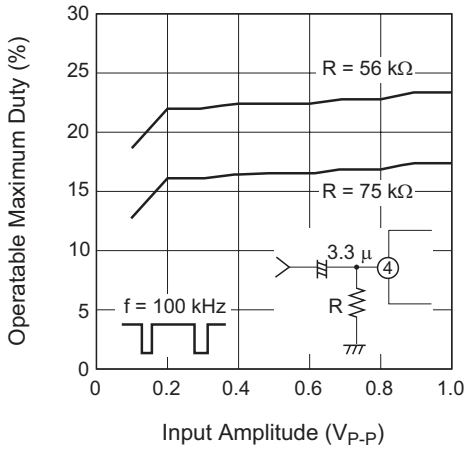


Figure 1

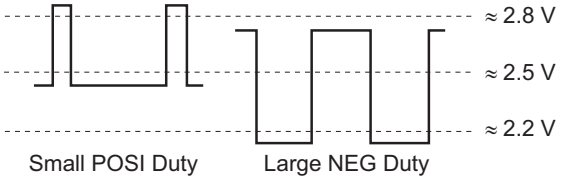


Figure 2

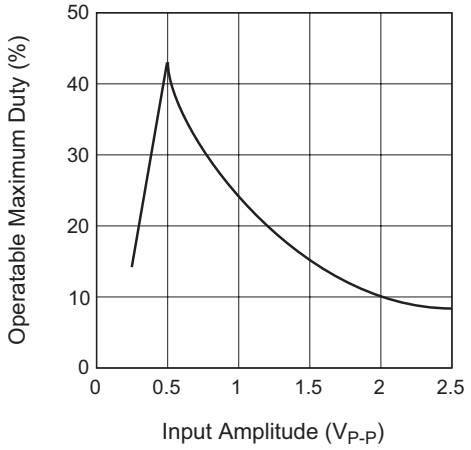


Figure 3

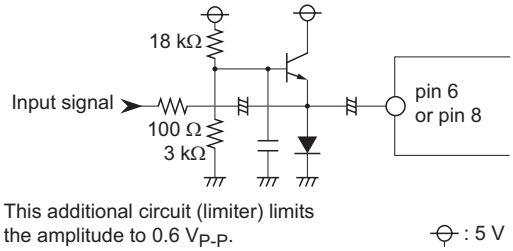


Figure 4

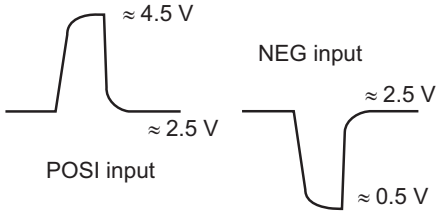
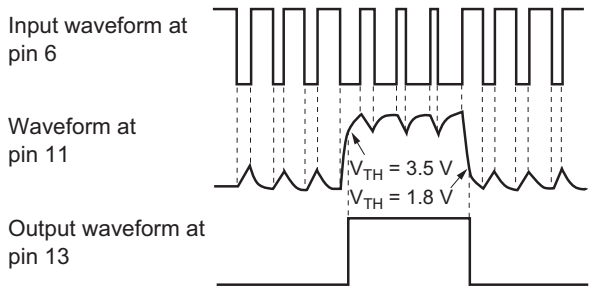


Figure 5

3) Polarity detection and non-input detection (pins 7 and 8)
External capacitance is required as a filter pin to detect polarity and non-input. As the value is larger, the ripple is smaller and less malfunction occurs. However, the response speed for detection is lower. A sufficient external capacitance is 0.05 µF with input of 15 kHz and 10 µF with input of 60 kHz. However, check the frequency of the input signal in use and the filter pin waveform with the duty ratio conditions, and then check that the value is 3.1 V or more (2.8 V in capability) with positive polarity input and 1.9 V or less (2.2 V in capability) with negative polarity input.

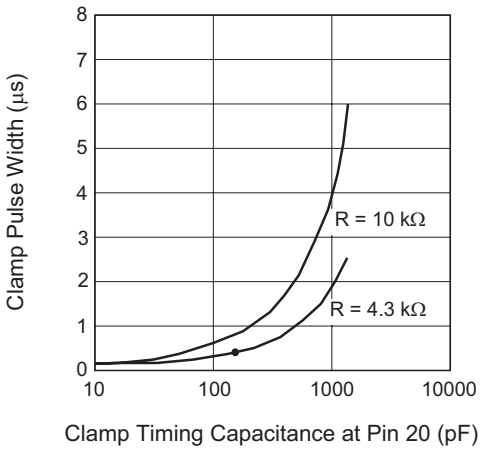
4) V S/S IN (pin 11)
Input a signal of having externally integrated composite sync for V sync separation.
Composite sync input into pin 6 is output to pin 12. Output at 12 is externally integrated and is input into pin 11 for V sync separation. With the waveform at pin 11, check that the H element has been fully dropped.
The threshold levels of sync separation, given hysteresis, are 3.5 V and 1.8 V.



2. Clamp Pulse

1) Clamp pulse width
CLAMP TIMING (Pin 20)
The clamp pulse width is determined by the external resistance and the capacitance. As the resistance value and capacitance value are larger, the clamp pulse width is wider.
The time constant is determined by the current flowing out of pin 20 and the capacitance value of the timing pin. The flow current at pin 20 is determined by the pin voltage and external resistance value. When the external resistance is 4.3 (that is 700 µA) and the external capacitance is 220 pF, the pulse width is 0.4 µs.

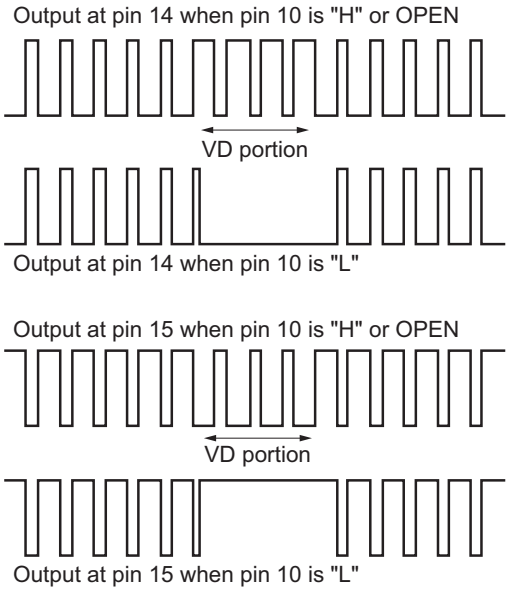
2) Clamp pulse position
CLAMP SW (pin 3)
When pin 3 is "M" or "L", fixing a higher-priority signal to the trailing edge results in occurrence of a clamp pulse. When pin 3 is "H", and only GREEN is input, clamp pulse occurs at the trailing edge. A clamp pulse also occurs at the leading edge when COMP/H only is input or when both COMP/H and GREEN are input.



3. Sampling Pulse from VD Portion

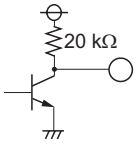
V TIME GATE SW (Pin 10)

Whether to output the pulse of VD portion from pins 14 and 15 can be selected. When pin 10 is "H" or OPEN, pulse of the VD portion is output. When pin 10 is "L", the pulse of the VD portion is not output.

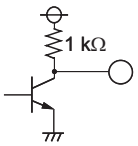


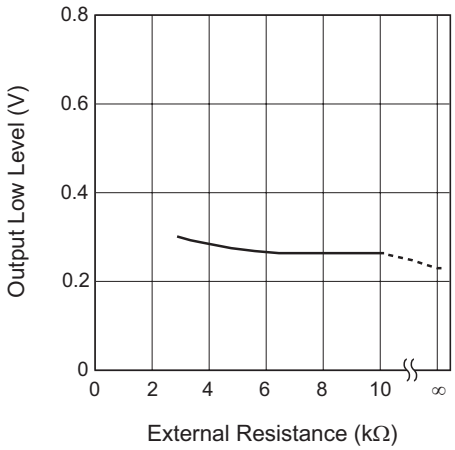
4. Output Stage

1) Logic output (pins 1, 2, 18 and 19)
The output format is as shown in the diagram below.
When the internal load resistance of the IC is 20 kΩ, a current of approx. 3 mA flows to the inside of the IC, no problem will occur.

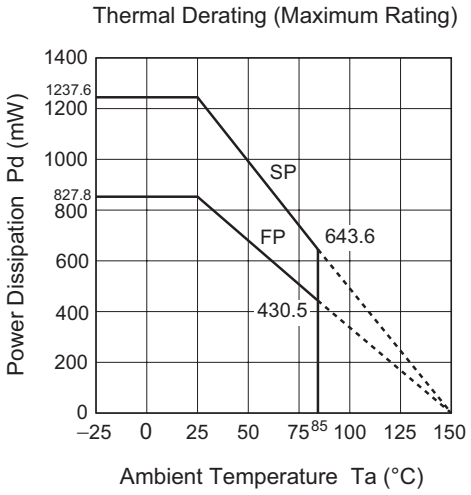


2) Pulse output (pins 12, 13, 14, 15 and 17)
The output format is as shown in the diagram below.
When the internal load resistance of the IC is 1 kΩ, a current of approx. 6 mA flows to the inside of the IC, no problem will occur.
To improve the rising speed, connect a resistance between power supplies. Note that the low level of the output pulse goes up.

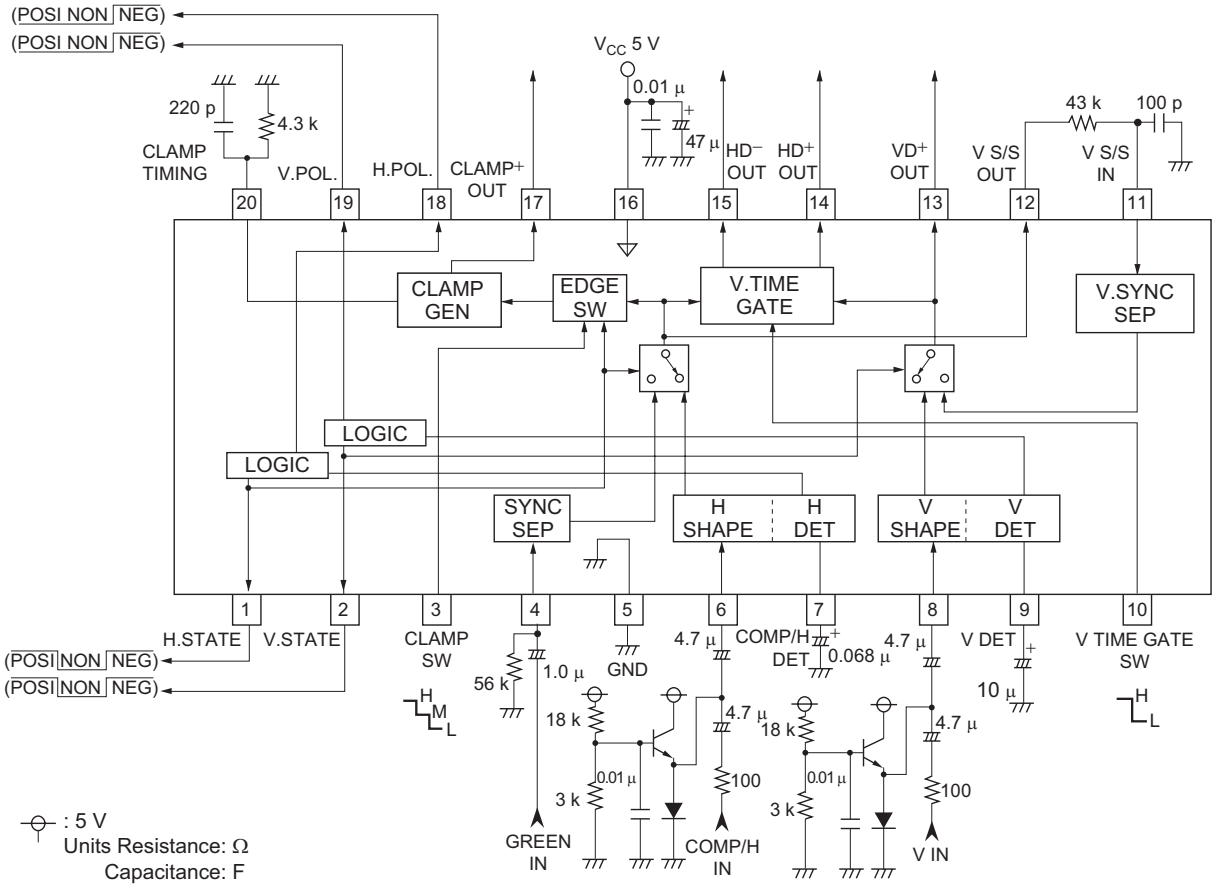




Typical Characteristics



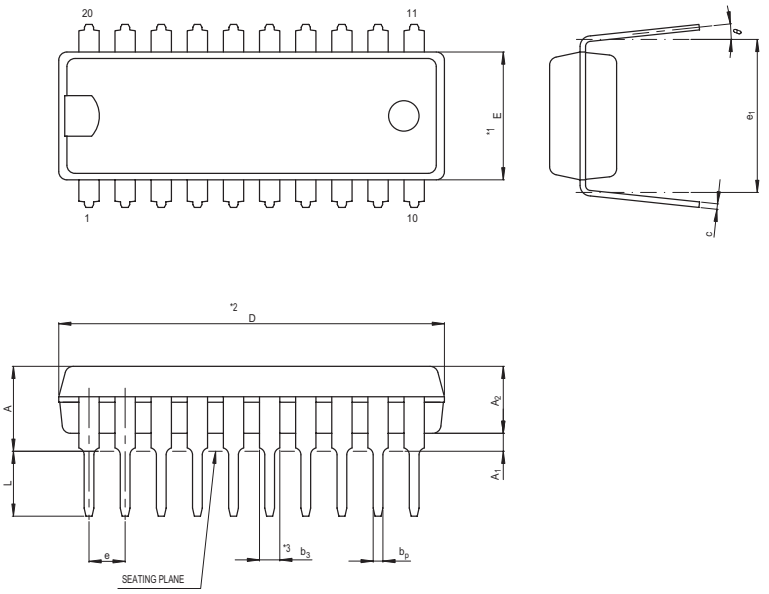
Application Example (f_H = 50 kHz, f_V = 80 Hz)



Note: External circuit for input of pins 6 and 8
When amplitude of up to 5 V_{P-P} is entered into this circuit, can be kept constant at approx. 0.6 V_{P-P}.
When the duty of input signal at pins 6 and 8 changes, the most broad support range is obtained with amplitude of 0.6 V_{P-P}.

Package Dimensions

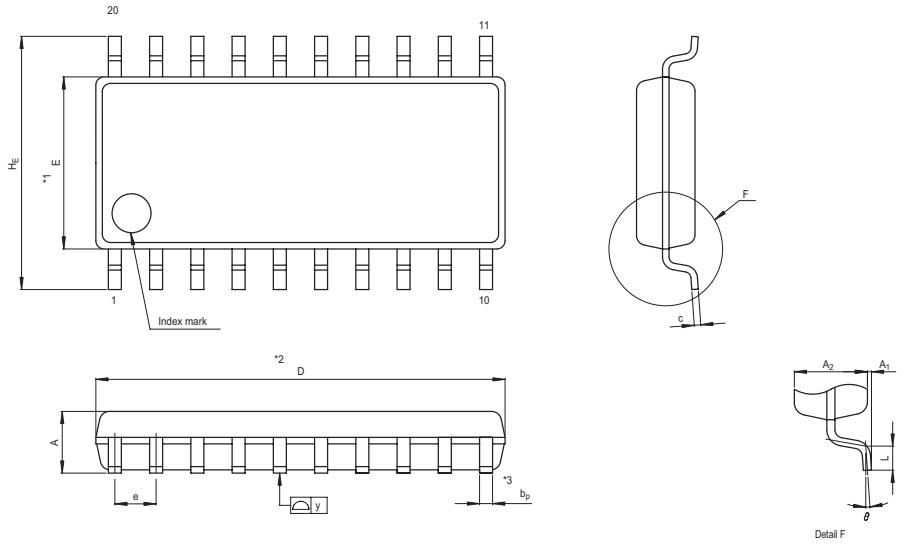
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

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