NEC

MOS INTEGRATED CIRCUIT

μPD98405

155M ATM INTEGRATED SAR CONTROLLER

DESCRIPTION

The μPD98405 (NEASCOT-S20™) is a high-performance SAR chip that performs segmentation and reassembly of ATM cells. It has a PCI bus interface, a SONET/SDH 155 Mbps framer, and a clock recovery circuit and supports an ABR function in hardware. The μPD98405 conforms to ATM Forum and has the functions of the AAL-5 SAR sublayer, ATM layer, and TC sublayer.

FEATURES

- Conforms to ATM Forum.
- Host bus interface supporting PCI bus/generic bus.
  - PCI interface (5/3.3 V, 32/64 bits, 33 MHz): Conforms to PCI Specification 2.1
  - Generic bus interface (5/3.3 V, 32 bits, 33 MHz)
- AAL-5 SAR sublayer, ATM layer, and TC sublayer functions
- Hardware support of AAL-5 processing
- Software support of non-AAL-5 traffic
- SONET STS-3c/SDH STM-1 155 Mbps framer function
- Clock recovery/clock synthesizer function
- Supports up to 32 K virtual channels (VCs)
- Sixteen traffic shapers for VBR for transmission scheduling
- Hardware support of CBR/VBR/ABR/UBR service
- Supports multi-cell burst transfer for transmission and reception
- MIB counter function
- Supports LAN emulation function
- Receive FIFO of 96 cells
- External PHY devices connectable: UTOPIA Level-1 interface
- 0.35 μm CMOS process, +5/3.3 V power supply
  - Bus interface +5 V: +5/3.3 V power supply
  - Bus interface +3.3 V: +3.3 V power supply
- 304-pin plastic QFP and 304-pin plastic FBGA

ORDERING INFORMATION

Part Number	Package
μPD98405GL-PMU	304-pin plastic QFP (0.5 mm fine pitch) (40 × 40)
★ μPD98405S1-6C	304-pin plastic FBGA (0.8 mm pitch) (19 × 19)

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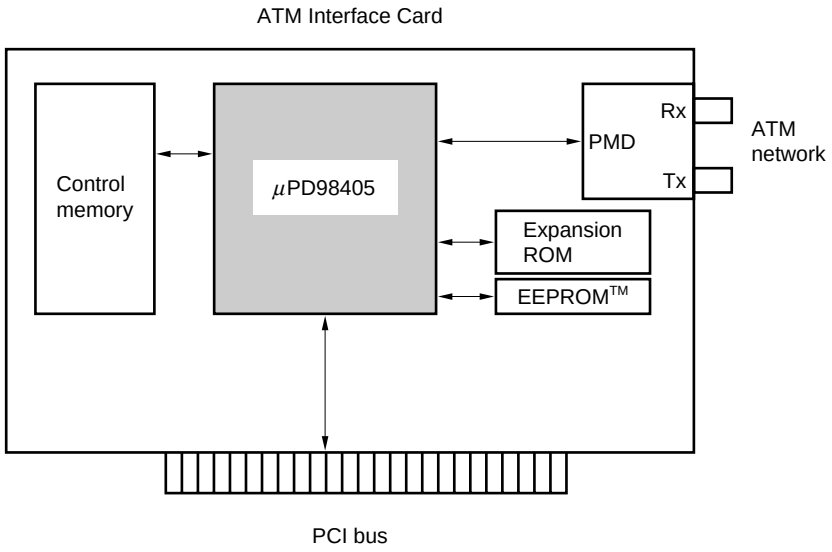
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

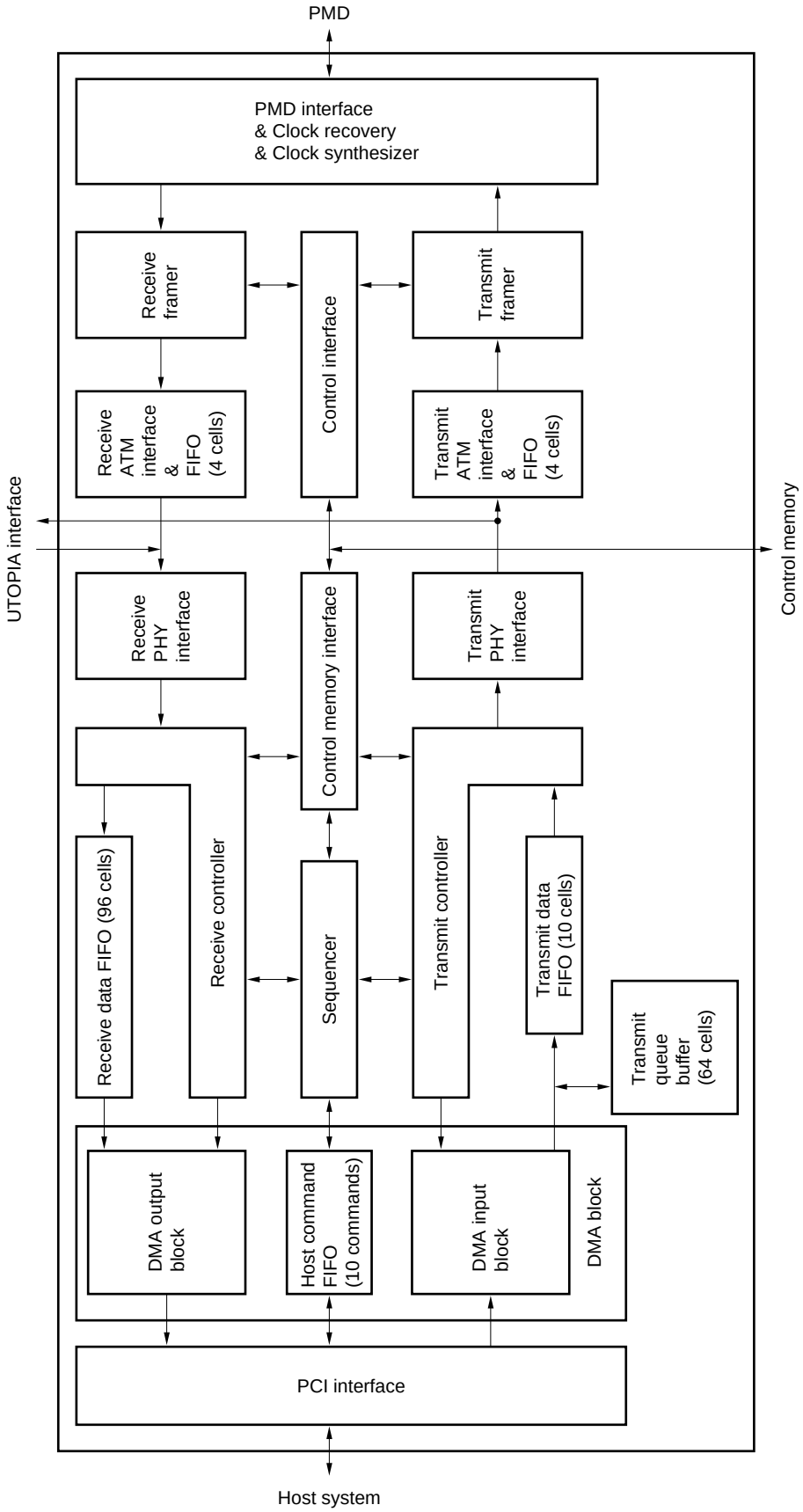
Document No. S12689EJ3V0DS00 (3rd edition)
Date Published January 2001 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

SYSTEM CONFIGURATION EXAMPLE

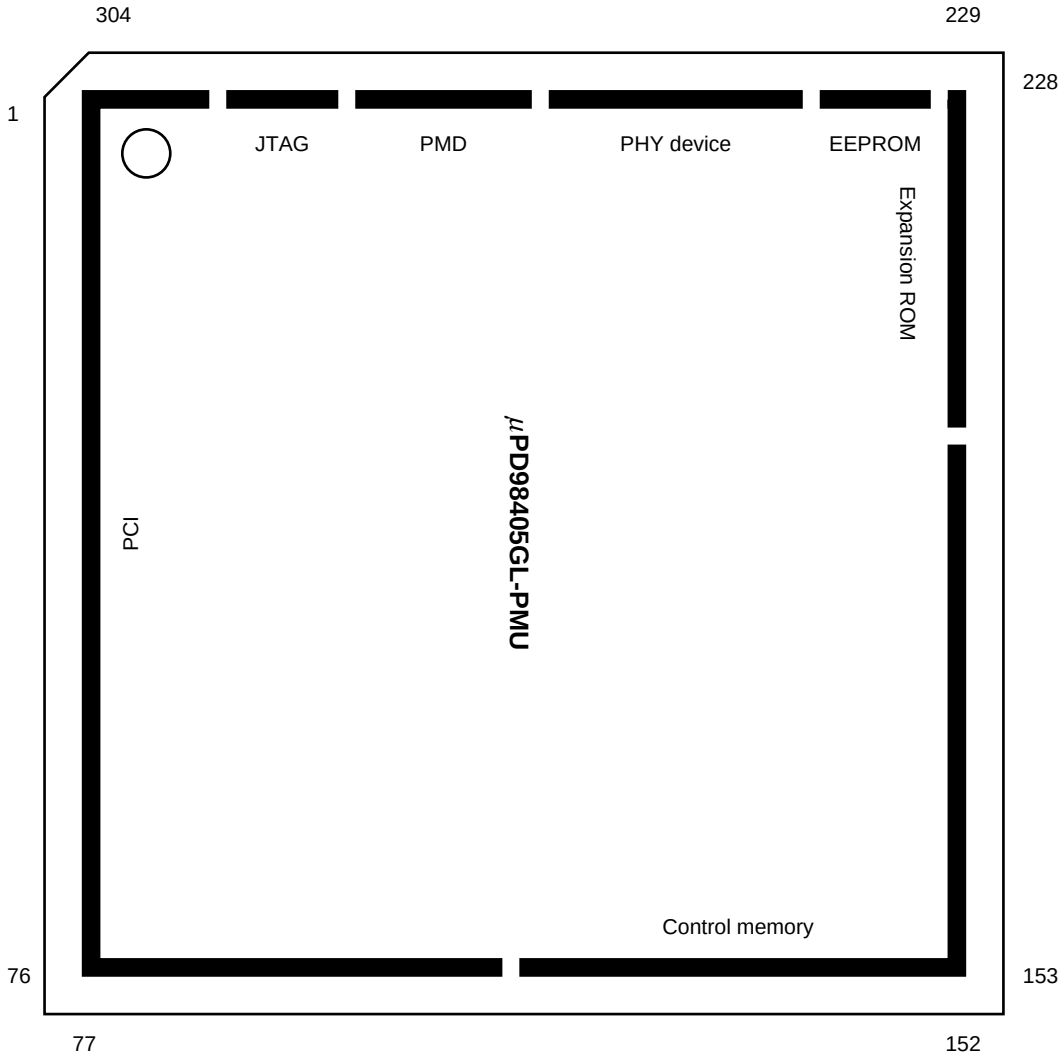


BLOCK DIAGRAM



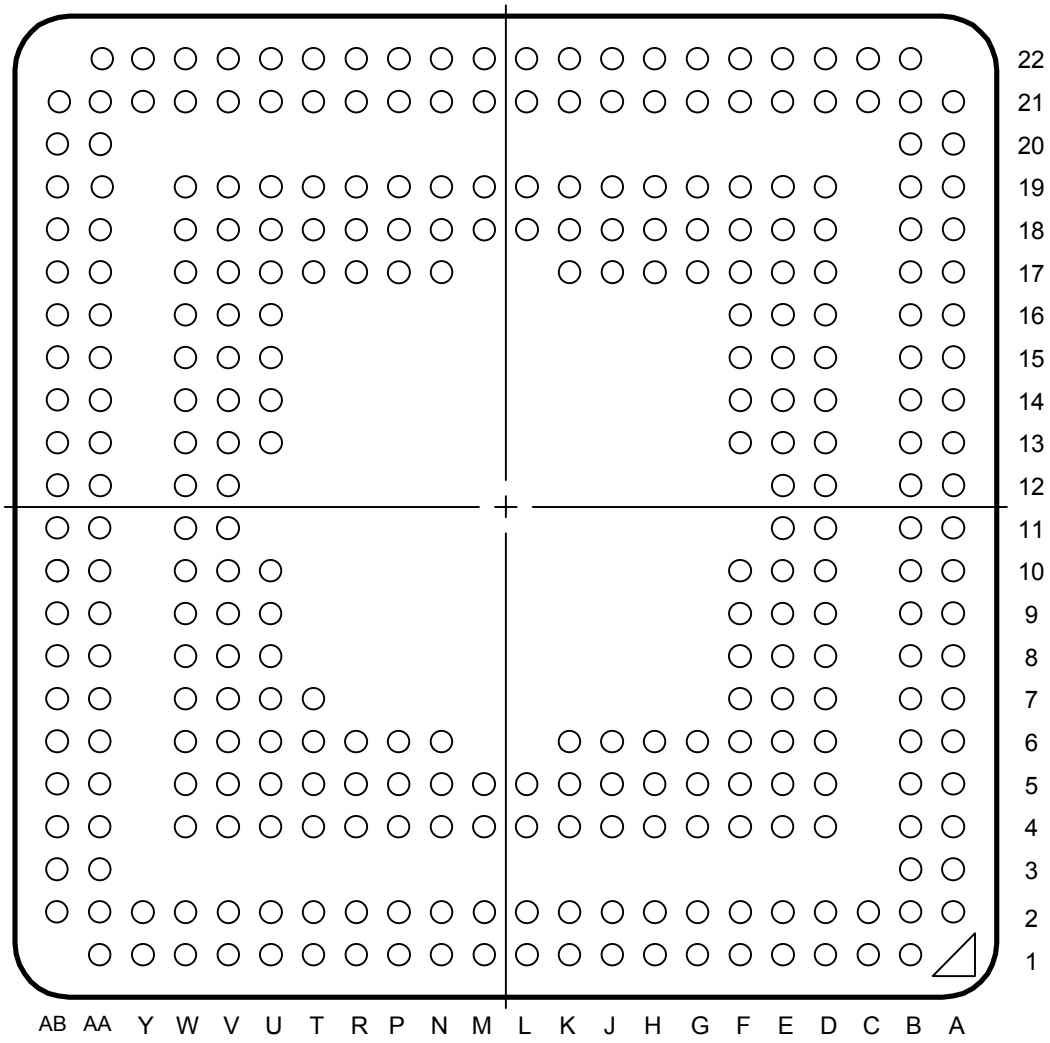
OUTLINE OF PINS

304-pin plastic QFP (0.5 mm fine pitch) (40 × 40)



★ **304-pin plastic FBGA (0.8 mm pitch) (19 × 19) (Bottom view)**

μPD98405S1-6C



PIN NAME

ABRT_B:	Abort
ACK64_B:	Acknowledge 64-bit transfer
AD63 to AD0:	Address/data
AGND:	Ground for analog part
ASEL_B:	Slave address select
ATTN_B:	Attention
AV_{DD3}:	+3.3 V power supply for analog part
BE3_B to BE0_B:	Byte enable
CA18 to CA0:	Control memory address
CBE3_B to CBE0_B:	Local port byte enable
CD31 to CD0:	Control memory data
CLK:	Clock
COE_B:	Control memory output enable
CPAR3 to CPAR0:	Control memory parity
CWE_B:	Control memory write enable
DEVSEL_B:	Device select
DR/W_B:	DMA read/write
EMPTY_B/RCLAV:	PHY empty/Rx cell available
ERR_B:	Error
E2PCLK:	Clock for EEPROM
E2PCS:	EEPROM chip select
E2PDI:	Serial data input from EEPROM
E2PDO:	Serial data output to EEPROM
FRAME_B:	Cycle frame
FULL_B/TCLAV:	PHY buffer full/Tx cell available
GND:	Ground for digital part
GNT_B:	Grant
HGND:	Ground for high-speed part
HV_{DD3}:	+3.3 V power supply for high-speed part
IDSEL:	ID select
INITD:	Initialization disable
INTR_B:	Interrupt
IRDY_B:	Initiator ready
JCK:	JTAG test pin
JDI:	JTAG test pin
JDO:	JTAG test pin
JMS:	JTAG test pin
JRST_B:	JTAG test pin
OE_B:	Output enable
PAR:	Parity
PAR3 to PAR0:	Bus party
PAR64:	Parity 64 bits
PCBE7_B to PCBE0_B:	Bus command and byte enables
PCI_MODE:	PCI mode
PERR_B:	Parity error
PHCE_B:	PHY chip enable
PHINT_B:	PHY interrupt
PHOE_B:	PHY output enable
PHRST_B:	PHY reset
PHR/W_B:	PHY read/write
PHYALM:	Physical alarm
RCLK:	Receive clock
RCIC:	Receive clock input complement
RCIT:	Receive clock input true
RDIC:	Receive data input complement
RDIT:	Receive data input true
PDY_B:	Target ready
REFCLK:	Reference clock
RENBL_B:	Receive enable
REQ64_B:	Request 64-bit transfer
REQ_B:	Request
RGND:	Ground for receive PLL part
ROMA15 to ROMA0:	Expansion ROM address
ROMCS_B:	Expansion ROM chip select
ROMD7 to ROMD0:	Expansion ROM input data
ROMOE_B:	Expansion ROM output enable
RSOC:	Receive start cell
RST_B:	Reset
RV_{DD3}:	+3.3 V power supply for receive PLL part
Rx7 to Rx0:	Receive data bus
SCLK:	SAR system clock
SD:	Signal detect
SEL_B:	Slave select
SERR_B:	System error
SIZE2 to SIZE0:	Burst size
SR/W_B:	Slave read /write
STOP_B:	Stop
TCLK:	Transmit clock
TDOC:	Transmit data output complement
TDOT:	Transmit data output true
TENBL_B:	Transmit enable
TEST:	Test mode pin
TFKC:	Transmit reference clock complement
TFKT:	Transmit reference clock true
TRDY_B:	Target ready
TSOC:	Transmit start of cell
Tx7 to Tx0:	Transmit data bus
V_{DD3}:	+3.3 V power supply for digital part
V_{DD5}:	+5 V power supply for digital part

PIN CONFIGURATION

304-pin plastic QFP (0.5 mm fine pitch) (40 × 40)

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No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode
1	GND	GND	38	V_{DD3}	V_{DD3}	75	AD58	–	112	AD35	–
2	V_{DD3}	V_{DD3}	39	AD12	AD12	76	GND	GND	113	AD34	–
3	AD24	AD24	40	AD11	AD11	77	GND	GND	114	AD33	–
4	PCBE3_B	BE3_B	41	AD10	AD10	78	V_{DD3}	V_{DD3}	115	AD32	–
5	IDSEL	–	42	AD9	AD9	79	AD57	–	116	PAR64	–
6	AD23	AD23	43	GND	GND	80	AD56	–	117	GND	GND
7	GND	GND	44	V_{DD5}	V_{DD5}	81	V_{DD5}	V_{DD5}	118	PCI_MODE	PCI_MODE
8	V_{DD5}	V_{DD5}	45	AD8	AD8	82	AD55	–	119	CD31	CD31
9	AD22	AD22	46	PCBE0_B	BE0_B	83	AD54	–	120	CD30	CD30
10	AD21	AD21	47	AD7	AD7	84	AD53	–	121	CD29	CD29
11	AD20	AD20	48	AD6	AD6	85	AD52	–	122	CD28	CD28
12	AD19	AD19	49	GND	GND	86	GND	GND	123	CD27	CD27
13	GND	GND	50	V_{DD3}	V_{DD3}	87	V_{DD3}	V_{DD3}	124	GND	GND
14	V_{DD3}	V_{DD3}	51	AD5	AD5	88	AD51	–	125	V_{DD3}	V_{DD3}
15	AD18	AD18	52	AD4	AD4	89	AD50	–	126	CD26	CD26
16	AD17	AD17	53	AD3	AD3	90	AD49	–	127	CD25	CD25
17	AD16	AD16	54	AD2	AD2	91	AD48	–	128	CD24	CD24
18	PCBE2_B	BE2_B	55	GND	GND	92	GND	GND	129	CD23	CD23
19	GND	GND	56	V_{DD5}	V_{DD5}	93	V_{DD5}	V_{DD5}	130	CD22	CD22
20	V_{DD5}	V_{DD5}	57	AD1	AD1	94	AD47	–	131	GND	GND
21	FRAME_B	SEL_B	58	AD0	AD0	95	AD46	–	132	CD21	CD21
22	IRDY_B	ASEL_B	59	ACK64_B	OE_B	96	AD45	–	133	CD20	CD20
23	TRDY_B	RDY_B	60	REQ64_B	DR/W_B	97	AD44	–	134	CD19	CD19
24	DEVSEL_B	SR/W_B	61	GND	GND	98	GND	GND	135	CD18	CD18
25	GND	GND	62	V_{DD3}	V_{DD3}	99	V_{DD3}	V_{DD3}	136	CD17	CD17
26	V_{DD3}	V_{DD3}	63	PCBE7_B	SIZE2	100	AD43	–	137	GND	GND
27	STOP_B	ABRT_B	64	PCBE6_B	SIZE1	101	AD42	–	138	V_{DD3}	V_{DD3}
28	PERR_B	ERR_B	65	PCBE5_B	SIZE0	102	AD41	–	139	CD16	CD16
29	SERR_B	–	66	PCBE4_B	PAR3	103	AD40	–	140	CD15	CD15
30	PAR	–	67	V_{DD5}	V_{DD5}	104	GND	GND	141	CD14	CD14
31	GND	GND	68	GND	GND	105	V_{DD5}	V_{DD5}	142	CD13	CD13
32	V_{DD5}	V_{DD5}	69	AD63	PAR2	106	AD39	–	143	CD12	CD12
33	PCBE1_B	BE1_B	70	AD62	PAR1	107	AD38	–	144	CD11	CD11
34	AD15	AD15	71	AD61	PAR0	108	AD37	–	145	GND	GND
35	AD14	AD14	72	V_{DD3}	V_{DD3}	109	AD36	–	146	CD10	CD10
36	AD13	AD13	73	AD60	–	110	GND	GND	147	CD9	CD9
37	GND	GND	74	AD59	–	111	V_{DD3}	V_{DD3}	148	CD8	CD8

Remark In this document, the active-low pin and active-low signal are represented as XXX_B (_B suffix following the pin/signal name).

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No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode
149	CD7	CD7	188	CA0	CA0	227	V_{DD3}	V_{DD3}	266	PHYALM/ PHR/W_B	PHYALM/ PHR/W_B
150	CD6	CD6	189	GND	GND	228	GND	GND	267	SD/PHCE_B	SD/PHCE_B
151	V_{DD3}	V_{DD3}	190	V_{DD3}	V_{DD3}	229	GND	GND	268	REFCLK/ PHINT_B	REFCLK/ PHINT_B
152	GND	GND	191	CBE3_B	CBE3_B	230	ROMOE_B	–	269	AV_{DD3}	AV_{DD3}
153	GND	GND	192	CBE2_B	CBE2_B	231	E2PDI	–	270	AGND	AGND
154	V_{DD3}	V_{DD3}	193	CBE1_B	CBE1_B	232	E2PDO	–	271	TEST	TEST
155	CD5	CD5	194	CBE0_B	CBE0_B	233	E2PCLK	–	272	HGND	HGND
156	CD4	CD4	195	CWE_B	CWE_B	234	E2PCS	–	273	TDOT	TDOT
157	CD3	CD3	196	COE_B	COE_B	235	Rx7	Rx7	274	TDOC	TDOC
158	CD2	CD2	197	INITD	INITD	236	Rx6	Rx6	275	HV_{DD3}	HV_{DD3}
159	CD1	CD1	198	SCLK	SCLK	237	Rx5	Rx5	276	HV_{DD3}	HV_{DD3}
160	GND	GND	199	GND	GND	238	Rx4	Rx4	277	RDIC	RDIC
161	CD0	CD0	200	ROMA15	–	239	Rx3	Rx3	278	RDIT	RDIT
162	CPAR3	CPAR3	201	ROMA14	–	240	Rx2	Rx2	279	HGND	HGND
163	CPAR2	CPAR2	202	ROMA13	–	241	Rx1/TFKC	Rx1/TFKC	280	RV_{DD3}	RV_{DD3}
164	CPAR1	CPAR1	203	ROMA12	–	242	Rx0/TFKT	Rx0/TFKT	281	JRST_B	JRST_B
165	CPAR0	CPAR0	204	ROMA11	–	243	GND	GND	282	JCK	JCK
166	CA18	CA18	205	ROMA10	–	244	RCLK	RCLK	283	JMS	JMS
167	GND	GND	206	ROMA9	–	245	V_{DD3}	V_{DD3}	284	JDO	JDO
168	CA17	CA17	207	ROMA8	–	246	RENBL_B	RENBL_B	285	JDI	JDI
169	CA16	CA16	208	V_{DD3}	V_{DD3}	247	RSOC	RSOC	286	RGND	RGND
170	CA15	CA15	209	ROMA7	–	248	EMPTY_B/ RCLAV/ RCIC	EMPTY_B/ RCLAV/ RCIC	287	V_{DD5}	V_{DD5}
171	CA14	CA14	210	ROMA6	–	249	FULL_B/ TCLAV/ RCIT	FULL_B/ TCLAV/ RCIT	288	INTR_B	INTR_B
172	CA13	CA13	211	ROMA5	–	250	TSOC	TSOC	289	RST_B	RST_B
173	CA12	CA12	212	ROMA4	–	251	TENBL_B	TENBL_B	290	CLK	CLK
174	GND	GND	213	ROMA3	–	252	GND	GND	291	GNT_B	GNT_B
175	V_{DD3}	V_{DD3}	214	GND	GND	253	TCLK	TCLK	292	GND	GND
176	CA11	CA11	215	ROMA2	–	254	V_{DD3}	V_{DD3}	293	V_{DD3}	V_{DD3}
177	CA10	CA10	216	ROMA1	–	255	Tx7	Tx7	294	REQ_B	REQ_B
178	CA9	CA9	217	ROMA0	–	256	Tx6	Tx6	295	AD31	AD31
179	CA8	CA8	218	ROMD7	–	257	Tx5	Tx5	296	AD30	AD30
180	CA7	CA7	219	ROMD6	–	258	Tx4	Tx4	297	AD29	AD29
181	CA6	CA6	220	ROMD5	–	259	GND	GND	298	GND	GND
182	GND	GND	221	ROMD4	–	260	Tx3	Tx3	299	V_{DD5}	V_{DD5}
183	CA5	CA5	222	ROMD3	–	261	Tx2	Tx2	300	AD28	AD28
184	CA4	CA4	223	ROMD2	–	262	Tx1	Tx1	301	AD27	AD27
185	CA3	CA3	224	ROMD1	–	263	Tx0	Tx0	302	AD26	AD26
186	CA2	CA2	225	ROMD0	–	264	PHRST_B	PHRST_B	303	AD25	AD25
187	CA1	CA1	226	ROMCS_B	–	265	PHOE_B	PHOE_B	304	GND	GND

Remarks 1. Open the pins to which no function is allocated (pins marked "–" in the Generic Mode column in the above table) in the Generic mode. Fix pin 5 (IDSEL) to the low/high level.

2. In this document, the active-low pin and active-low signal are represented as XXX_B (_B suffix following the pin/signal name).

304-pin plastic FBGA (0.8 mm pitch) (19 × 19)

(1/2)

No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode
B2	GND	GND	N1	AD8	AD8	AB5	AD50	–	V15	CD20	CD20
C2	VDD3	VDD3	N2	PCBE0_B	BE0_B	AA6	AD49	–	AB16	CD19	CD19
B1	AD24	AD24	N4	AD7	AD7	AB6	AD48	–	AA16	CD18	CD18
C1	PCBE3_B	BE3_B	P6	AD6	AD6	U7	GND	GND	W16	CD17	CD17
D2	IDSEL	–	P5	GND	GND	W7	VDD5	VDD5	U16	GND	GND
E5	AD23	AD23	P1	VDD3	VDD3	AA7	AD47	–	AB17	VDD3	VDD3
E4	GND	GND	P2	AD5	AD5	AB7	AD46	–	AA17	CD16	CD16
E2	VDD5	VDD5	P4	AD4	AD4	V8	AD45	–	AB18	CD15	CD15
D1	AD22	AD22	R1	AD3	AD3	U8	AD44	–	V16	CD14	CD14
F5	AD21	AD21	R2	AD2	AD2	W8	GND	GND	W17	CD13	CD13
F4	AD20	AD20	R4	GND	GND	AA8	VDD3	VDD3	V17	CD12	CD12
G5	AD19	AD19	R6	VDD5	VDD5	AB8	AD43	–	AB19	CD11	CD11
E1	GND	GND	R5	AD1	AD1	W9	AD42	–	AA18	GND	GND
F2	VDD3	VDD3	T1	AD0	AD0	AA9	AD41	–	W18	CD10	CD10
F1	AD18	AD18	T2	ACK64_B	OE_B	AB9	AD40	–	U17	CD9	CD9
G6	AD17	AD17	T4	REQ64_B	DR/W_B	V9	GND	GND	AA19	CD8	CD8
G4	AD16	AD16	T6	GND	GND	U9	VDD5	VDD5	AB20	CD7	CD7
G2	PCBE2_B	BE2_B	U1	VDD3	VDD3	W10	AD39	–	W19	CD6	CD6
G1	GND	GND	U2	PCBE7_B	SIZE2	AA10	AD38	–	AA20	VDD3	VDD3
H5	VDD5	VDD5	V1	PCBE6_B	SIZE1	AB10	AD37	–	AB21	GND	GND
H6	FRAME_B	SEL_B	T5	PCBE5_B	SIZE0	V10	AD36	–	AA21	GND	GND
H4	IRDY_B	ASEL_B	U4	PCBE4_B	PAR3	U10	GND	GND	Y21	VDD3	VDD3
H2	TRDY_B	RDY_B	U5	VDD5	VDD5	V11	VDD3	VDD3	AA22	CD5	CD5
H1	DEVSEL_B	SR/W_B	W1	GND	GND	AA11	AD35	–	Y22	CD4	CD4
J4	GND	GND	V2	AD63	PAR2	AB11	AD34	–	W21	CD3	CD3
J2	VDD3	VDD3	V4	AD62	PAR1	W11	AD33	–	V18	CD2	CD2
J1	STOP_B	ABRT_B	V5	AD61	PAR0	W12	AD32	–	V19	CD1	CD1
J5	PERR_B	ERR_B	W2	VDD3	VDD3	AB12	PAR64	–	V21	GND	GND
J6	SERR_B	–	Y1	AD60	–	AA12	GND	GND	W22	CD0	CD0
K4	PAR	–	AA1	AD59	–	V12	PCI_MODE	PCI_MODE	U18	CPAR3	CPAR3
K2	GND	GND	Y2	AD58	–	U13	CD31	CD31	U19	CPAR2	CPAR2
K1	VDD5	VDD5	AA2	GND	GND	V13	CD30	CD30	T18	CPAR1	CPAR1
K5	PCBE1_B	BE1_B	AB2	GND	GND	AB13	CD29	CD29	V22	CPAR0	CPAR0
K6	AD15	AD15	AA3	VDD3	VDD3	AA13	CD28	CD28	U21	CA18	CA18
L5	AD14	AD14	W4	AD57	–	W13	CD27	CD27	U22	GND	GND
L2	AD13	AD13	AB3	AD56	–	U14	GND	GND	T17	CA17	CA17
L1	GND	GND	AA4	VDD5	VDD5	V14	VDD3	VDD3	T19	CA16	CA16
L4	VDD3	VDD3	U6	AD55	–	AB14	CD26	CD26	T21	CA15	CA15
M4	AD12	AD12	W5	AD54	–	AA14	CD25	CD25	T22	CA14	CA14
M1	AD11	AD11	AA5	AD53	–	W14	CD24	CD24	R18	CA13	CA13
M2	AD10	AD10	AB4	AD52	–	AB15	CD23	CD23	R17	CA12	CA12
M5	AD9	AD9	V6	GND	GND	AA15	CD22	CD22	R19	GND	GND
N6	GND	GND	W6	VDD3	VDD3	W15	GND	GND	R21	VDD3	VDD3
N5	VDD5	VDD5	V7	AD51	–	U15	CD21	CD21	R22	CA11	CA11

Remark In this document, the active-low pin and active-low signal are represented as XXX_B (_B suffix following the pin/signal name).

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No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode	No.	PCI Mode	Generic Mode
P19	CA10	CA10	H18	ROMA7	–	A18	Rx1/TFKC	Rx1/TFKC	A10	TDOT	TDOT
P21	CA9	CA9	G22	ROMA6	–	B17	Rx0/TFKT	Rx0/TFKT	B10	TDOC	TDOC
P22	CA8	CA8	G21	ROMA5	–	A17	GND	GND	D10	HV_{DD3}	HV_{DD3}
P18	CA7	CA7	G19	ROMA4	–	F16	RCLK	RCLK	F9	HV_{DD3}	HV_{DD3}
P17	CA6	CA6	G17	ROMA3	–	D16	V_{DD3}	V_{DD3}	E9	RDIC	RDIC
N19	GND	GND	F22	GND	GND	B16	RENBL_B	RENBL_B	A9	RDIT	RDIT
N21	CA5	CA5	F21	ROMA2	–	A16	RSOC	RSOC	B9	HGND	HGND
N22	CA4	CA4	E22	ROMA1	–	E15	EMPTY_B/ RCLAV/R CIC	EMPTY_B / RCLAV/ RCIC	D9	RV_{DD3}	RV_{DD3}
N18	CA3	CA3	G18	ROMA0	–	F15	FULL_B/ TCLAV/ RCIT	FULL_B/ TCLAV/ RCIT	A8	JRST_B	JRST_B
N17	CA2	CA2	F19	ROMD7	–	D15	TSOC	TSOC	B8	JCK	JCK
M18	CA1	CA1	F18	ROMD6	–	B15	TENBL_B	TENBL_B	D8	JMS	JMS
M21	CA0	CA0	D22	ROMD5	–	A15	GND	GND	F8	JDO	JDO
M22	GND	GND	E21	ROMD4	–	D14	TCLK	TCLK	E8	JDI	JDI
M19	V_{DD3}	V_{DD3}	E19	ROMD3	–	B14	VDD3	VDD3	A7	RGND	RGND
L19	CBE3_B	CBE3_B	E18	ROMD2	–	A14	Tx7	Tx7	B7	V_{DD5}	V_{DD5}
L22	CBE2_B	CBE2_B	D21	ROMD1	–	E14	Tx6	Tx6	D7	INTR_B	INTR_B
L21	CBE1_B	CBE1_B	C22	ROMD0	–	F14	Tx5	Tx5	F7	RST_B	RST_B
L18	CBE0_B	CBE0_B	B22	ROMCS_B	–	D13	Tx4	Tx4	A6	CLK	CLK
K17	CWE_B	CWE_B	C21	V_{DD3}	V_{DD3}	B13	GND	GND	B6	GNT_B	GNT_B
K18	COE_B	COE_B	B21	GND	GND	A13	Tx3	Tx3	A5	GND	GND
K22	INITD	INITD	A21	GND	GND	E13	Tx2	Tx2	E7	V_{DD3}	V_{DD3}
K21	SCLK	SCLK	B20	ROMOE_B	–	F13	Tx1	Tx1	D6	REQ_B	ATTN_B
K19	GND	GND	D19	E2PDI	–	E12	Tx0	Tx0	E6	AD31	AD31
J17	ROMA15	–	A20	E2PDO	–	B12	PHRST_B	PHRST_B	A4	AD30	AD30
J18	ROMA14	–	B19	E2PCLK	–	A12	PHOE_B	PHOE_B	B5	AD29	AD29
J22	ROMA13	–	F17	E2PCS	–	D12	PHYALM/ PHR/W_B	PHYALM/ PHR/W_B	D5	GND	GND
J21	ROMA12	–	D18	Rx7	Rx7	D11	SD/PHCE_B	SD/PHCE_B	F6	V_{DD5}	V_{DD5}
J19	ROMA11	–	B18	Rx6	Rx6	A11	REFCLK/ PHINT_B	REFCLK/ PHINT_B	B4	AD28	AD28
H22	ROMA10	–	A19	Rx5	Rx5	B11	AV_{DD3}	AV_{DD3}	A3	AD27	AD27
H21	ROMA9	–	E17	Rx4	Rx4	E11	AGND	AGND	D4	AD26	AD26
H19	ROMA8	–	D17	Rx3	Rx3	F10	TEST	TEST	B3	AD25	AD25
H17	V_{DD3}	V_{DD3}	E16	Rx2	Rx2	E10	HGND	HGND	A2	GND	GND

Remarks 1. Open the pins to which no function is allocated (pins marked "–" in the Generic Mode column in the above table) in the Generic mode. Fix pin 5 (IDSEL) to the low/high level.

2. In this document, the active-low pin and active-low signal are represented as XXX_B (_B suffix following the pin/signal name).

CONTENTS

1. PIN FUNCTIONS

The package of the μPD98405 has 304 pins. For details on how to use each pin, refer to **μPD98405 User's Manual (S12250E)**.

1.1 PHY Layer Device Interface Signal

The PHY Layer device interfaces include a UTOPIA interface by which the μPD98405 exchanges ATM cells with a PHY device, and PHY control interface that is used to control a PHY device. The μPD98405 supports two types of PHY layer device interfaces: UTOPIA octet and cell level. These modes are selected by setting the UOC bit of the GMR register.

The PHY layer device interface signals are for an external PHY layer device. When using an internal PHY layer, open all the pins except the common pins. Even when the internal PHY layer is used, an external receive FIFO can be connected to the μPD98405 via the UTOPIA interface.

1.1.1 UTOPIA interface

(1/2)

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
Rx7 to Rx0 (Rx1 and Rx0: Shared with TFKC and TFKT)	235 to 242	D18, B18, A19, E17, D17, E16, A18, B17	I	TTL	Receive data bus. These pins constitute an 8-bit input bus that inputs receive data from the network to the μPD98405 from the PHY layer device in byte format. The μPD98405 reads the data on this bus in synchronization with the rising edge of RCLK. Rx7 to Rx2 are internally pulled down. Open the pins of this bus when they are not used. Pull up Rx1 when it is not used, and pull down Rx0 when it is not used.
RSOC	247	A16	I	TTL	Receive cell start position. This signal is input from the PHY layer device in synchronization with the first byte of cell data. It is high while the first byte of a header is input to Rx7 to Rx0. This signal is internally pulled down.
RENBL_B	246	B16	O	TTL	Receive enable. This signal informs the PHY layer device that the μPD98405 is ready to receive data in the next clock cycle.

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Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
EMPTY_B/ RCLAV (shared with RCIC)	248	E15	I	TTL	PHY layer buffer empty/receive cell available. This signal informs the μPD98405 that the PHY receive FIFO has no cell data to be transferred and that the PHY device cannot supply receive data. This signal functions as EMPTY_B when the UTOPIA interface is in the octet level handshake mode, to indicate that the data on Rx7 to Rx0 is invalid in the current clock cycle. In the cell level handshake mode, it functions as RCLAV, informing the μPD98405 that no more cells are to be supplied after transfer of the current cell is completed. Pull down this pin when it is not used.
RCLK	244	F16	O	TTL	Receive clock. This clock is used for synchronization when the μPD98405 transfers cell data to and from the PHY layer device at the reception side. The SAR system clock input to the SCLK pin is output from this pin as is, immediately after the μPD98405 has been reset.
Tx7 to Tx0	255 to 258, 260 to 263	A14, E14, F14, D13, A13, E13, F13, E12	O	TTL	Transmit data bus. These pins form an 8-bit output bus that outputs data to be transmitted to the network, to the PHY layer device in byte format. The μPD98405 outputs the data in synchronization with the rising edge of TCLK.
TSOC	250	D15	O	TTL	Transmit cell start position. This signal is output in synchronization with the first byte of transmit cell data.
TENBL_B	251	B15	O	TTL	Transmit enable. This signal informs the PHY layer device that data has been output to Tx7 to Tx0 in the current clock cycle.
FULL_B/ TCLAV (shared with RCIT)	249	F15	I	TTL	PHY layer buffer full/transmit cell available. The FULL_B signal informs the μPD98405 that the input buffer of the PHY device is full and that the device can receive no more data. When the UTOPIA interface is in the octet level handshake mode, the PHY device inputs an inactive level as this signal if the device can receive cell data. In the cell level handshake mode, this signal functions as TCLAV, informing the μPD98405 that the PHY device can receive the next single cell after transfer of the current cell is completed. Pull up this pin when it is not used.
TCLK	253	D14	O	TTL	Transmit clock. This clock is used for synchronization when the μPD98405 transfers cell data to and from the PHY layer device at the transmission side. The SAR system clock input to the SCLK pin is output as this clock as is.

1.1.2 PHY device control interface (external PHY mode, PHM of GMR register = 1)

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
PHR/W_B (shared with PHYALM)	266	D12	O	TTL	PHY read/write. The μPD98405 indicates the PHY layer device control direction by using this pin. 1: Read 0: Write
PHOE_B	265	A12	O	TTL	PHY layer output enable. The μPD98405 enables output by the PHY layer device by making this signal low.
PHCE_B (shared with SD)	267	D11	O	TTL	PHY layer chip enable. The μPD98405 makes this signal low when it accesses the PHY layer device.
PHINT_B (shared with REFCLK)	268	A11	I	TTL	PHY layer interrupt. This pin inputs an interrupt signal to the μPD98405 from the PHY layer device. The PHY layer device informs the μPD98405 that it has an interrupt source by inputting a low level to this pin. Pull up this pin when it is not used.
PHRST_B	264	B12	O	TTL	PHY layer reset. This signal is used to reset the PHY layer device. The μPD98405 keeps this pin low for the duration of 17 clock cycles when a low level is input to the RST_B pin or when software reset is executed.

Caution The PHCE_B/SD pins are multiplexed pins and their functions differ depending on whether the internal PHY mode or external PHY mode is selected (by using the PHM bit of the GMR register). Because the PHCE_B/SD pins change the mode between input and output depending on the selected mode, be sure to correctly set the PHM bit of the GMR register.

1.2 Bus Interface Signals

The μPD98405 supports a PCI bus interface or generic bus interface. Whether the PCI bus interface or generic bus interface is to be supported is selected by the PCI_MODE signal.

The PCI bus interface can be directly connected to a PCI bus. The generic bus interface can be connected to a general I/O bus with a few circuits.

1.2.1 Generic bus interface signals (PCI_MODE pin: low level)

(1/3)

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
AD31 to AD0	295 to 297, 300 to 303, 3, 6, 9 to 12, 15 to 17, 34 to 36, 39 to 42, 45, 47, 48, 51 to 54, 57 to 58	E6, A4, B5, B4, A3, D4, B3, B1, E5, D1, F5, F4, G5, F1, G6, G4, K6, L5, L2, M4, M1, M2, M5, N1, N4, P6, P2, P4, R1, R2, R5, T1	I/O 3-state	TTL	Address/data. These pins constitute a 32-bit address/data bus. They are input/output pins multiplexing an address bus and a data bus. An address is transferred at the first input/output clock. From the second clock and onward, data is transferred. When the μPD98405 is not accessing the bus, the AD bus goes into a high-impedance state.
BE3_B BE2_B BE1_B BE0_B	4 18 33 46	C1 G2 K5 N2	O 3-state	TTL	Byte enable. These pins determine the byte that becomes valid in the master cycle of the μPD98405. BE3_B corresponds to AD31 to AD24, and BE0_B corresponds to AD7 to AD0. BE3_B to BE0_B go into a high-impedance state when the μPD98405 is not accessing a bus or when it is accessing a slave.
PAR3 PAR2 PAR1 PAR0	66 69 70 71	U4 V2 V4 V5	I/O 3-state	TTL	Bus parity. These pins indicate the parity of AD31 to AD0. A parity check mode is set by the GMR register. Whether the parity is enabled or disabled, whether an odd parity or even parity is used, and whether a word parity or byte parity is used can be specified. When byte parity is used, PAR3 indicates the parity of AD31 to AD24, and PAR0 indicates the parity of AD7 to AD0. In the case of word parity, PAR2 to PAR0 do not function, and PAR3 serves as an input/output pin. These pins function as output pins when an address is output and when data is written, and as input pins when data is read. When the μPD98405 is not accessing a bus, PAR3 to PAR0 go into a high-impedance state. Pull up these pins when they are not used.
OE_B	59	T2	I	TTL	Output enable. When this pin is low, the μPD98405 allows AD31 to AD0 and PAR3 to PAR0 to operate normally as 3-state I/O pins. These pins go into a high-impedance state while a high level is input to this pin. Fix this pin to the low level in a system where the above pins do not have to forcibly go into a high-impedance state.

(2/3)

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">I/O Level</th><th rowspan="2">Function</th></tr>
<tr><th>QFP</th><th>FBGA</th></tr>
<tr><td>SIZE2
SIZE1
SIZE0</td><td>63
64
65</td><td>U2
V1
T5</td><td>O</td><td>TTL</td><td>Burst size.
These pins indicate the size of current DMA transfer. They are used to interface with a bus (such as S bus) that requires an explicit burst size.

<table><tr><th>SIZE2</th><th>SIZE1</th><th>SIZE0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1-word transfer</td></tr><tr><td>0</td><td>0</td><td>1</td><td>2-word burst</td></tr><tr><td>0</td><td>1</td><td>0</td><td>4-word burst</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-word burst</td></tr><tr><td>1</td><td>0</td><td>0</td><td>16-word burst</td></tr><tr><td>1</td><td>0</td><td>1</td><td>12-word burst</td></tr><tr><td colspan="3">Other than above</td><td>Undefined</td></tr></table></td></tr>
<tr><td>DR/W_B</td><td>60</td><td>T4</td><td>O</td><td>TTL</td><td>DMA read/write.
This pin indicates the direction of DMA access.
1: Read access
0: Write access</td></tr>
<tr><td>ATTN_B</td><td>294</td><td>D6</td><td>O</td><td>TTL</td><td>Attention (DMA request).
The μPD98405 makes the ATTN_B signal low when it is to execute a DMA operation. The ATTN_B signal becomes inactive in synchronization with the rising edge of CLK when only one more word of data is to be transferred by means of DMA.</td></tr>
<tr><td>GNT_B</td><td>291</td><td>B6</td><td>I</td><td>TTL</td><td>Bus enable.
The GNT_B signal goes low when the bus arbiter grants the μPD98405 the bus mastership in response to a DMA request from the μPD98405. When the μPD98405 detects that the GNT_B signal has gone low, it starts a DMA operation, assuming that the bus mastership has been granted.</td></tr>
<tr><td>RDY_B</td><td>23</td><td>H2</td><td>I</td><td>TTL</td><td>Target device ready.
This signal informs the μPD98405 in the DMA cycle that the target device is ready for input/output. The μPD98405 makes the RDY_B signal low if valid data exists on AD31 to AD0 when it executes a DMA read operation. When executing a DMA write operation, the μPD98405 makes the ATTN_B signal low if the target device is ready for reception.
The timing at which the μPD98405 samples the RDY_B and ABRT_B signals can be bring forward by 1 clock depending on the setting of an internal register (GMR register).</td></tr>
</table>

(3/3)

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
ABRT_B	27	J1	I	TTL	Abort. This signal is used to abort a data transfer cycle. If this signal goes low in the middle of a data transfer cycle, that cycle is aborted, and the μPD98405 resumes burst starting from the aborted data. While a low level is input to ABRT_B, the RDY_B signal does not function. The user can bring forward the timing at which the μPD98405 samples the RDY_B and ABRT_B signals by 1 clock (early mode) by using an internal register (GMR register). Pull up this pin when it is not used.
ERR_B	28	J5	I	TTL	System bus error. If an error is detected on the system bus, the device that manages the bus uses this pin to stop the operation by the μPD98405. When a low level is input to this pin, the μPD98405 stops all bus operations, sets the system bus error bit (bit 25) of the GSR register (when not masked), and generates an interrupt. Pull up this pin when it is not used.
SR/W_B	24	H1	I	TTL	Slave read/write. This signal determines the direction of slave access. 1: Read access 0: Write access
SEL_B	21	H6	I	TTL	Slave select. This signal is asserted active (low) when slave access is selected for the μPD98405. Make sure that the SEL_B signal goes low at the same time as or after the ASEL_B signal has gone low. In addition, insert an inactive period of two system clocks or more after the SEL_B signal has become inactive and before it becomes active next time.
ASEL_B	22	H4	I	TTL	Slave address select. The ASEL_B signal selects the direct address register of the μPD98405. When a low level is input to ASEL_B, the μPD98405 samples the AD bus at the first rising edge of CLK.
CLK	290	A6	I	TTL	Clock. This is a system bus clock input pin. A clock of up to 33 MHz can be input.
RST_B	289	F7	I	TTL	Reset. The RST_B signal initializes the μPD98405 (on starting). After reset, the μPD98405 can start normal operation. When a low level is input to RST_B, the internal state machine and registers of the μPD98405 are reset, and all the 3-state signals go into a high-impedance state. Reset input is asynchronous. If it is input during operation, the operation status at that time is lost. Keep RST_B low at least for the duration of one clock cycle.
INTR_B	288	D7	O	N-ch open-drain	Interrupt output. Pull up this signal because it is an open-drain signal. This signal informs the CPU that an unmasked interrupt bit of the interrupt GSR register has been set.

1.2.2 PCI bus interface signal (PCI_MODE pin: high level)

The μPD98405 has a 32-/64-bit PCI bus interface. This bus interface can be directly connected to a PCI bus. In addition, the μPD98405 also has a serial EEPROM interface and an expansion ROM interface.

<1> PCI bus interface signals

(1/2)

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
AD31 to AD0	295 to 297, 300 to 303, 3, 6, 9 to 12, 15 to 17, 34 to 36, 39 to 42, 45, 47, 48, 51 to 54, 57 to 58	E6, A4, B5, B4, A3, D4, B3, B1, E5, D1, F5, F4, G5, F1, G6, G4, K6, L5, L2, M4, M1, M2, M5, N1, N4, P6, P2, P4, R1, R2, R5, T1	I/O 3-state	PCI	Address/data. AD31 to AD0 constitute a 32-bit multiplexed address/data bus. When the μPD98405 operates as a bus master, it drives an address at the first clock and transfers data at the second clock and onward.
PCBE3_B PCBE2_B PCBE1_B PCBE0_B	4 18 33 46	C1 G2 K5 N2	I/O 3-state	PCI	Bus command/byte enable. These signals define a “bus command” (bus transaction that occurs) in the address phase. In the data phase, they indicate which byte lane holds valid data. The PCBE3_B pin corresponds to byte 3 (bits 31 to 24), and PCBE0_B pin corresponds to byte 0 (bits 7 to 0).
PAR	30	K4	I/O 3-state	PCI	Parity. This signal indicates an even parity on the AD31 to AD0 and PCBE3_B to PCBE0_B pins, including the PAR signal. When the μPD98405 is operating as a master, the PAR signal becomes active in the address and write data phases. When the μPD98405 is operating as a target, this signal becomes active in the read data phase.
FRAME_B	21	H6	I/O Sustained 3-state	PCI	Frame. This signal indicates the start and period of a bus transaction. When this signal is asserted active, it indicates the start of a bus transaction. While it is active, data is transferred. It is deasserted inactive when the next data transfer phase will transfer last data of the transaction.
TRDY_B	23	H2	I/O Sustained 3-state	PCI	Target ready. This signal goes low when the target device is ready to complete the transaction of the current data. This signal is used in combination with IRDY_B, and read/write data transfer is executed when both IRDY_B and TRDY_B signals are low.
IRDY_B	22	H4	I/O Sustained 3-state	PCI	Initiator ready. This signal goes low when the initiator is ready to complete the transaction of the current data. This signal is used in combination with TRDY_B, and read/write data transfer is executed when both IRDY_B and TRDY_B are low. If FRAME_B and IRDY_B are both inactive, the bus cycle is not executed. A wait cycle is inserted until both IRDY_B and TRDY_B are asserted active.

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Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
STOP_B	27	J1	I/O Sustained 3-state	PCI	Stop. This signal goes low when the target device requests the master device to stop the current transaction.
DEVSEL_B	24	H1	I/O Sustained 3-state	PCI	Device select. When the μPD98405 is operating as a target, it makes this signal low after the FRAME_B signal has been asserted active and the μPD98405 has recognized an address. When the μPD98405 is operating as a master, it samples this signal to check to see if a target device has been selected.
IDSEL	5	D2	I	PCI	Initialization device select. This signal is high when the configuration register of the μPD98405 is read or written.
REQ_B	294	D6	O[Note]	PCI	Request. The μPD98405 makes this signal low to request the arbiter for the bus mastership.
GNT_B	291	B6	I	PCI	Grant. This signal goes low when the arbiter grants the μPD98405 the bus mastership.
PERR_B	28	J5	I/O Sustained 3-state	PCI	Parity error. This signal indicates that the μPD98405 has detected a data parity error. It is enabled when the “Parity Error Response” bit of the configuration register is set to 1.
SERR_B	29	J6	O	N-ch open-drain	System error. This signal indicates that the μPD98405 has detected an address parity error. It is enabled when both the “Parity Error Response” and “System Error Enable” bits of the configuration register are set to 1.
INTR_B	288	D7	O	N-ch open-drain	Interrupt output. Pull up this signal because it is an open-drain signal. INTR_B informs the CPU that an unmasked interrupt bit of the interrupt GSR register has been set.
CLK	290	A6	I	PCI	Clock. This is a system bus clock input pin. A clock of up to 33 MHz is input.
RST_B	289	F7	I	PCI	Reset. This signal initializes the μPD98405 (on starting, etc.). When a low level is input to RST_B, the internal state machine and registers of the μPD98405 are reset, and all the 3-state signals go into a high-impedance state. The reset input is asynchronous. When this signal is input during operation, the operating status at that time is lost. Keep RST_B low at least for the duration of one clock cycle. After reset, do not access the μPD98405 for the duration of at least 20 clocks.

Note According to “PCI Local Bus Specification Revision 2.1”, the REQ_B pin should go into a high-impedance state while a low level is input to the RST_B pin. The REQ_B pin of the μPD98405, however, outputs a high level.

<2> PCI bus 64-bit expansion interface signals

Open AD63 to AD32, PCBE7_B to PCBE4_B, and PAR64 when using the 32-bit PCI bus interface.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
AD63 to AD32	69 to 71, 73 to 75, 79, 80, 82 to 85, 88 to 91, 94 to 97, 100 to 103, 106 to 109, 112 to 115	V2, V4, V5, Y1, AA1, Y2, W4, AB3, U6, W5, AA5, AB4, V7, AB5, AA6, AB6, AA7, AB7, V8, U8, AB8, W9, AA9, AB9, W10, AA10, AB10, V10, AA11, AB11, W11, W12	I/O 3-state	PCI	Address/data. AD63 to AD32 constitutes a 32-bit multiplexed address/data bus that extends the PCI bus to 64 bits. This address/data bus transfers the higher 32 bits of a 64-bit address in the address phase. It outputs the higher 32 bits of 64-bit data in the data phase when both REQ64_B and ACK64_B are asserted.
PCBE7_B PCBE6_B PCBE5_B PCBE4_B	63 64 65 66	U2 V1 T5 U4	I/O 3-state	PCI	Bus command/byte enable. These signals define a “bus command” (bus transaction that occurs) in the address phase. In the data phase, they indicate which byte lane holds valid data. The PCBE7_B pin corresponds to AD63 to AD56, and PCBE4_B pin corresponds to AD39 to AD32.
PAR64	116	AB12	I/O 3-state	PCI	Parity 64. This signal indicates an even parity on AD63 to AD32 and PCBE7_B to PCBE4_B pins, including the PAR64 signal. When the μPD98405 is operating as a master, the PAR signal becomes active in the address and write data phases. When the μPD98405 is operating as a target, it becomes active in the read data phase.
★ REQ64_B	60	T4	I/O Sustained 3-state	PCI	Request 64. This signal indicates the start and period of a 64-bit bus transaction. When the μPD98405 is operating as a master, it asserts REQ64_B active to request 64-bit data transfer. REQ64_B is the same as FRAME_B in timing. Connect an external pull-up resistor when using a 32-bit PCI bus.
★ ACK64_B	59	T2	I	PCI	Acknowledge 64. When the μPD98405 is operating as a target, it makes this signal low after the REQ64_B signal has been asserted active and the μPD98405 has recognized an address. When the μPD98405 is operating as a master, it samples this signal to check whether the target device has acknowledged 64-bit transfer. ACK64_B is the same as DEVSEL_B in timing. Connect an external pull-up resistor when using a 32-bit PCI bus.

<3> Serial EEPROM interface signals

The μPD98405 has a serial EEPROM interface supporting MICROWIRE™ interface. Through this serial EEPROM interface, the contents of the PCI configuration register can be loaded from an EEPROM connected.

Remark It is recommended that National Semiconductor's "NM93C46" be connected as the EEPROM.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
E2PCS	234	F17	O	TTL	EEPROM chip select. This is a chip select signal for EEPROM.
E2PDI	231	D19	I	TTL	EEPROM data input. This signal is connected to the data output pin of the EEPROM. This signal is internally pulled down.
E2PDO	232	A20	O	TTL	EEPROM data output. This signal is connected to the data input pin of the EEPROM.
E2PCLK	233	B19	O	TTL	EEPROM clock. This pin supplies the clock necessary for transferring data with the EEPROM. It divides the clock input to the CLK pin by 36 for output.

<4> Expansion ROM interface signals.

The μPD98405 has an expansion ROM interface as option.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
ROMA15 to ROMA0	200 to 207, 209 to 213, 215 to 217	J17, J18, J22, J21, J19, H22, H21, H19, H18, G22, G21, G19, G17, F21, E22, G18	O	TTL	ROM address. These are address signals to access the 64K expansion ROM.
ROMD7 to ROMD0	218 to 225	F19, F18, D22, E21, E19, E18, D21, C22	I	TTL	ROM data. These are expansion ROM data signals and are internally pulled down.
ROMCS_B	226	B22	O	TTL	ROM select. This is a chip select signal for the expansion ROM.
ROMOE_B	230	B20	O	TTL	ROM output enable. This signal enables the output buffer of the expansion ROM during a read operation.

1.3 Control Memory Interface Signals

The control memory interface is used by the μPD98405 to access the external control memory and external PHY layer device. This interface consists of a 19-bit address bus, a 32-bit data bus. The control memory of the host system can be accessed only through this interface.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
CD31 to CD0	119 to 123, 126 to 130, 132 to 136, 139 to 144, 146 to 150, 155 to 159, 161	U13, V13, AB13, AA13, W13, AB14, AA14, W14, AB15, AA15, U15, V15, AB16, AA16, W16, AA17, AB18, V16, W17, V17, AB19, W18, U17, AA19, AB20, W19, AA22, Y22, W21, V18, V19, W22	I/O 3-state	TTL	Control memory data. These 3-state I/O pins constitute a 32-bit data bus that is used to transfer data to and from the control memory or PHY layer device. These signals are internally pulled down.
CPAR3 to CPAR0	162 to 165	U18, U19, T18, V22	I/O	TTL	Control memory parity. These signals indicate the parity of CD31 to CD0 every 8 bits. In the read cycle, the μPD98405 checks the parity (when enabled). In the write cycle, it outputs the parity. These signals are internally pulled down.
CA18 to CA0	166, 168 to 173, 176 to 181, 183 to 188	U21, T17, T19, T21, T22, R18, R17, R22, P19, P21, P22, P18, P17, N21, N22, N18, N17, M18, M21	O	TTL	Control memory address. These signals constitute a 19-bit address bus that outputs an address to the control memory or PHY layer device during a read/write operation.
CWE_B	195	K17	O	TTL	Control memory write enable. This signal indicates the direction in which the control memory is accessed. 1: Read access 0: Write access
COE_B	196	K18	O	TTL	Control memory output enable. This signal enables or disables data output of the control memory.
CBE3_B to CBE0_B	191 to 194	L19, L22, L21, L18	O	TTL	Local port byte enable. These signals indicate the byte of the control port to be read or written.
INITD	197	K22	I	TTL	Initialization disable. This signal is used to disable automatic initialization of the control memory during chip test. Directly connect INITD to GND during normal operation other than test.

1.4 PMD Interface Signals (internal PHY mode, PHM of GMR register = 0)

The PMD interface is used to connect a module such as an optical transceiver/receiver.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
RDIT	278	A9	I	P-ECL True (+)	Receive serial data input. Pull up this pin when it is not used.
RDIC	277	E9	I	P-ECL complement (–)	Receive serial data input. Pull down this pin when it is not used.
RCIT (shared with FULL_B)	249	F15	I	P-ECL True (+)	Receive serial clock input. This pin is used when an external clock recovery/synthesizer is connected (PLL of GMR register = 1). Pull up this pin when it is not used.
RCIC (shared with EMPTY_B)	248	E15	I	P-ECL complement (–)	Receive serial clock input. This pin is used when an external clock recovery/synthesizer is connected (PLL of GMR register = 1). Pull down this pin when it is not used.
REFCLK (shared with PHINT_B)	268	A11	I	TTL	Reference clock. This pin inputs a system clock (19.44 MHz) to the internal clock recovery/synthesizer. Pull up this pin when it is not used.
TDOT	273	A10	O	P-ECL True (+)	Transmit serial data output.
TDOC	274	B10	O	P-ECL complement (–)	Transmit serial data output.
TFKT (shared with Rx0)	242	B17	I	P-ECL True (+)	Transmit serial clock input. This pin is used when an external clock recovery/synthesizer is connected (PLL of GMR register = 1). Pull up this pin when it is not used.
TFKC (shared with Rx1)	241	A18	I	P-ECL complement (–)	Transmit serial clock input. This pin is used when an external clock recovery/synthesizer is connected (PLL of GMR register = 1). Pull down this pin when it is not used.
PHYALM (shared with PHR/W_B)	266	D12	O	TTL	PHY layer alarm detection signal. This signal is asserted active (high) when any of the internally monitored error statuses (CMDARM, LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, and Path RDI) is detected. The error status to be reported can be selected by using the internal AMR1 and AMR2 registers. One or more error statuses can be selected.
SD (shared with PHCE_B)	267	D11	I	TTL	Signal detect. This pin inputs the signal detect signal (when LOS is detected, etc.) of the PMD device. When a low level is input to this pin, the μPD98405 assumes LOS detection. Pull up this pin when it is not used.

1.5 JTAG Boundary Scan Signals

Remark This function can be supported upon request.

These signals conform to IEEE1149.1 JTAG Boundary-Scan Standard.

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
JDI	285	E8	I	TTL	Boundary scan data input. Connect this pin to ground when it is not used.
JDO	284	F8	O 3-state	TTL	Boundary scan data output. Open this pin when it is not used.
JMS	283	D8	I	TTL	Boundary scan mode select. Connect this pin to ground when it is not used.
★ JCK	282	B8	I	TTL	Boundary scan clock input. Input a clock of up to 1 MHz. Connect this pin to ground when it is not used.
JRST_B	281	A8	I	TTL	Boundary scan reset. Connect this pin to ground when it is not used.

1.6 Other Signals

Pin Name	Pin No.		I/O	I/O Level	Function
	QFP	FBGA			
★ SCLK	198	K21	I	TTL	SAR system clock. This pin supplies a clock for a SAR block operation. The maximum clock frequency is 25 MHz. Ver. 3.1 or before: 25 MHz MAX. Ver. 4.0: 33 MHz MAX.
PCI_MODE	118	V12	I	TTL	PCI/generic bus mode. This pin selects PCI or generic bus mode. 0: Generic bus mode 1: PCI bus mode
TEST	271	F10	I	TTL	Internal test pin. Open this pin. When a high level is input to this pin, the test mode is selected. This signal is internally pulled down. The test mode is used for internal testing and cannot be used by the user.

1.7 Power and Ground

Pin Name	Pin No.		I/O	Function
	QFP	FBGA		
V_{DD5}	8, 20, 32, 44, 56, 67, 81, 93, 105, 287, 299	E2, H5, K1, N5, R6, U5, AA4, W7, U9, B7, F6	–	+5 V power (digital block). Supply +5 V to these pins when using the bus interface 5 V mode. In the 3.3 V mode, supply +3.3 V.
V_{DD3}	2, 14, 26, 38, 50, 62, 72, 78, 87, 99, 111, 125, 138, 151, 154, 175, 190, 208, 227, 245, 254, 293	C2, F2, J2, L4, P1, U1, W2, AA3, W6, AA8, V11, V14, AB17, AA20, Y21, R21, M19, H17, C21, D16, B14, E7	–	+3.3 V power (digital block). These pins supply +3.3 V to the chip.
AV_{DD3}	269	B11	–	+3.3 V power (analog block). Supply power with a high quality to this pin by inserting a filter between AV_{DD3} and GND.
HV_{DD3}	275, 276	D10, F9	–	+3.3 V power (high-speed block). Supply power with a high quality to this pin by inserting a filter between HV_{DD3} and HGND.
RV_{DD3}	280	D9	–	+3.3 V power (receive PLL block). Supply power with a high quality to this pin by inserting a filter between RGND and this pin.
GND	1, 7, 13, 19, 25, 31, 37, 43, 49, 55, 61, 68, 76, 77, 86, 92, 98, 104, 110, 117, 124, 131, 137, 145, 152, 153, 160, 167, 174, 182, 189, 199, 214, 228, 229, 243, 252, 259, 292, 298, 304	B2, E4, E1, G1, J4, K2, L1, N6, P5, R4, T6, W1, AA2, AB2, V6, U7, W8, V9, U10, AA12, U14, W15, U16, AA18, AB21, AA21, V21, U22, R19, N19, M22, K19, F22, B21, A21, A17, A15, B13, A5, D5, A2	–	Ground (digital block). These pins ground the chip.
AGND	270	E11	–	Ground (analog block)
HGND	272, 279	E10, B9	–	Ground (high-speed block)
RGND	286	A7	–	Ground (receive PLL block)

1.8 Pin Status during and After Reset

(1/2)

Pin Name	During Reset	After Reset
★ RENBL_B	1	0
RCLK	CLK output	CLK output
Tx7 to Tx0	0	0
TSOC	0	0
★ TENBL_B	1	1
TCLK	CLK output	CLK output
PHR/W_B (external PHY)/PHYALM (internal PHY)	0	0
PHOE_B	1	1
PHCE_B (external PHY)/SD (internal PHY)	Hi-Z (input)	Hi-Z (input)
AD31 to AD0	Hi-Z (input)	Hi-Z (input)
PCBE3_B to PCBE0_B (PCI)/BE3_B to BE0_B (Generic)	Hi-Z (input)	Hi-Z (input)
PAR	Hi-Z (input)	Hi-Z (input)
FRAME_B	Hi-Z (input)	Hi-Z (input)
TRDY_B	Hi-Z (input)	Hi-Z (input)
IRDY_B	Hi-Z (input)	Hi-Z (input)
STOP_B	Hi-Z (input)	Hi-Z (input)
DEVSEL_B	Hi-Z (input)	Hi-Z (input)
REQ_B (PCI)/ATTN_B (Generic)	1	1
PERR_B	Hi-Z (input)	Hi-Z (input)
SERR_B	Hi-Z	Hi-Z
INTR_B	Hi-Z	Hi-Z
AD63 to AD61 (PCI)/PAR2 to PAR0 (Generic)	Hi-Z (input)	Hi-Z (input)
AD60 to AD56 (PCI)/(Generic)	Hi-Z (input)/Hi-Z (output)	Hi-Z (input)/Hi-Z (output)
AD55 to AD32 (PCI)/(Generic)	Hi-Z (input)/0	Hi-Z (input)/0
PCBE7_B to PCBE5_B (PCI)/SIZE2 to SIZE0 (Generic)	Hi-Z (input)/0	Hi-Z (input)/0
PCBE4_B (PCI)/PAR3 (Generic)	Hi-Z (input)	Hi-Z (input)
PAR64	Hi-Z (input)	Hi-Z (input)
REQ64_B(PCI)/DR/W_B (Generic)	Hi-Z/1	Hi-Z/1
E2PCS	0	0
E2PDO	0	0
E2PCLK	0	0
ROMA15 to ROMA0	0	0
ROMCS_B	1	1
ROMOE_B	1	1
CD31 to CD0	0	0
CPAR3 to CPAR0	0	0
CA18 to CA0	0	0

(2/2)

Pin Name	During Reset	After Reset
CWE_B	1	1
COE_B	1	1
TDOT	Undefined	Undefined
TDOC	Undefined	Undefined
JDO[Note]	Hi-Z	Hi-Z

★ **Note** During JRST_B input

Remark The internal PHY mode is set (PHM of GMR register = 0) after reset.

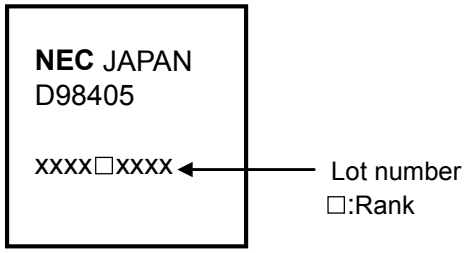
2. ELECTRICAL SPECIFICATIONS

★ Some of the electrical specifications for the μPD98405 vary depending on the device version. The version history is described below for explanation.

Device Version History

Part Number	Version	VER Register	Rank
μPD98405GL-PMU	V3.0	0102H	K or P
	V3.1	0103H	E or X
	V4.0	0104H	M
μPD98405S1-6C	V3.1	0103H	K
	V4.0	0104H	E

A rank is assigned to the corresponding version. The rank is indicated by the marking on the actual device (see the figure below).



Hereafter, electrical specification items are indicated for an individual device version if the specifications vary depending on the device version. Ranks for each version are defined as follows.

V4.0: μPD98405GL-PMU Rank M
μPD98405S1-6C Rank E

V3.1 or before: μPD98405GL-PMU Ranks K, P, E, or X
μPD98405S1-6C Rank K

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
	V_{DD5} Note 1		–0.5 to +6.5	V
Input/output voltage	V_I/V_O	Normal I/O pin	–0.5 to +6.6	V
		PCI I/O pin Note 2	–0.5 to +6.6	V
		P-ECL pin	–0.5 to +4.6 and V_{DD} + 0.5	V
★ Operating ambient frequency	T_A	V4.0	–40 to +85	°C
		V3.1 or before	0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Notes 1. V_{DD5}: Clamping diode-dedicated power supply

2. By supplying 5 V for clamping diode, the device can be protected from an 11 V reflection wave.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Supply voltage	V_{DD}	T_A = –40 to +85°C	+3.15	+3.3	+3.45	V
		T_A = 0 to +70°C	+3.0	+3.3	+3.6	V
	V_{DD5} Note	+3.3 V PCI T_A = –40 to +85°C	+3.15	+3.3	+3.45	V
		+3.3 V PCI T_A = 0 to +70°C	+3.0	+3.3	+3.6	V
		+5 V PCI	+4.75	+5.00	+5.25	V
Operating ambient temperature	T_A	V4.0	–40		+85	°C
		V3.1 or before	0		+70	°C
Input voltage, high	V_{IH1}	Input pins other than PCI and P-ECL	+2.0		+5.5	V
	V_{IH2}	+5 V PCI pin	+2.0		V_{DD5} + 0.5	V
	V_{IH3}	+3.3 V PCI pin	0.5 × V_{DD}		V_{DD} + 0.5	V
	V_{IH4}	P-ECL pin	V_{DD} – 1.49		V_{DD} – 0.40	V
Input voltage, low	V_{IL1}	Input pins other than PCI and P-ECL	0		+0.8	V
	V_{IL2}	+5 V PCI pin	–0.5		+0.8	V
	V_{IL3}	+3.3 V PCI pin	–0.5		0.3 × V_{DD}	V
	V_{IL4}	P-ECL pin	V_{DD} – 2.82		V_{DD} – 1.50	V
★ Input differential voltage	V_{IDIFF}		300		1900	mV

Note V_{DD5}: Clamping diode-dedicated power supply

★ **DC Characteristics**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –3.0 mA[Note 1]	+2.4			V
	V_{OH2}	I_{OH} = –500 μA[Note 2] (+3.3 V PCI)	0.88 × V_{DD}			V
	V_{OH3}	I_{OH} = –2.0 mA[Note 2] (+5 V PCI)	+2.4			V
	V_{OH4}	R_L = 50 Ω, V_T = V_{DD} – 2 V (P-ECL)	V_{DD} – 1.140		V_{DD} – 0.690	V
Output voltage, low	V_{OL1}	I_{OL} = 9.0 mA[Note 1]			0.144 × V_{DD}	V
	V_{OL2}	I_{OL} = 1500 μA[Note 2] (+3.3 V PCI)			+0.4	V
	V_{OL3}	I_{OL} = 3.0 mA[Note 2] (+5 V PCI)			+0.55	V
	V_{OL4}	I_{OL} = 6.0 mA[Note 4] (+5 V PCI)			+0.55	V
	V_{OL5}	R_L = 50 Ω, V_T = V_{DD} – 2 V (P-ECL)	V_{DD} – 2.175		V_{DD} – 1.755	V
Supply current	I_{DD}	f_{CLK} = 33 MHz, normal operation		650	900	mA
★ Input leakage current (normal input)	I_{I1}	V_I = V_{DD} or GND			±10	μA
★ Input leakage current[Note 5]	I_{I2}	V_I = V_{DD}, T_A = –40 to +85°C	28		190	μA
		V_I = V_{DD}, T_A = 0 to +70°C	28		160	μA

Notes 1. V_{OH1} and V_{OL1} are applied to the following pins (output pins other than PCI):
CD31 to CD0, CPAR3 to CPAR0, CA18 to CA0, CBE3_B to CBE0_B, CWE_B, COE_B, JDO, RCLK, RENBL_B, TSOC, TENBL_B, TCLK, Tx7 to Tx0, PHCE_B, PHOE_B, PHRW_B, E2PCS, E2PDO, E2PCLK

2. V_{OH2}, V_{OH3}, and V_{OL2} are applied to the following pins (PCI output pins):
AD63 to AD0, PCBE7_B to PCBE0_B, PAR, PAR64, REQ_B, INTR_B, FRAME_B, REQ64_B, TRDY_B, IRDY_B, DEVSEL_B, STOP_B, SERR_B, PERR_B

3. V_{OL3} is applied to the following pins (with +5 V PCI):
AD31 to AD0, PCBE3_B to PCBE0_B, PAR, REQ_B, INTR_B

4. V_{OL4} is applied to the following pins (with +5 V PCI):
FRAME_B, TRDY_B, IRDY_B, DEVSEL_B, STOP_B, SERR_B, PERR_B, AD64 to AD32, PCBE7_B to PCBE4_B, ACK64_B, REQ64_B, PAR64

5. I_{I2} is applied to the following pins:
★ E2PDI, ROMD7 to ROMD0, RSOC, Rx7 to Rx2, CPAR3 to CPAR0, CD31 to CD0, PCI_MODE, SD, TEST

Capacitance (T_A = +25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}				10	pF
CLK input capacitance	C_{CLK}		5		12	pF
IDSEL input capacitance	C_{IDSEL}				8	pF
Output capacitance	C_{OUT}		8		10	pF
I/O capacitance	$C_{I/O}$				8	pF

★ **On-chip pull-down resistor**

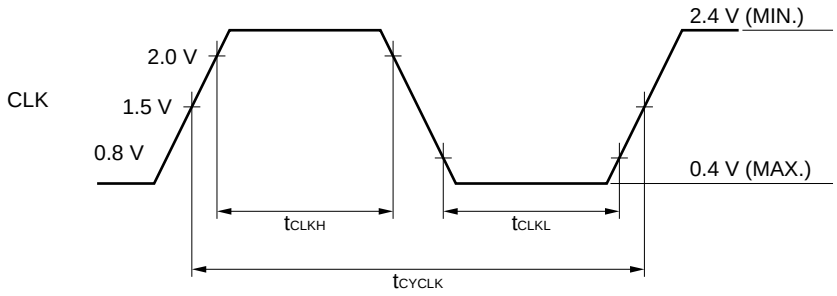
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
On-chip pull-down resistance[Note]	R_{PD}	T_A = –40 to +85°C	18.8		107.1	kΩ
		T_A = 0 to +70°C	21.8		107.1	kΩ

Note R_{PD} is applied to the following pins:
E2PDI, ROMD7 to ROMD0, RSOC, Rx7 to Rx2, CPAR3 to CPAR0, CD31 to CD0, PCI_MODE, SD, TEST

★ **AC Characteristics (Output pin load: 50 pF)**

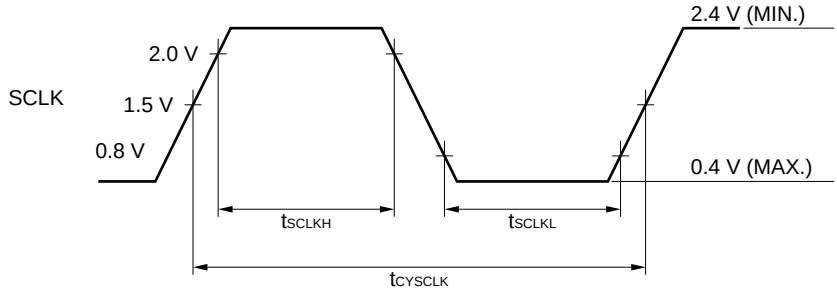
CLK input (BUS interface clock - CLK pin)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK cycle time	t_{CYCLK}		30		125	ns
CLK high-level width	t_{CLKH}		11			ns
CLK low-level width	t_{CLKL}		11			ns
CLK slew rate	$slew_{CLK}$		1		4	V/ns



SCLK input (internal system clock - SCLK pin)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ SCLK cycle time	t_{CYSCLK}	V4.0	30		125	ns
		V3.1 or before	40		125	ns
★ SCLK high-level width	t_{SCLKH}	V4.0	11			ns
		V3.1 or before	15			ns
★ SCLK low-level width	t_{SCLKL}	V4.0	11			ns
		V3.1 or before	15			ns
SCLK slew rate	$slew_{SCLK}$		1		4	V/ns



RST input

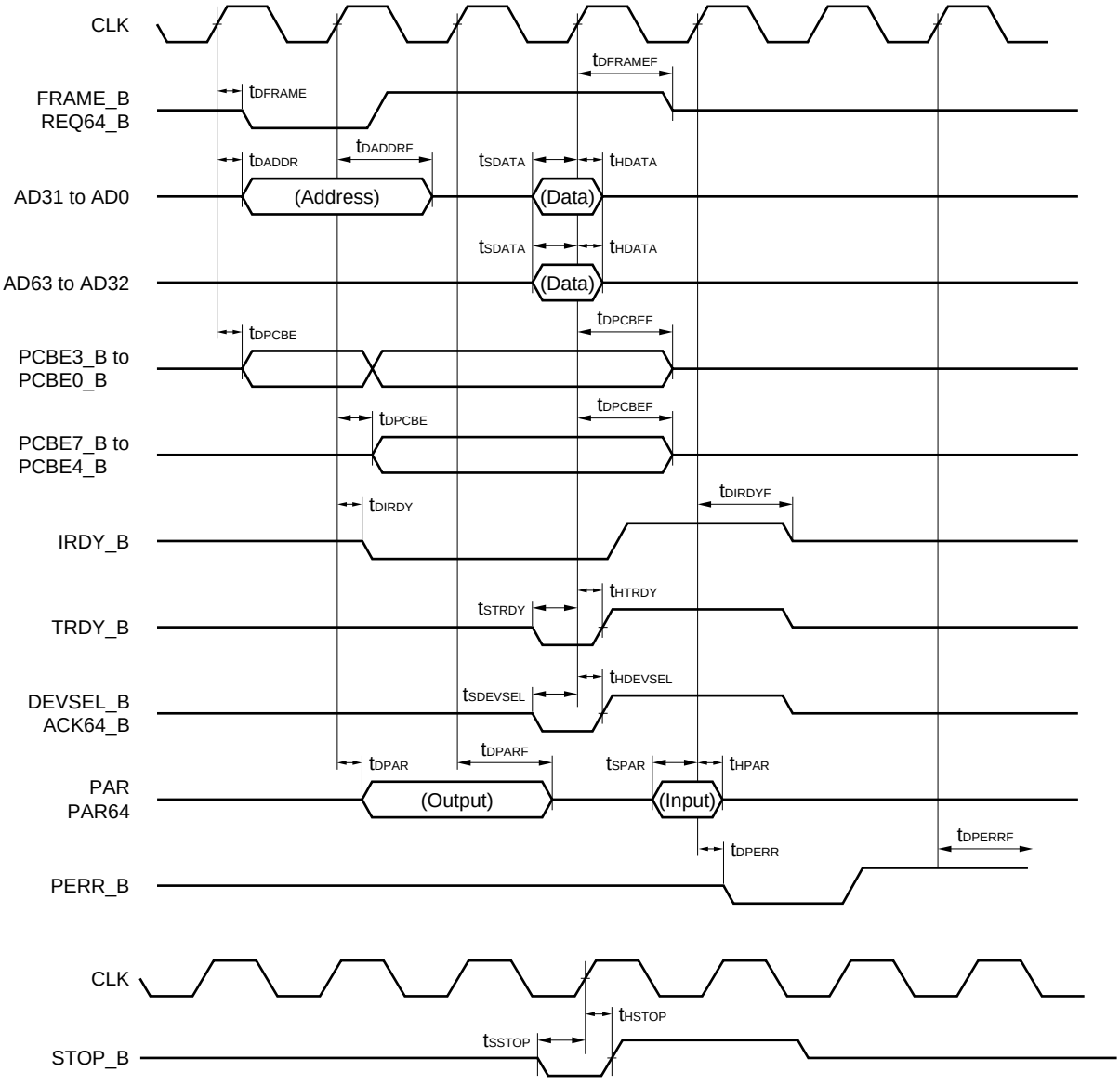
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RST low-level width	t_{RSTL}		t_{CYCLK}			ns
RST slew rate	$slew_{RST}$		50			mV/ns

PCI Bus Interface

Bus master read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK ↑→ FRAME_B, REQ64_B valid time	t_{DFRAME}		1		11	ns
CLK ↑→ FRAME_B, REQ64_B float time	$t_{DFRAMEF}$				28	ns
CLK ↑→ AD (Address) valid time	t_{DADDR}		1		11	ns
CLK ↑→ AD (Address) float time	t_{DADDRF}				28	ns
AD (Data) setup time	t_{SDATA}		8			ns
AD (Data) hold time	t_{HDATA}		1			ns
CLK ↑→ PCBE_B valid time	t_{DPCBE}		1		11	ns
CLK ↑→ PCBE_B float time	t_{DPCBEF}				28	ns
CLK ↑→IRDY_B valid time	t_{DIRDY}		1		11	ns
CLK ↑→ IRDY_B float time	t_{DIRDYF}				28	ns
TRDY_B setup time	t_{STRDY}		8			ns
TRDY_B hold time	t_{HTRDY}		1			ns
DEVSEL_B, ACK64_B setup time	$t_{SDEVSEL}$		8			ns
DEVSEL_B, ACK64_B hold time	$t_{HDEVSEL}$		1			ns
STOP_B setup time	t_{SSTOP}		8			ns
STOP_B hold time	t_{HSTOP}		1			ns
CLK ↑→ PAR valid time	t_{DPAR}		1		11	ns
CLK ↑→ PAR float time	t_{DPARF}				28	ns
PAR setup time	t_{SPAR}		8			ns
PAR hold time	t_{HPAR}		1			ns
CLK ↑→ PERR_B valid time	t_{DPERR}		1		11	ns
CLK ↑ → PERR_B float time	t_{DPERRF}				28	ns

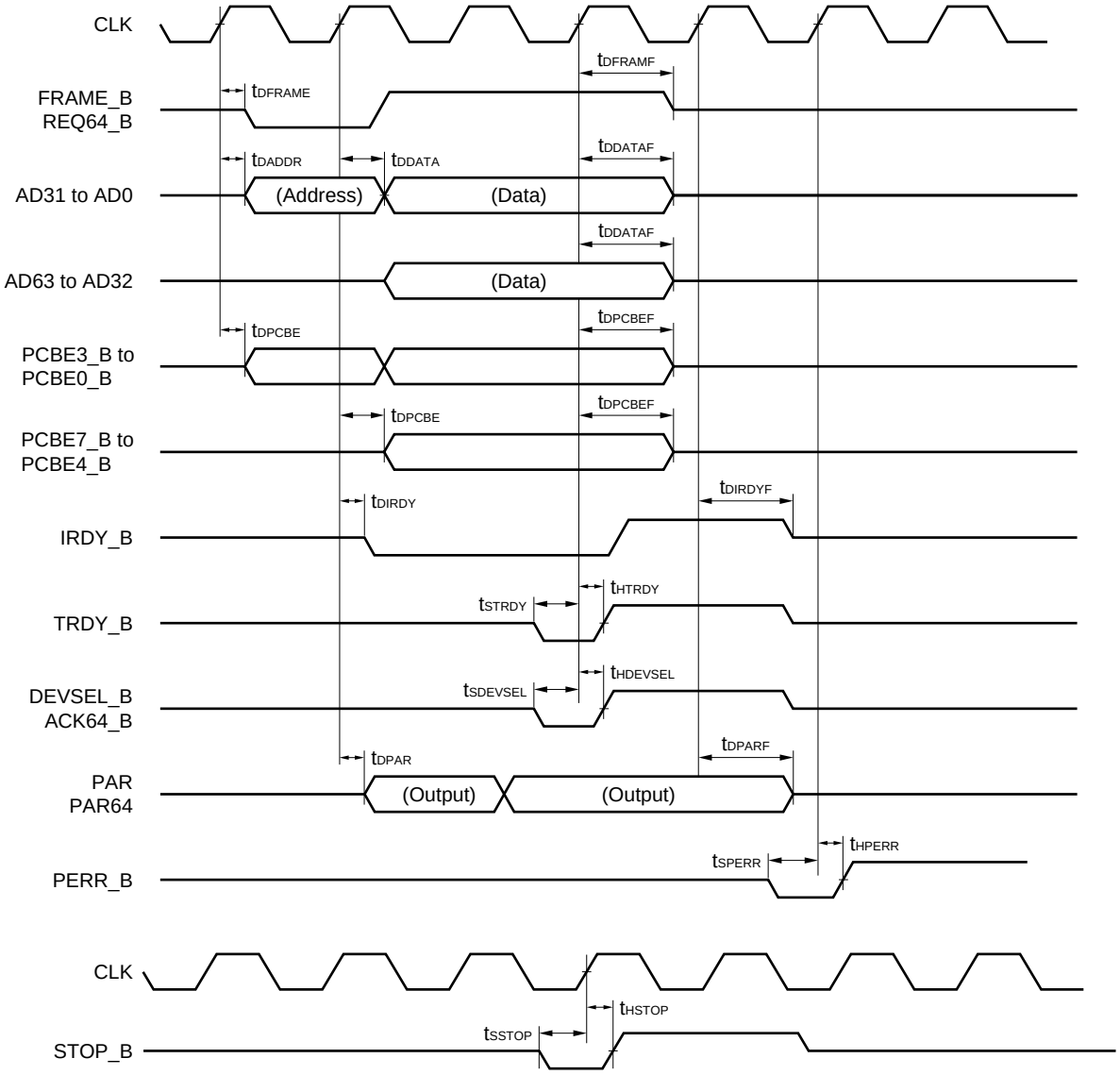
Bus master read



Bus master write

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK ↑→ FRAME_B, REQ64_B valid time	t_{DFRAME}		1		11	ns
CLK ↑→ FRAME_B, REQ64_B float time	$t_{DFRAMEF}$				28	ns
CLK ↑→ AD (Address) valid time	t_{DADDR}		1		11	ns
CLK ↑→ Data valid time	t_{DDATA}		1		11	ns
CLK ↑→ Data float time	t_{DDATAF}				28	ns
CLK ↑→ PCBE_B valid time	t_{DPCBE}		1		11	ns
CLK ↑→ PCBE_B float time	t_{DPCBEF}				28	ns
CLK ↑→IRDY_B valid time	t_{DIRDY}		1		11	ns
CLK ↑→ IRDY_B float time	t_{DIRDYF}				28	ns
TRDY_B setup time	t_{STRDY}		8			ns
TRDY_B hold time	t_{HTRDY}		1			ns
STOP_B setup time	t_{SSTOP}		8			ns
STOP_B hold time	t_{HSTOP}		1			ns
DEVSEL_B, ACK64_B setup time	$t_{SDEVSEL}$		8			ns
DEVSEL_B, ACK64_B hold time	$t_{HDEVSEL}$		1			ns
CLK ↑→ PAR valid time	t_{DPAR}		1		11	ns
CLK ↑→ PAR float time	t_{DPARF}				28	ns
PERR_B setup time	t_{SPERR}		8			ns
PERR_B hold time	t_{HPERR}		1			ns

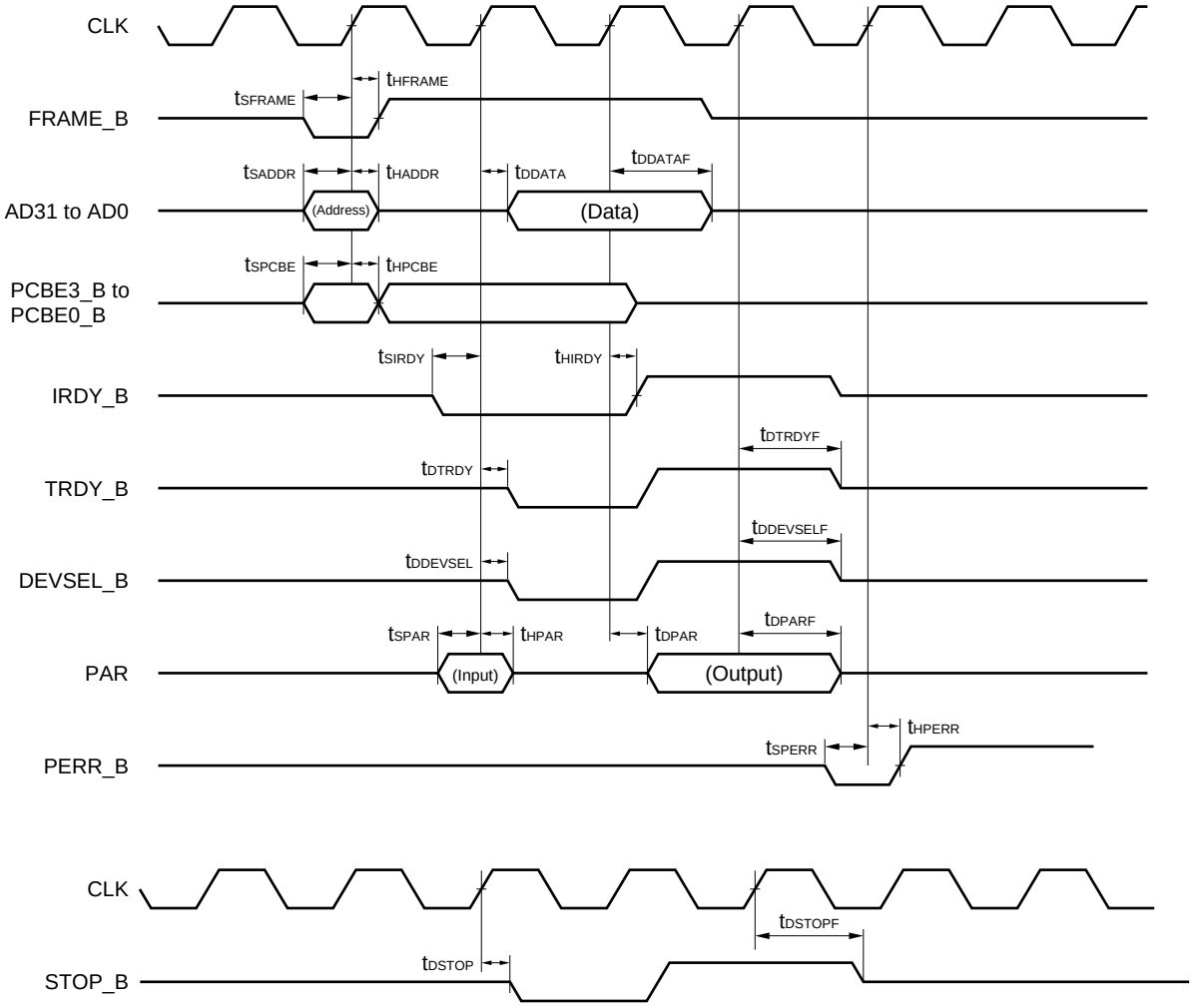
Bus master write



Target read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t_{SFRAME}		8			ns
FRAME_B hold time	t_{HFRAME}		1			ns
AD (Address) setup time	t_{SADDR}		8			ns
AD (Address) hold time	t_{HADDR}		1			ns
CLK ↑→ AD (Data) valid time	t_{DDATA}		1		11	ns
CLK ↑→ AD (Data) float time	t_{DDATAF}				28	ns
PCBE_B setup time	t_{SPCBE}		8			ns
PCBE_B hold time	t_{HPCBE}		1			ns
IRDY_B setup time	t_{SIRDY}		8			ns
IRDY_B hold time	t_{HIRDY}		1			ns
CLK ↑→ TRDY_B valid time	t_{DTRDY}		1		11	ns
CLK ↑→ TRDY_B float time	t_{DTRDYF}				28	ns
CLK ↑→ STOP_B valid time	t_{DSTOP}		1		11	ns
CLK ↑→ STOP_B float time	t_{DSTOPF}				28	ns
CLK ↑→ DEVSEL_B valid time	$t_{DDEVSEL}$		1		11	ns
CLK ↑→ DEVSEL_B float time	$t_{DDEVSELF}$				28	ns
PAR setup time	t_{SPAR}		8			ns
PAR hold time	t_{HPAR}		1			ns
CLK ↑→ PAR valid time	t_{DPAR}		1		11	ns
CLK ↑→ PAR float time	t_{DPARF}				28	ns
PERR_B setup time	t_{SPERR}		8			ns
PERR_B hold time	t_{HPERR}		1			ns

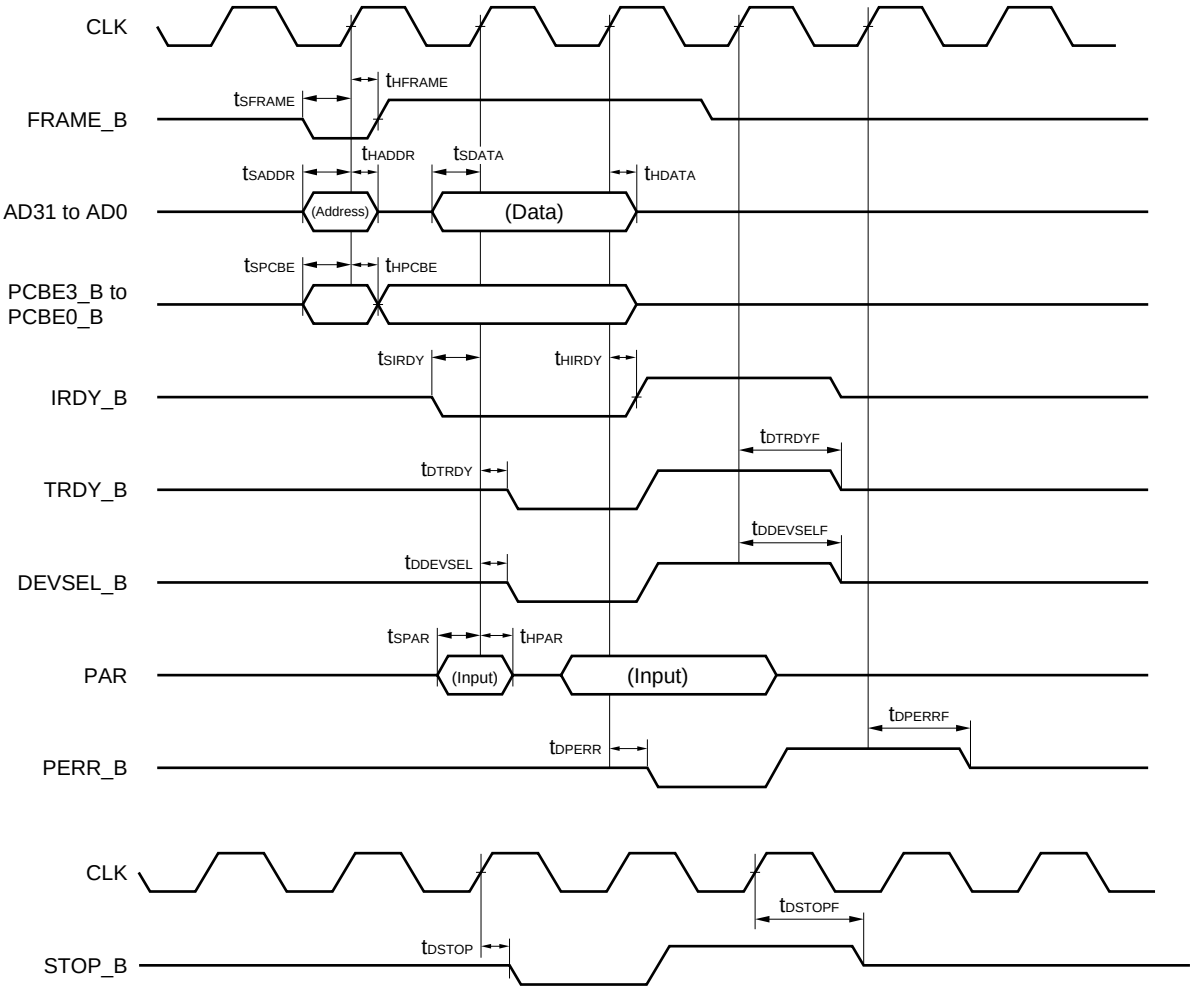
Target read



Target write

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t_{SFRAME}		8			ns
FRAME_B hold time	t_{HFRAME}		1			ns
AD (Address) setup time	t_{SADDR}		8			ns
AD (Address) hold time	t_{HADDR}		1			ns
AD (Data) setup time	t_{SDATA}		8			ns
AD (Data) hold time	t_{HDATA}		1			ns
PCBE_B setup time	t_{SPCBE}		8			ns
PCBE_B hold time	t_{HPCBE}		1			ns
IRDY_B setup time	t_{SIRDY}		8			ns
IRDY_B hold time	t_{HIRDY}		1			ns
CLK ↑→ TRDY_B valid time	t_{DTRDY}		1		11	ns
CLK ↑→ TRDY_B float time	t_{DTRDYF}				28	ns
CLK ↑→ STOP_B valid time	t_{DSTOP}		1		11	ns
CLK ↑→ STOP_B float time	t_{DSTOPF}				28	ns
CLK ↑→ DEVSEL_B valid time	$t_{DDEVSEL}$		1		11	ns
CLK ↑→ DEVSEL_B float time	$t_{DDEVSELF}$				28	ns
PAR setup time	t_{SPAR}		8			ns
PAR hold time	t_{HPAR}		1			ns
CLK ↑→ PERR_B valid time	t_{DPERR}		1		11	ns
CLK ↑→ PERR_B float time	t_{DPERRF}				28	ns

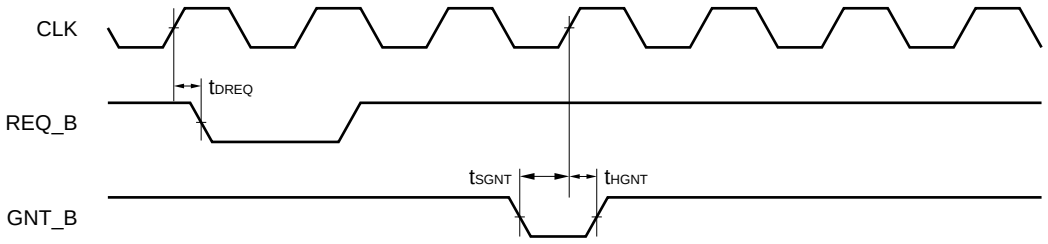
Target write



Bus arbitration

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK ↑→ REQ_B valid time	t_{DREQ}		1		12	ns
GNT_B setup time	t_{SGNT}		10			ns
GNT_B hold time	t_{HGNT}		1			ns

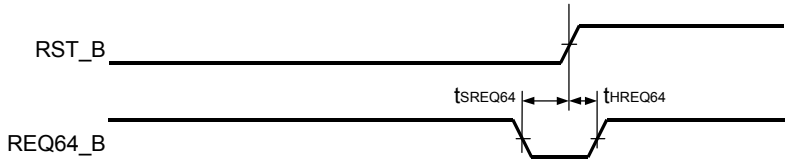
Bus arbitration



★ 64-bit bus expansion

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REQ64_B setup time (to RST_B ↑)	t_{SREQ64}		$t_{CYCLK} \times 10$			ns
REQ64_B hold time (from RST_B ↑)	t_{HREQ64}	V4.0	0			ns
		V3.1 or before	30			ns

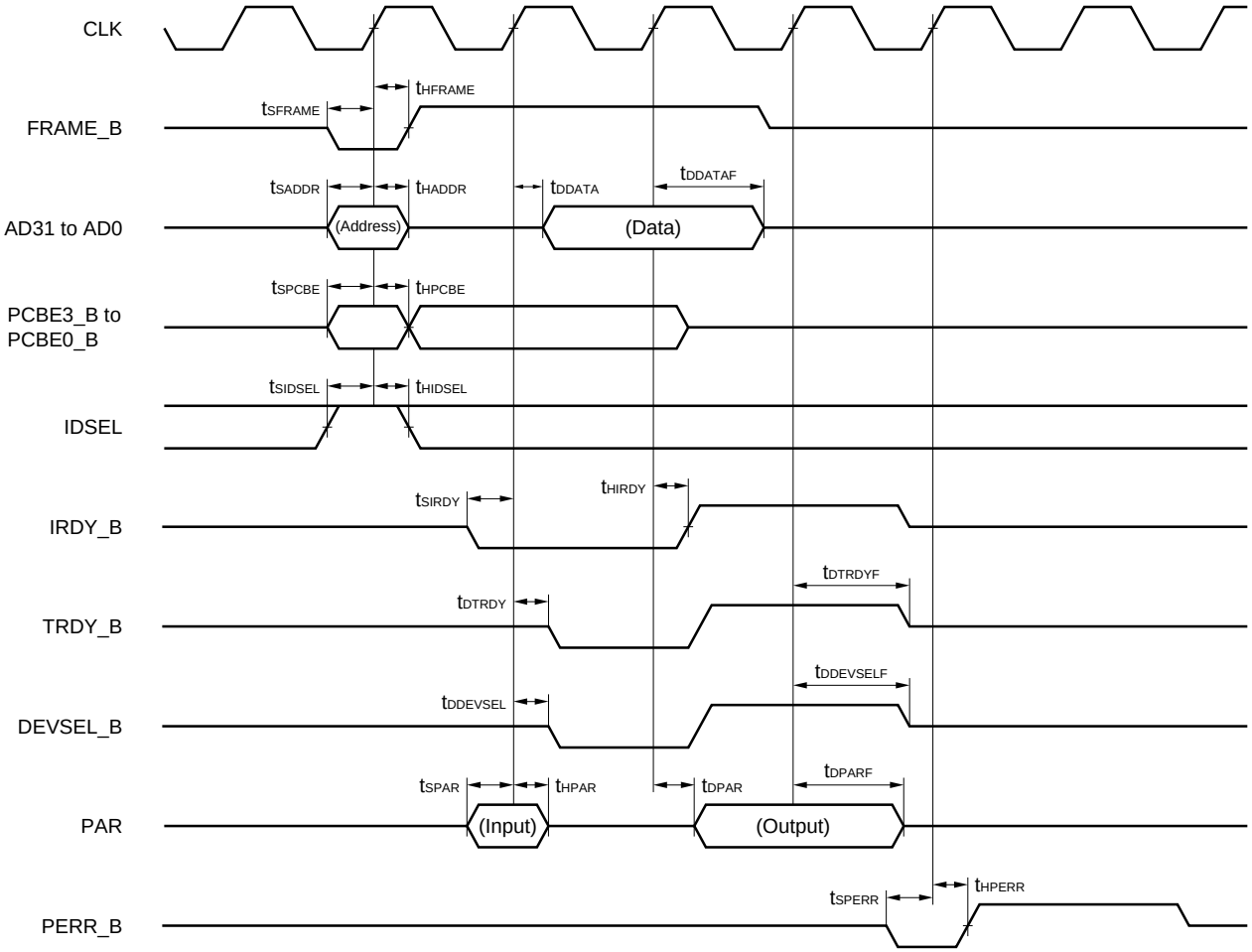
64-bit bus extension



Configuration read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t_{SFRAME}		8			ns
FRAME_B hold time	t_{HFRAME}		1			ns
AD (Address) setup time	t_{SADDR}		8			ns
AD (Address) hold time	t_{HADDR}		1			ns
CLK ↑→ AD (Data) valid time	t_{DDATA}		1		11	ns
CLK ↑→ AD (Data) float time	t_{DDATAF}				28	ns
PCBE_B setup time	t_{SPCBE}		8			ns
PCBE_B hold time	t_{HPCBE}		1			ns
IDSEL setup time	t_{SIDSEL}		8			ns
IDSEL hold time	t_{HIDSEL}		1			ns
IRDY_B setup time	t_{SIRDY}		8			ns
IRDY_B hold time	t_{HIRDY}		1			ns
CLK ↑→ TRDY_B valid time	t_{DTRDY}		1		11	ns
CLK ↑→ TRDY_B float time	t_{DTRDYF}				28	ns
CLK ↑→ DEVSEL_B valid time	$t_{DDEVSEL}$		1		11	ns
CLK ↑→ DEVSEL_B float time	$t_{DDEVSELF}$				28	ns
CLK ↑→ PAR valid time	t_{DPAR}		1		11	ns
CLK ↑→ PAR float time	t_{DPARF}				28	ns
PAR setup time	t_{SPAR}		8			ns
PAR hold time	t_{HPAR}		1			ns
PERR_B setup time	t_{SPERR}		8			ns
PERR_B hold time	t_{HPERR}		1			ns

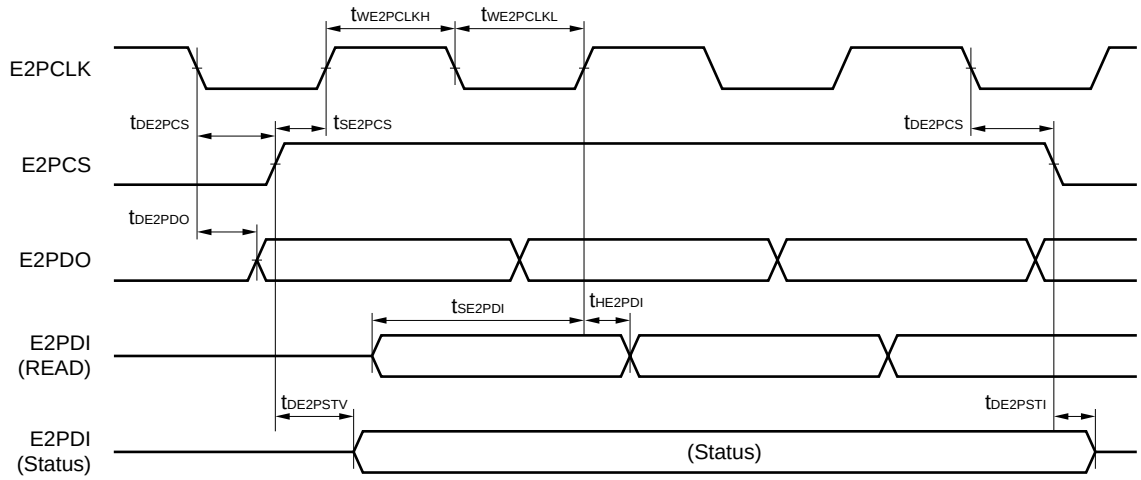
Configuration read



EEPROM interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
E2PCLK high-level width	$t_{WE2PCKLH}$		$t_{CYCLK} \times 18 - 50$	$t_{CYCLK} \times 18$	$t_{CYCLK} \times 18 + 50$	ns
E2PCLK low-level width	$t_{WE2PCLKL}$		$t_{CYCLK} \times 18 - 50$	$t_{CYCLK} \times 18$	$t_{CYCLK} \times 18 + 50$	ns
E2PCLK ↓→ E2PCS valid time	t_{DE2PCS}		50			ns
E2PCS ↑→ E2PCLK	t_{SE2PCS}		50			ns
E2PCLK ↓→ E2PDO valid time	t_{DE2PDO}				300	ns
E2PDI → E2PCLK setup time	t_{SE2PDI}		500			ns
E2PCLK → E2PDI hold time	t_{HE2PDI}		70			ns
E2PCS ↑→ E2PDI (Status) valid delay time	$t_{DE2PSTV}$				500	ns
E2PCS ↓→ E2PDI (Status) invalid delay time	$t_{DE2PSTI}$		0		100	ns

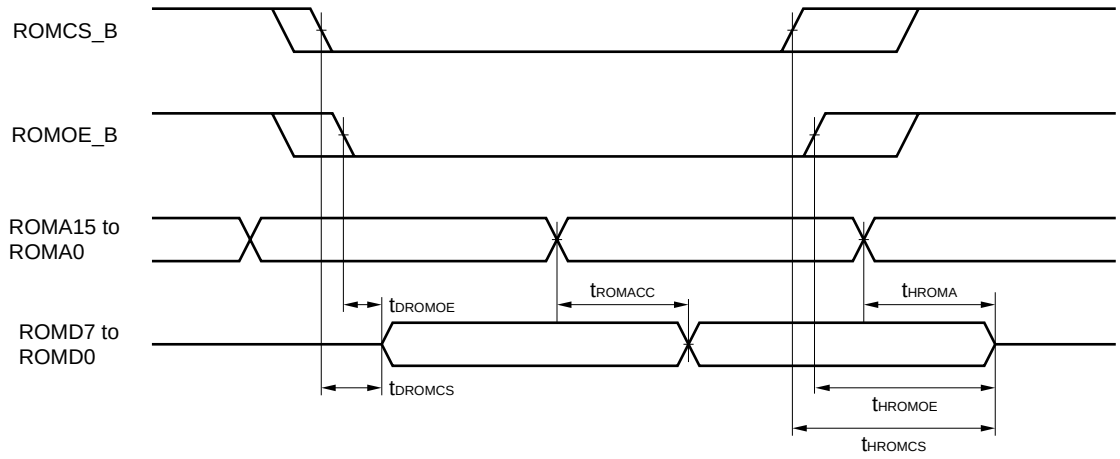
EEPROM interface



Expansion ROM interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ROMOE_B ↓→ ROMD valid time	t_{DROMOE}	ROMCS_B = V_{OL}, ROMA valid			200	ns
ROMCS_B ↓→ ROMD valid time	t_{DROMCS}	ROMOE_B = V_{OL}, ROMA valid			200	ns
ROMA valid time → ROMD valid time	t_{ROMACC}	ROMCS_B = ROMOE_B = V_{OL}			200	ns
ROMOE_B ↑→ ROMD float time	t_{HROMOE}	ROMCS_B = V_{OL}, ROMA valid	0			ns
ROMCS_B ↑→ ROMD float time	t_{HROMCS}	ROMOE_B = V_{OL}, ROMA valid	0			ns
ROMA invalid time → ROMD hold time	t_{HROMA}	ROMCS_B = ROMOE_B = V_{OL}	0			ns

Expansion ROM interface

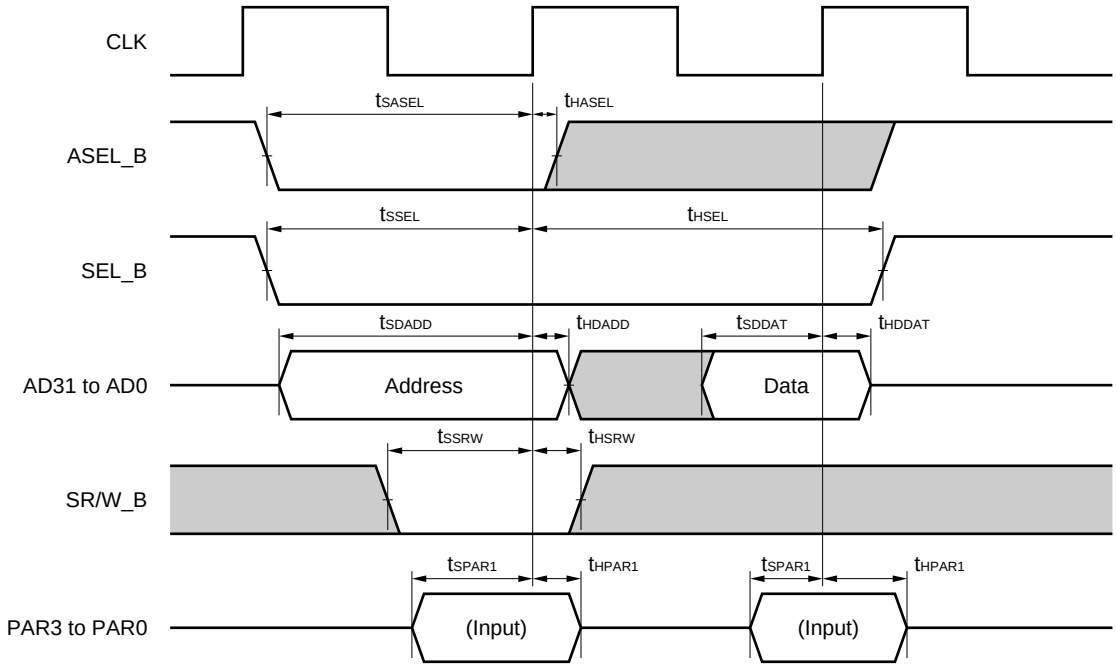


Generic bus interface

Slave write access

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASEL_B setup time	t_{SASEL}		8			ns
ASEL_B hold time	t_{HASEL}		3			ns
SEL_B setup time	t_{SSEL}		8			ns
SEL_B hold time	t_{HSEL}		1 t_{CYCLK} + 3			ns
Address setup time	t_{SDADD}		8			ns
Address hold time	t_{HDADD}		3			ns
Data setup time	t_{SDDAT}		8			ns
Data hold time	t_{HDDAT}		3			ns
PAR setup time	t_{SPAR1}		8			ns
PAR hold time	t_{HPAR1}		3			ns
SR/W_B setup time	t_{SSRW}		8			ns
SR/W_B hold time	t_{HSRW}		3			ns

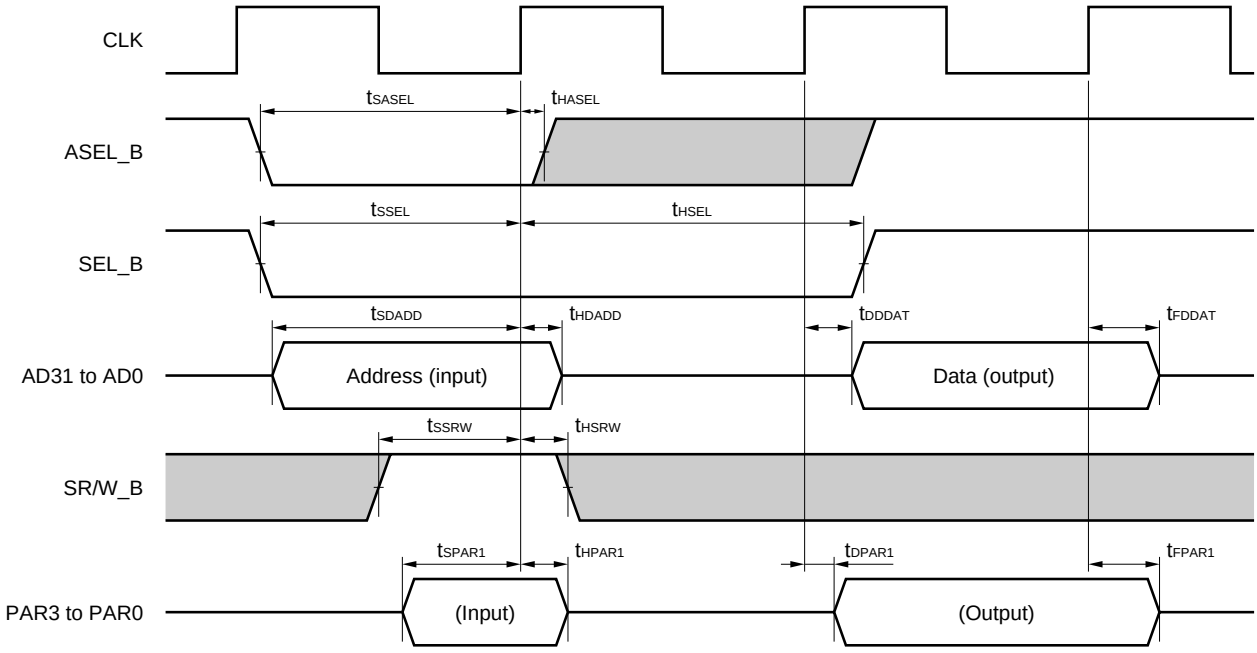
Slave write access



Slave read access

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	ASEL_B setup time	t_{SASEL}		8			ns
	ASEL_B hold time	t_{HASEL}		3			ns
	SEL_B setup time	t_{SSEL}		8			ns
	SEL_B hold time	t_{HSEL}		1 t_{CYCLK} + 3			ns
	Address setup time	t_{SDADD}		8			ns
	Address hold time	t_{HDADD}		3			ns
★	CLK ↑→ data delay time	t_{DDDAT}		2		18	ns
★	CLK ↑→ data float time	t_{FDDAT}				18	ns
	PAR setup time	t_{SPAR1}		8			ns
	PAR hold time	t_{HPAR1}		3			ns
★	CLK ↑→ PAR delay time	t_{DPAR1}		2		18	ns
★	CLK ↑→ PAR float time	t_{FPAR1}				18	ns
	SR/W_B setup time	t_{SSRW}		8			ns
	SR/W_B hold time	t_{HSRW}		3			ns

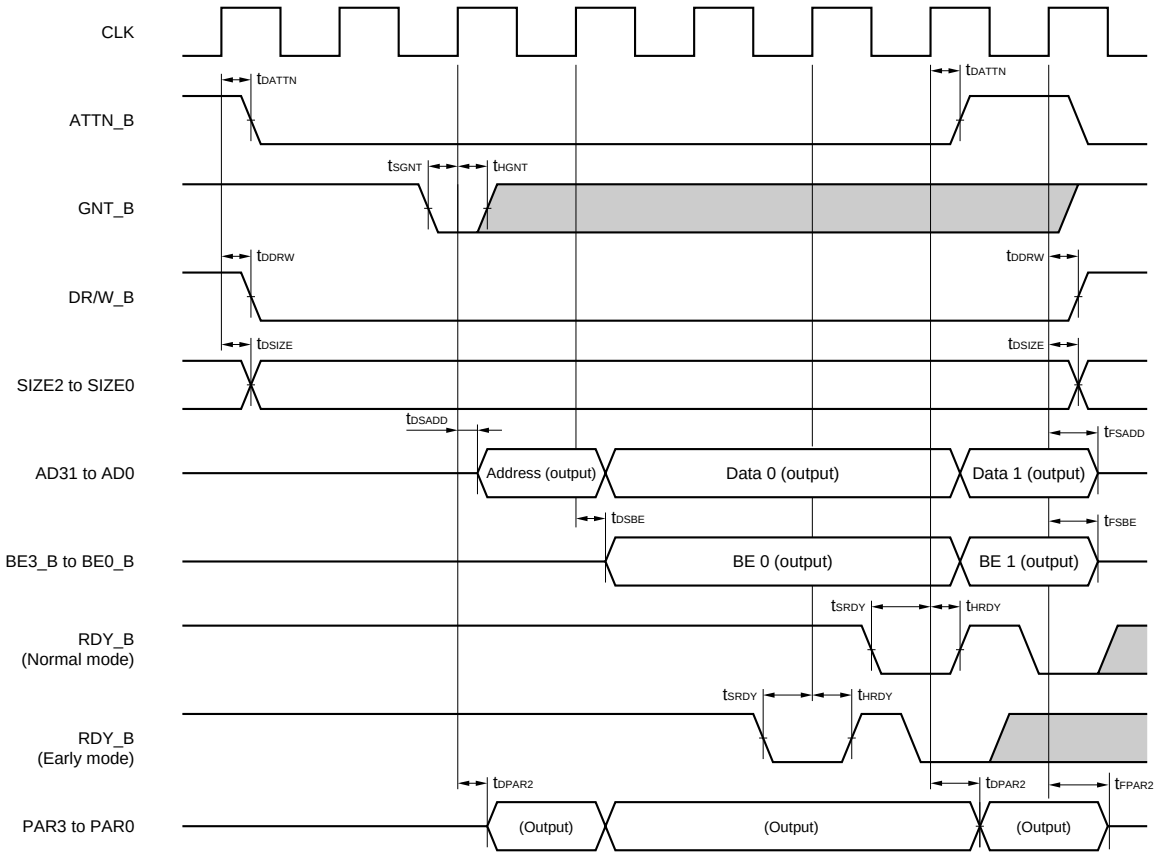
Slave read access



DMA write access

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	CLK ↑→ ATTN_B delay time	t_{DATTN}		2		18	ns
	GNT_B setup time	t_{SGNT}		8			ns
	GNT_B hold time	t_{HGNT}		3			ns
	CLK ↑→ DR/W_B delay time	t_{DDRW}		2		18	ns
	CLK ↑→ SIZE delay time	t_{DSIZE}		2		18	ns
★	CLK ↑→ address delay time	t_{DSADD}		2		18	ns
★	CLK ↑→ address/data float time	t_{FSADD}				18	ns
★	CLK ↑→ BE_B delay time	t_{DSBE}		2		18	ns
★	CLK ↑→ BE_B float time	t_{FSBE}				18	ns
★	CLK ↑→ PAR delay time	t_{DPAR2}		2		18	ns
★	CLK ↑→ PAR float time	t_{FPAR2}				18	ns
	RDY_B setup time	t_{SRDY}		8			ns
	RDY_B hold time	t_{HRDY}		3			ns

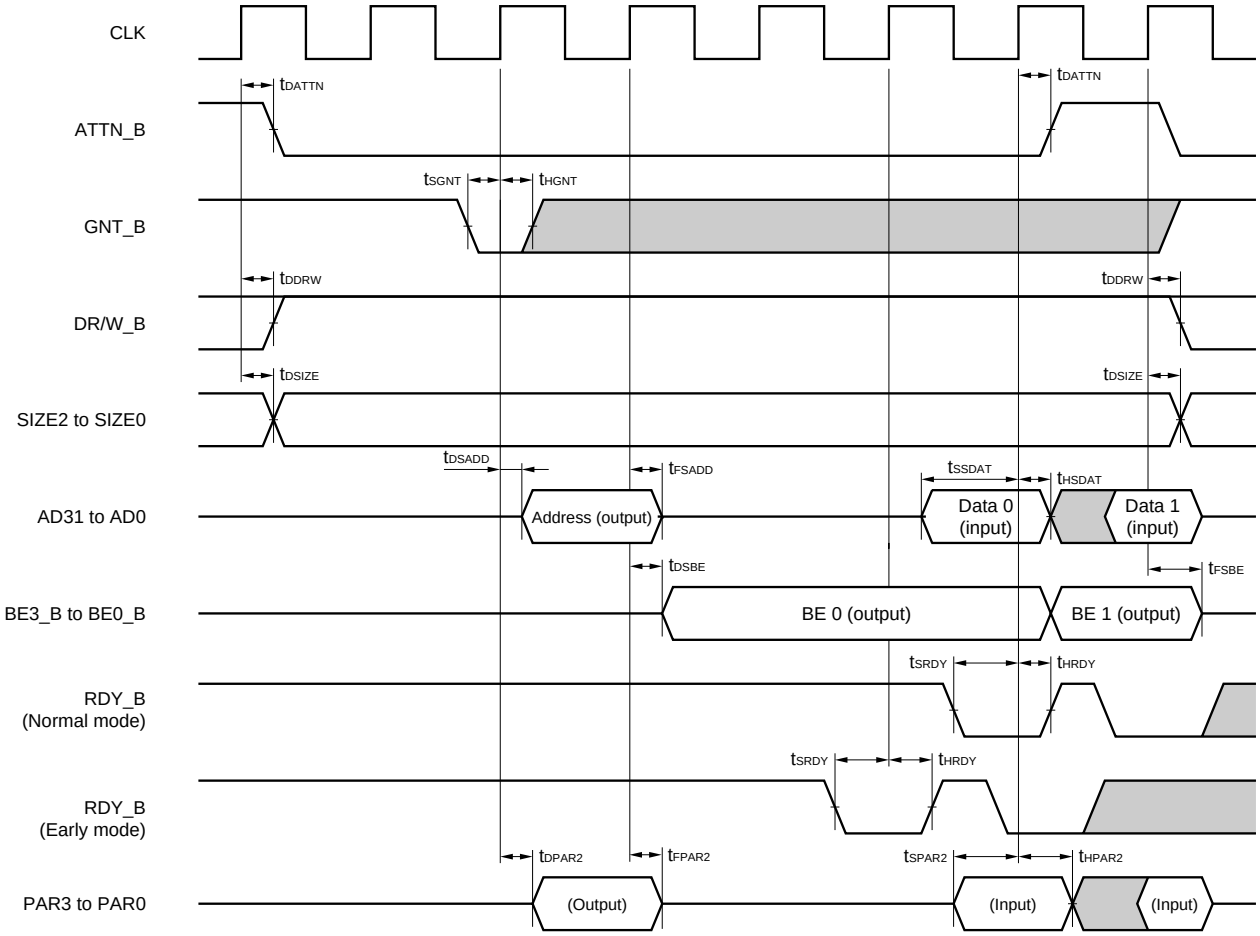
★ **DMA write access (Example: 2-word burst)**



DMA read access

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	CLK ↑→ ATTN_B delay time	t_{DATTN}		2		18	ns
	GNT_B setup time	t_{SGNT}		8			ns
	GNT_B hold time	t_{HGNT}		3			ns
	CLK ↑→ DR/W_B delay time	t_{DDRW}		2		18	ns
	CLK ↑→ SIZE delay time	t_{DSIZE}		2		18	ns
★	CLK ↑→ address delay time	t_{DSADD}		2		18	ns
★	CLK ↑→ address/data float time	t_{FSADD}				18	ns
★	CLK ↑→ BE_B delay time	t_{DSBE}		2		18	ns
★	CLK ↑→ BE_B float time	t_{FSBE}				18	ns
★	CLK ↑→ PAR delay time	t_{DPAR2}		2		18	ns
★	CLK ↑→ PAR float time	t_{FPAR2}				18	ns
	RDY_B setup time	t_{SRDY}		8			ns
	RDY_B hold time	t_{HRDY}		3			ns
	Data setup time	t_{SSDAT}		8			ns
	Data hold time	t_{HSDAT}		3			ns
	PAR setup time	t_{SPAR2}		8			ns
	PAR hold time	t_{HPAR2}		3			ns

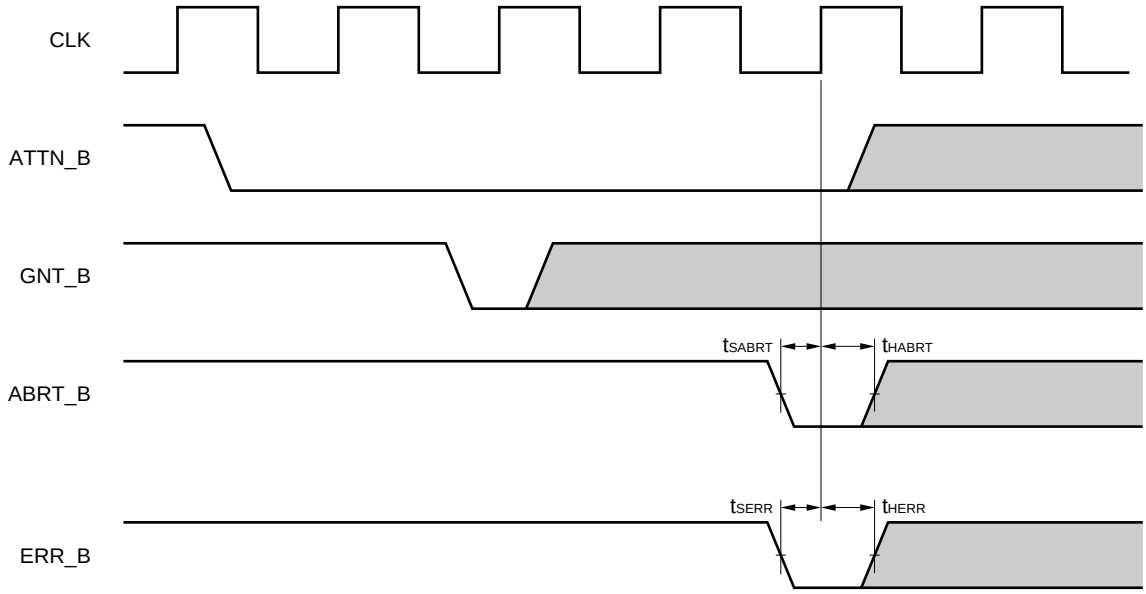
★ **DMA read access (Example: 2-word burst)**



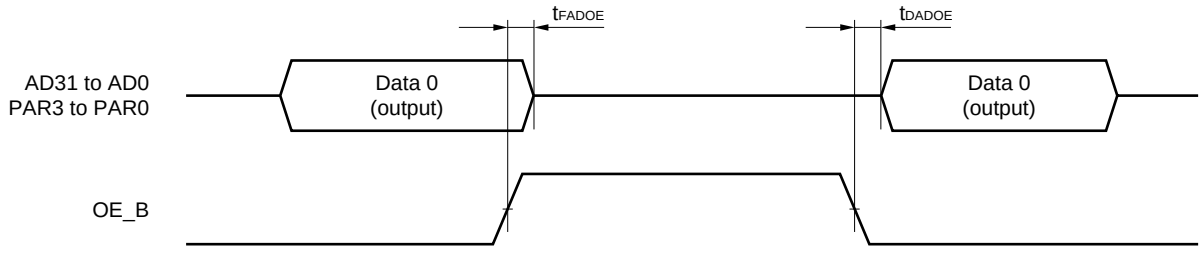
ABRT_B, ERR_B, and OE_B pins

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ABRT_B setup time	t_{SABRT}		8			ns
ABRT_B hold time	t_{HABRT}		3			ns
ERR_B setup time	t_{SERR}		8			ns
ERR_B hold time	t_{HERR}		3			ns
★ OE_B ↓→ AD/PAR output determination time	t_{DADOE}		0		18	ns
OE_B ↑→ AD/PAR high-impedance determination time	t_{FADOE}				18	ns

DMA abort/ERR_B timing



OE_B timing



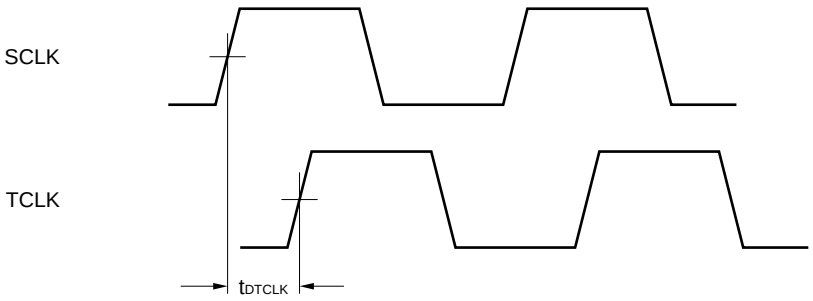
UTOPIA interface (external PHY mode)

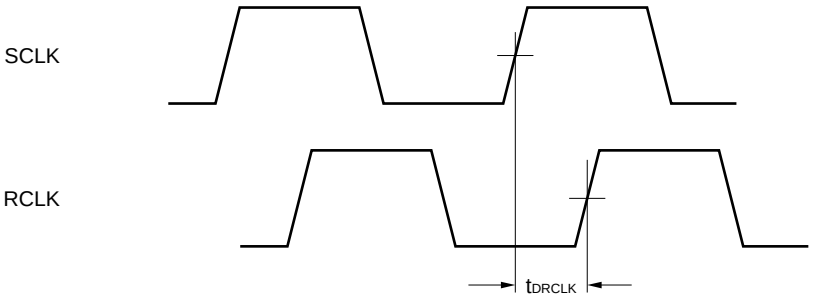
Transmission operation

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	SCLK ↑→ TCLK ↑ delay time	t_{DTCLK}				15	ns
	TCLK ↑→ Tx delay time	t_{DTX}		2		18	ns
★	TCLK ↑→ TSOC delay time	t_{DTSOC}		2		14	ns
★	TCLK ↑→ TENBL_B delay time	t_{DTEN}		2		14	ns
	FULL_B setup time	t_{SFULL}		8			ns
	FULL_B hold time	t_{HFULL}		1			ns

Reception operation

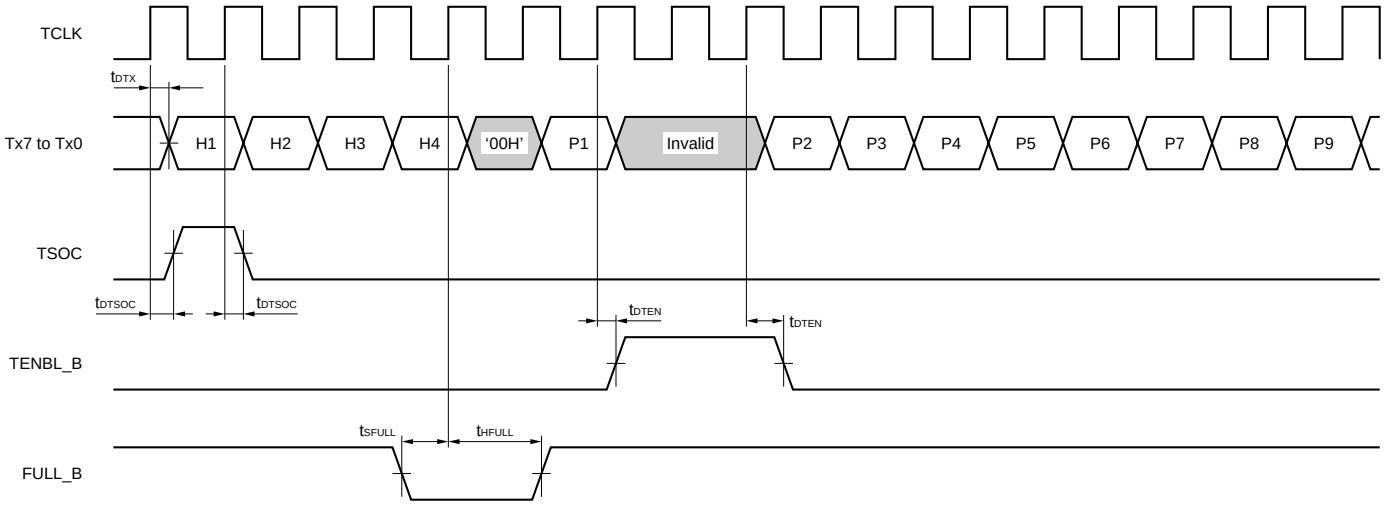
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	SCLK ↑→ RCLK ↑ delay time	t_{DRCLK}				15	ns
	Rx setup time	t_{SRX}		8			ns
	Rx hold time	t_{HRX}		1			ns
	RSOC setup time	t_{SRSOC}		8			ns
	RSOC hold time	t_{HRSOC}		1			ns
★	RCLK ↑→ RENBL_B delay time	t_{DREN}		2		14	ns
	EMPTY_B setup time	t_{SEMPT}		8			ns
	EMPTY_B hold time	t_{HEMPT}		1			ns





UTOPIA interface (1)

Transmission timing

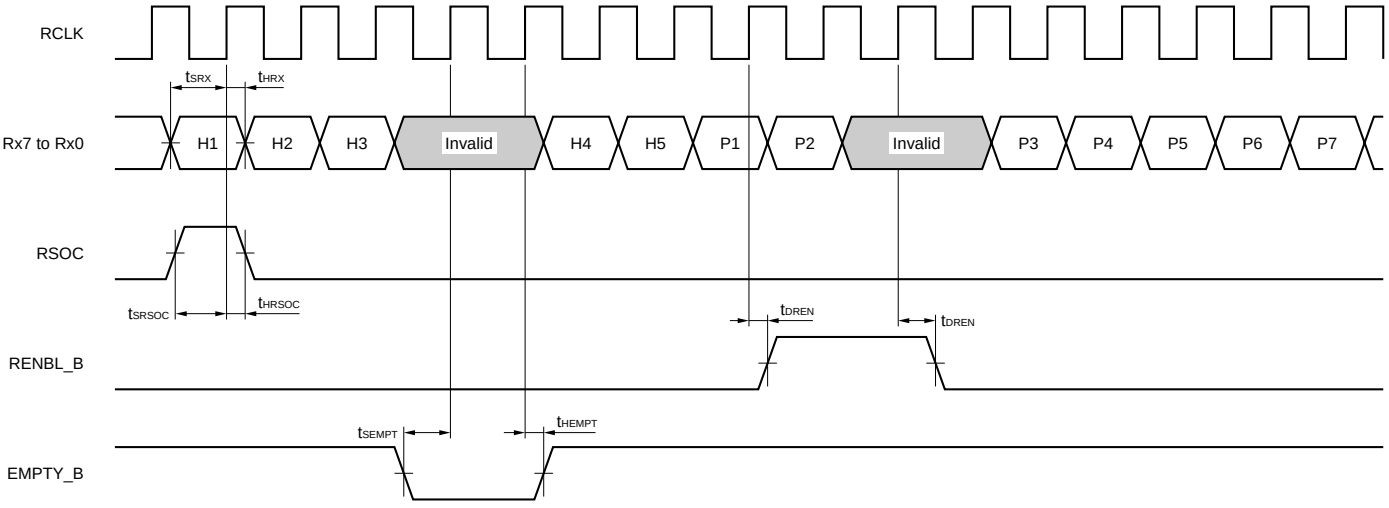


H1 to H4: ATM header

P1 to P9: Payload data

UTOPIA interface (2)

Reception timing



H1 to H4: ATM header

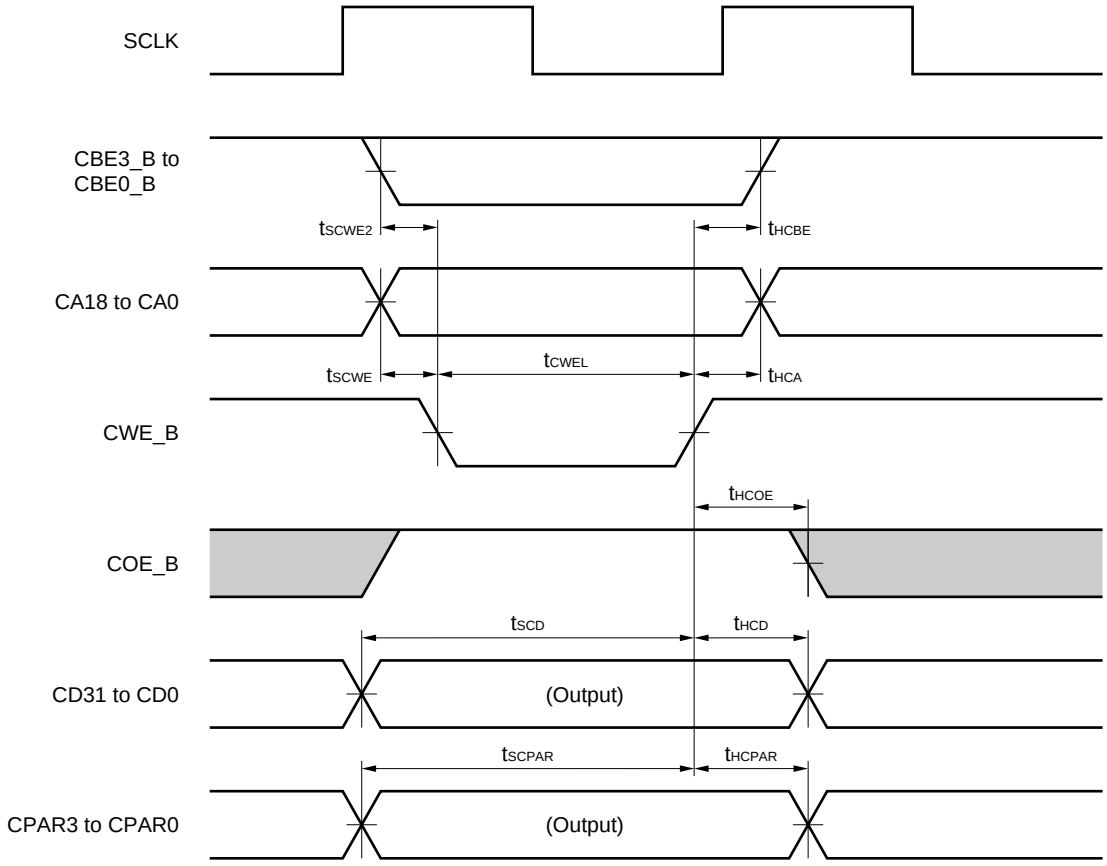
P1 to P7: Payload data

Control memory access

Write

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	CA → CWE_B ↓ setup time	t_{SCWE}			0			ns
	CBE_B → CWE_B ↓ setup time	t_{SCWE2}			0			ns
★	CWE_B low-level width	t_{CWEL}	V4.0	t_{CYSCLK} < 40 ns	1 t_{SCLKL} – 3			ns
				t_{CYSCLK} ≥ 40 ns	1 t_{SCLKL} – 2			ns
			V3.1 or before		1 t_{SCLKL} – 2			ns
★	CD hold time (from CWE_ B ↑)	t_{HCD}			0			ns
★	COE_B hold time (from CWE_ B ↑)	t_{HCOE}			0			ns
	CA hold time (from CWE_B ↑)	t_{HCA}			0			ns
	CBE_B hold time (from CWE_B ↑)	t_{HCBE}			0			ns
	CD output time (to CWE_B ↑)	t_{SCD}			15			ns
★	CPAR hold time (from CWE_B ↑)	t_{HCPAR}			0			ns
	CPAR output time (to CWE_B ↑)	t_{SCPAR}			15			ns

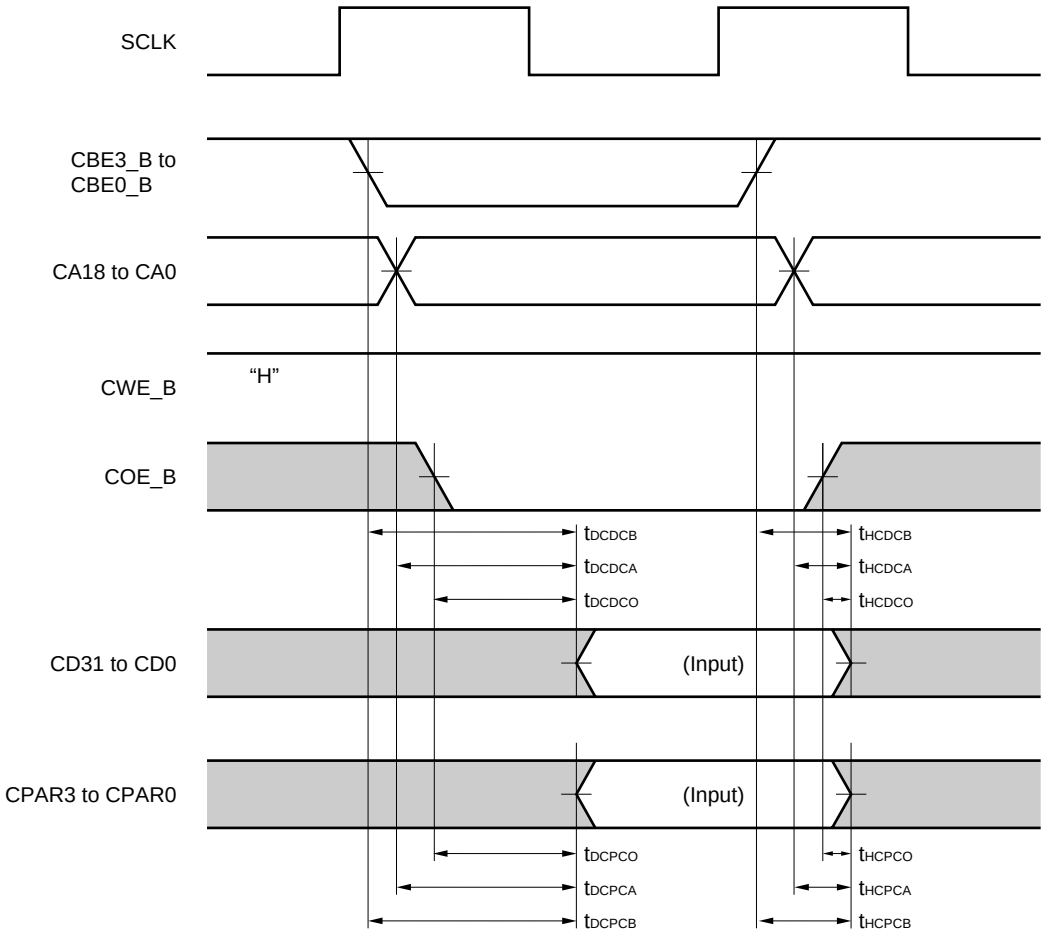
★ **Write timing**



Read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Permissible CD delay time (from CBE_B ↓)	t_{DCDCB}				1 t_{CYSCLK} – 18	ns
Permissible CD delay time (from CA)	t_{DCDCA}				1 t_{CYSCLK} – 18	ns
Permissible CD delay time (from COE_B ↓)	t_{DCDCO}				1 t_{CYSCLK} – 18	ns
CD hold time (from CBE_B ↑)	t_{HCDCB}		0			ns
CD hold time (from CA)	t_{HCDCA}		0			ns
CD hold time (from COE_B ↑)	t_{HCDCO}		0			ns
Permissible CPAR delay time (from CBE_B ↓)	t_{DCPCB}				1 t_{CYSCLK} – 18	ns
Permissible CPAR delay time (from CA)	t_{DCPCA}				1 t_{CYSCLK} – 18	ns
Permissible CPAR delay time (from COE_B ↓)	t_{DCPCO}				1 t_{CYSCLK} – 18	ns
CPAR hold time (from CBE_B ↑)	t_{HCPCB}		0			ns
CPAR hold time (from CA)	t_{HCPCA}		0			ns
CPAR hold time (from COE_B ↑)	t_{HCPCO}		0			ns

Read timing

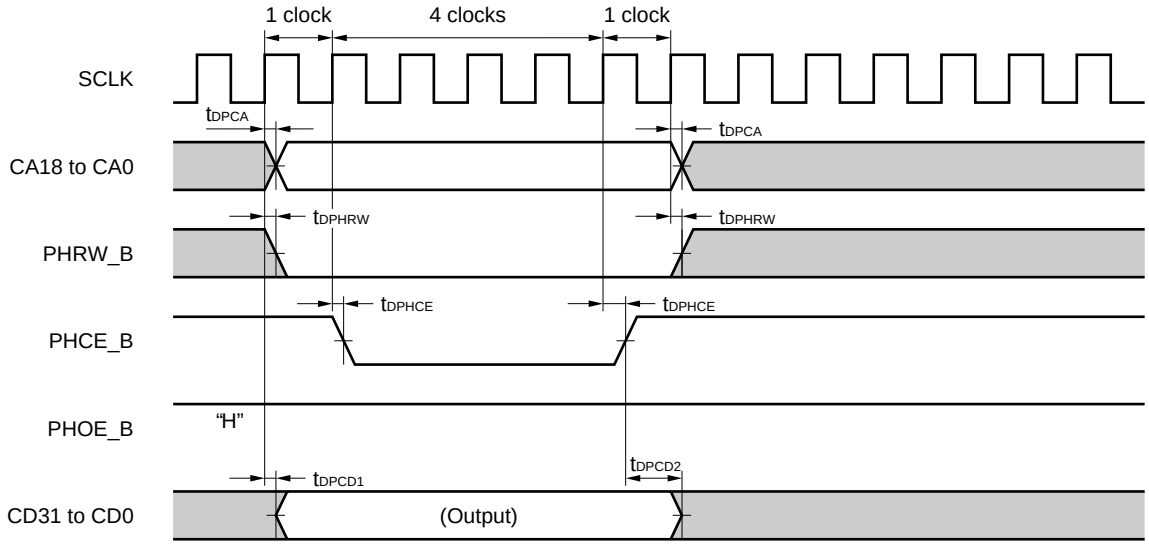


PHY status access

Write

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	SCLK ↑→ CA delay time	t_{DPCA}				20	ns
	SCLK ↑→ PHRW_B delay time	t_{DPHRW}				20	ns
	SCLK ↑→ PHCE_B delay time	t_{DPHCE}				20	ns
★	SCLK ↑→ CD delay time	t_{DPCD1}				20	ns
★	PHCE_B ↑→ CD delay time	t_{DPCD2}		1 t_{CYSCLK} – 10		1 t_{CYSCLK} + 10	ns

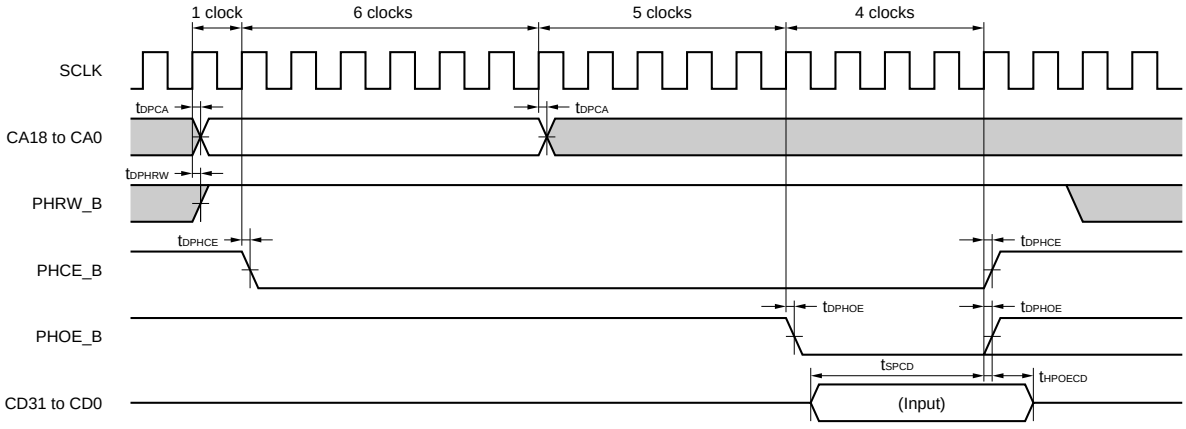
★ **Write timing**



Read

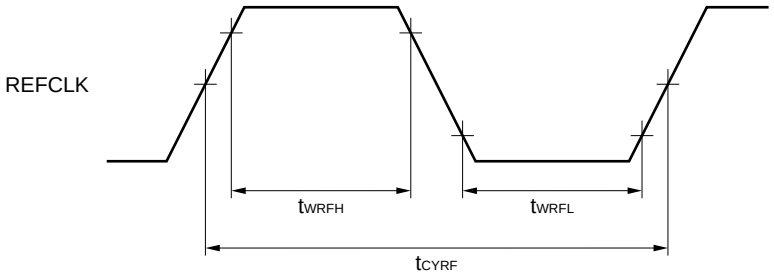
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CD setup time	t_{SPCD}		10			ns
CD hold time	t_{HPOECD}		0			ns
SCLK ↑→ CA delay time	t_{DPCA}				20	ns
SCLK ↑→ PHRW_B delay time	t_{DPHRW}				20	ns
SCLK ↑→ PHCE_B delay time	t_{DPHCE}				20	ns
SCLK ↑→ PHOE_B delay time	t_{DPHOE}				20	ns

Read timing



PMD serial interface (internal PHY mode)

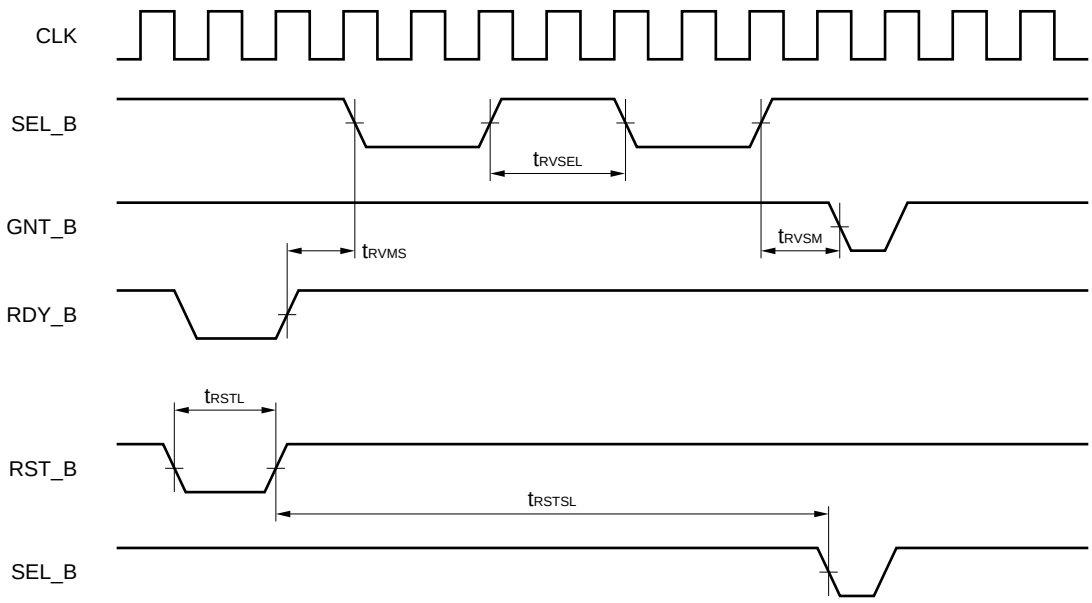
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REFCLK cycle time	t_{CYRF}		–20 ppm	51.4403	+20 ppm	ns
REFCLK high-level width	t_{WRFH}		0.4 × t_{CYRF}		0.4 × t_{CYRF}	ns
REFCLK low-level width	t_{WRFL}		0.4 × t_{CYRF}		0.4 × t_{CYRF}	ns



Others

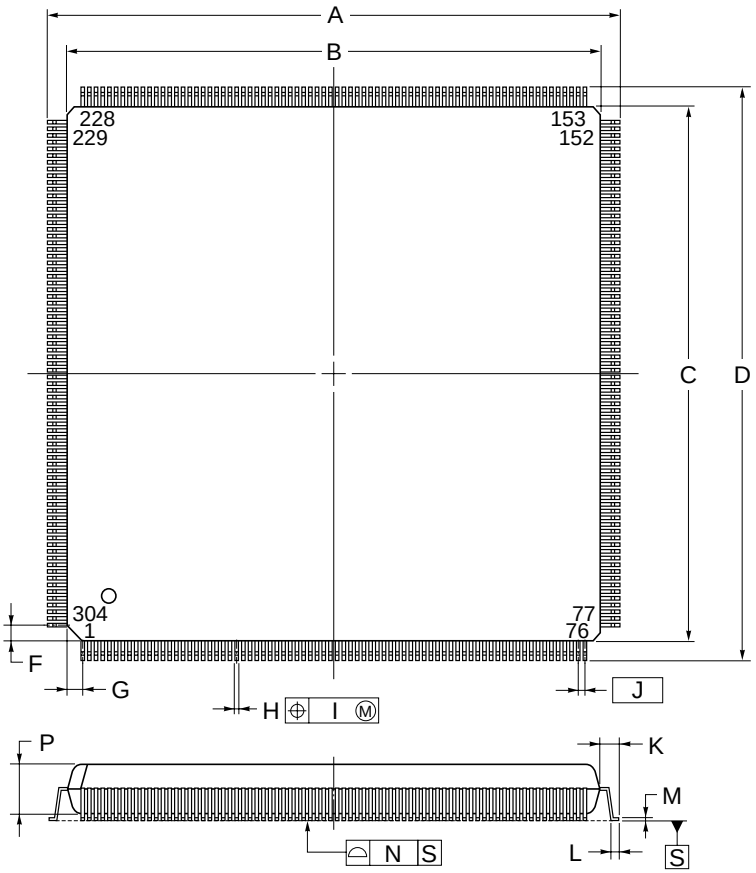
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SEL_B recovery time	t_{RVSEL}		2			t_{CYCLK}
SEL_B ↑→ GNT_B ↓ recovery time	t_{RVSM}		1			t_{CYCLK}
RDY_B ↑→ SEL_B ↓ recovery time	t_{RVMS}	RDY_B mode during normal operation	1			t_{CYCLK}
RST_B input pulse width	t_{RSTL}		1			t_{CYCLK}
RST_B ↑→ SEL_B ↓ recovery time	t_{RSTSL}		20			t_{CYCLK}

Others timing

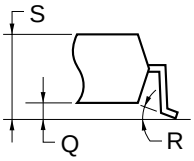


3. PACKAGE DRAWING

304 PIN PLASTIC QFP (FINE PITCH) (40x40)



detail of lead end



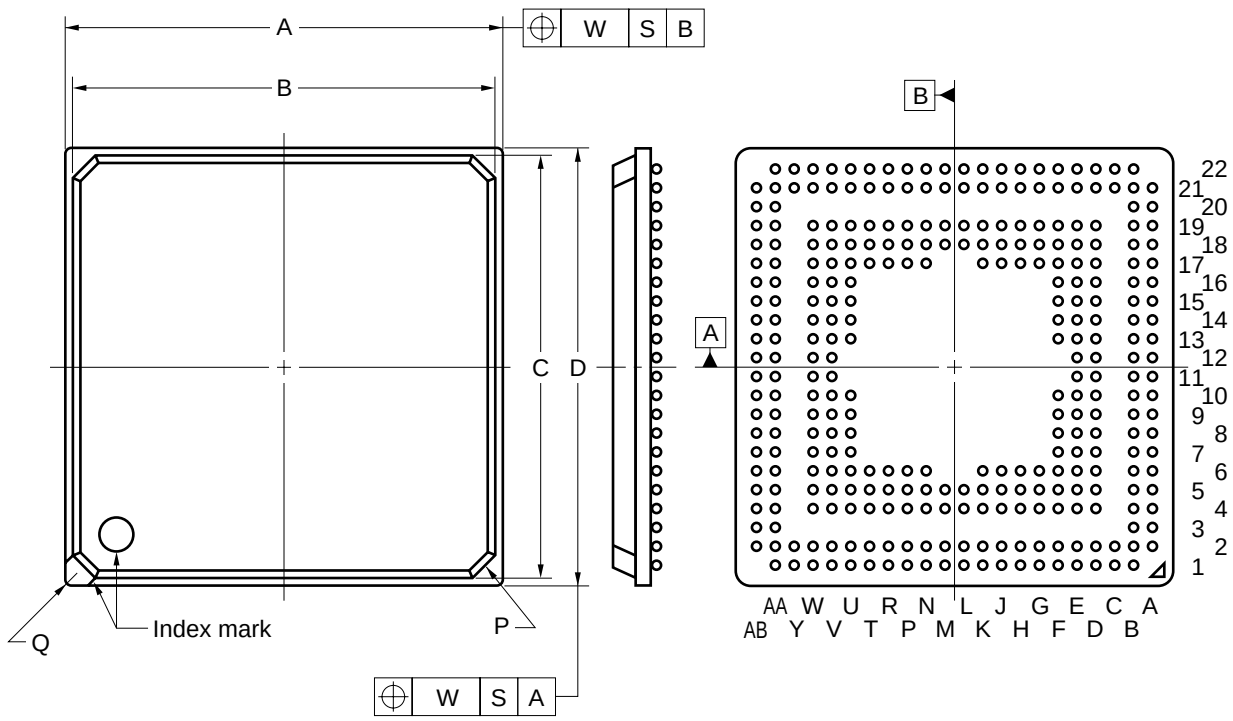
NOTE

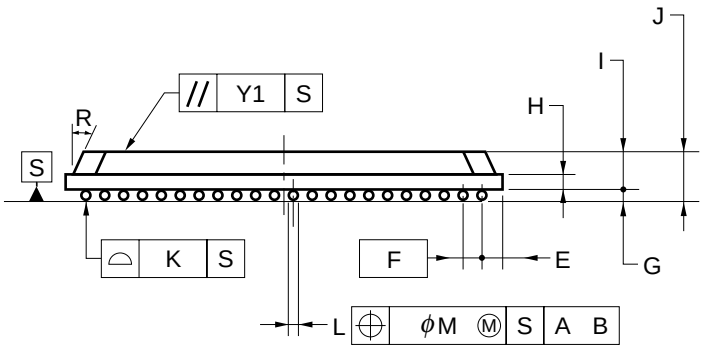
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	42.6±0.2
B	40.0±0.2
C	40.0±0.2
D	42.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	3.7±0.1
Q	0.4±0.1
R	5°±5°
S	4.3 MAX.

P304GL-50-NMU, PMU-3

★ 304-PIN PLASTIC FBGA (19x19)





ITEM	MILLIMETERS
A	19.00±0.10
B	18.40
C	18.40
D	19.00±0.10
E	1.10
F	0.8 (T.P.)
G	0.35±0.1
H	0.36
I	1.16
J	1.51±0.15
K	0.10
L	$\phi 0.50^{+0.05}_{-0.10}$
M	0.08
P	C1.0
Q	R0.3
R	25°
W	0.20
Y1	0.20

S304S1-80-6C-1

4. RECOMMENDED SOLDERING CONDITIONS

The μPD98405 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Surface mounting type

- **μPD98405GL-PMU: 304-pin plastic QFP (0.5 mm fine pitch) (40 × 40)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: once, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-203-1
Partial pin heating	Pin temperature: 300°C max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

★ • **μPD98405S1-6C: 304-pin plastic FBGA (0.8 mm pitch) (19 × 19)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 sec. max. (at 210°C or higher), Count: three times, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR30-103-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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