

# 32K x 16 Static RAM

## Features

- 5.0V operation ( $\pm 10\%$ )
- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - 825 mW (max., 10 ns, “L” version)
- Very Low standby power
  - 550  $\mu$ W (max., “L” version)
- Automatic power-down when deselected
- Independent Control of Upper and Lower bytes
- Available in 44-pin TSOP II and 400-mil SOJ

## Functional Description

The CY7C1020 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

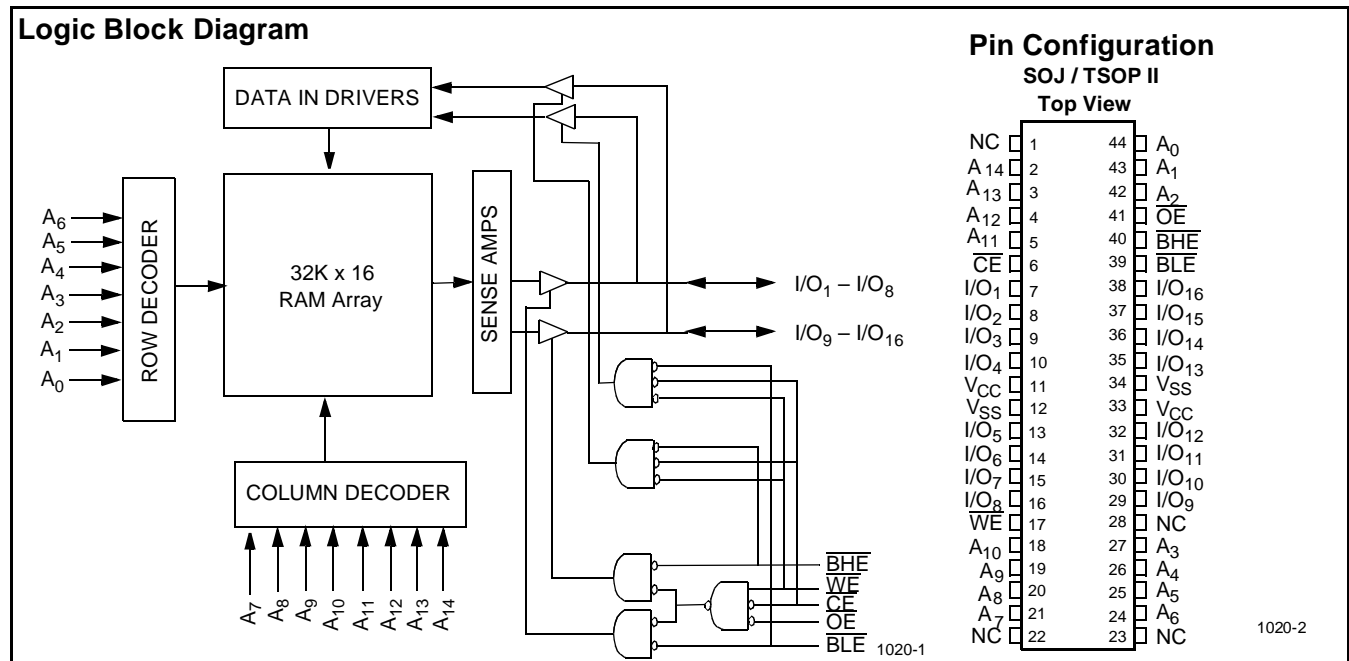
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable

( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1020 is available in standard 44-pin TSOP type II and 400-mil-wide SOJ packages.



## Selection Guide

	7C1020-10	7C1020-12	7C1020-15	7C1020-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)		180	170	160
	L	150	140	130
Maximum CMOS Standby Current (mA)		3	3	3
	L	0.1	0.1	0.1

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V–5.5V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1020-10		7C1020-12		7C1020-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	6.0	2.2	6.0	2.2	6.0	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-2	+2	-2	+2	-2	+2	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		180		170		160	mA
			L	150		140		130	
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		20		20		20	mA
			L	10		10		10	
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		3		3		3	mA
			L	100		100		100	μA

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the case temperature.

**Electrical Characteristics** Over the Operating Range (continued)

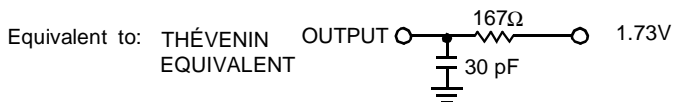
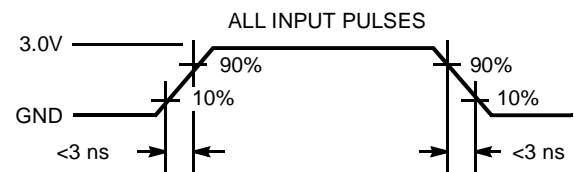
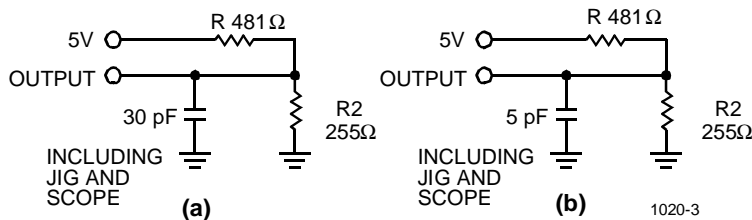
Parameter	Description	Test Conditions	7C1020-20		Unit
			Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	6.0	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-2	+2	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		160	mA
			L	130	
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		20	mA
			L	10	
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ , or $V_{IN} \leq 0.3\text{V}$ , $f = 0$		3	mA
			L	100	$\mu\text{A}$

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


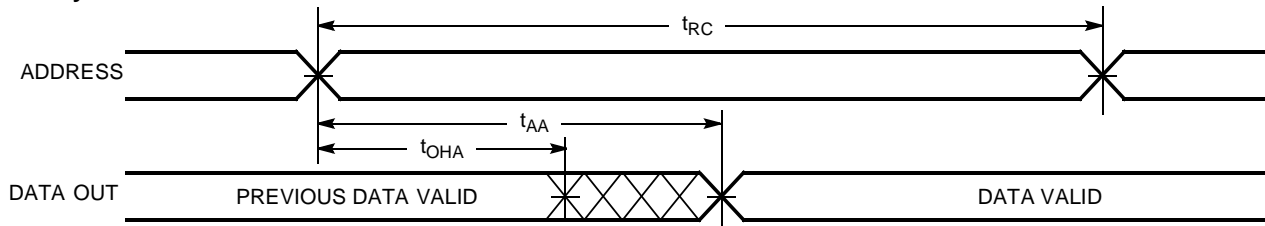
1020-4

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

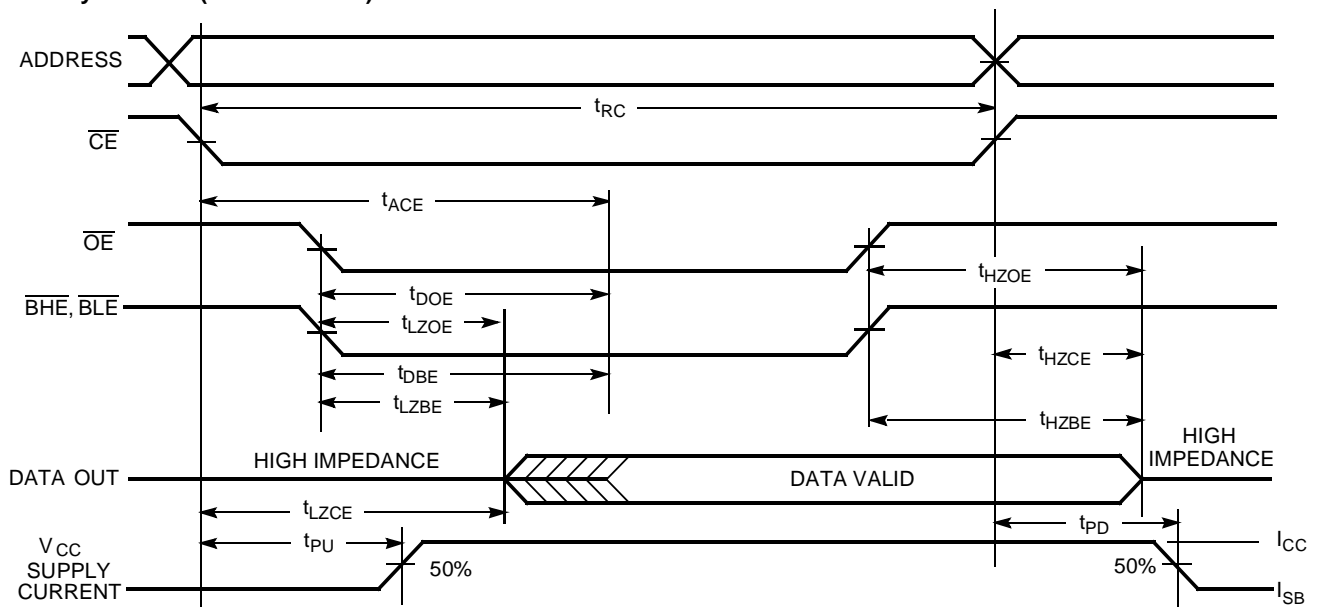
Parameter	Description	7C1020-10		7C1020-12		7C1020-15		7C1020-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	10		12		15		20		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15		20	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		5		7		9	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7		8	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7		8	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		12		15		20	ns
t <sub>DBE</sub>	Byte enable to Data Valid		5		6		7		9	ns
t <sub>LZBE</sub>	Byte enable to Low Z	0		0		0		0		ns
t <sub>HZBE</sub>	Byte disable to High Z		5		6		7		9	ns
<b>WRITE CYCLE<sup>[7]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	10		12		15		12		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		9		10		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		8		10		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	7		8		10		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		6		10		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		5		6		7		9	ns
t <sub>BW</sub>	Byte enable to end of write	7		8		9		12		ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and BHE / BLE LOW.  $\overline{CE}$ ,  $\overline{WE}$  and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1** <sup>[8, 9]</sup>


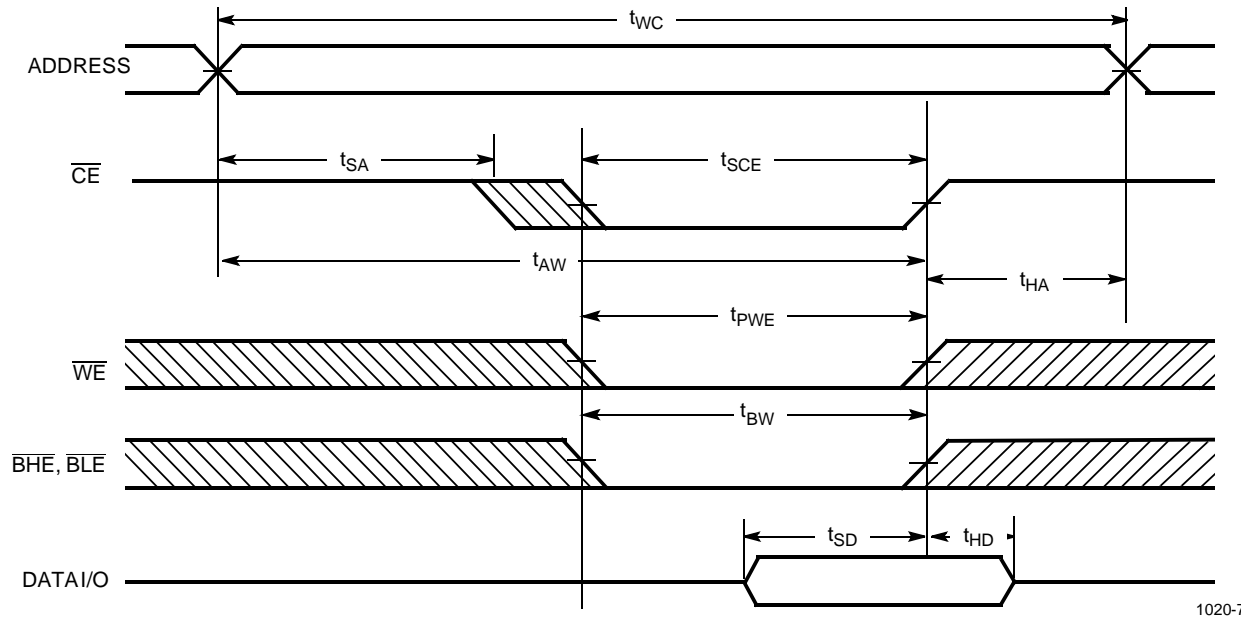
1020-5

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** <sup>[9, 10]</sup>


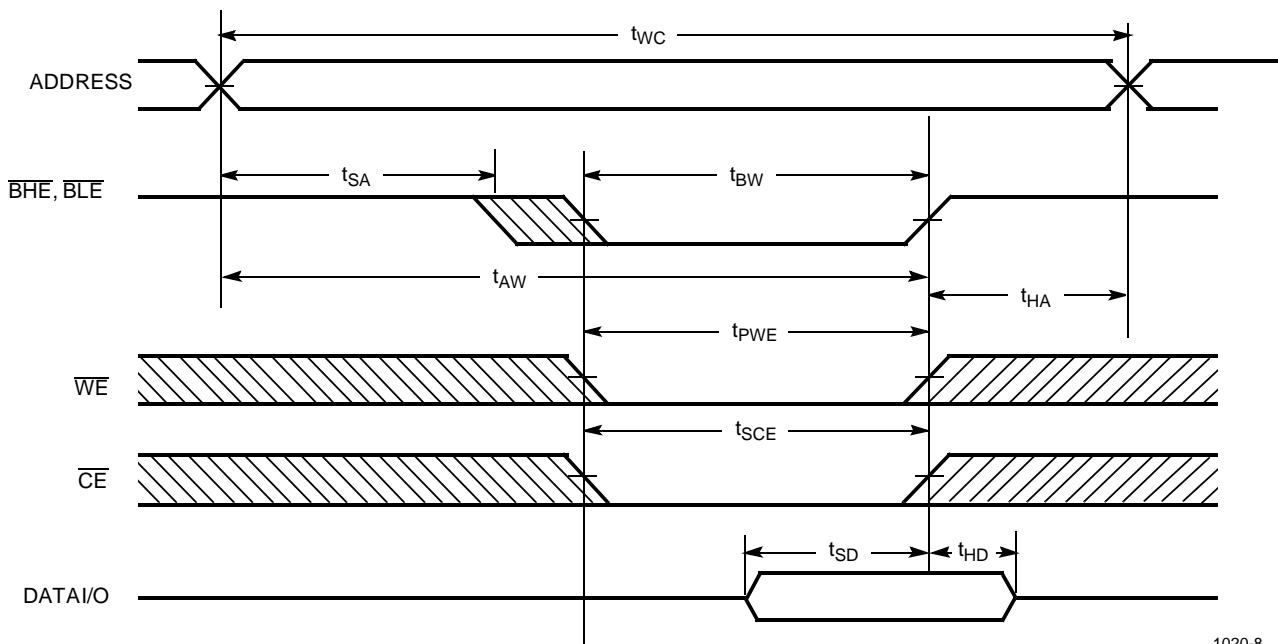
1020-6

**Notes:**

8. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
9.  $\overline{WE}$  is HIGH for read cycle.
10. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[11, 12]</sup>**


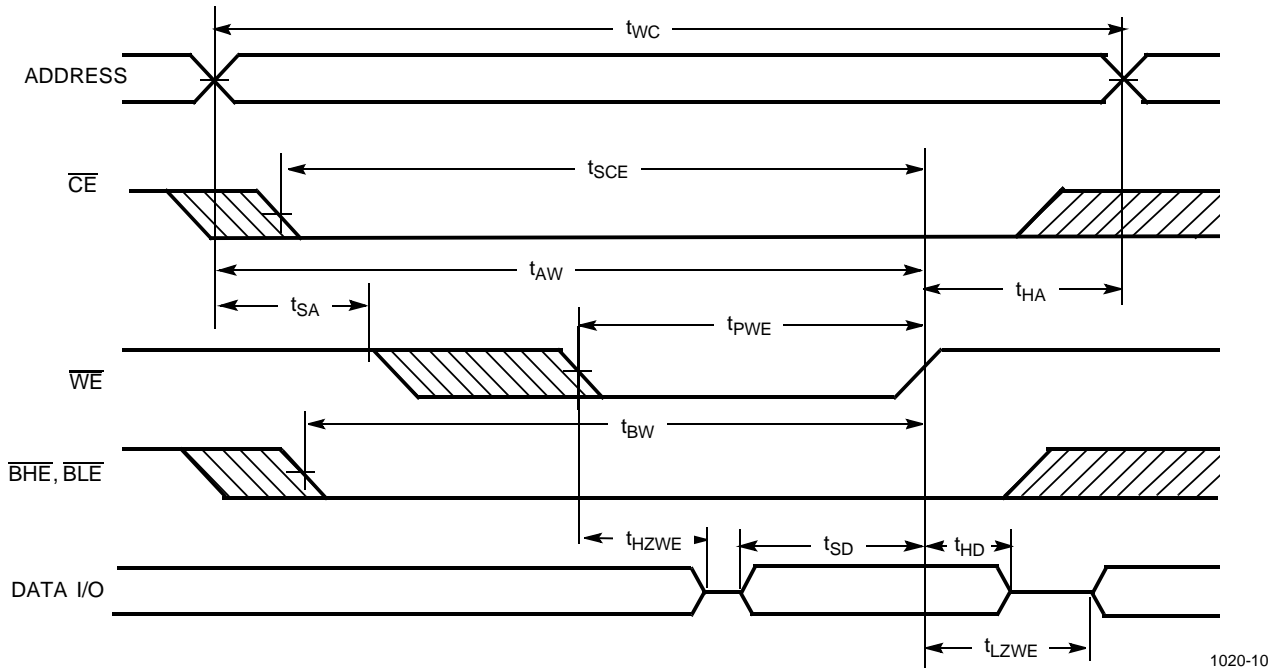
1020-7

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**


1020-8

**Notes:**

11. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
12. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**


1020-10

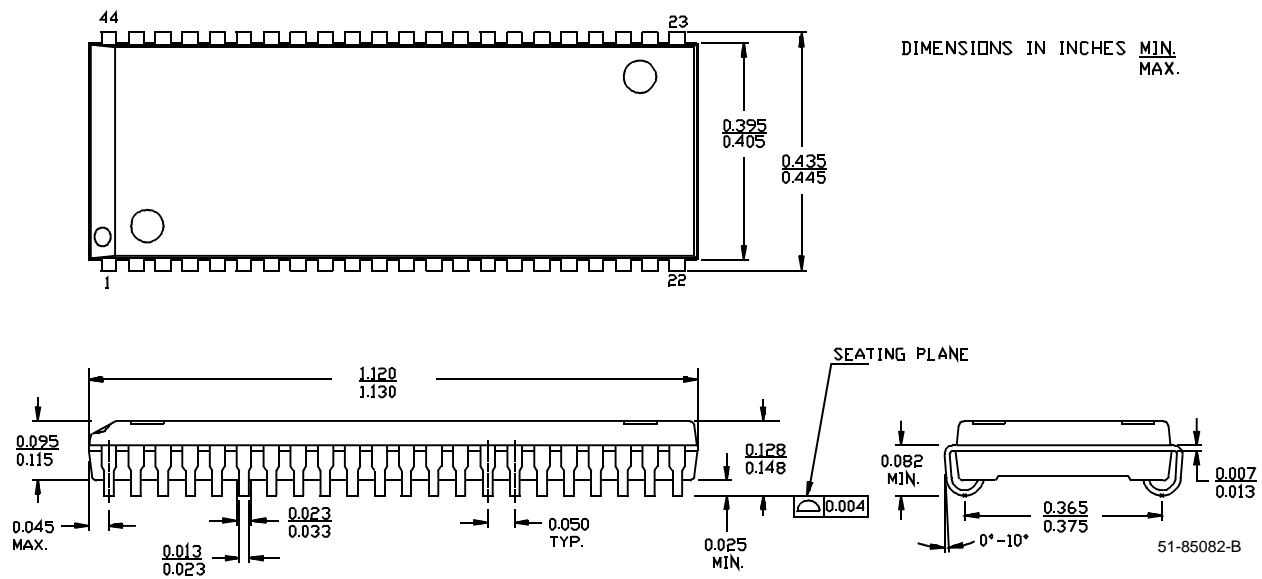
**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

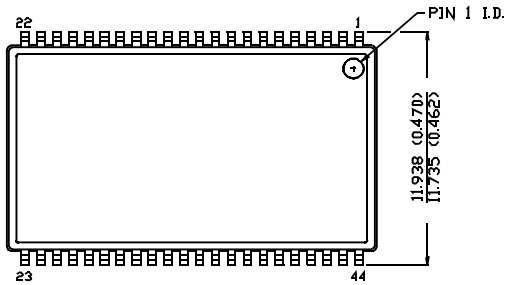
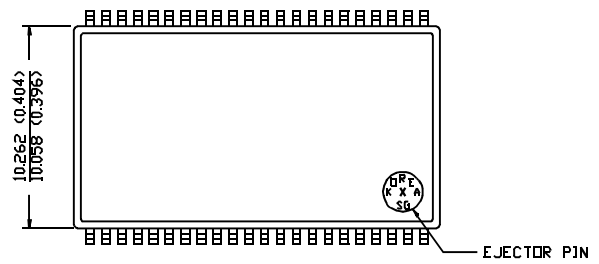
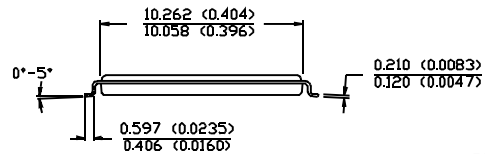
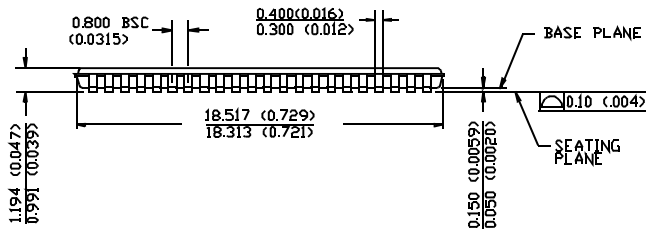
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1020-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1020-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1020-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-15ZC	Z44	44-Lead TSOP Type II	Commercial
20	CY7C1020-20VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020L-20VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020-20ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020L-20ZC	Z44	44-Lead TSOP Type II	Commercial

Document #: 38-00542-C

**Package Diagrams**
**44-Lead (400-Mil) Molded SOJ V34**




**Package Diagrams (continued)**
**44-Pin TSOP II Z44**

 DIMENSION IN MM (INCH)  
 MAX  
 MIN.

**TOP VIEW**

**BOTTOM VIEW**


51-85087-A