

HM514400B/BL Series

HM514400C/CL Series

1,048,576-word × 4-bit Dynamic Random Access Memory

HITACHI

Rev. 1.0
Nov. 29, 1994

The Hitachi HM514400B/BL, HM514400C/CL are CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514400B/BL, HM514400C/CL have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400B/BL, HM514400C/CL offer Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM514400B/BL, HM514400C/CL to be packaged in standard 300-mil 26-pin plastic SOJ, standard 400-mil 20-pin plastic ZIP and 26-pin plastic TSOP II.

- Test function
- Battery back up operation
 - HM514400BL Series (L-version)
 - HM514400CL Series (L-version)

Features

- Single 5 V (±10%)
- High speed
 - Access time
60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode
605 mW/550 mW/495 mW (max)
 - Standby mode 11 mW (max)
0.55 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycles : 16 ms
1024 refresh cycles : 128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh



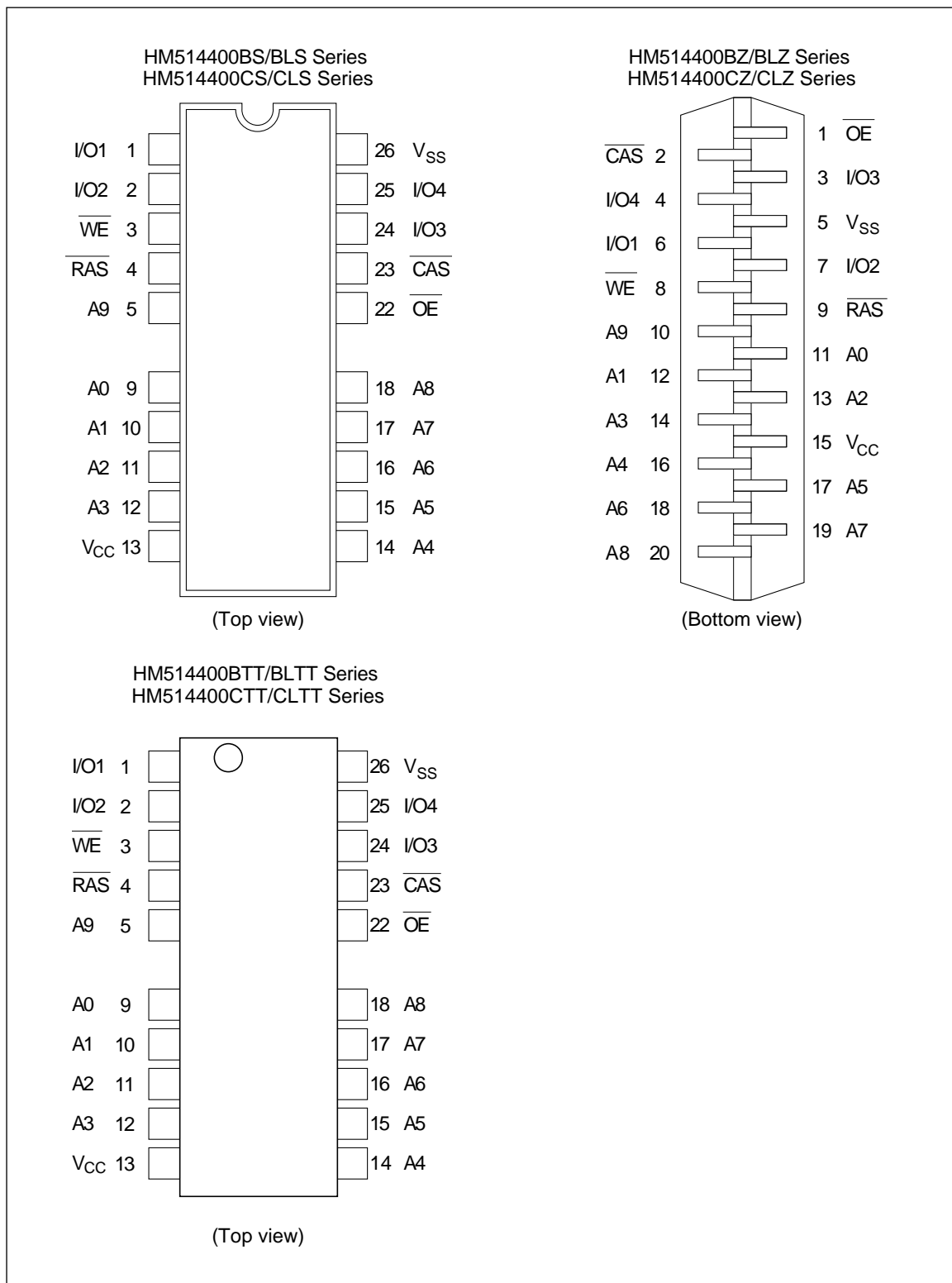
HM514400B/BL, HM514400C/CL Series

Ordering Information

Type No.	Access time	Package	Type No.	Access time	Package
HM514400BS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/20D)	HM514400CZ-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514400BS-7	70 ns				
HM514400BS-8	80 ns				
HM514400BLS-6	60 ns		HM514400CLZ-6	60 ns	
HM514400BLS-7	70 ns				
HM514400BLS-8	80 ns				
HM514400CS-6	60 ns		HM514400BTT-6	60 ns	26-pin plastic TSOPII (TTP-26/20D)
HM514400CS-7	70 ns				
HM514400CS-8	80 ns				
HM514400CLS-6	60 ns		HM514400BLTT-6	60 ns	
HM514400CLS-7	70 ns				
HM514400CLS-8	80 ns				
HM514400BZ-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)	HM514400CTT-6	60 ns	
HM514400BZ-7	70 ns				
HM514400BZ-8	80 ns				
HM514400BLZ-6	60 ns		HM514400CLTT-6	60 ns	
HM514400BLZ-7	70 ns				
HM514400BLZ-8	80 ns				
			HM514400CLTT-7	70 ns	
			HM514400CLTT-8	80 ns	

HM514400B/BL, HM514400C/CL Series

Pin Arrangement



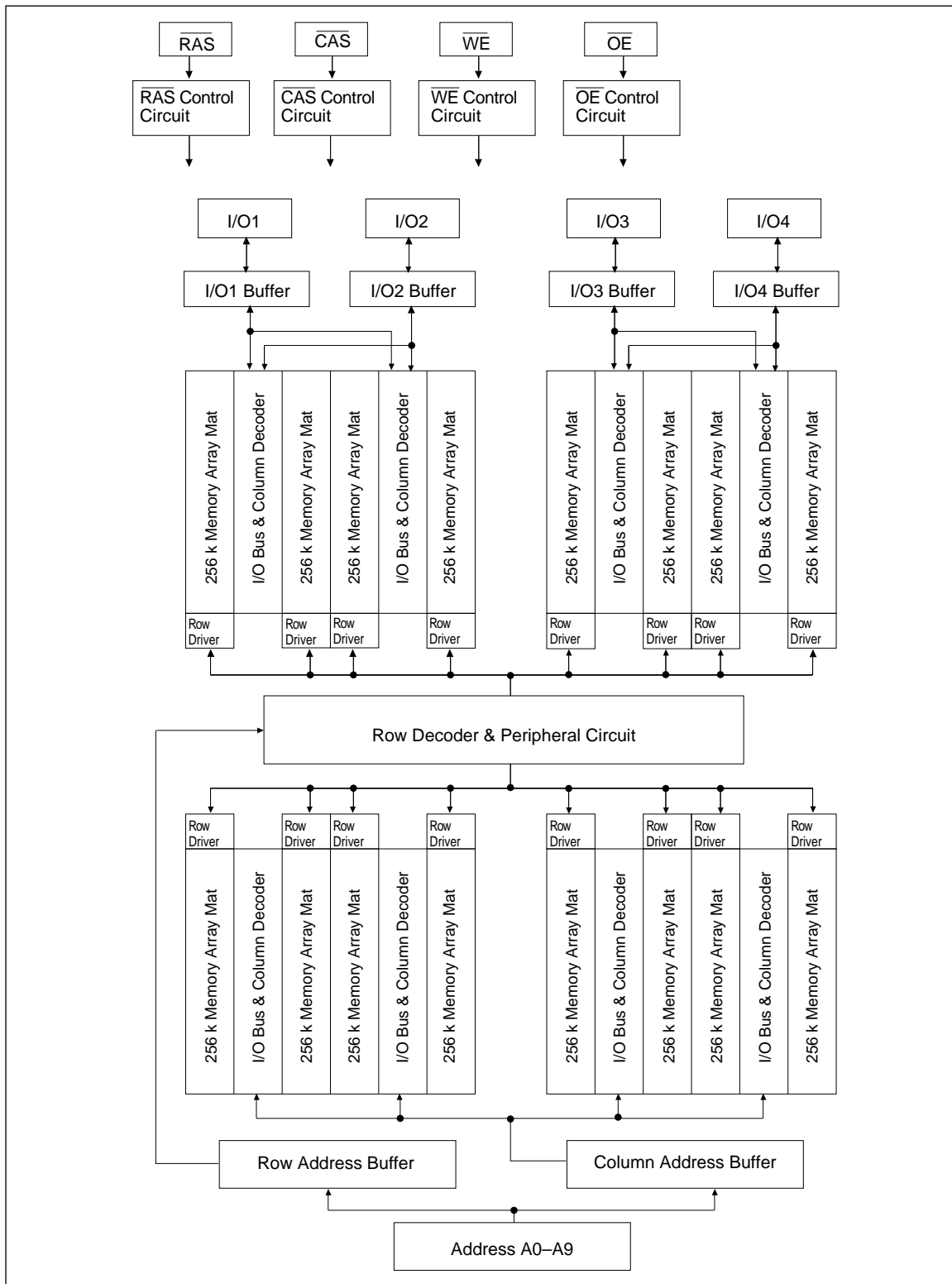
HM514400B/BL, HM514400C/CL Series

Pin Description

Pin name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O1 to I/O4	Data-in/Data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

HM514400B/BL, HM514400C/CL Series

Block Diagram



HM514400B/BL, HM514400C/CL Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HM514400B/BL, HM514400C/CL Series

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

		HM514400B/BL, HM514400C/CL								
		-6		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	100	—	100	—	100	μA	CMOS interface $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z	4
$\overline{\text{RAS}}$ -only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I_{CC6}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	
Fast page mode current	I_{CC7}	—	110	—	100	—	90	mA	$t_{PC} = \text{min}$	1, 3
Battery back up current (Standby with CBR refresh) (L-version)	I_{CC10}	—	200	—	200	—	200	μA	$t_{RC} = 125\ \mu\text{s}$ $t_{RAS} \leq 1\ \mu\text{s}$ $\overline{\text{WE}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$ $\overline{\text{OE}}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed twice or less while $\overline{\text{RAS}} = V_{IL}$.

3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$ and $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.

HM514400B/BL, HM514400C/CL Series

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *14, *15, *16

Test Conditions

- Input rise and fall times : 5 ns
- Input timing reference levels : 0.8 V, 2.4 V
- Output load : 2 TTL gate + C_L (100 pF) (Including scope and jig)

HM514400B/BL, HM514400C/CL Series

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
\overline{RAS} precharge time	t_{RP}	40	—	50	—	60	—	ns	
\overline{RAS} pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	19
\overline{CAS} pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	20
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	8
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
\overline{RAS} hold time	t_{RSH}	15	—	20	—	20	—	ns	
\overline{CAS} hold time	t_{CSH}	60	—	70	—	80	—	ns	
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	10	—	10	—	10	—	ns	
\overline{OE} to Din delay time	t_{ODD}	15	—	20	—	20	—	ns	
\overline{OE} delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
\overline{CAS} setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

HM514400B/BL, HM514400C/CL Series

Read Cycle

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 17
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13, 17
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	—	20	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	18
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	20	0	20	ns	6
Output buffer turn-off time to $\overline{\text{OE}}$	t_{OFF2}	0	15	0	20	0	20	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	20	—	20	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	—	20	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	11

HM514400B/BL, HM514400C/CL Series

Read-Modify-Write Cycle

		HM514400B/BL, HM514400C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	150	—	180	—	200	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	80	—	95	—	105	—	ns	10
\overline{CAS} to \overline{WE} delay time	t_{CWD}	35	—	45	—	45	—	ns	10
Column address to \overline{WE} delay time	t_{AWD}	50	—	60	—	65	—	ns	10
\overline{OE} hold time from \overline{WE}	t_{OEh}	15	—	20	—	20	—	ns	

Refresh Cycle

		HM514400B/BL, HM514400C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
\overline{CAS} setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
\overline{CAS} hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	10	—	10	—	10	—	ns	
\overline{CAS} precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HM514400B/BL, HM514400C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode \overline{CAS} precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode \overline{RAS} pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from \overline{CAS} precharge	t_{ACP}	—	35	—	40	—	45	ns	3, 13, 17
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	35	—	40	—	45	—	ns	

HM514400B/BL, HM514400C/CL Series

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	t _{PCM}	80	—	95	—	100	—	ns	
Fast page mode read-modify-write cycle $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPW}	55	—	65	—	70	—	ns	10

Test Mode Cycle

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Test mode $\overline{\text{WE}}$ setup time	t _{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{\text{WE}}$ hold time	t _{WH}	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514400B/BL, HM514400C/CL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ precharge time in counter test cycle	t _{CPT}	40	—	40	—	40	—	ns	

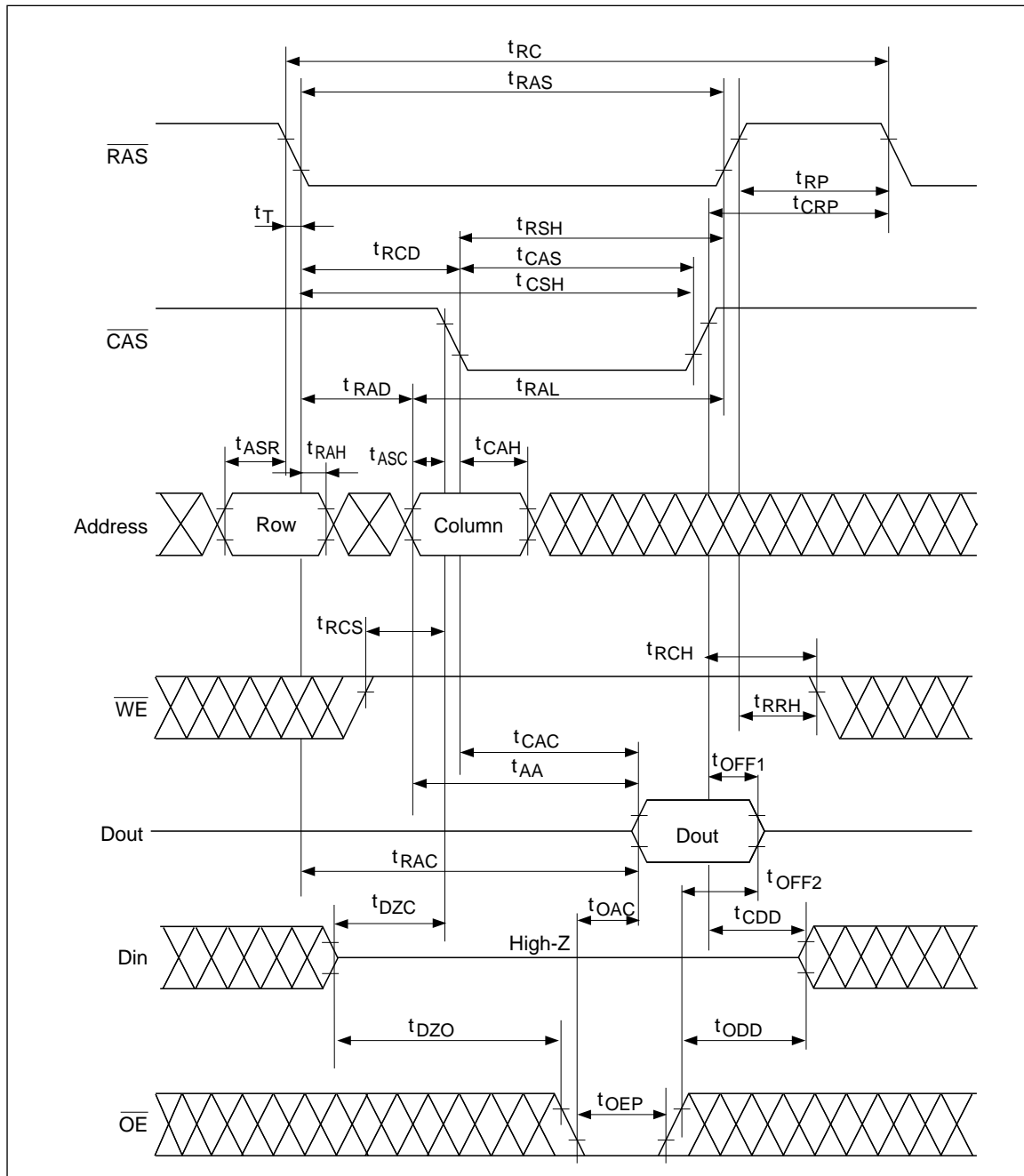
HM514400B/BL, HM514400C/CL Series


- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \geq t_{RAD}(\max)$.
 6. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RAD}(\max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, $t_{CPW} \geq t_{CPW}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to \overline{CAS} leading edge in an early write cycle and to \overline{WE} leading edge in a delayed write or read-modify-write cycle.
 12. t_{RASC} defines \overline{RAS} pulse width in fast page mode cycles.
 13. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
 14. An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (\overline{RAS} -only refresh cycle or \overline{CAS} -before- \overline{RAS} refresh cycle). If the internal refresh counter is used, a minimum of eight \overline{CAS} -before- \overline{RAS} refresh cycles is required.
 15. In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device.
 16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits - - - CA0. This test mode operation can be performed by \overline{WE} -and- \overline{CAS} -before- \overline{RAS} (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a \overline{RAS} -only refresh cycle or a \overline{CAS} -before- \overline{RAS} refresh cycle.
 17. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
 18. Either t_{RCH} or t_{RRH} must be satisfied
 19. $t_{RAS}(\min) = t_{RWD}(\min) + t_{RWL}(\min) + t_T$ in read-modify-write cycle.
 20. $t_{CAS}(\min) = t_{CWD}(\min) + t_{CWL}(\min) + t_T$ in read-modify-write cycle.

HM514400B/BL, HM514400C/CL Series

Timing Waveforms*21

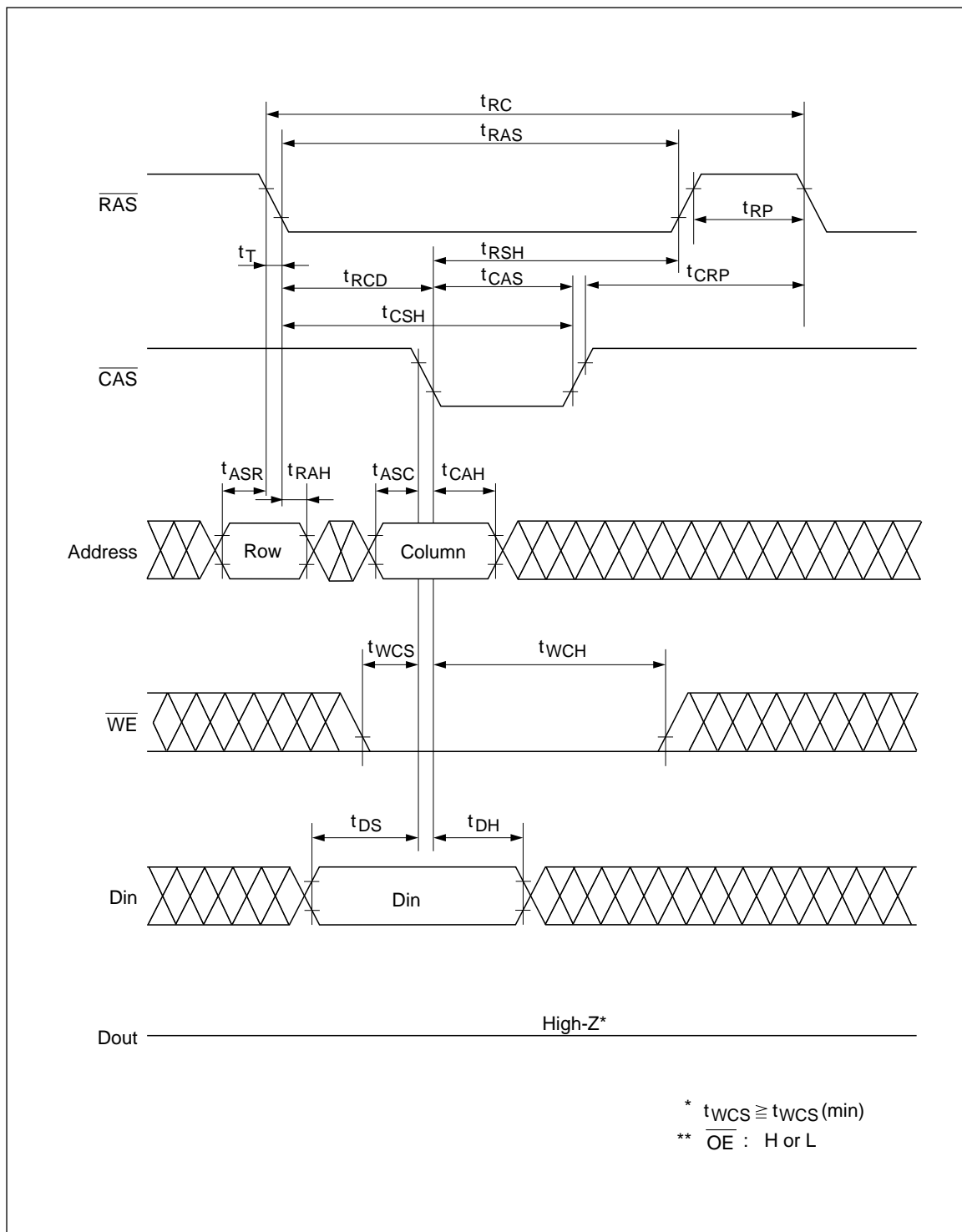
Read Cycle



Notes: 21.  H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)

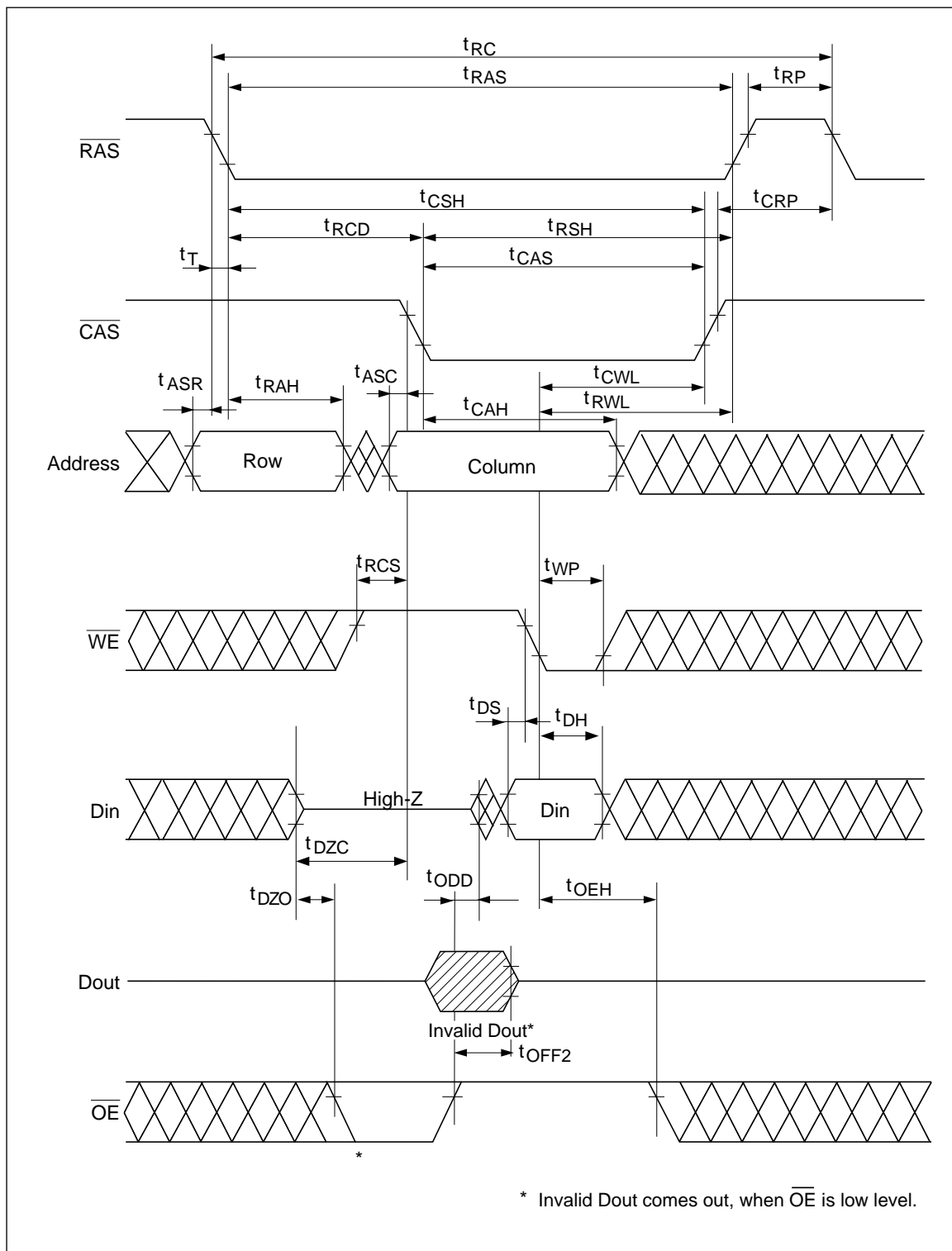
 Invalid Dout

Early Write Cycle

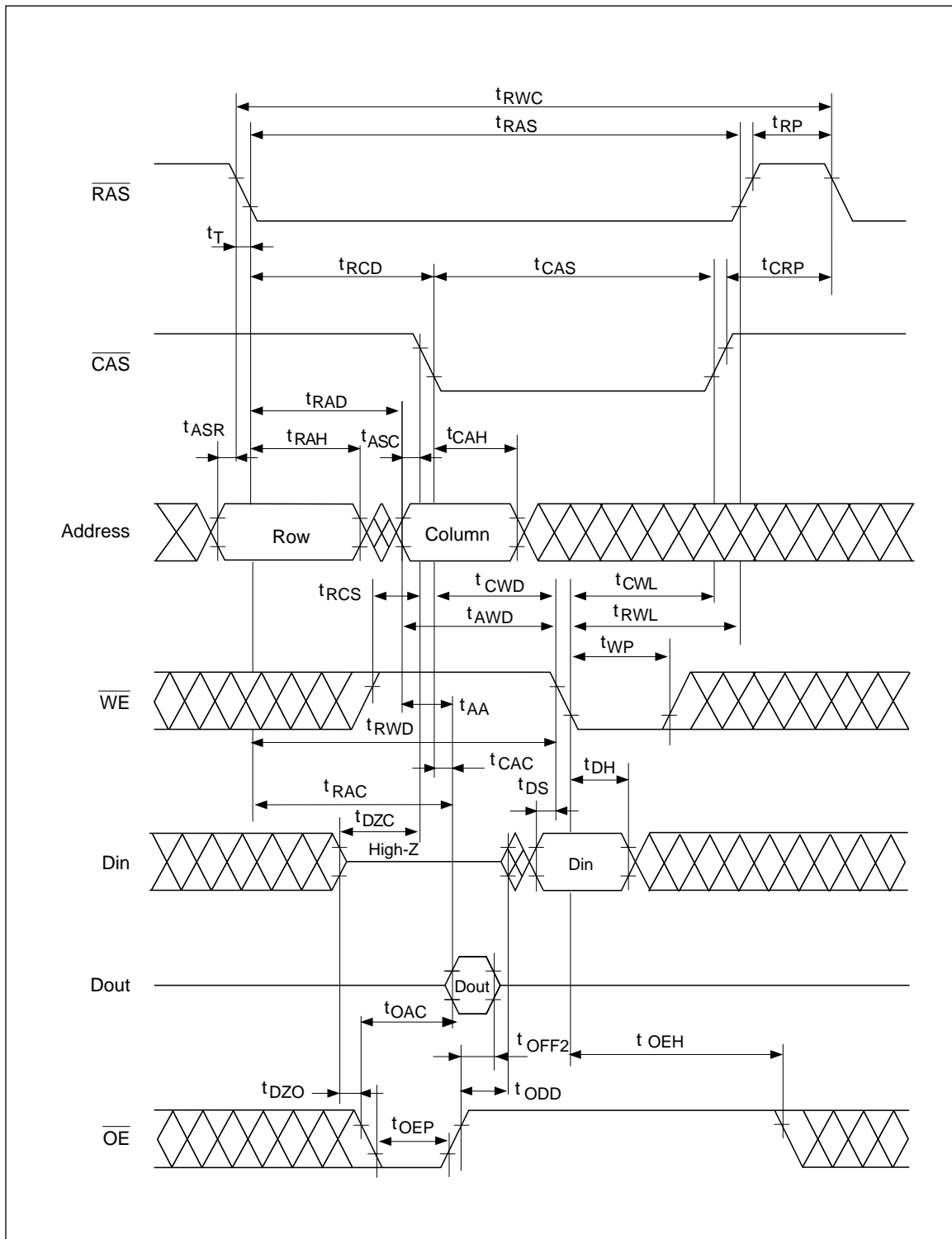


HM514400B/BL, HM514400C/CL Series

Delayed Write Cycle

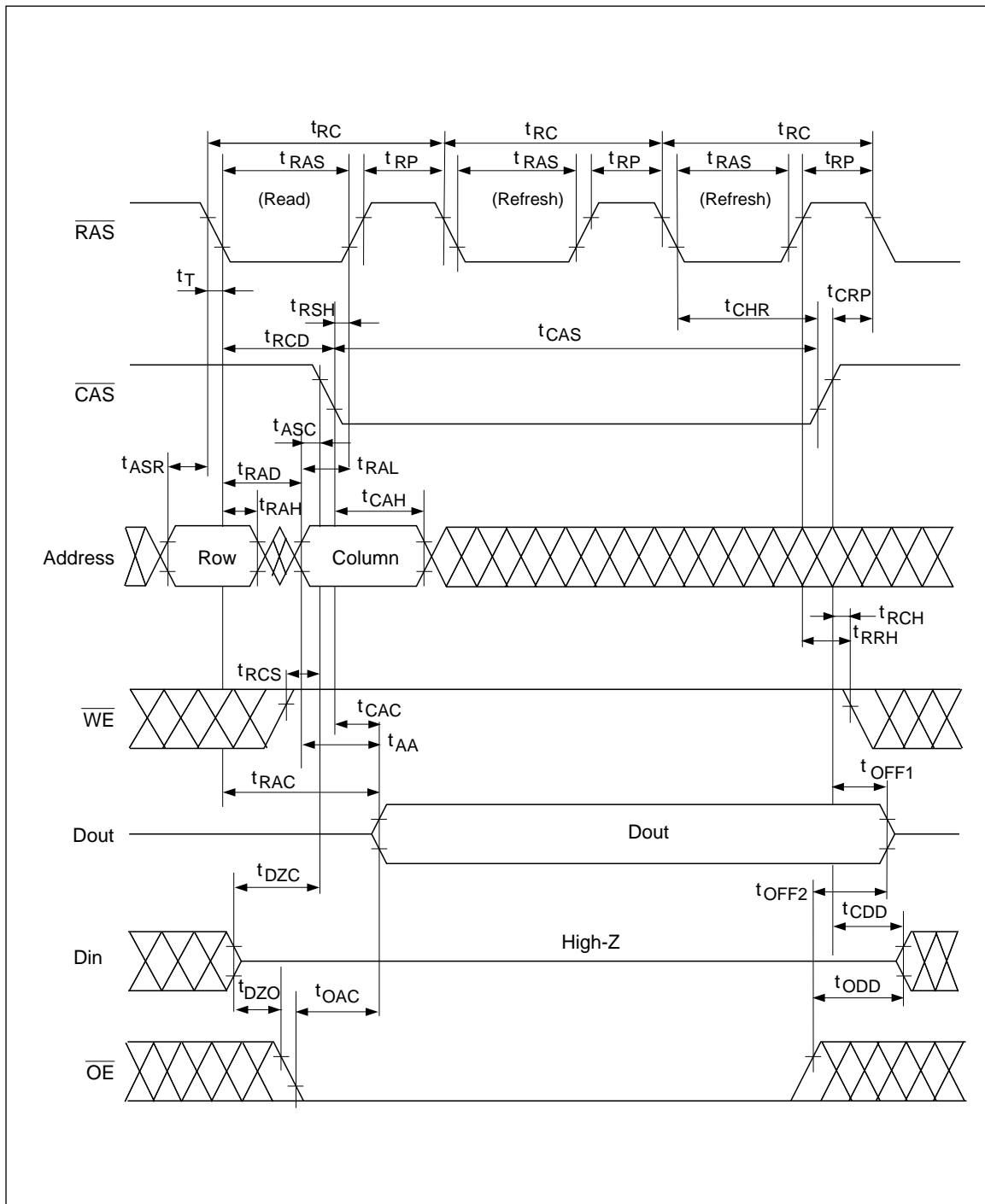


Read-Modify-Write Cycle

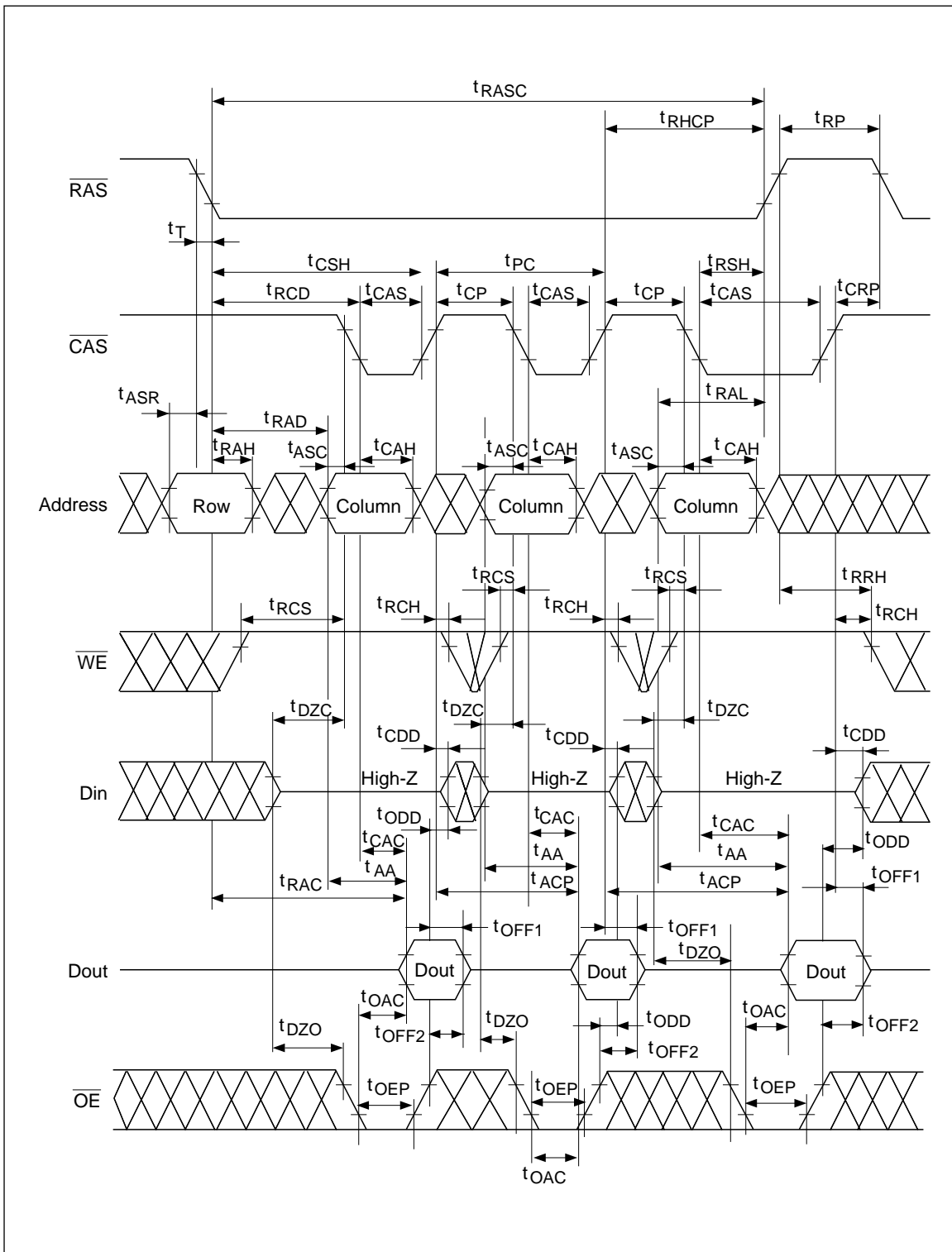


HM514400B/BL, HM514400C/CL Series

Hidden Refresh Cycle

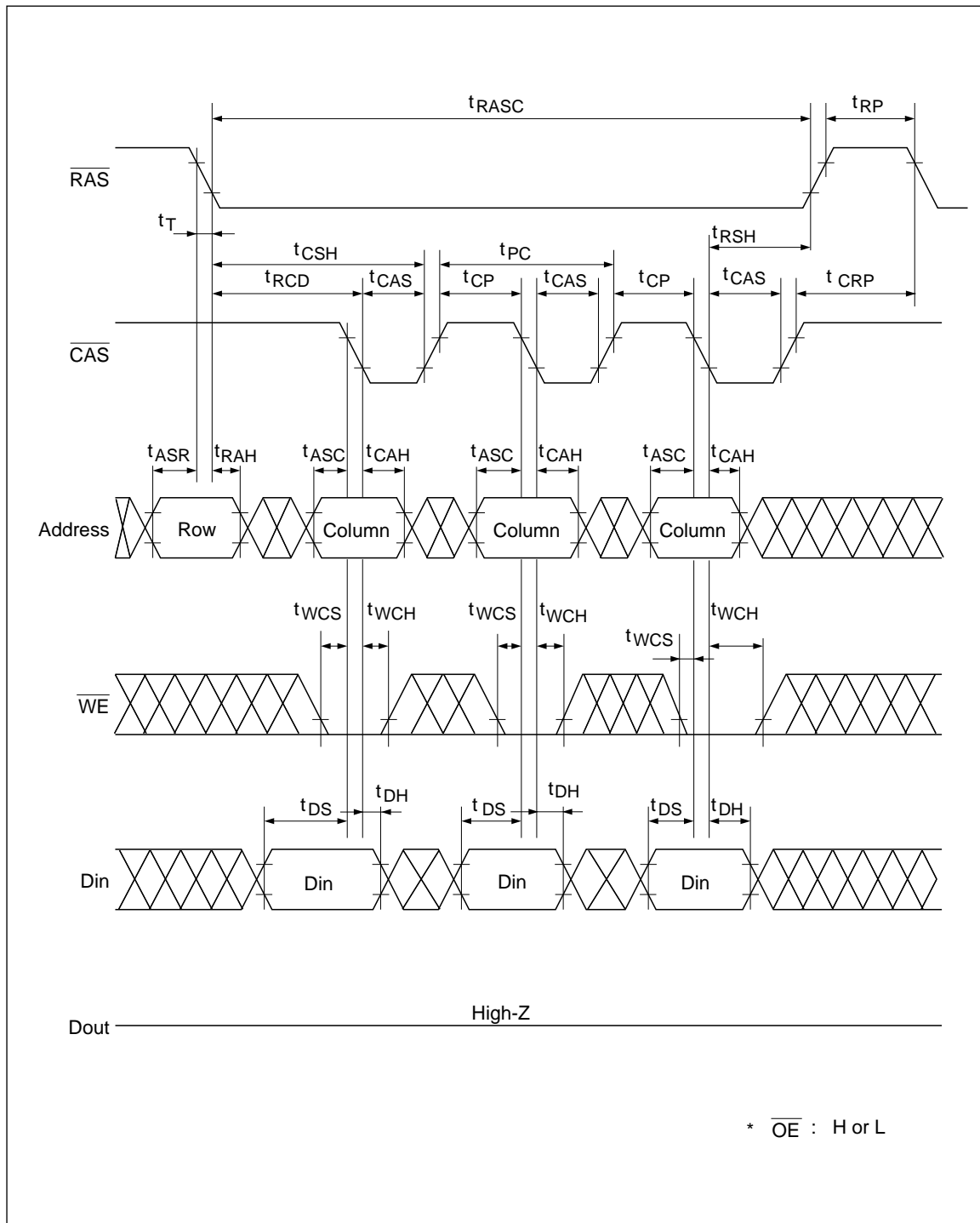


Fast Page Mode Read Cycle

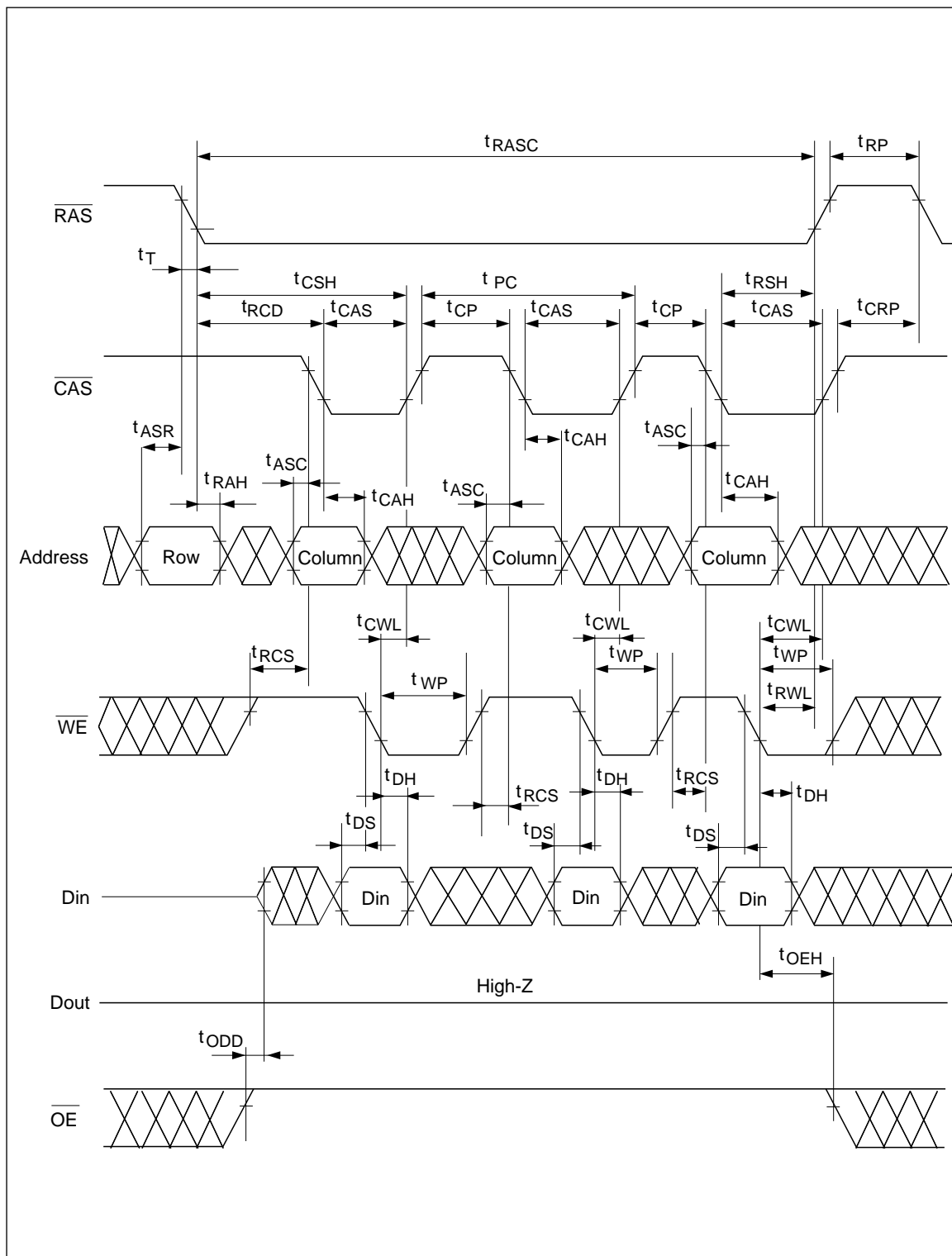


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Fast Page Mode Early Write Cycle

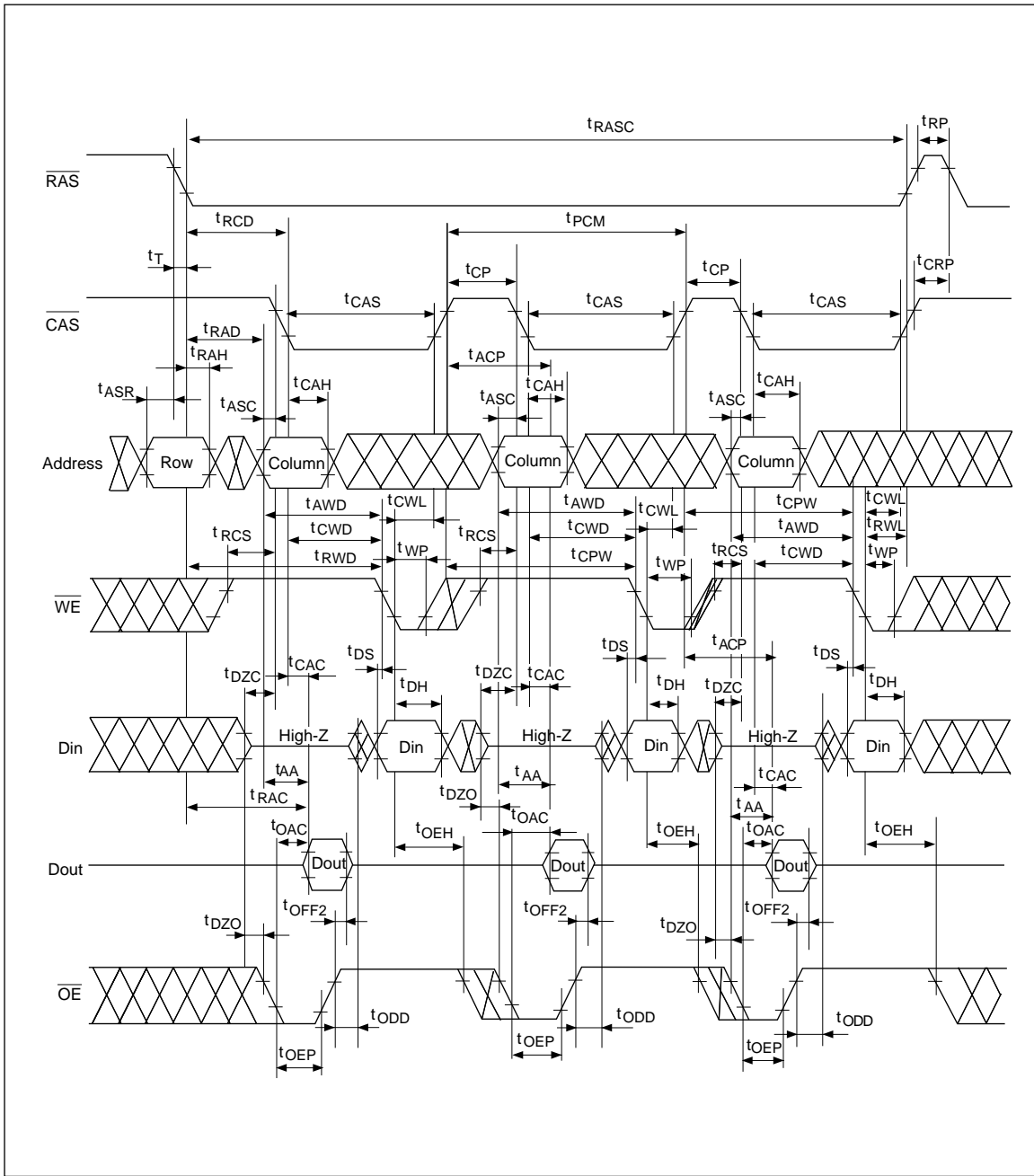


Fast Page Mode Delayed Write Cycle



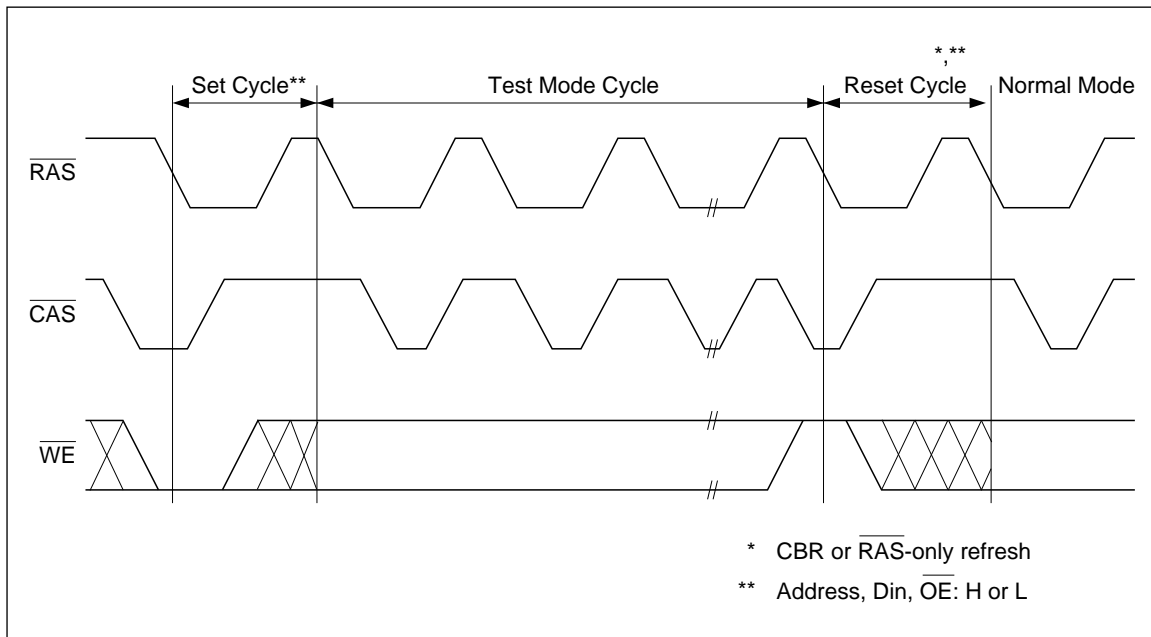
HM514400B/BL, HM514400C/CL Series

Fast Page Mode Read-Modify-Write Cycle



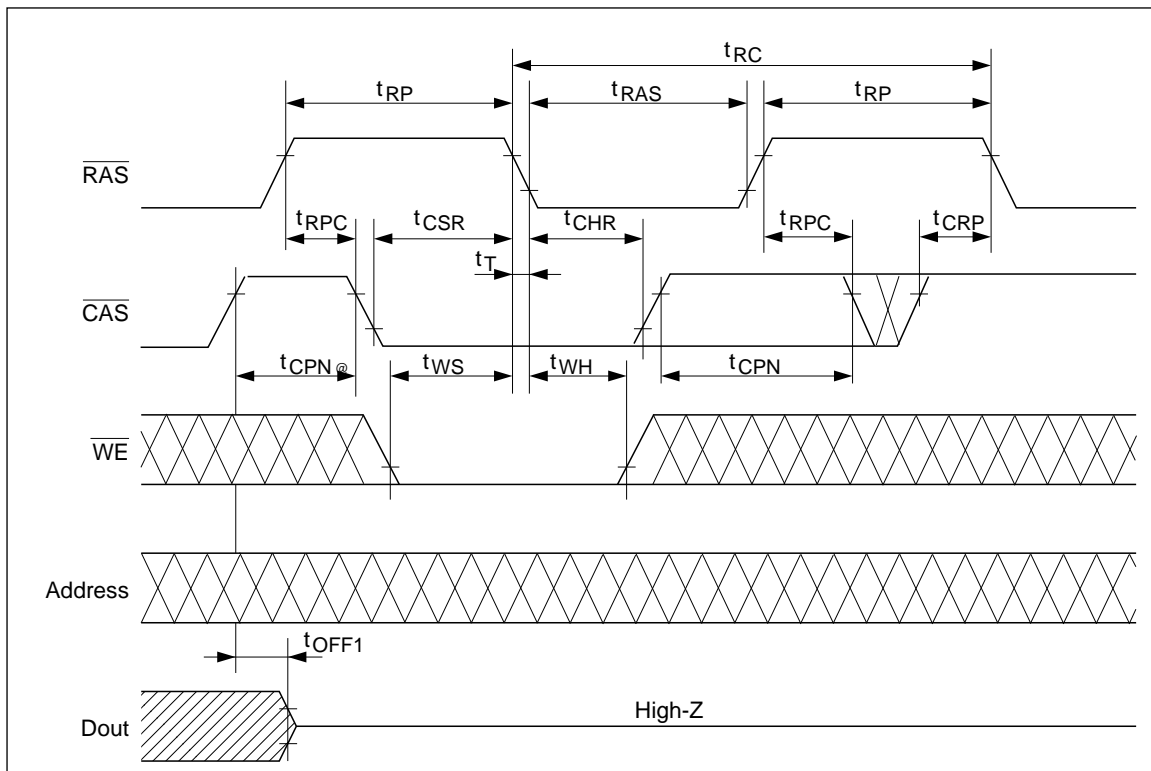
HM514400B/BL, HM514400C/CL Series

Test Mode Cycle



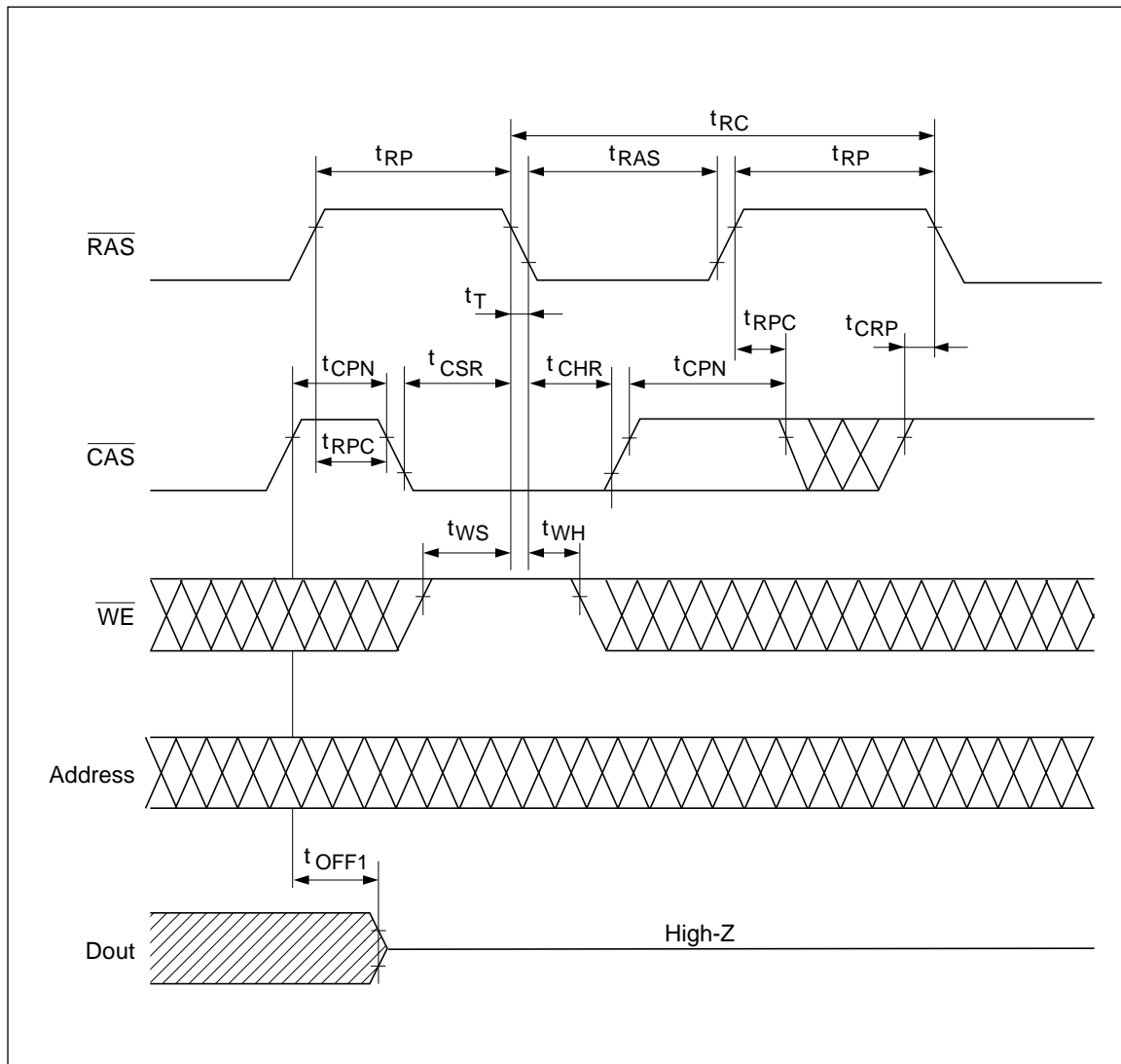
Test Mode Set Cycle

$\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -Before $\overline{\text{RAS}}$ -Refresh Cycle

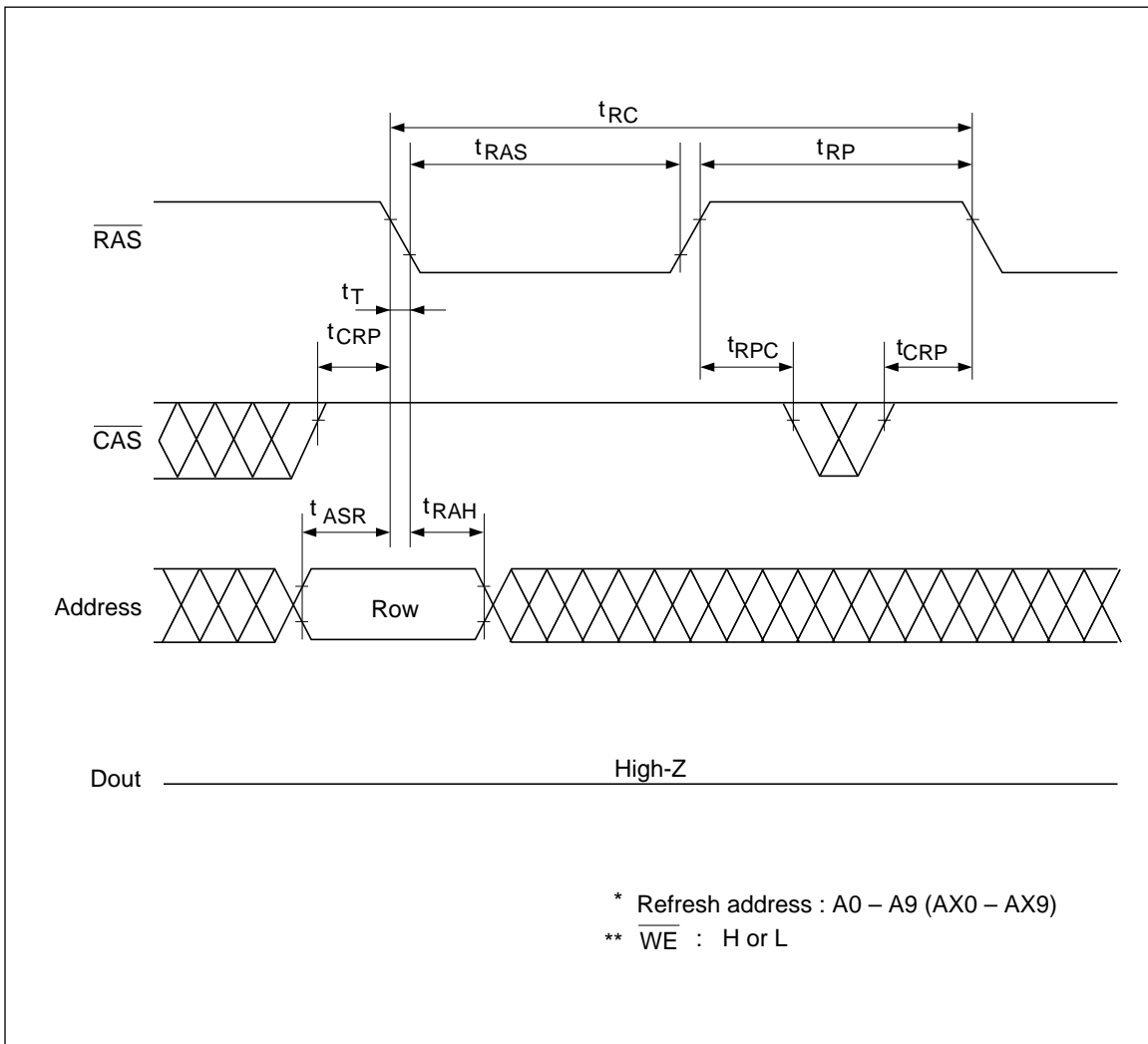


HM514400B/BL, HM514400C/CL Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

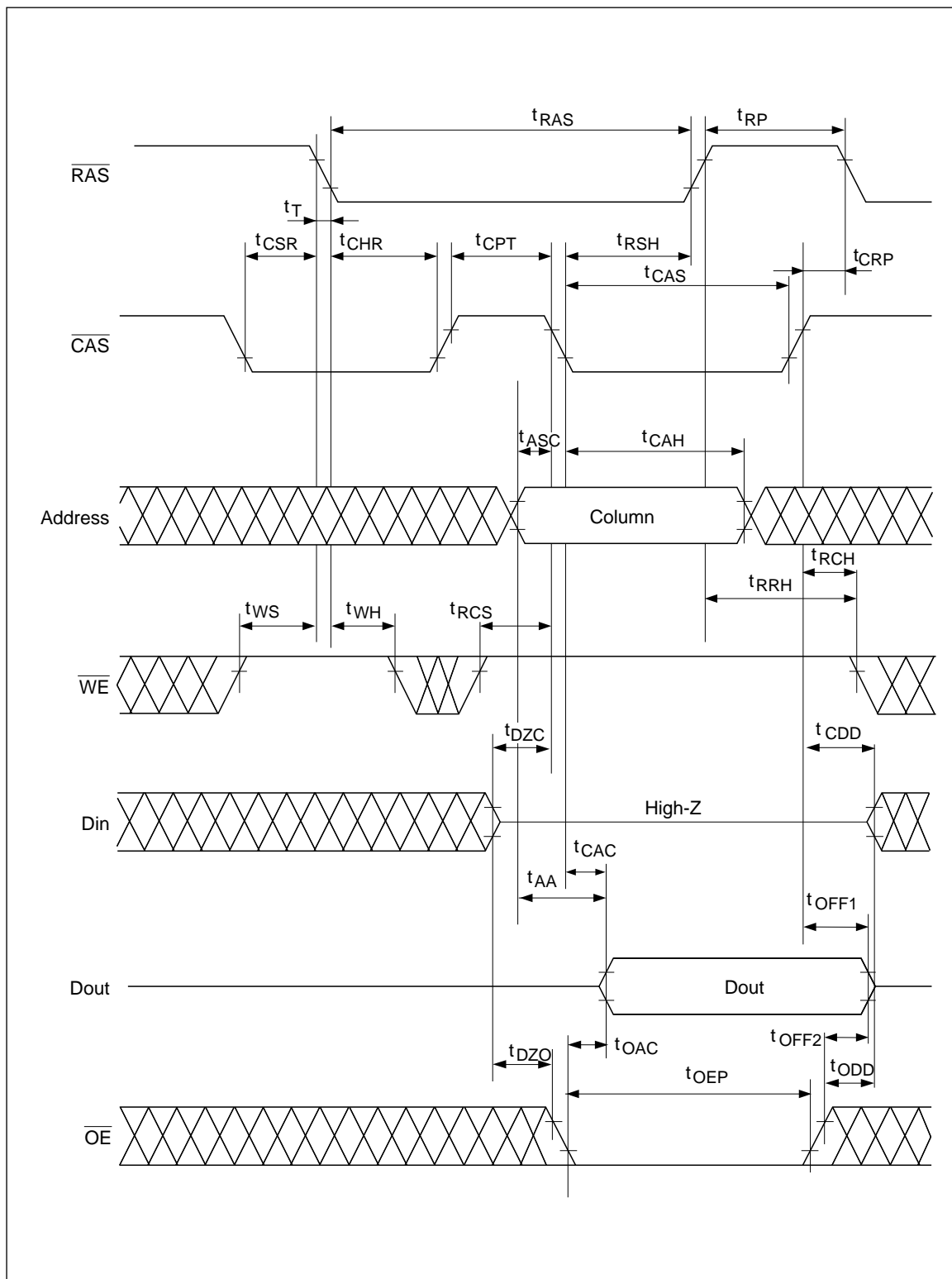


$\overline{\text{RAS}}$ -Only Refresh Cycle



HM514400B/BL, HM514400C/CL Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Counter Check Cycle (Read)



HM514400B/BL, HM514400C/CL Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Counter Check Cycle (Write)

