TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO IC

TLP553

Low input current line receiver

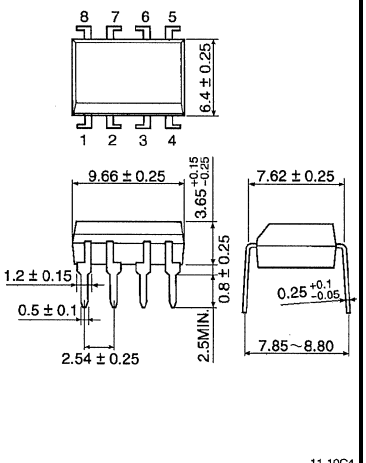
Telephone ring detector

Current loop receiver

Interfaces for computer, measurement equipment and control equipment

Data transfer between circuits of different potentials

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11-10C4

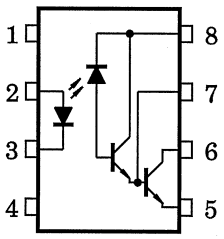
Weight: 0.54 g (typ)

TLP553 is a darlington 8-pin DIP photocoupler, which consists of a GaAℓAs IRED LED, and a photodiode and a high-gain transistor integrated into a detector chip.

As it uses a high-speed, high-gain detector element, TLP553 is ideal for applications which require low-input current and high-speed data transmission.

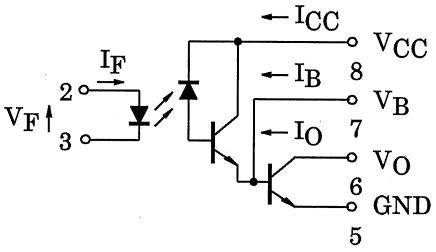
- Current transfer ratio: 400% (min) @I_F = 0.5 mA
- Operating temperature: 0 to 70°C (guaranteed)
- Switching speed: t_{pHL} = 2 µs, t_{pLH} = 4 µs (typ.) @R_L = 4.7 kΩ, I_F = 0.5 mA
- Isolation voltage: 2500 V_{rms} (min)
- UL recognized: UL1577, file no. E67349

Pin Configurations



1: N.C. 5: GND(emitter)
2: Anode 6: V_O(collector)
3: Cathode 7: Base
4: N.C. 8: V_{CC}

Schematic



Absolute Maximum Rating (Ta = 25°C)

Characteristics			Symbol	Rating	Unit
LED	Forward current	(Note 1)	I_F	20	mA
	Pulse forward current	(Note 2)	I_{FP}	40	mA
	Peak transient forward current	(Note 3)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Diode power dissipation	(Note 4)	P_D	35	mW
Detector	Output current	(Note 5)	I_O	60	mA
	Output voltage		V_O	−0.5 to 18	V
	Supply voltage		V_{CC}	−0.5 to 18	V
	Emitter-base voltage		V_{EB}	0.5	V
	Output power dissipation	(Note 6)	P_O	100	mW
Storage temperature range			T_{stg}	−55 to 125	°C
Operating temperature range			T_{opr}	−40 to 85	°C
Lead solder temperature	(10 s)	(Note 7)	T_{sol}	260	°C
Isolation voltage		(Note 8)	BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. application of high temperature/current/voltage and a significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Derate 0.27 mA/°C above 50°C.

Note 2: 50% duty cycle, 1 ms pulse width.

Note 3: Pulse width ≤ 1 μs, 300 pps.

Note 4: Derate 0.47 mW/°C above 50°C.

Note 5: Derate 0.6 mA/°C above 25°C.

Note 6: Derate 1 mW/°C above 25°C.

Note 7: Soldering is performed 2mm from the bottom of the package.

Note 8: AC, 1min, R.H. ≤ 60%

Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	—	—	16	V
Input current	I_F	0.5	—	15	mA
Output current	I_O	—	—	30	mA
Operating temperature	T_{opr}	0	—	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

Electrical Characteristics (Unless otherwise specified Ta = 0 to 70°C)

Characteristics	Symbol	Test Conditions	Min	Typ*	Max	Unit
Forward voltage	V_F	I_F = 1.6 mA, Ta = 25°C	—	1.55	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta Ta$	I_F = 1.6 mA	—	−2.1	—	mV/°C
Input reverse current	I_R	V_R = 5 V, Ta = 25°C	—	—	10	μA
Input capacitance	C_T	V_F = 0 V, f = 1 MHz, Ta = 25°C	—	45	—	pF
"H" level output current	I_{OH}	V_F = 0.8 V, V_O = V_{CC} = 18 V	—	0.1	100	μA
"H" level supply current	I_{CCH}	V_{CC} = 5 V, I_F = 0 mA V_O = Open	—	10	—	nA
"L" level supply current	I_{CCL}	V_{CC} = 5 V, I_F = 1.6 mA V_O = Open	—	0.3	—	mA
Current transfer ratio	I_O / I_F	I_F = 0.5 mA, V_O = 0.4 V V_{CC} = 4.5 V	400	1000	—	%
		I_F = 1.6 mA, V_O = 0.4 V V_{CC} = 4.5 V	500	900	—	
"L" level output voltage	V_{OL}	I_F = 1.6 mA, I_O = 6.4 mA V_{CC} = 4.5 V	—	0.1	0.4	V
		I_F = 5 mA, I_O = 15 mA V_{CC} = 4.5 V	—	0.1	0.4	
		I_F = 12 mA, I_O = 24 mA V_{CC} = 4.5 V	—	0.2	0.4	
Isolation resistance	R_S	V_S = 500 V, R.H. ≤ 60% Ta = 25°C (Note 9)	5×10^{10}	10^{14}	—	Ω
Input to output capacitance	C_S	V = 0 V, f = 1 MHz, Ta = 25°C (Note 9)	—	0.6	—	pF

* : All typical values are at Ta = 25°C.

Note 9: Device considered a 2-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

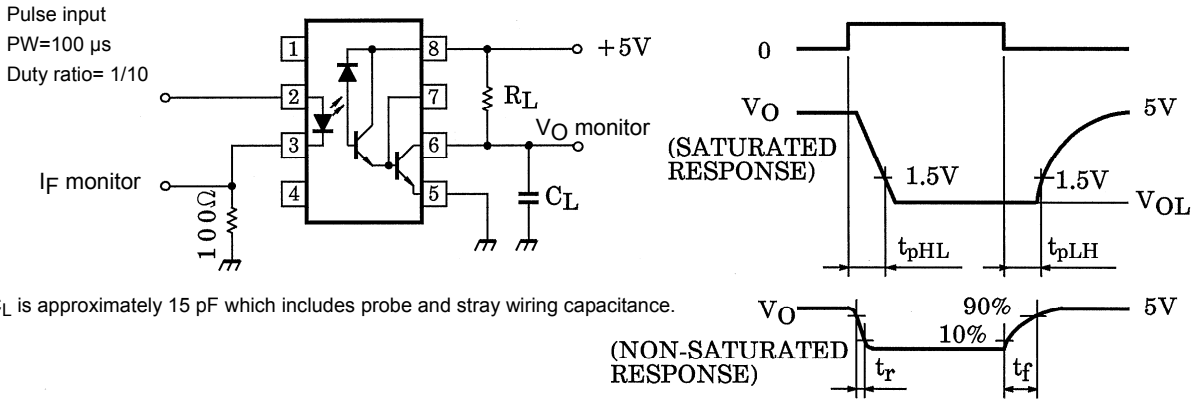
Switching Characteristics (Ta = 25°C, V_{CC} = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Propagation delay time (H→L)	t_{pHL}	1	I_F = 0.5 mA, R_L = 4.7 kΩ	—	2	25	μs
			I_F = 12 mA, R_L = 270 Ω	—	0.3	1	
			I_F = 1.6 mA, R_L = 2.2 kΩ	—	—	—	
Propagation delay time (L→H)	t_{pLH}		I_F = 0.5 mA, R_L = 4.7 kΩ	—	4	60	μs
			I_F = 12 mA, R_L = 270 Ω	—	1	7	
			I_F = 1.6 mA, R_L = 2.2 kΩ	—	—	—	
Common mode transient immunity at HIGH level output	CM_H	2	I_F = 0 mA, R_L = 2.2 kΩ (Note 10) V_{CM} = 400 V $V_{O\ (min)}$ = 2 V	—	500	—	V/μs
Common mode transient immunity at LOW level output	CM_L		I_F = 1.6 mA, R_L = 2.2 kΩ (Note 11) V_{CM} = 400 V $V_{O\ (max)}$ = 0.8 V	—	−500	—	V/μs

Note 10: CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e., V_O > 2.0 V). Measured in volts per microsecond (V / μs).

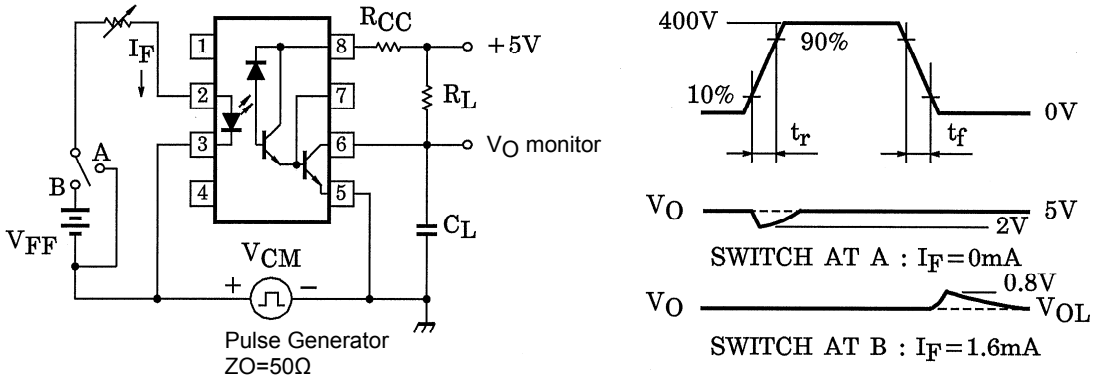
Note 11: CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_O < 0.8 V). Measured in volts per microsecond (V / μs).

Test Circuit 1: t_{pHL}, t_{pLH} Test Circuit



C_L is approximately 15 pF which includes probe and stray wiring capacitance.

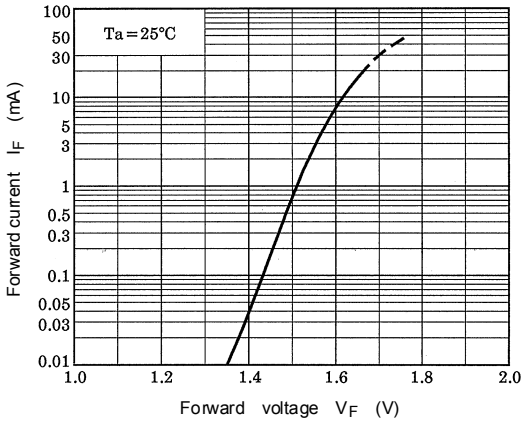
Test Circuit 2: Common Mode Noise Immunity Test Circuit



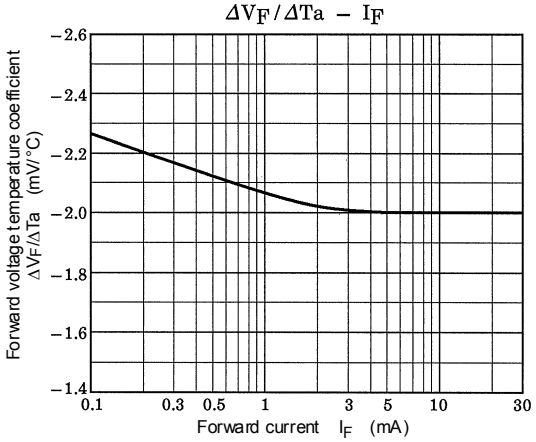
$$CM_H = \frac{320(V)}{t_r(\mu s)}, \quad CM_L = \frac{320(V)}{t_f(\mu s)}$$

C_L is approximately 15 pF which includes probe and stray wiring capacitance.

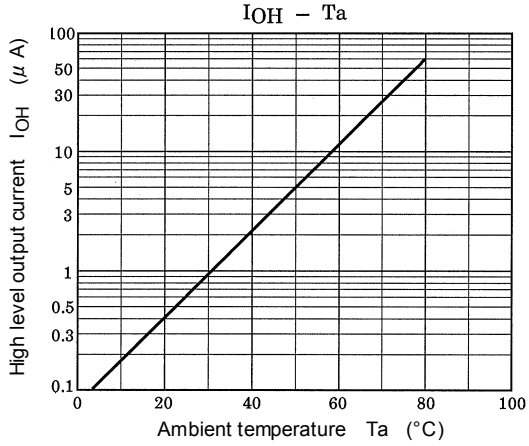
$I_F - V_F$



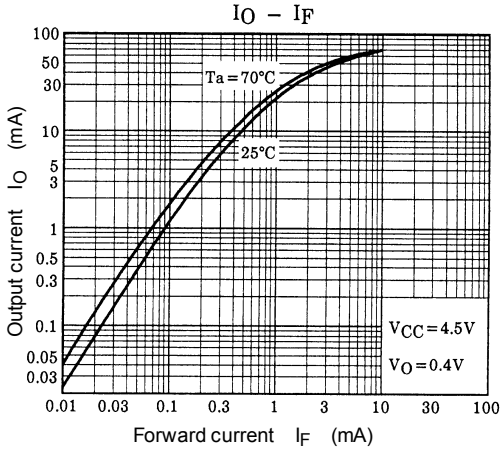
$\Delta V_F / \Delta Ta - I_F$



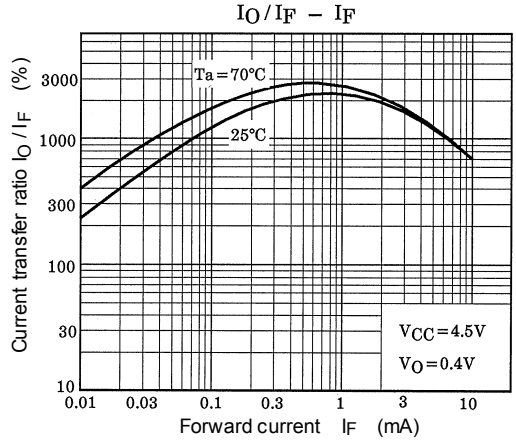
$I_{OH} - Ta$



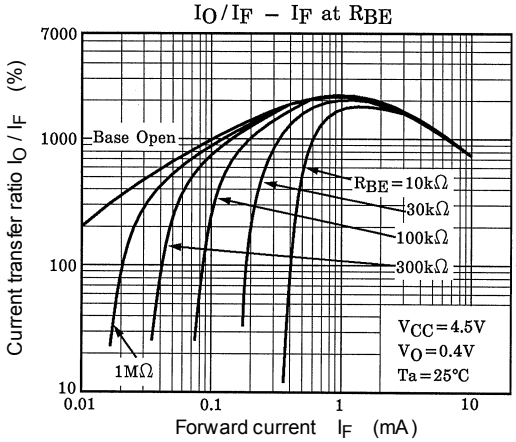
$I_O - I_F$



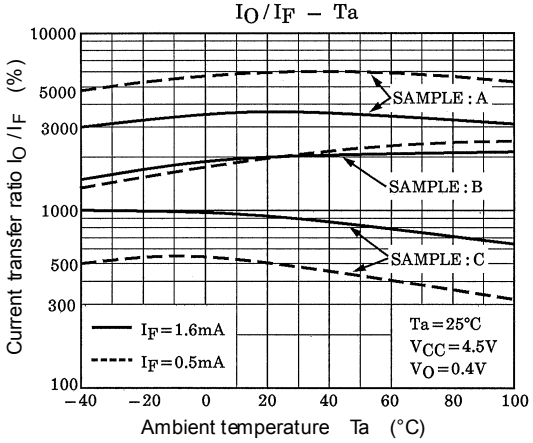
$I_O / I_F - I_F$



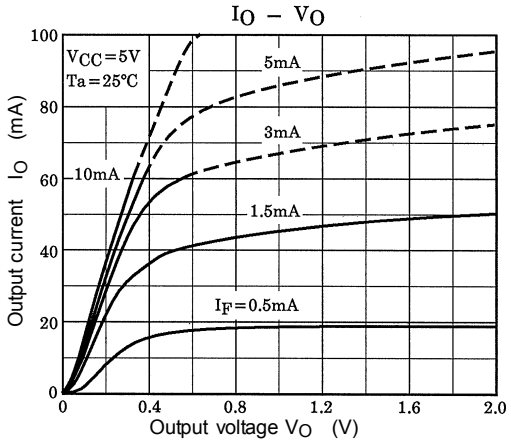
$I_O / I_F - I_F$ at R_{BE}



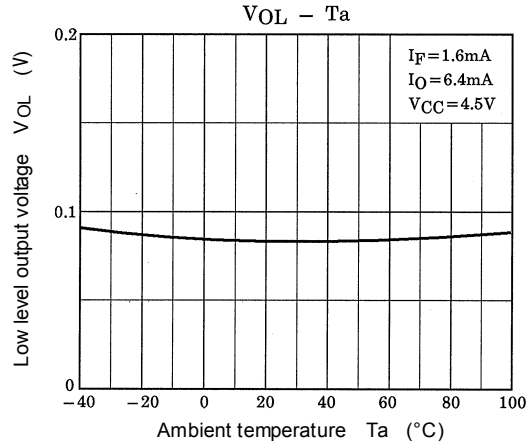
I_O / I_F – Ta



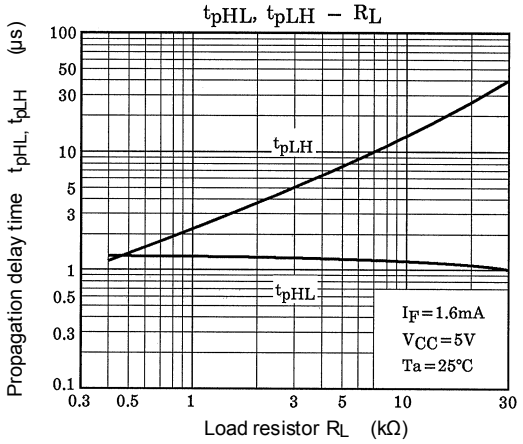
I_O – V_O



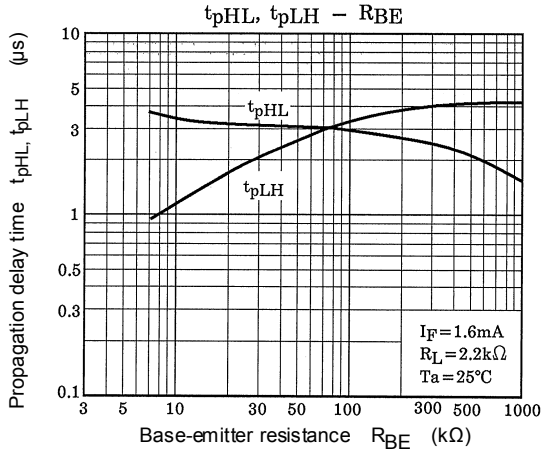
V_{OL} – Ta



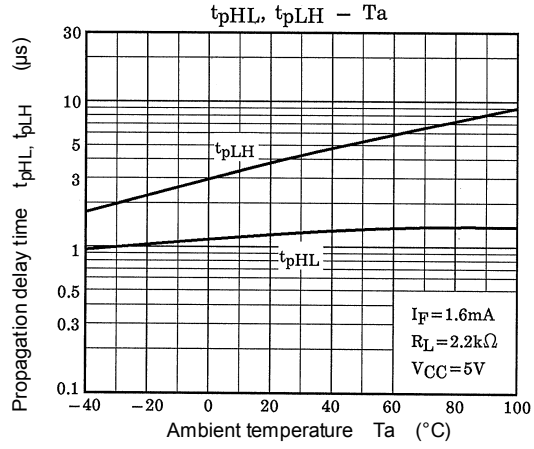
t_{pHL}, t_{pLH} – R_L



t_{pHL}, t_{pLH} – R_{BE}



t_{pHL}, t_{pLH} – Ta



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