

DESCRIPTION

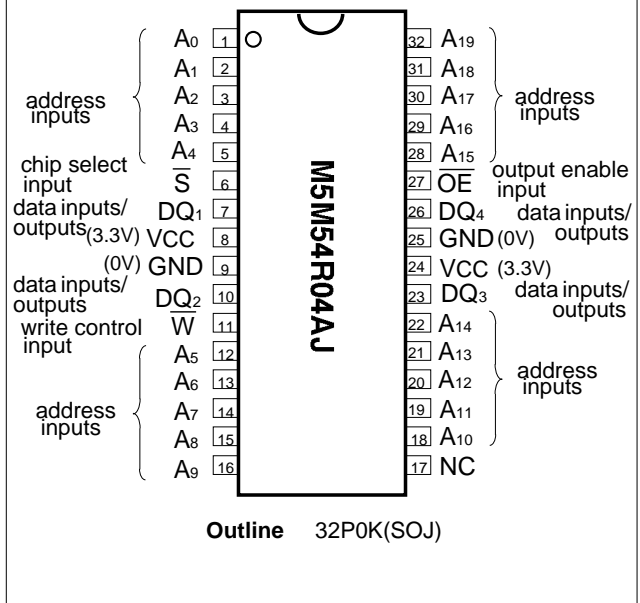
The M5M54R04AJ is a family of 1048576-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

- Fast access time M5M54R04AJ-10 ... 10ns(max)
M5M54R04AJ-12 ... 12ns(max)
M5M54R04AJ-15 ... 15ns(max)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by S
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PIN CONFIGURATION (TOP VIEW)



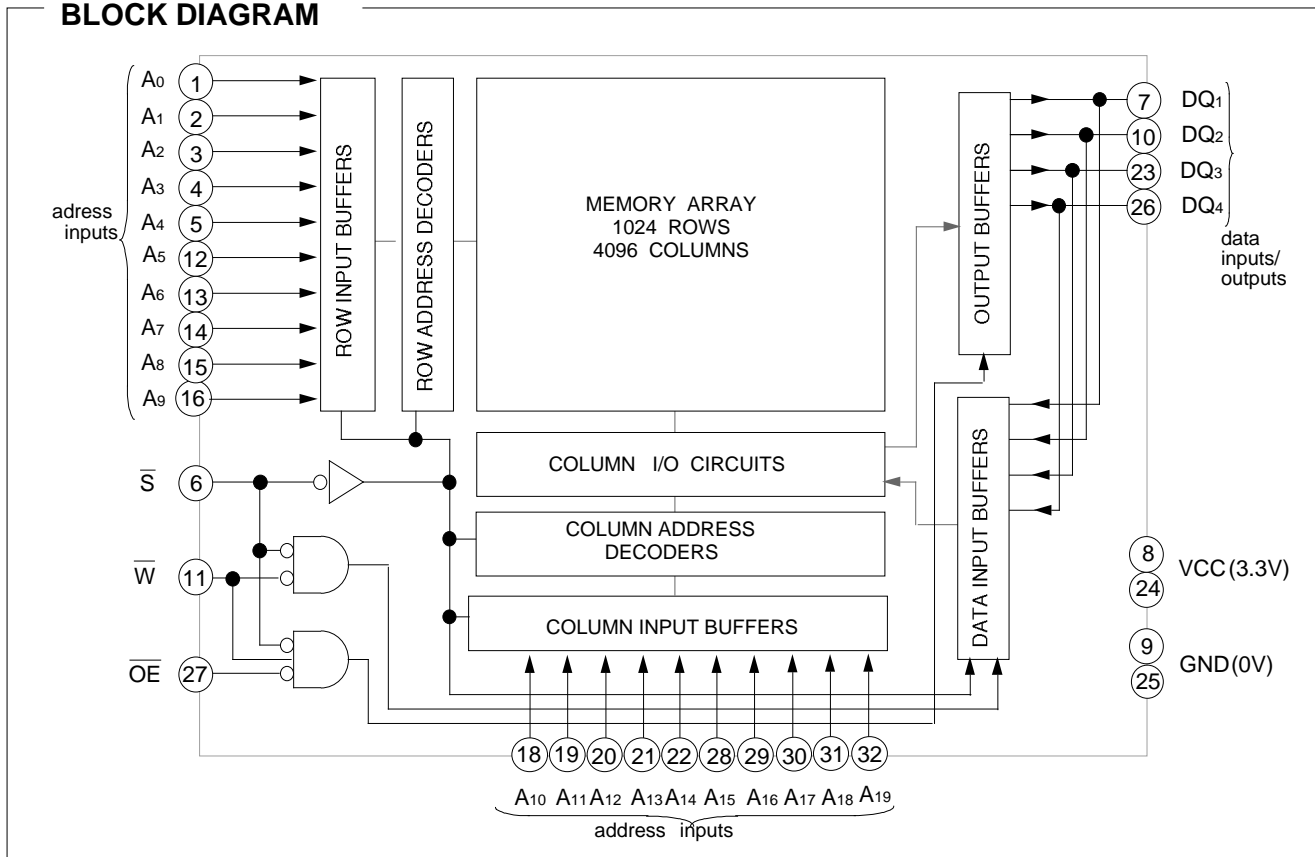
APPLICATION

High-speed memory units

PACKAGE

M5M54R04AJ : 32pin 400mil SOJ

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M54R04AJ is determined by a combination of the device control inputs \bar{S} , \bar{W} and \bar{OE} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S} . The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of \bar{W} or \bar{S} , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high impedance state, and the data bus

contention problem in the write cycle is eliminated.

A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S} are in an active state ($\bar{S}=\text{L}$).

When setting \bar{S} at high level, the chip is in a non-selectable mode in which both reading and writing are disable. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S} .

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced extremely. The access time from \bar{S} is equivalent to the address access time.

FUNCTION TABLE

\bar{S}	\bar{W}	\bar{OE}	Mode	DQ	I _{cc}
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 2.0* ~ 4.6	V
V _I	Input voltage		- 2.0* ~ V _{CC} +0.5	V
V _O	Output voltage		- 2.0* ~ V _{CC}	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg(bias)}	Storage temperature(bias)		- 10 ~ 85	°C
T _{stg}	Storage temperature		- 65 ~ 150	°C

* Pulse width_3ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{cc}=3.3V ^{+10%}/_{-5%}, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min	Typ	Max		
V _{IH}	High-level input voltage		2.0		V _{cc} +0.3	V	
V _{IL}	Low-level input voltage				0.8	V	
V _{OH}	High-level output voltage	I _{OH} = - 4mA	2.4			V	
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V	
I _I	Input current	V _I = 0 ~ V _{cc}			2	uA	
I _{OZ}	Output current in off-state	V _I (\bar{S})=V _{IH} V _I O= 0 ~ V _{cc}			2	uA	
I _{cc1}	Active supply current (TTL level)	V _I (\bar{S})=V _{IL} other inpus=V _{IH} or V _{IL} Output-open(duty 100%)	AC	10ns cycle		190	mA
				12ns cycle		180	
				15ns cycle		160	
			DC			90	
I _{cc2}	Stand by current (TTL level)	V _I (\bar{S})=V _{IH}	AC	10ns cycle		90	mA
				12ns cycle		70	
				15ns cycle		60	
			DC			40	
I _{cc3}	Stand by current	V _I (\bar{S})=V _{cc} -0.2V other inputs V _I 0.2V or V _I V _{cc} - 0.2V			10	mA	

Note 1: Direction for current flowing into an IC is positive (no mark).

CAPACITANCE ($T_a=0\sim 70^\circ\text{C}$, $V_{cc}=3.3\text{V}^{+10\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C _I	Input capacitance	$V_I = \text{GND}, V_I = 25\text{mVrms}, f=1\text{MHz}$			7	pF
C _O	Output capacitance	$V_O = \text{GND}, V_O = 25\text{mVrms}, f=1\text{MHz}$			8	pF

Note 2: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, $V_{cc}=3.3\text{V}^{+10\%}_{-5\%}$, unless otherwise noted)

(1) MEASUREMENT CONDITION

Input pulse levels $V_{IH}=3.0\text{V}, V_{IL}=0.0\text{V}$
 Input rise and fall time 3ns
 Input timing reference levels $V_{IH}=1.5\text{V}, V_{IL}=1.5\text{V}$
 Output timing reference levels $V_{OH}=1.5\text{V}, V_{OL}=1.5\text{V}$
 Output loads Fig.1, Fig.2

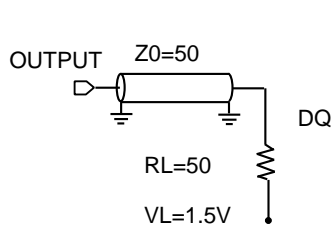


Fig.1 Output load

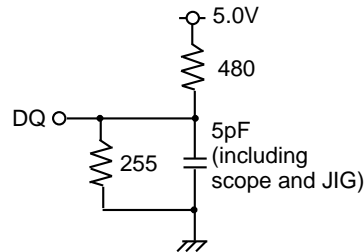


Fig.2 Output load for t_{en}, t_{dis}

MITSUBISHI LSIs
M5M54R04AJ-10,-12,-15

4194304-BIT (1048576-WORD BY 4-BIT) CMOS STATIC RAM

(2)READ CYCLE

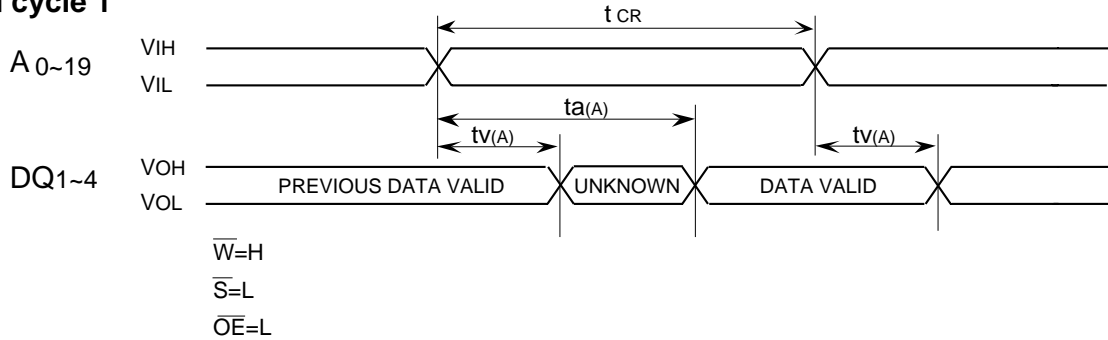
Symbol	Parameter	Limits						Unit
		M5M54R04AJ-10		M5M54R04AJ-12		M5M54R04AJ-15		
		Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	10		12		15		ns
t _{a(A)}	Address access time		10		12		15	ns
t _{a(S)}	Chip select access time		10		12		15	ns
t _{a(OE)}	Output enable access time		5		6		7	ns
t _{dis(S)}	Output disable time after \overline{S} high	0	5	0	6	0	7	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	5	0	6	0	7	ns
t _{en(S)}	Output enable time after \overline{S} low	2		3		3		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		1		1		ns
t _{v(A)}	Data valid time after address change	2		3		3		ns
t _{PU}	Power-up time after chip selection	0		0		0		ns
t _{PD}	Power-down time after chip selection		10		12		15	ns

(3)WRITE CYCLE

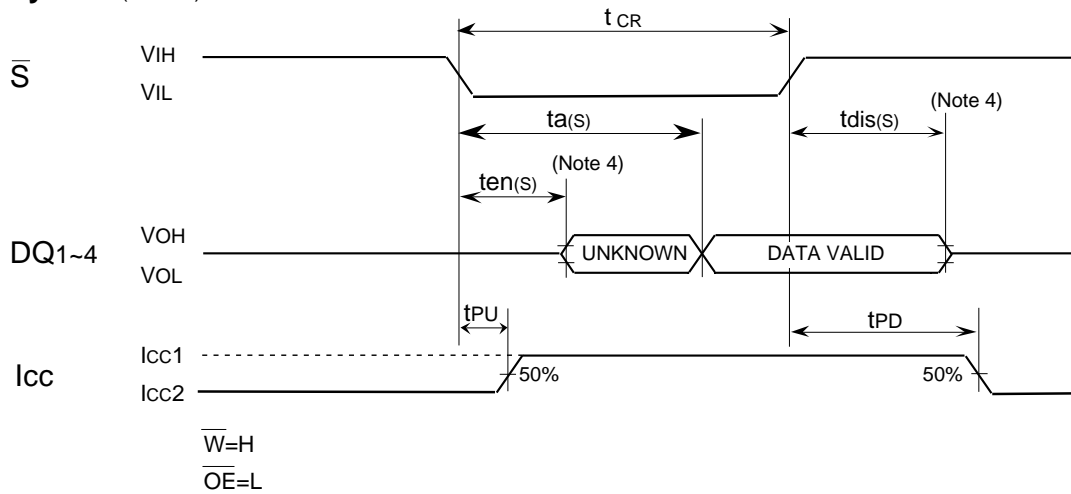
Symbol	Parameter	Limits						Unit
		M5M54R04AJ-10		M5M54R04AJ-12		M5M54R04AJ-15		
		Min	Max	Min	Max	Min	Max	
t _{CW}	Write cycle time	10		12		15		ns
t _{w(W)}	Write pulse width (\overline{OE} low)	10		12		15		ns
t _{w(W)}	Write pulse width(\overline{OE} high)	8		10		10		ns
t _{su(A)1}	Address setup time(\overline{W})	0		0		0		ns
t _{su(A)2}	Address setup time(\overline{S})	0		0		0		ns
t _{su(S)}	Chip select setup time	8		10		10		ns
t _{su(D)}	Data setup time	5		6		7		ns
t _{h(D)}	Data hold time	0		0		0		ns
t _{rec(W)}	Write recovery time	1		1		1		ns
t _{dis(W)}	Output disable time after \overline{W} low	0	5	0	6	0	7	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	5	0	6	0	7	ns
t _{en(W)}	Output enable time after \overline{W} high	0		0		0		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		0		0		ns
t _{su(A-\overline{W})}	Address to \overline{W} High	8		10		10		ns

(4)TIMING DIAGRAMS

Read cycle 1



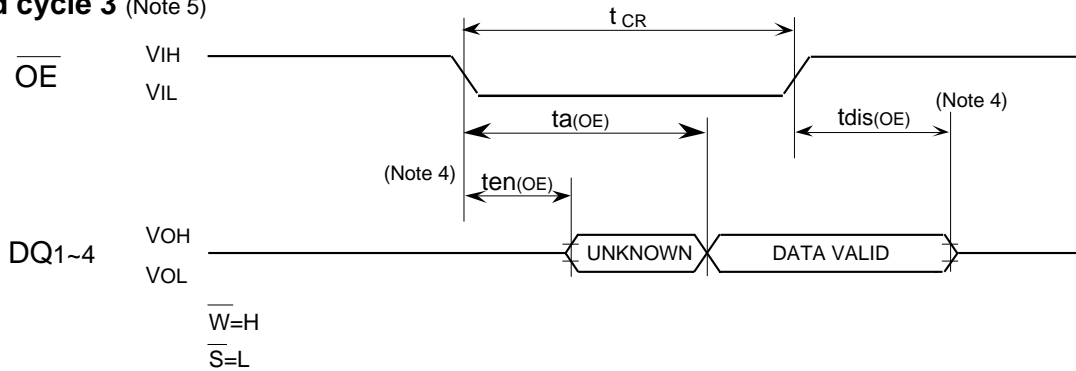
Read cycle 2 (Note 3)



Note 3. Addresses valid prior to or coincident with \overline{S} transition low.

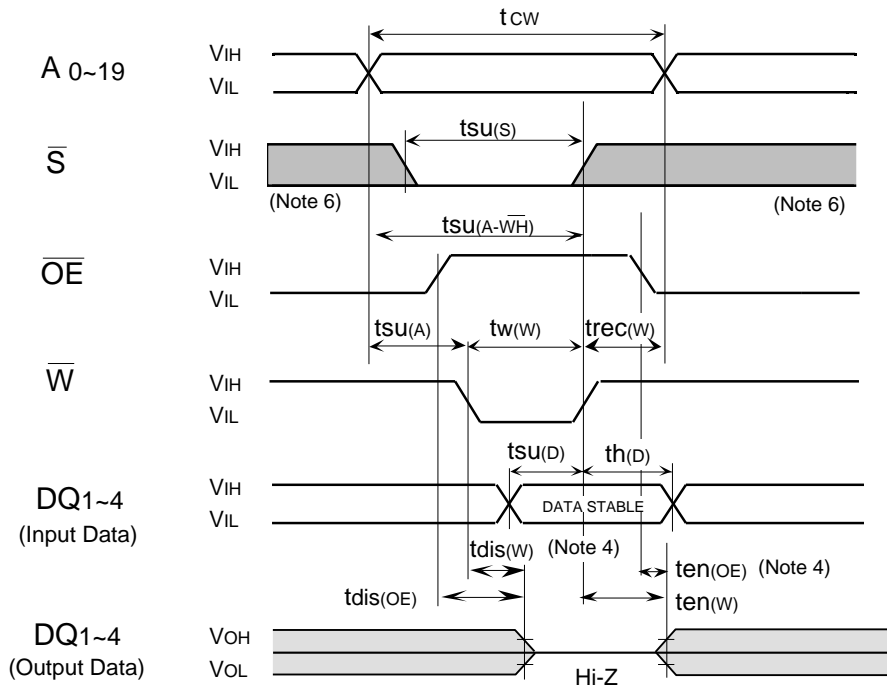
4. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)

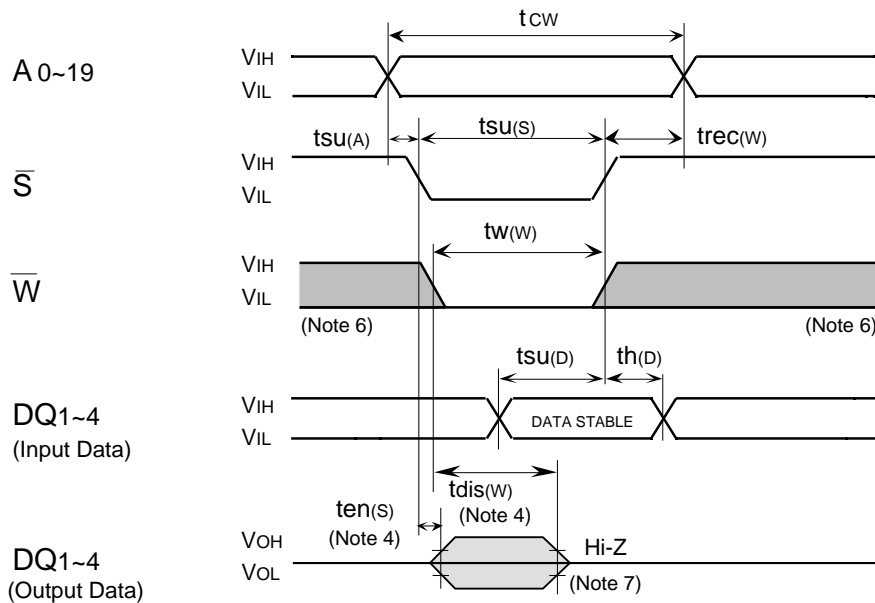


Note 5. Addresses and \overline{S} valid prior to \overline{OE} transition low by $(t_{a(A)} - t_{a(OE)})$, $(t_{a(S)} - t_{a(OE)})$

Write cycle (\overline{W} control mode)



Write cycle (\overline{S} control)



Note 6: Hatching indicates the state is don't care.

7: When the falling edge of \overline{W} is simultaneous or prior to the falling edge of \overline{S} , the output is maintained in the high impedance.

8: t_{en} , t_{dis} are periodically sampled and are not 100% tested.