MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC138

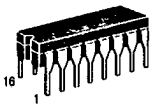
1-of-8 Decoder/Demultiplexer

High-Performance Silicon-Gate CMOS

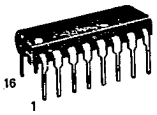
The MC54/74HC138 is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138 decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06

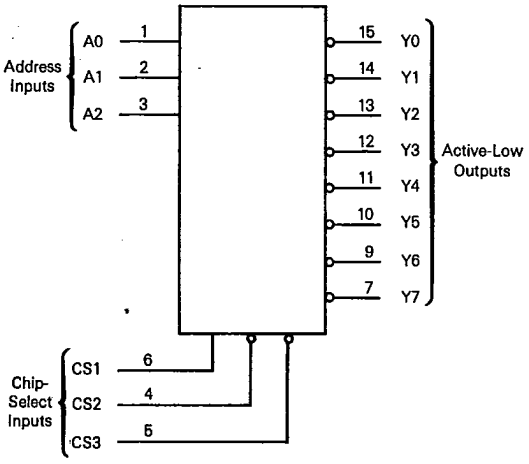
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

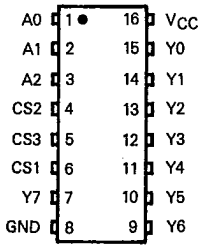
T_A = −55° to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 16 = V_{CC}
Pin 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	V_{CC}=2.0 V	0	1000	ns
		V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 5.2$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PHL}		2.0	200	250	300	
		4.5	40	50	60	
		6.0	34	43	51	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PLH}	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 55	pF

SWITCHING WAVEFORMS

FIGURE 1

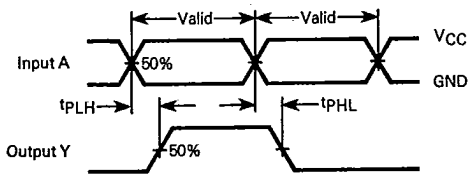


FIGURE 2

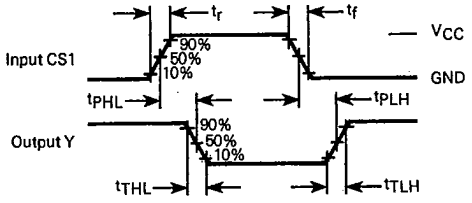


FIGURE 3

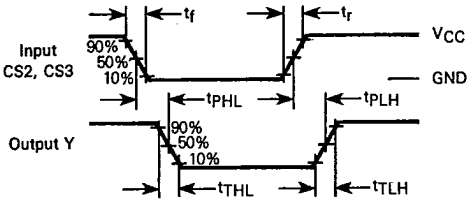
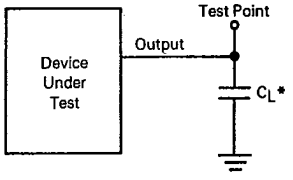


FIGURE 4 — TEST CIRCUIT



* Includes all probe and jig capacitance.

MC54/74HC138

T-66-21-55

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

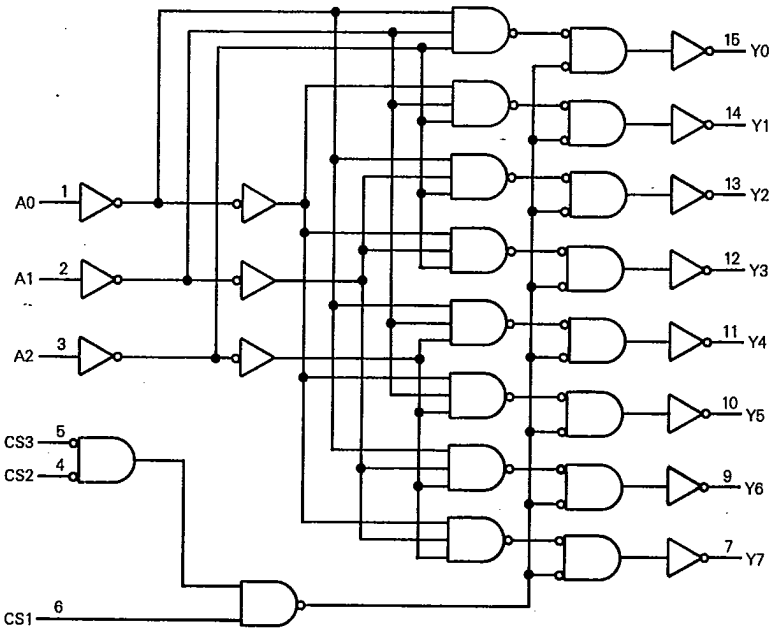
CONTROL INPUTS

CS1, CS2, CS3 (PINS 6, 4, 5) — Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

OUTPUTS

Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) — Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

EXPANDED LOGIC DIAGRAM



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