

GENERAL DESCRIPTION

The EM92600/1A series are developed for 46/49 MHz of 10 channels band frequency of cordless telephone which is used in U.S.A.. These devices are dual phase-locked loop frequency synthesizers contained ROM counters for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are share by the receive and transmit circuits.

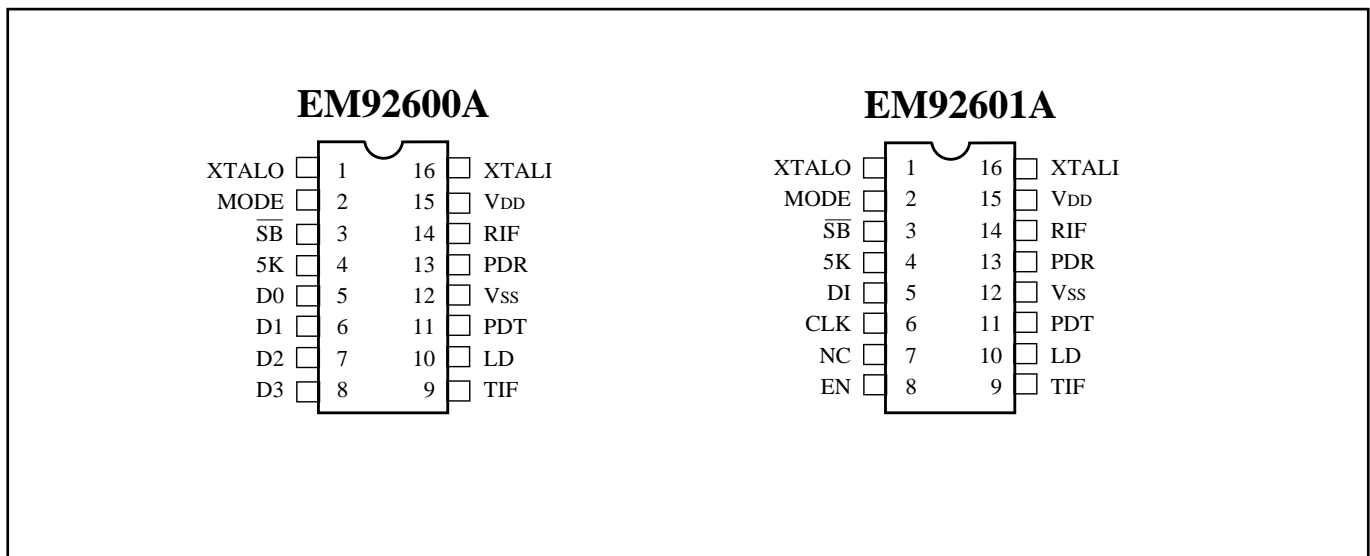
Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, 5KHz tone output . The EM92601A is designed for easy MPU interface. It provides the same features as the EM92600A , but accepts channel programming via a clocked, serial input instead of parallel BCD inputs. The EM92600A is selected channels via mechanical switches of parallel BCD input.

FEATURES

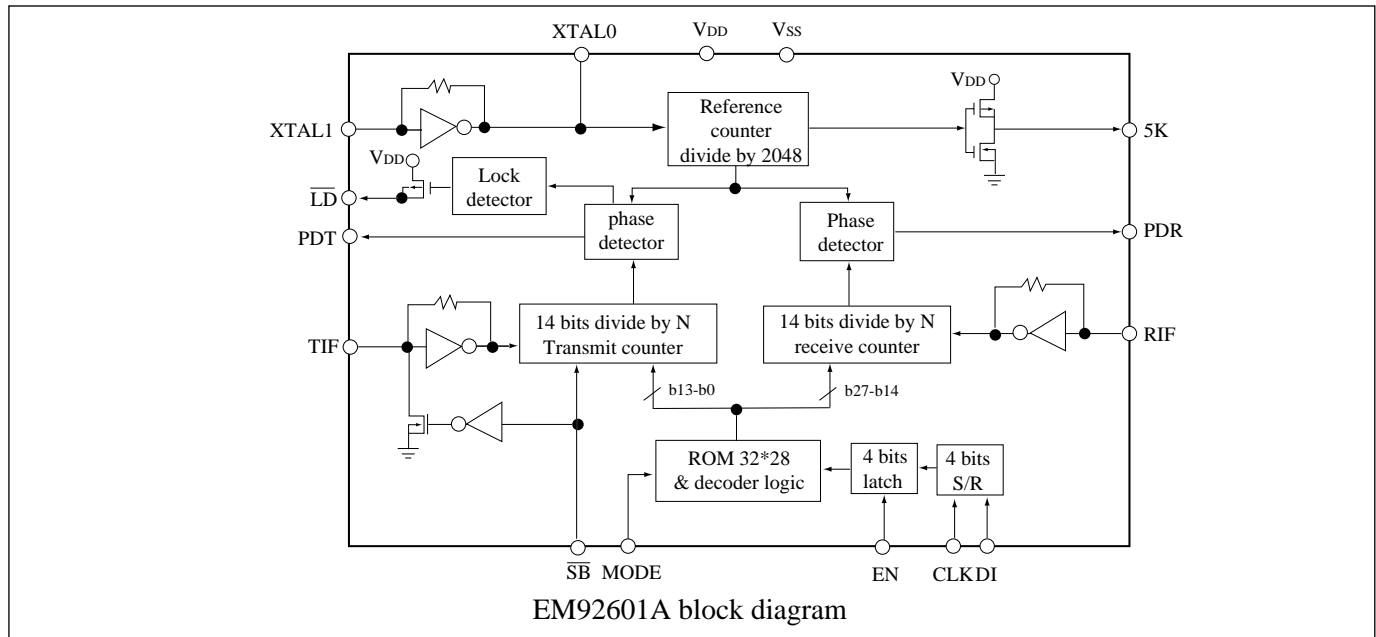
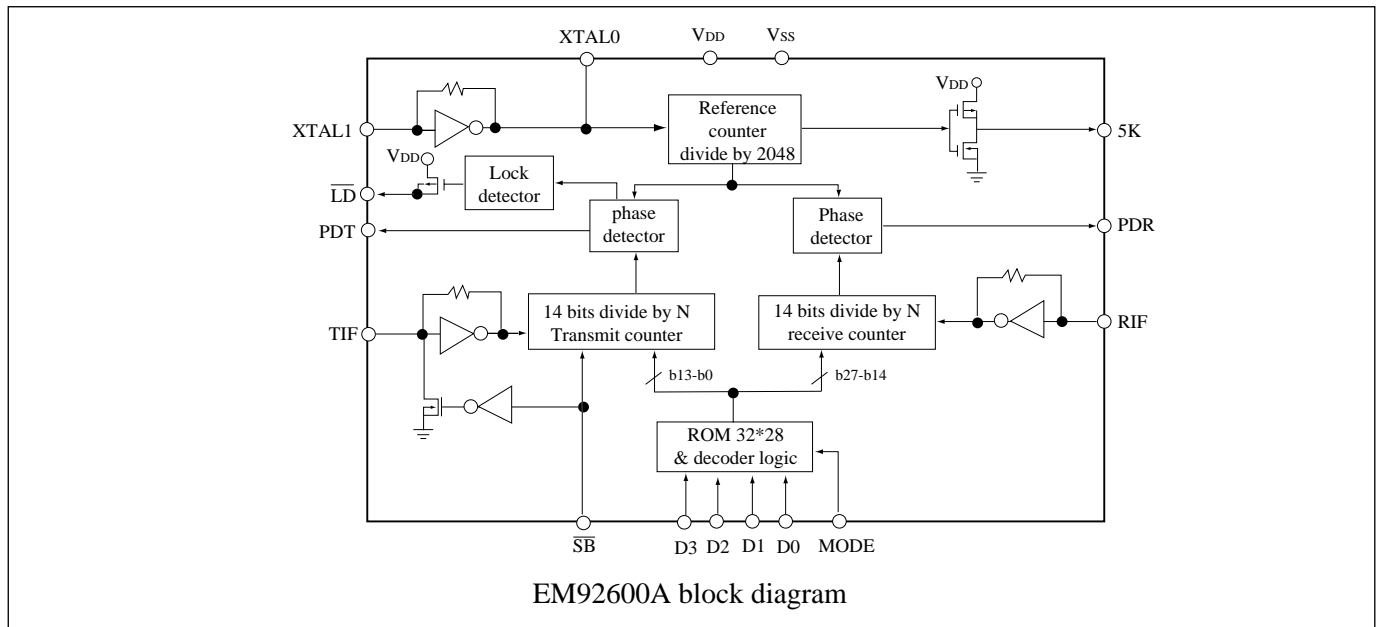
- Include oscillation circuit with external X-TAL (10.240 MHz).
- Unlock detector.
- 5KHz output for guard tone.
- Standby mode for power saving.
- 2.5 to 5.5V supply range.
- Baseset/Handset changeable.
- Available in 16 pin DIP or SOP.
- SERIES

Part Number	Package	Channel Selection
EM92600AP	DIP	parallel
EM92600AM	SOP	parallel
EM92601AP	DIP	serial
EM92601AM	SOP	serial

PIN ASSIGNMENTS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	Pin No.	Function
XTALO	O	This output generates reference frequency when it is connected to pin 16 with external OSC of which frequency is 10.240MHz
MODE	I	Base/remote changing. Internal pull down. V_{DD} =base, V_{SS} =remote.
\overline{SB}	I	The standby pin is used to save power when no transmit. Internal pull down. High: transmit and receive active Low: receive acts only
5K	O	The signal derived from the reference oscillator. 5KHz output.

* This specification are subject to be changed without notice.

Symbol	I/O	Function
D0	I	The channel selected pin. LSB.(internal pull down)
D1	I	The channel selected pin. (internal pull down)
D2	I	The channel selected pin. (internal pull down)
D3	I	The channel selected pin. MSB.(internal pull down)
Di	I	The serial input data pin.
CLK	I	Clock input. Each low to high transition of the clock shifts one bit of data into the on-chip shift register.
NC	-	Not connect.
EN	I	The enable pin controls the data transfer from the shift register to the 4-bit latch. A low to high transition latches the data.
TIF	I	Input to programmable divider of Tx. AC coupling with VCO. Min input voltage is 200mVpp.
$\overline{\text{LD}}$	O	Unlock detector output. V_{DD} level: unlock.
PDT	O	Phase detector output for Tx. PDT detects the phase error from Tx PLL and its output is connected to external low pass filter.
V_{SS}	-	Ground.
PDR	O	Phase detector output for Rx. PDR detects the phase error from Rx PLL and its output is connected to external low pass filter.
RIF	I	Input of programmable divider for Rx.AC coupling with VCO. Min input voltage is 200mVpp.
V_{DD}	-	Power supply.
XTAL1	I	To connect crystal (10.240MHz) and capacitor.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DD}	DC supply voltage	-0.5 to +6	V
V_{IN}	Input voltage	-0.5 to $V_{\text{DD}}+0.5$	V
$I_{\text{IN}}, I_{\text{OUT}}$	DC current drain per pin	10.0	mA
$I_{\text{DD}}, I_{\text{SS}}$	DC current drain V_{DD} or V_{SS} pins	30.0	mA
T_{A}	Operating temperature range	-30 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	2.5	-	5.5	V	
Input voltage	V_{IL} V_{IH}	2.2	-	0.8	V	$V_{DD}=3\text{V}$
Output voltage	V_{OL} V_{OH}	2.95	-	0.05	V	$V_{DD}=3\text{V}$
Input low current	I_{IL}	-36 -0.06	- -		μA	$v_{IL}=0$ pin 16,14,9 pin 2~8
Input high current	I_{IH}		- -	36 120	μA	$v_{IH}=V_{DD}-0.5\text{V}$ pin 16,14,9 pin 2~8
Output current	I_{OH} I_{OL}	-0.2 0.2	- -		mA	$V_{OH}=2.6\text{V}$ $V_{OL}=0.4\text{V}$
Standby current	I_{DS}		-	1.5	mA	$V_{DD}=3\text{V}$, note1
Operating current (0.2Vp-p input at RIF,TIF)	I_{DO}		-	3.0	mA	$V_{DD}=3\text{V}$, note2
3-state leakage current	I_{OZ}		-	± 1	μA	$V_{DD}=5\text{V}$

Note 1: XTALin: 10.24MHz ; MODE: V_{DD} ; $\overline{\text{SB}}$: V_{SS} ; TIF=20MHz(200 mVp-p); RIF=40MHz(200 mVp-p); others are open.

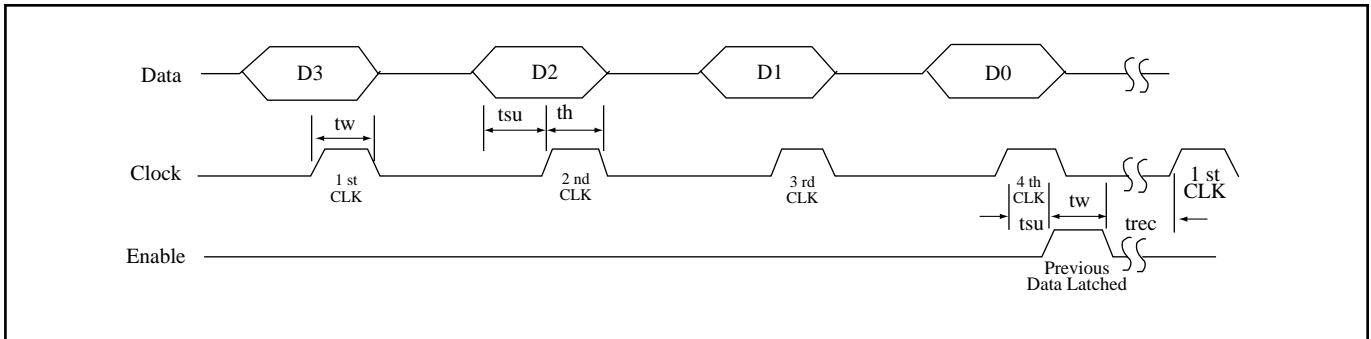
Note 2: XTALin: 10.24MHz ; MODE: V_{DD} ; $\overline{\text{SB}}$: V_{DD} ; TIF=20MHz(200 mVp-p); RIF=40MHz(200 mVp-p); others are open.

AC ELECTRICAL CHARACTERISTICS

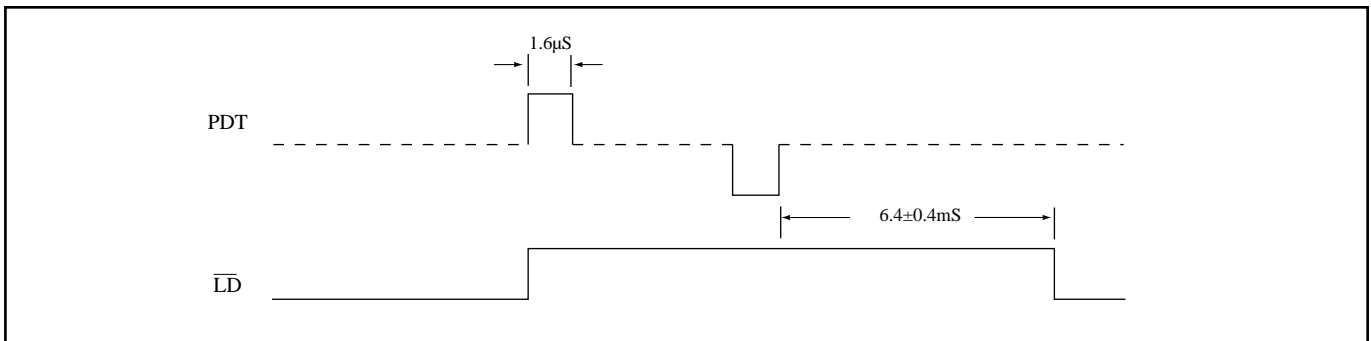
Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Output rise time	T_R			200	nS	$V_{DD}=3\text{V}$
Output fall time	T_F			200	nS	$V_{DD}=3\text{V}$
Input rise and fall time OSC in	T_R T_F			5	μS	XTAL1 $V_{DD}=3\text{V}$
Maximum frequency input =sine wave 0.2Vp-p	F_{MAX}			12 50 50	MHz	XTAL1 RIF ($V_{DD}=3\text{V}$) TIF
Setup time data to clock Enable to clock	T_{SU}	100 200			nS	EM92601A only
Hold time clock to data	T_H	80			nS	EM92601A only
Recovery time Enable to clock	T_{REC}	80			nS	EM92601A only
Input pulse width clock and Enable	T_W	80			nS	EM92601A only

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TIMING DIAGRAM

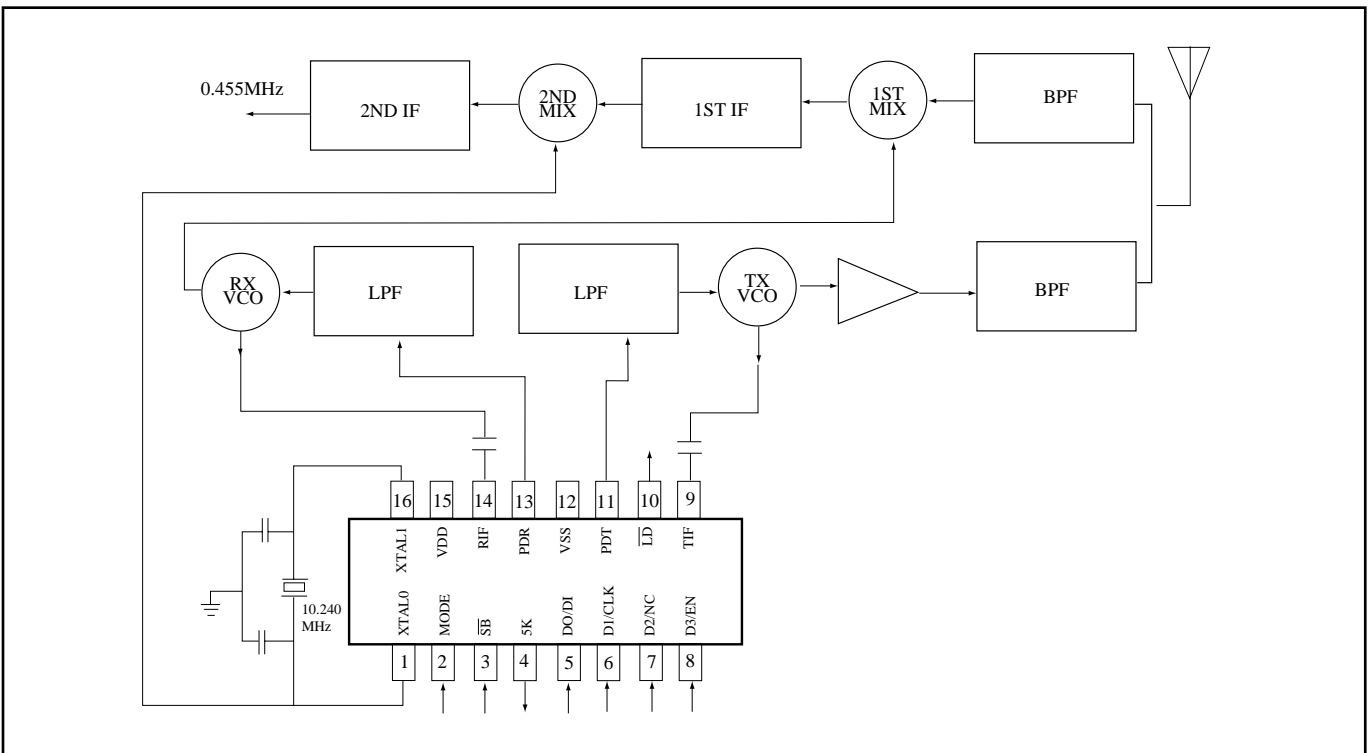


EM92601A Timing



Unlock Timing

APPLICATION CIRCUIT



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DIVIDE RATIO AND VCO FREQUENCIES

Base (MODE=1)	Input				CH	Rx (Fref=5KHz)			Tx=(Fref=5KHz)		
	D3	D2	D1	D0		FRx (MHz)	FVCO(MHz)	N	FTx(MHz)	FVCO(MHz)	N
	0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322
	0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326
	0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334
	0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342
	0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346
	0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354
	0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366
	1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374
	1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386
	1	0	1	0	10	49.770	39.275	7855	46.970	46.970	9394
	1	0	1	1		49.970	39.275	7855	46.970	46.970	9394
	1	1	0	0		49.970	39.275	7855	46.970	46.970	9394
	1	1	0	1		49.970	39.275	7855	46.970	46.970	9394
	1	1	1	0		49.970	39.275	7855	46.970	46.970	9394
	1	1	1	1		49.970	39.275	7855	46.970	46.970	9394
	0	0	0	0		49.970	39.275	7855	46.970	46.970	9394

REMOTE (MODE=0)	Input				CH	Rx (Fref=5KHz)			Tx=(Fref=5KHz)		
	D3	D2	D1	D0		FRx (MHz)	FVCO(MHz)	N	FTx(MHz)	FVCO(MHz)	N
	0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934
	0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969
	0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972
	0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954
	0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975
	0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966
	0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978
	1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986
	1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998
	1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994
	1	0	1	1		46.970	36.275	7255	49.970	49.970	9994
	1	1	0	0		46.970	36.275	7255	49.970	49.970	9994
	1	1	0	1		46.970	36.275	7255	49.970	49.970	9994
	1	1	1	0		46.970	36.275	7255	49.970	49.970	9994
	1	1	1	1		46.970	36.275	7255	49.970	49.970	9994
	0	0	0	0		46.970	36.275	7255	49.970	49.970	9994

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