

# DATA SHEET

## **TDA8310**

**PAL/NTSC colour processor for  
PIP applications**

Preliminary specification  
File under Integrated Circuits, IC02

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**Philips Semiconductors**



**PHILIPS**

## PAL/NTSC colour processor for PIP applications

## TDA8310

### FEATURES

- Multistandard vision IF circuit (positive and negative modulation)
- Video switch which automatically detects whether the incoming signal is CVBS or Y/C
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Automatic PAL/NTSC decoder which can decode all standards available in the world
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- Horizontal PLL with an alignment-free horizontal oscillator
- Vertical count-down circuit
- RGB/YUV and fast blanking switch with 3-state output and active clamping
- Low dissipation (560 mW)
- Small amount of peripheral components compared with competition ICs.

### GENERAL DESCRIPTION

The TDA8310 is an alignment-free PAL/NTSC colour processor for Picture-in-Picture (PIP) applications. The circuit contains a vision IF amplifier, a PAL/NTSC colour decoder, horizontal and vertical synchronization and an RGB/YUV switch.

As input for the colour decoder and sync processor the demodulated IF signal can be chosen but the circuit also has a video input which automatically detects whether the incoming signal is CVBS or Y/C. The output signals for the PIP processor are:

Luminance signal

Colour difference signals (U and V)

Horizontal and vertical synchronization pulses.

The RGB/YUV switch can select between two RGB or YUV sources, e.g. between the PIP processor and the SCART input signal.

The supply voltage for the IC is 8 V. It is available in a 52-pin SDIP package.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8310	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

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## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pins 19 and 41)	7.2	8.0	8.8	V
$I_P$	supply current	–	70	–	mA
<b>Input voltages</b>					
$V_{i(rms)}$	vision IF amplifier input sensitivity (RMS value)	–	70	100	$\mu$ V
$V_{17,20(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	–	1	1.4	V
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	–	0.3	–	V
$V_{i(p-p)}$	RGB/YUV input signal voltage amplitude (peak-to-peak value)	–	–	1.3	V
<b>Output signals</b>					
$V_{o(p-p)}$	demodulated CVBS output voltage (peak-to-peak value)	–	2.5	–	V
$V_{29}$	tuner AGC control output voltage	0	–	12	V
$V_{o(p-p)}$	luminance output voltage (peak-to-peak value)	–	1.4	–	V
$V_{50(p-p)}$	(B–Y) output voltage (peak-to-peak value)	1.06	1.33	1.60	V
$V_{51(p-p)}$	(R–Y) output voltage (peak-to-peak value)	0.84	1.05	1.26	V
$V_{39}$	horizontal sync pulse output voltage	–	4	–	V
$V_{36}$	vertical sync pulse output voltage	–	4	–	V
$G_V$	voltage gain of the RGB switches	–0.5	0	+0.5	dB
<b>Control voltage</b>					
$V_{control}$	control voltage for HUE	0	–	5	V

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### BLOCK DIAGRAM

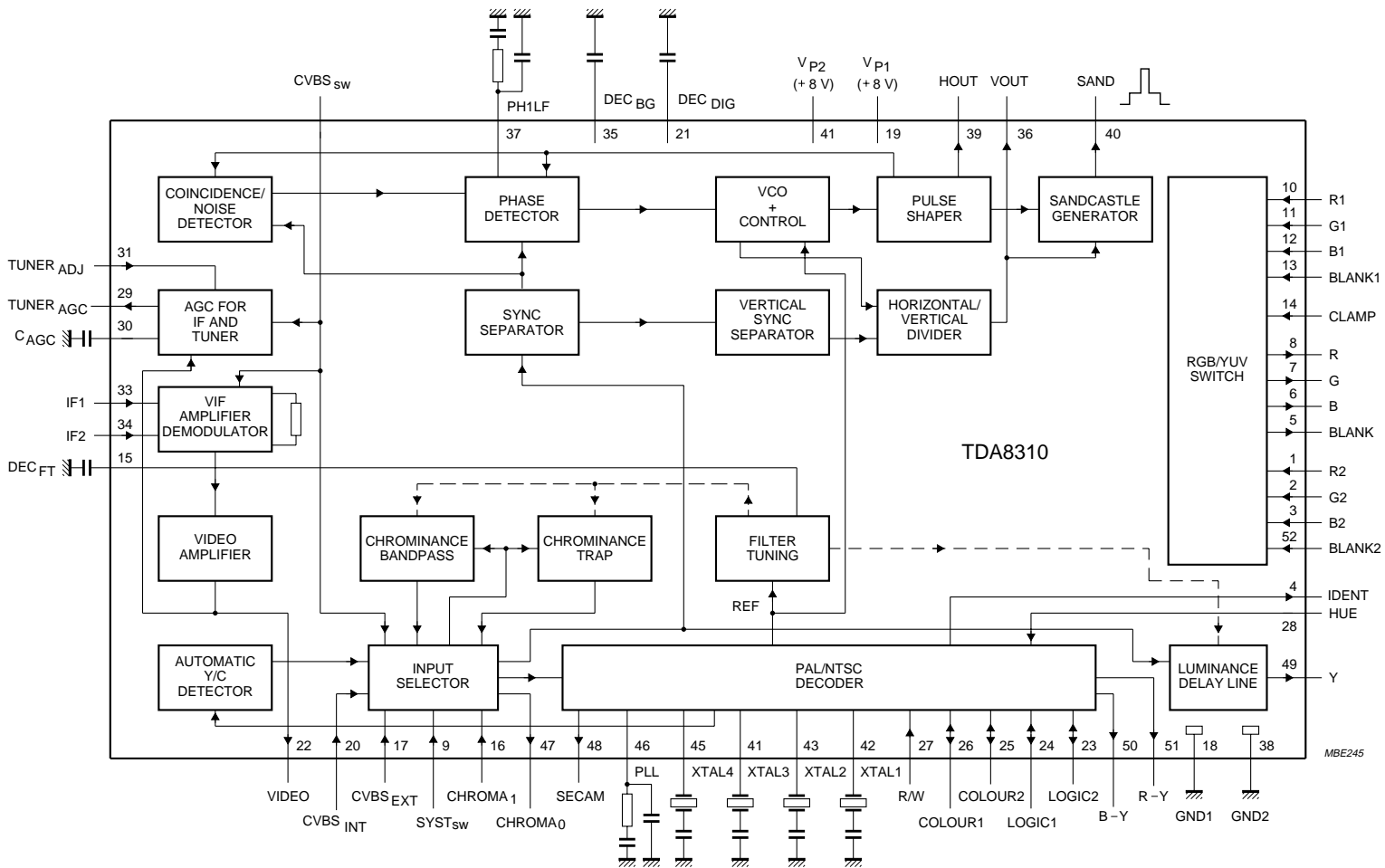


Fig.1 Block diagram.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
R2	1	RED input 2 (PIP)
G2	2	GREEN input 2 (PIP)
B2	3	BLUE input 2 (PIP)
IDENT	4	colour standard identification output
BLANK	5	blanking output
B	6	BLUE output
G	7	GREEN output
R	8	RED output
SYST <sub>SW</sub>	9	system switch
R1	10	RED input 1
G1	11	GREEN input 1
B1	12	BLUE input 1
BLANK1	13	blanking input 1
CLAMP	14	clamping pulse input
DEC <sub>FT</sub>	15	decoupling filter tuning
CHROMA <sub>I</sub>	16	chrominance input
CVBS <sub>EXT</sub>	17	external CVBS input
GND1	18	ground 1 (0 V)
V <sub>P1</sub>	19	supply voltage 1 (+8 V)
CVBS <sub>INT</sub>	20	internal CVBS input
DEC <sub>DIG</sub>	21	decoupling digital supply
VIDEO	22	IF video output
LOGIC2	23	crystal logic 2 input/output
LOGIC1	24	crystal logic 1 input/output
COLOUR2	25	colour system logic 2 input/output
COLOUR1	26	colour system logic 1 input/output
R/W	27	read/write selection input

SYMBOL	PIN	DESCRIPTION
HUE	28	HUE control input
TUNER <sub>AGC</sub>	29	tuner AGC output
C <sub>AGC</sub>	30	AGC filter capacitor
TUNER <sub>ADJ</sub>	31	tuner take-over adjustment input
CVBS <sub>SW</sub>	32	CVBS positive/negative modulation control switch input
IF1	33	IF input 1
IF2	34	IF input 2
DEC <sub>BG</sub>	35	bandgap decoupling
VOUT	36	vertical sync output pulse
PH1LF	37	phase 1 loop filter
GND2	38	ground 2 (0 V)
HOUT	39	horizontal sync output pulse
SAND	40	sandcastle pulse output
V <sub>P2</sub>	41	supply voltage 2 (+8 V)
XTAL1	42	4.4336 MHz crystal
XTAL2	43	3.5820 MHz crystal for PAL-N
XTAL3	44	3.5756 MHz crystal for PAL-M
XTAL4	45	3.5795 MHz crystal for NTSC
PLL	46	PLL colour filter
CHROMA <sub>O</sub>	47	chrominance output for TDA8395
SECAM	48	SECAM reference output
Y	49	Y output
B-Y	50	B-Y output
R-Y	51	R-Y output
BLANK2	52	blanking/insertion input 2 (PIP)

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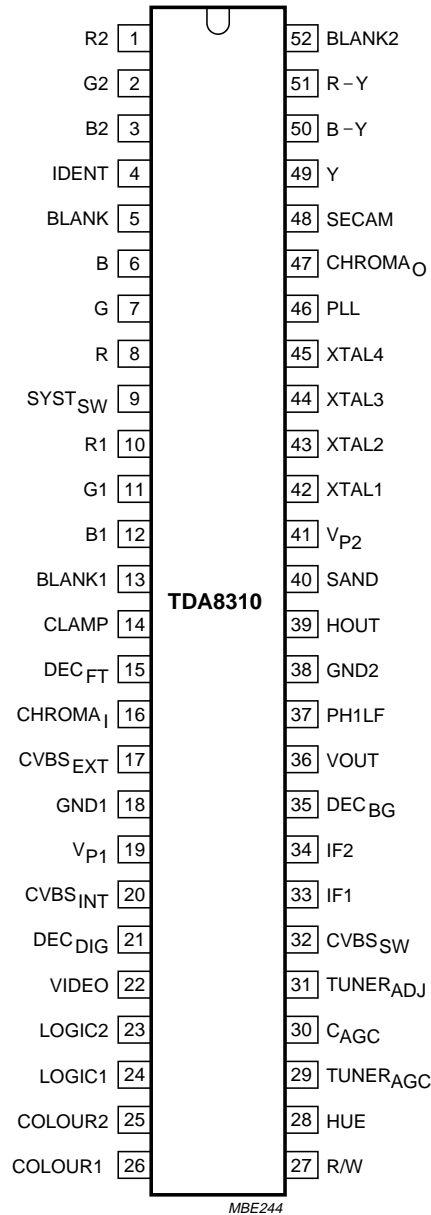


Fig.2 Pin configuration.

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### FUNCTIONAL DESCRIPTION

#### Vision IF amplifier

The IF amplifier contains three AC-coupled control stages with a total gain control range >60 dB. The sensitivity of the circuit is comparable with that of modern IF-ICs. The demodulation of the IF signal is achieved by a multiplier. The demodulator is alignment-free and does not require external components.

The polarity of the demodulator can be switched to make the circuit suitable for positive and negative modulated signals.

The AGC detector operates on top-sync or top white-level depending on the position of the demodulator. The AGC detector time-constant capacitor is externally connected to facilitate flexibility of the application. During positive modulation the time-constant of the AGC system is too long to avoid visible variations of the signal amplitude. To obtain an acceptable speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When no action is detected during three frame periods the speed of the system is increased.

#### Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are then fed to the slicing stage (separator) which operates at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used to detect whether the line oscillator is synchronized and for transmitter identification. The first PLL has a very high static steepness, this ensures that the phase of the picture is independent of the line frequency. The line oscillator operates at twice the line frequency.

The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC.

The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.

The horizontal output pulse is derived from the horizontal oscillator via a pulse shaper. The pulse width of the output pulse is 5.4  $\mu$ s, the front edge of this pulse coincides with the front edge of the sync pulse at the input.

The vertical output pulse is generated by a count-down circuit. The pulse width is approximately 380  $\mu$ s. Both the horizontal and vertical pulses will always be available at the outputs even when no input signal is available.

In addition to the horizontal and vertical sync pulse outputs the IC has a sandcastle pulse output which contains burst key and blanking pulses.

#### Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by gyrator circuits that are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. When a Y/C signal is supplied to the input the chrominance trap is automatically switched off by the Y/C detection circuit, but it is also possible to force the filters in the CVBS or Y/C position.

The luminance delay line is also realised by gyrator circuits.

#### Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally.

The colour decoder is very flexible. Together with the SECAM decoder TDA8395 an automatic multistandard decoder can be designed but it is also possible to use it for one standard when only one crystal is connected to the IC. The decoder can be forced to one of the standards via the "forced mode" pins. The crystal pins which are not used must be connected to the positive supply line via a 8.2 k $\Omega$  resistor. It is also possible to connect the non-used pins with one resistor to the positive supply line. In this event the resistor must have a value of 8.2 k $\Omega$  divided by the number of pins.

The chrominance output signal of the video switch is externally available and must be used as an input signal for the SECAM decoder.

#### RGB/YUV switch

The RGB/YUV switch is for switching between two RGB or YUV video sources. The outputs of the switch can be set to high impedance state so that other switches can be used in parallel.

The switch is controlled via pins 13 and 52. The details of switch control are shown in Table 5.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage		–	9.0	V
$T_{stg}$	storage temperature		–25	+150	°C
$T_{amb}$	operating ambient temperature		–25	+70	°C
$T_{sld}$	soldering temperature for 5 s		–	260	°C
$T_j$	maximum operating junction temperature		–	150	°C
$V_{es}$	electrostatic discharge	note 1	–2000	+2000	V
		note 2	–200	+200	V

## Notes

- Human body model 100 pF, 1500  $\Omega$ .
- Machine model 200 pF, 0  $\Omega$ .

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	$\leq 40$	K/W

## QUALITY SPECIFICATION

In accordance with "SNW-FQ-611 part E". The numbers of the quality specification can be found in the "Quality Reference Handbook". The handbook can be ordered using the code 9398 510 63011. All pins are protected against electrostatic discharge by means of internal clamping diodes.

## Latch up

At  $T_{amb} = 70$  °C most pins meet the specification:

$$I_{trigger} \geq 100 \text{ mA or } \geq 1.5 V_{DDmax}$$

$$I_{trigger} \leq -100 \text{ mA or } \leq -0.5 V_{DDmax}$$

The following pins do not meet this specification:

pin 7 +90 mA

pin 21 +90 mA

pin 32 –90 mA

pin 46 +90 mA.



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**CHARACTERISTICS** $V_P = 8\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_P$	supply voltage (pins 19 and 41)		7.2	8.0	8.8	V
$I_{P1}$	supply current (pin 19)		45	65	80	mA
$I_{P2}$	supply current (pin 41)		3	5	10	mA
$P_{tot}$	total power dissipation		–	560	–	mW
<b>IF circuit</b>						
VISION IF AMPLIFIER INPUT (PINS 33 AND 34)						
$V_{i(rms)}$	input sensitivity (RMS value)	note 1 $f_i = 38.90\text{ MHz}$ $f_i = 45.75\text{ MHz}$ $f_i = 58.75$	– – –	70 70 70	100 100 100	$\mu\text{V}$ $\mu\text{V}$ $\mu\text{V}$
$R_I$	Input resistance (differential)	note 2	1.6	2.0	2.4	$\text{k}\Omega$
$C_I$	Input capacitance (differential)	note 2	–	3	–	pF
$G_{cr}$	gain control range	note 3	64	–	–	dB
$V_{i(rms)}$	maximum input signal (RMS value)		100	150	–	mV
VIDEO AMPLIFIER OUTPUT; note 4 (PIN 22)						
$V_{22(neg)}$	negative modulation zero signal output level top sync level	note 5	4.45 1.9	4.60 2.0	4.75 2.1	V V
$V_{22(pos)}$	positive modulation zero signal output level white level	note 5	1.85 4.2	2.00 4.3	2.15 4.4	V V
$\Delta V_{22}$	difference in amplitude between negative and positive modulation		–	0	15	%
$Z_O$	video output impedance		–	–	75	$\Omega$
$I_{bias}$	internal bias current of NPN emitter follower output transistor		1	–	–	mA
$I_{source}$	maximum source current		–	–	5	mA
S/N	signal-to-noise ratio	notes 6 and 7 $V_i = 10\text{ mV}$ end of control range	52 52	60 61	– –	dB dB
$V_{22(rc)}$	residual carrier signal	note 6	–	2.5	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>IF AND TUNER AGC</b>						
<i>Timing of IF-AGC (<math>C_{30} = 2.2 \mu F</math>)</i>						
	modulated video interference	30% AM for 1 to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
$t_{inc}$	response time for an IF input signal amplitude increase of 52 dB for positive and negative modulation		–	2	5	ms
$t_{dec}$	response time for an IF input signal amplitude decrease of 52 dB for negative modulation for positive modulation		– –	25 100	50 200	ms ms
$I_{leak}$	allowed leakage current of the AGC capacitor for negative modulation for positive modulation	note 8	– –	– –	10 200	$\mu A$ nA
<i>Tuner take-over adjustment (pin 31)</i>						
$V_{31(rms)}$	minimum starting level voltage for tuner take-over (RMS value)		–	0.2	0.5	mV
$V_{31(rms)}$	maximum starting level voltage for tuner take-over (RMS value)		100	150	–	mV
$V_{cr}$	control voltage range		0.5	–	4.5	V
<i>Tuner control output (pin 29)</i>						
$V_{29}$	maximum tuner AGC output voltage	maximum gain	–	–	12	V
$V_{29(sat)}$	output saturation voltage	minimum gain; $I_{29} = 2 \text{ mA}$	–	–	300	mV
$I_{29}$	maximum tuner AGC output current swing		5	–	–	mA
$I_{leak}$	leakage current RF AGC		–	–	1	$\mu A$
$\Delta V_{29}$	input signal voltage variation for complete tuner control	$I_{O(max)} = 1 \text{ mA}$	0.5	2.0	4.0	dB
<b>CVBS and Y/C switch</b>						
INTERNAL CVBS AND EXTERNAL CVBS/Y INPUTS (PINS 20 AND 17)						
$V_{20,17(p-p)}$	CVBS/Y input voltage (peak-to-peak value)	notes 2 and 9	–	1	1.4	V
$I_{20,17}$	input current		–	4	6	$\mu A$
$V_{clamp}$	top sync clamping voltage level		–	3.3	–	V
$I_{clamp}$	clamping input current		80	100	–	$\mu A$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>CHROMINANCE INPUT (PIN 16)</b>						
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	notes 2, 10 and 17	–	0.3	–	V
$V_{16(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)	note 6	1.0	–	–	V
$R_I$	chrominance input resistance		14	20	26	k $\Omega$
$C_I$	chrominance input capacitance	note 2	–	–	5	pF
<b>CHROMINANCE OUTPUT (PIN 47)</b>						
$V_{47(p-p)}$	output signal voltage amplitude (peak-to-peak value)		0.18	0.20	0.22	V
$Z_O$	output impedance		200	250	300	$\Omega$
$V_O$	DC output voltage	open-circuit output	1.2	1.4	1.6	V
<b>SWITCH CONTROL INPUT FOR INTERNAL/EXTERNAL POSITIVE/NEGATIVE MODULATION; note 11 (PIN 32)</b>						
$V_{32}$	internal CVBS signal selected with negative modulation	note 12	–	–	1	V
	with positive modulation		2	–	3	V
$V_{32}$	external CVBS or Y/C signal selected	IF switched to negative modulation	3.9	–	$V_P$	V
$Z_I$	input impedance		25	–	–	k $\Omega$
ISS	suppression of non-selected video input signal	note 6	50	–	–	dB
<b>SWITCH CONTROL INPUT FOR EXTERNAL CVBS OR Y/C SELECTION (PIN 9)</b>						
$V_9$	filters switched to CVBS condition		–	–	1	V
$V_9$	filters switched to Y/C condition	note 12	2	–	3	V
$V_9$	automatic selection of CVBS or Y/C		3.9	–	$V_P$	V
$Z_I$	input impedance		25	–	–	k $\Omega$
<b>Chrominance filters, luminance delay line and luminance output</b>						
<b>CHROMINANCE TRAP CIRCUIT</b>						
$f_{trap}$	trap frequency		–	$f_{osc}$	–	MHz
QF	trap quality factor	notes 6 and 13	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
<b>CHROMINANCE BANDPASS CIRCUIT</b>						
$f_c$	centre frequency		–	$f_{osc}$	–	MHz
QBP	bandpass quality factor	note 6	–	3	–	
<b>Y DELAY LINE</b>						
$\Delta t_d$	difference in delay time between the luminance and the demodulated chrominance signals	note 6	0	50	100	ns
B	bandwidth of internal delay line	note 6	8	–	–	MHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Y OUTPUT (PIN 49)</b>						
$V_{49(b-w)}$	output signal voltage amplitude (black-to-white value)	note 29	0.8	1.0	1.2	V
$Z_O$	output impedance		80	100	120	$\Omega$
$V_{49(DC)}$	DC output voltage level (top sync)		2.7	2.9	3.1	V
$I_{bias}$	internal bias current of NPN emitter follower output transistor		0.4	0.5	–	mA
$I_{source}$	maximum source current		–	–	2	mA
<b>Horizontal and vertical synchronization circuits</b>						
<b>SYNC VIDEO INPUT (PINS 17 AND 20)</b>						
$V_{17,20}$	sync pulse voltage amplitude	note 2	50	300	–	mV
SL	slicing level	note 14	–	50	–	%
<b>VERTICAL SYNC</b>						
$t_W$	width of the vertical sync pulse without sync instability	note 15	22	–	–	$\mu$ s
<b>HORIZONTAL OSCILLATOR</b>						
$f_{fr}$	free running frequency		–	15625	–	Hz
$\Delta f_{fr}$	spread on free running frequency		–	–	$\pm 2$	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	$V_P = 8\text{ V} \pm 10\%$ ; note 6	–	0.2	0.5	%
$\Delta f_{osc}$	frequency variation with temperature	$T_{amb} = 0\text{ to }70\text{ }^\circ\text{C}$ ; note 6	–	–	80	Hz
$\Delta f_{osc(max)}$	maximum frequency deviation at the start of the horizontal output	no calibration	–	–	75	%
<b>HORIZONTAL PLL; note 16 (FILTER CONNECTED TO PIN 37)</b>						
$f_{HR}$	holding range PLL		–	$\pm 0.9$	$\pm 1.2$	kHz
$f_{CR}$	catching range PLL	note 6	$\pm 0.6$	$\pm 0.9$	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		14	20	26	dB
HYS	hysteresis at the switching point		1	3	6	dB
<b>HORIZONTAL OUTPUT (PIN 39)</b>						
$V_{OH}$	HIGH level output voltage	$I_O = 2\text{ mA}$	2.4	4.0	–	V
$V_{OL}$	LOW level output voltage	$I_O = 2\text{ mA}$	–	0.3	0.6	V
$I_{sink}$	sink current		–	–	2	mA
$I_{source}$	source current		–	–	2	mA
$t_W$	pulse width		–	5.4	–	$\mu$ s
$t_d$	delay between the positive edge of the horizontal output pulse and the start of the horizontal sync pulse at the input		–	0	–	$\mu$ s

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL OUTPUT; note 17 (PIN 36)						
$f_{fr}$	free running frequency		–	50/60	–	Hz
$f_{lock}$	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	lines
	locking range		488	–	722	lines/ frame
$V_{OH}$	HIGH level output voltage	$I_O = 2 \text{ mA}$	2.4	4.0	–	V
$V_{OL}$	LOW level output voltage	$I_O = 2 \text{ mA}$	–	0.3	0.6	V
$I_{sink}$	sink current		–	–	2	mA
$I_{source}$	source current		–	–	2	mA
$t_W$	pulse width		–	380	–	$\mu\text{s}$
$t_d$	delay between the start of the vertical sync pulse at the input and the positive edge of the output pulse		–	37.5	–	$\mu\text{s}$
SANDCASTLE PULSE OUTPUT; note 18 (PIN 40)						
$V_O$	output voltage during scan	$I_O = 1 \text{ mA}$ ; note 30	–	–	0.9	V
$V_O$	output voltage during burst key	$I_O = 1 \text{ mA}$ ; note 30	4.1	–	5.2	V
$Z_O$	output impedance during blanking		1.0	–	–	$M\Omega$
$t_W$	pulse width					
	burst key		3.3	3.5	3.7	$\mu\text{s}$
	line blanking		8.4	8.7	9.0	$\mu\text{s}$
	vertical blanking		–	14	–	lines
$t_d$	delay of start of burst key to start of sync		5.2	5.4	5.6	$\mu\text{s}$
<b>Colour demodulation part</b>						
CHROMINANCE AMPLIFIER						
$ACC_{cr}$	ACC control range	note 19	26	–	–	dB
$\Delta V$	change in amplitude of the output signals over the ACC range		–	–	2	dB
$THR_{on}$	threshold colour killer ON		–38	–41	–44	dB
$HYS_{off}$	hysteresis colour killer OFF	note 6				
	strong input signal	$S/N \geq 40 \text{ dB}$	0	+3	+6	dB
	noisy input signal		0	+1	+8	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REFERENCE PART						
<i>Phase-locked loop; note 20</i>						
$f_{CR}$	catching range		300	500	–	Hz
$\Delta\phi$	phase shift for a $\pm 300$ Hz deviation of the oscillator frequency	note 6	–	–	2	deg
<i>Oscillator</i>						
$TC_{osc}$	temperature coefficient of $f_{osc}$	note 6	–	2.0	2.5	Hz/K
$\Delta f_{osc}$	$f_{osc}$ deviation with respect to $V_P$	note 6; $V_P = 8\text{ V} \pm 10\%$	–	–	250	Hz
$R_I$	input resistance (pins 43 to 45)	$f_i = 3.58\text{ MHz}$ ; note 2	–	1.5	–	$k\Omega$
$R_I$	input resistance (pin 42)	$f_i = 4.43\text{ MHz}$ ; note 2	–	1	–	$k\Omega$
$C_I$	input capacitance (pins 42 to 45)	note 2	–	–	10	pF
R	required resistance to $V_P$ for a crystal pin which is not used	note 21	7.8	8.2	8.6	$k\Omega$
HUE CONTROL INPUT; note 22 (PIN 28)						
$HUE_{cr}$	HUE control range	see also Fig.3	$\pm 35$	$\pm 40$	–	deg
$R_I$	input resistance		45	–	–	$k\Omega$
$V_{control}$	control voltage to switch the colour PLL in the free-running mode	note 20	$V_P - 1$	–	–	V
DEMODULATOR OUTPUTS (PINS 50 AND 51)						
$V_{50(p-p)}$	(B–Y) output signal voltage amplitude (peak-to-peak value)	note 31	1.06	1.33	1.60	V
$V_{51(p-p)}$	(R–Y) output signal voltage amplitude (peak-to-peak value)	note 31	0.84	1.05	1.26	V
	spread of signal amplitude ratio PAL/NTSC	note 6	–1	–	+1	dB
$Z_O$	output impedance (R–Y)/(B–Y) output		–	–	500	$\Omega$
B	bandwidth of demodulators	–3 dB; note 23	–	650	–	kHz
$V_{50(p-p)}$	(B–Y) residual carrier output voltage (peak-to-peak value)	$f = f_{osc}$	–	–	1	mV
		$f = 2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	(R–Y) residual carrier output voltage (peak-to-peak value)	$f = f_{osc}$	–	–	1	mV
		$f = 2f_{osc}$	–	–	5	mV
$V_{51(p-p)}$	H/2 ripple at (R–Y) output (peak-to-peak value)	only burst fed to input	–	–	25	mV
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature	note 6	–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage	note 6	–	–	$\pm 0.1$	dB
$I_{bias}$	internal bias current of NPN emitter follower output transistor		0.16	0.20	–	mA
$I_{source}$	maximum source current		–	–	1	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DEMODULATION ANGLE AND GAIN RATIO</b>						
	demodulation angle		85	90	95	deg
G	gain ratio of both demodulators G(B-Y) to G(R-Y)		1.60	1.78	1.96	
<b>REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 48)</b>						
f <sub>ref</sub>	reference frequency	note 24	–	4.43	–	MHz
V <sub>48(p-p)</sub>	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V <sub>O</sub>	output voltage level	PAL/NTSC identified	1.5	1.6	1.7	V
V <sub>O</sub>	output voltage level	no PAL/NTSC; SECAM (by TDA8395) identified	4.3	4.5	4.7	V
I <sub>48</sub>	required current to force the decoder in SECAM mode		120	–	–	μA
<b>STANDARD IDENTIFICATION AND FORCED SYSTEM SWITCHING; note 25 (PINS 4 AND 23 TO 27)</b>						
V <sub>I/O</sub>	input/output voltage in "low" condition in "high" condition		– 4.0	– –	1 5.3	V V
V <sub>I(max)</sub>	maximum input voltage	note 26	–	–	V <sub>P</sub>	V
I <sub>load</sub>	maximum load current (pins 23 to 26)		–	–	1	mA
I <sub>I</sub>	input current (pins 23 to 26) in "low" or "high" condition when connected to V <sub>P</sub>	note 26	– –	– –	1 10	μA μA
R <sub>I</sub>	input resistance (pin 27)		80	–	–	kΩ
V <sub>O</sub>	output voltage (pin 4) during PAL during SECAM	notes 27 and 30	– 4.1	– –	0.9 5.5	V V
Z <sub>O</sub>	output impedance pin 4 during NTSC	note 27	1	–	–	MΩ
I <sub>load</sub>	maximum load current (pin 4)		–	–	0.5	mA
<b>RGB switch</b>						
<b>RGB INPUTS (PINS 1 TO 3 AND 10 TO 12)</b>						
V <sub>i(p-p)</sub>	signal voltage amplitude (peak-to-peak value)		–	–	1.3	V
Z <sub>I</sub>	input impedance		100	–	–	kΩ
V <sub>clamp</sub>	active clamping voltage level		2.6	2.8	3.0	V
I <sub>LI</sub>	input leakage current	note 6	–	–	3	μA
I <sub>clamp</sub>	active clamping current		–200	–	+200	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING/SWITCH INPUTS; note 28 (PINS 13 AND 52)						
$V_{IH}$	HIGH level input voltage		0.9	–	3.0	V
$V_{IL}$	LOW level input voltage		0	–	0.5	V
$I_I$	input current		–	–0.2	–0.3	mA
$t_d$	delay between input and output pulse		–	–	50	ns
$t_d$	delay between switch input and RGB output		–	–	70	ns
$V_{13}$	input voltage on pin 13 to make RGB outputs and the fast blanking output high-ohmic		4	–	$V_P$	V
CLAMPING PULSE INPUT (PIN 14)						
$V_{IH}$	HIGH level input voltage		4.0	4.5	$V_P$	V
$V_{IL}$	LOW level input voltage		–	–	1	V
$Z_I$	input impedance		1	–	–	M $\Omega$
RGB OUTPUTS (PINS 6 TO 8)						
$G_v$	voltage gain of the switches	$f = 1$ MHz	–0.5	0	+0.5	dB
$G_{diff}$	gain difference of the three channels		–	–	0.5	dB
$Z_O$	output impedance		–	–	150	$\Omega$
$Z_{O(off)}$	output impedance in the “off” state	$f = 10$ MHz	100	–	–	k $\Omega$
$V_O$	output voltage during blanking	open-circuit output	1.2	1.4	1.6	V
$V_{os}$	blanking off-set voltage of the two sources		–	–	5	mV
$I_{bias}$	internal bias current of NPN emitter follower output transistor		0.16	0.2	–	mA
$I_{source(max)}$	maximum source current		–	–	1	mA
ISS	input signal suppression when RGB outputs are high-ohmic	$f = 5$ MHz; note 6	60	–	–	dB
		$f = 10$ MHz; note 6	50	–	–	dB
		$f = 22$ MHz; note 6	40	–	–	dB
CT	crosstalk between the two RGB channels	$f = 5$ MHz; note 6	–60	–	–	dB
		$f = 10$ MHz; note 6	–50	–	–	dB
		$f = 22$ MHz; note 6	–40	–	–	dB
B	bandwidth of the RGB channels gain reduction –0.5 dB gain reduction –1 dB gain reduction –3 dB	$C_L = 20$ pF; note 6	5	–	–	MHz
			10	–	–	MHz
			22	–	–	MHz
$t_d$	delay from RGB input to output	note 6	–	–	20	ns



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING OUTPUT (PIN 5)						
V <sub>OH</sub>	HIGH level output voltage		2	–	3	V
V <sub>OL</sub>	LOW level output voltage		0	–	0.3	V
Z <sub>O</sub>	output impedance		–	–	300	Ω
Z <sub>O(off)</sub>	output impedance in the “off” state		100	–	–	kΩ
t <sub>r</sub>	rise time of the output pulse		–	–	30	ns
t <sub>f</sub>	fall time of the output pulse		–	–	30	ns
t <sub>d</sub>	delay difference between fast blanking and RGB at the outputs		–	–	30	ns
I <sub>load</sub>	maximum load current		–	–	1	mA

## Notes

- On set AGC.
- This parameter is not tested during production and is just given as application information for the designer of the television receiver.
- Measured with 0 dB = 500 μV.
- Measured at 10 mV RMS top sync input signal.
- So called projected zero point, i.e. with switched demodulator.
- This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
- Measured with a source impedance of 75 Ω, where:
 
$$S/N = 20 \log \frac{V_O \text{ (black-to-white)}}{V_{m(rms)} \text{ (B = 5 MHz)}}$$
- When the leakage current of the capacitor exceeds this value it will result in a reduced performance of the AGC (amplitude variation during line or frame up to 20% maximum) but it will not result in a hang-up situation.
- Signal with negative-going sync. Amplitude includes sync pulse amplitude.
- Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
- The IC has two 3-level switch control inputs for the selection of the video signal for the decoder and synchronization circuits. The video source for internal or external signal is selected via pin 32, also the polarity of the demodulation for the internal signal. When the video switch is in the external position the voltage level of pin 9 determines whether the video filters are switched to CVBS or Y/C. It is also possible via pin 9 to select an automatic detection of the Y/C signal.
- This value is internally generated when the pin is left open-circuit (the minimum value of the series resistor is 25 kΩ).
- The –3 dB bandwidth of the circuit can be calculated by means of the following equation:
 
$$f_{-3 \text{ dB}} = f_{\text{osc}} \left( 1 - \frac{1}{2Q} \right)$$
- Slicing level is independent of sync pulse amplitude.
- The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization. The value given is the delay caused by the vertical sync pulse integrator. The integrator has been designed such that the vertical sync is not disturbed for special anti-copy tapes with vertical sync pulses with an on/off time of 10/22 μs.

## PAL/NTSC colour processor for PIP applications

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16. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when excessive noise is present in the signal. This occurs when the internal video signal is selected or for an external CVBS signal when the chrominance input (pin 16) is left open-circuit. The time constant is always 'fast' when the chrominance input pin is connected to ground and the input is switched to the Y/C mode. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible.
- During weak signal conditions (noise detector active) the phase detector is gated and the width of the gate pulse has a value of 5.7  $\mu\text{s}$  so that the effect of the noise is reduced to a minimum.
- The output current of the phase detector for the various conditions is shown in Table 1.
17. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 2 search modes of operation:
- The 'large window' mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz)
  - The 'narrow window' mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.
18. To obtain a simple interface between the TDA8310 and the PIP processor the sandcastle output has been designed such that the output is pulled down during scan and pulled up during the burst key pulse. During blanking the output is high-ohmic and therefore the output voltage is determined by the load.
19. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) as given in Characteristics first parameter of Section "Chrominance input (pin 16)" the dynamic range of the ACC is +6 and -20 dB.
20. All frequency variations are referenced to 3.58/4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9922 520. If the spurious response of the 4.43 MHz crystal is lower than -3 dB with respect to the fundamental frequency for a damping resistance of 1 k $\Omega$ , oscillation at the fundamental frequency is guaranteed. The spurious response of the 3.58 MHz crystal must be lower than -3 dB with respect to the fundamental frequency for a damping resistance of 1.5 k $\Omega$ . The catching and detuning range are measured for nominal crystal parameters. These are:
- load resonance frequency  $f_0$  ( $C_L = 20$  pF) = 4.433619 or 3.579545 MHz
  - motional capacitance  $C_M = 20.6$  fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal)
  - parallel capacitance  $C_0 = 5.5$  pF (4.43 MHz crystal) or 4.5 pF (3.58 MHz crystal).
- The actual load capacitance in the application should be  $C_L = 18$  pF to account for parasitic capacitances on and off chip.
- The free-running frequency of the oscillator can be checked by the HUE control pin to the positive supply rail. In that condition the colour killer is not active so that the frequency off-set is visible on the screen. When two or more crystals are connected to the IC the circuit must be forced to one of the crystals during this test to prevent the oscillator continuously switching between the various frequencies.
21. The crystal pins which are not used must be connected to the positive supply line via an 8.2 k $\Omega$  resistor. It is also possible to connect the non-used pins together and use a resistor with a value of 8.2 k $\Omega$  divided by the number of pins which are not used.
22. When this pin is left open-circuit the HUE control is set to the nominal value.
23. This value indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the demodulator low-pass filter is approximately 1 MHz.

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24. The reference signal for the TDA8395 is available only when the crystal oscillator is operating at a frequency of 4.43 MHz. When a SECAM signal is identified this signal is only available during the vertical retrace period thus avoiding crosstalk with the incoming SECAM signal during scan.
25. The identified colour standard can be read from the IC in two ways:
- From the voltage level of pin 4. The voltage during the demodulation of the various standards is given in the last three parameters of this section.
  - From the pins 23 to 26 when pin 27 is in the "read" mode.
- When pin 27 is in the "write" mode the colour decoder can be forced to one of the colour standards. The levels for the various standards are given in Tables 2, 3 and 4.
26. When one or more pins have to be connected to the positive supply line the **total** current must be limited to 40  $\mu$ A. This can be achieved by connecting these pins together and connecting them to a positive supply line via a 100 k $\Omega$  resistor. When separate resistors are used a resistor with a higher value must be used so that the total current is limited to the required level.
27. The output of pin 4 is designed similar to the sandcastle output. The output is pulled down during PAL and pulled up during SECAM. During NTSC the pin is floating so that the output level is determined by the load.
28. The control possibilities of the RGB switch via pins 13 and 52 are shown in Table 5.
29. This output signal value is obtained when the CVBS or Y input signal at pins 17 and/or 20 has an amplitude of 0.7 V (black-to-white value).
30. The output buffer consists of a combination of a PMOS and an NMOS. The maximum output impedance in the low state can be calculated by dividing the maximum output voltage (for this parameter 0.9 V) by the specified current. For the high state this resistance can be calculated by dividing the difference between the maximum and minimum output voltage by the specified current. The output impedance is independent of the value of the output current.
31. These output signal values are obtained for a colour bar input signal with 75% saturation.

**Table 1** Output current of phase detector

CURRENT PHASE DETECTOR DURING	SCAN ( $\mu$ A)	VERTICAL RETRACE ( $\mu$ A)	GATED YES/NO
Weak signal and synchronized	30	30	YES (5.7 $\mu$ s)
Strong signal and synchronized	180	270	NO
Not synchronized	180	270	NO

**Table 2** Read/write pin input (pin 27)

MODE	LEVEL
Decoder automatic	LOW
Forced decoder mode	HIGH

**Table 3** Colour system logic (pins 25 and 26)

PIN 25	PIN 26	STANDARD
LOW	LOW	auto/no colour
LOW	HIGH	PAL
HIGH	LOW	NTSC
HIGH	HIGH	SECAM

**Table 4** Crystal logic (pins 23 and 24)

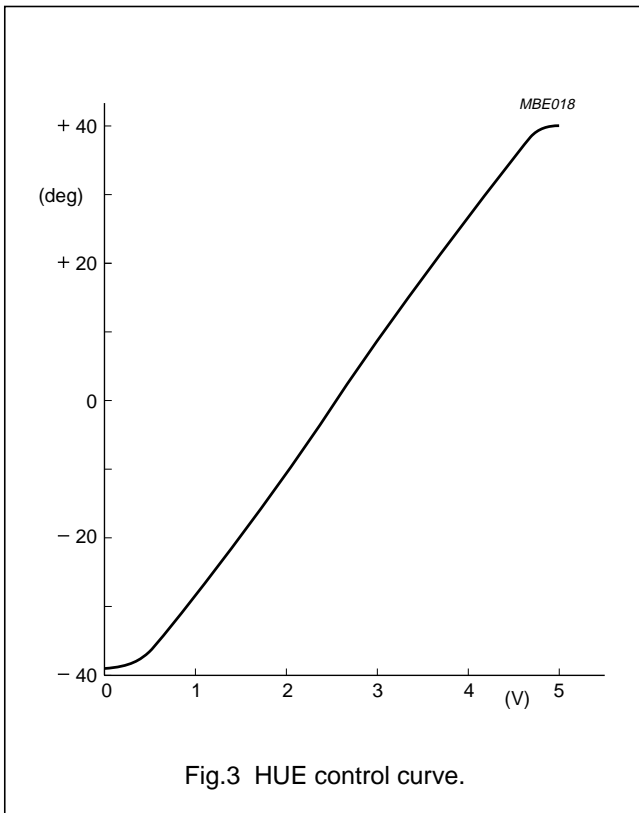
PIN 23	PIN 24	SELECTED CRYSTAL (MHz)
LOW	LOW	4.43
LOW	HIGH	3.579 (NTSC)
HIGH	LOW	3.575 (PAL-M)
HIGH	HIGH	3.582 (PAL-N)

**Table 5** Control logic RGB switch (pins 13 and 52)

PIN 13	PIN 52	RGB OUTPUT	FAST BLANKING OUTPUT
LOW	LOW	black	LOW
LOW	HIGH	RGB 2	HIGH
HIGH	LOW	RGB 1	HIGH
HIGH	HIGH	RGB 2	HIGH

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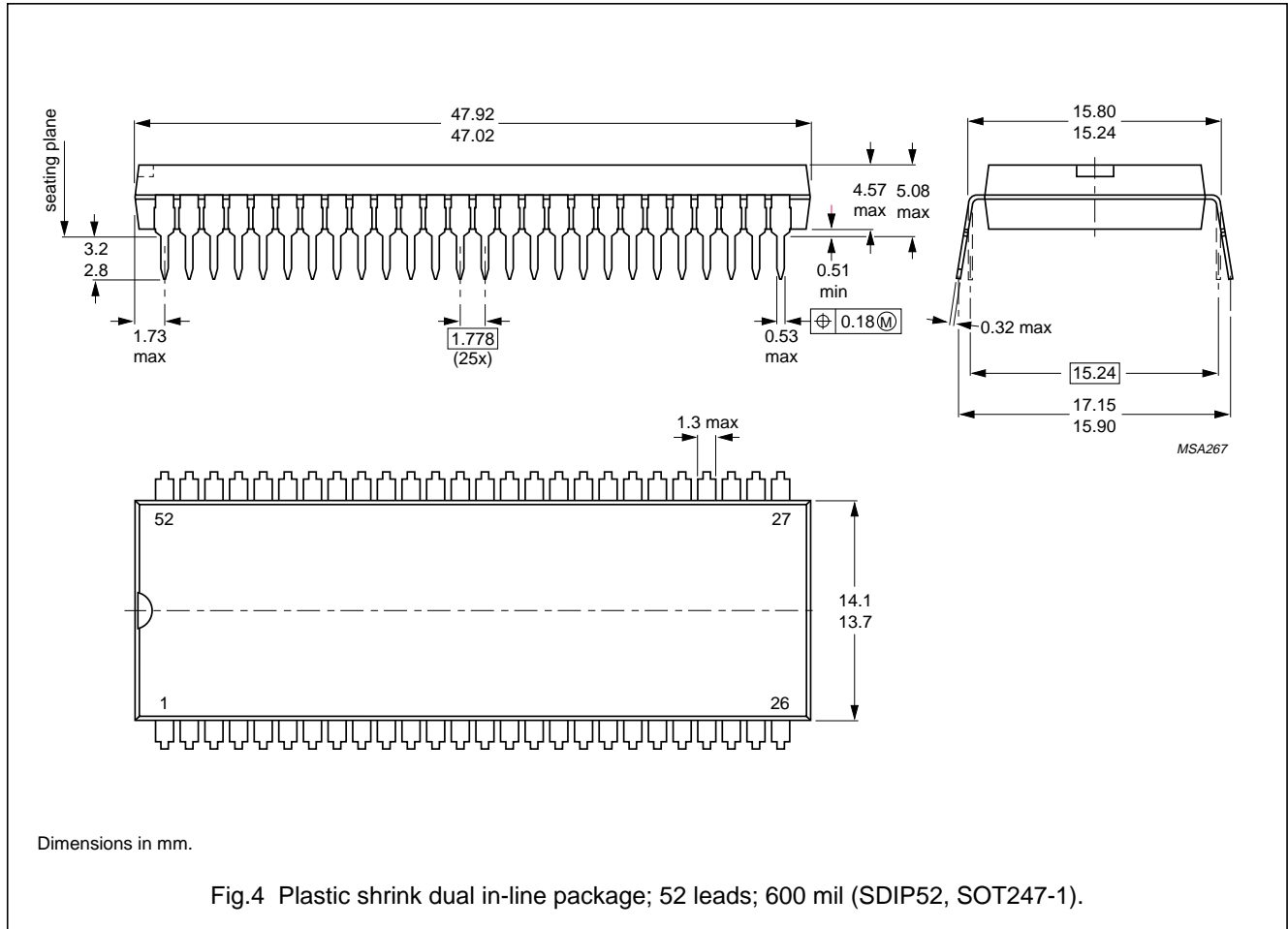
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PACKAGE OUTLINE



**SOLDERING**

**Plastic dual in-line packages**

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**REPAIRING SOLDERED JOINTS**

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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