

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LCX16245AFT

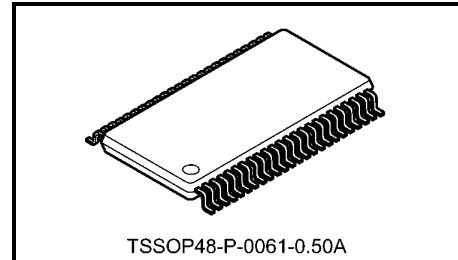
## Low-Voltage 16-Bit Bus Transceiver with 5-V Tolerant Inputs and Outputs

The TC74LCX16245AFT is a high-performance CMOS 16-bit bus transceiver. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 16-bit bus transceiver is controlled by direction control (DIR) inputs and output enable ( $\overline{OE}$ ) inputs which are common to each byte. It can be used as two 8-bit transceiver or one 16-bit transceiver. The direction of data transmission is determined by the level of the DIR inputs. The  $\overline{OE}$  inputs can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



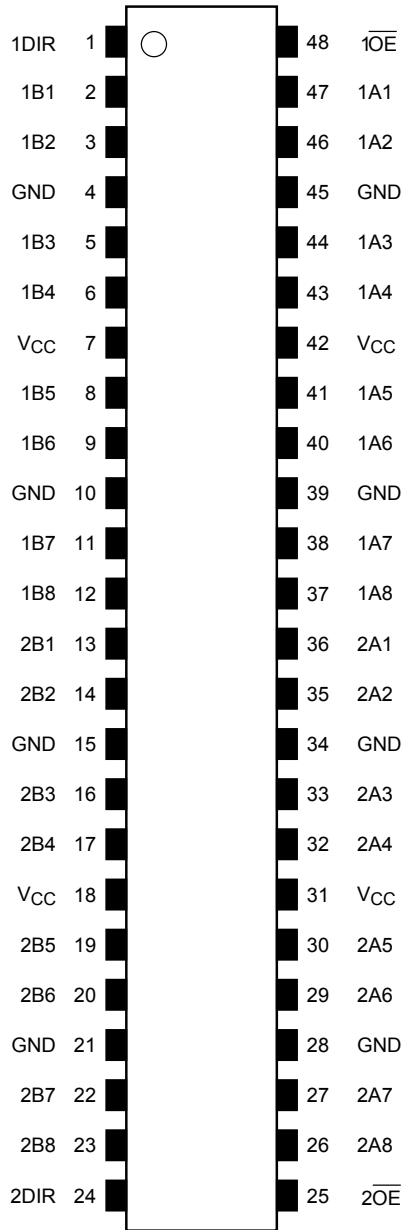
Weight: 0.25 g (typ.)

### Features (Note)

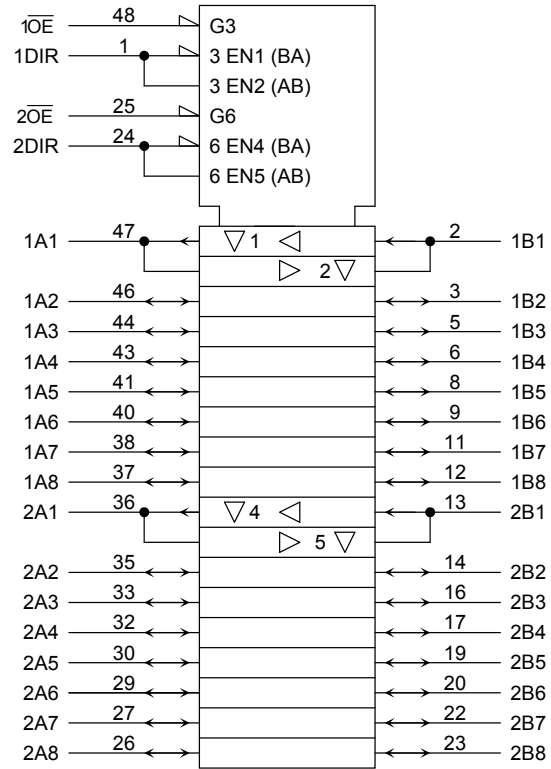
- Low-voltage operation:  $V_{CC} = 2.0$  to  $3.6$  V
- High-speed operation:  $t_{pd} = 5.2$  ns (max) ( $V_{CC} = 3.0$  to  $3.6$  V)
- Output current:  $|I_{OH}|/I_{OL} = 24$  mA (min) ( $V_{CC} = 3.0$  V)
- Latch-up performance:  $-500$  mA
- Package: TSSOP
- Bidirectional interface between 5.0 V and 3.3 V signals
- Power-down protection provided on all inputs and outputs

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.  
All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

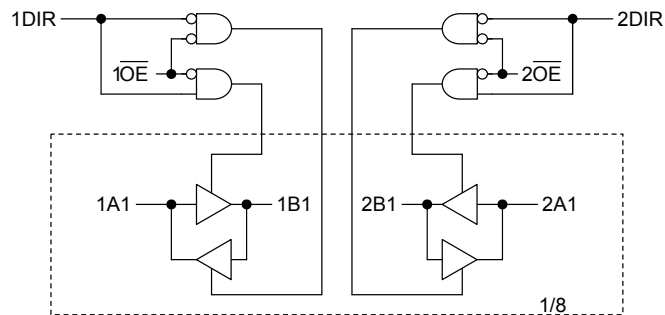
Inputs		Function		Outputs
$\overline{1OE}$	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

Inputs		Function		Outputs
$\overline{2OE}$	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don't care

Z: High impedance

## System Diagram



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 7.0	V
DC input voltage (DIR, $\overline{OE}$ )	$V_{IN}$	-0.5 to 7.0	V
DC bus I/O voltage	$V_{I/O}$	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 4)	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	400	mW
DC $V_{CC}$ /ground current per supply pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND, V_{OUT} > V_{CC}$

**Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	2.0 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage (DIR, $\overline{OE}$ )	$V_{IN}$	0 to 5.5	V
Bus I/O voltage	$V_{I/O}$	0 to 5.5 (Note 3)	V
		0 to $V_{CC}$ (Note 4)	
Output current	$I_{OH}/I_{OL}$	$\pm 24$ (Note 5)	mA
		$\pm 12$ (Note 6)	
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5:  $V_{CC} = 3.0$  to  $3.6$  V

Note 6:  $V_{CC} = 2.7$  to  $3.0$  V

Note 7:  $V_{IN} = 0.8$  to  $2.0$  V,  $V_{CC} = 3.0$  V

## Electrical Characteristics

### DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.7 to 3.6	2.0	—	V
	L-level	V <sub>IL</sub>	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12 mA	2.7	2.2	—	
				I <sub>OH</sub> = -18 mA	3.0	2.4	—	
				I <sub>OH</sub> = -24 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7 to 3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	—	20.0	μA
			V <sub>IN</sub> /V <sub>OUT</sub> = 3.6 to 5.5 V		2.7 to 3.6	—	±20.0	
Increase in I <sub>CC</sub> per input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7 to 3.6	—	500	

**AC Characteristics (Ta = -40 to 85°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2	2.7	—	6.2	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	5.2	
3-state output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	2.7	—	7.5	ns
	t <sub>pZH</sub>		3.3 ± 0.3	1.5	6.5	
3-state output disable time	t <sub>pLZ</sub>	Figure 1, Figure 3	2.7	—	7.0	ns
	t <sub>pHZ</sub>		3.3 ± 0.3	1.5	6.0	
Output to output skew	t <sub>osLH</sub>	(Note)	2.7	—	—	ns
	t <sub>osHL</sub>		3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.  
 (t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)

**Dynamic Switching Characteristics  
 (Ta = 25°C, input: t<sub>r</sub> = t<sub>f</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

**Capacitive Characteristics (Ta = 25°C)**

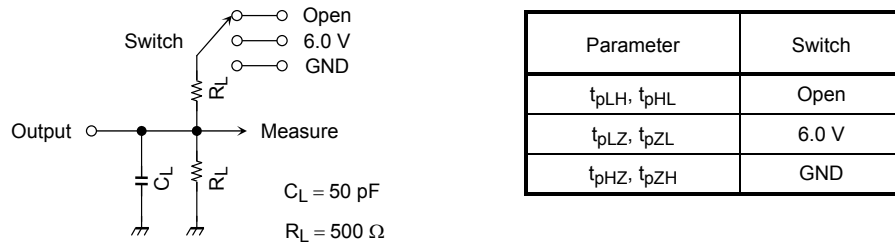
Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Input capacitance	C <sub>IN</sub>	—	3.3	7	pF
Bus input capacitance	C <sub>I/O</sub>	—	3.3	8	pF
Power dissipation capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note)	3.3	25	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

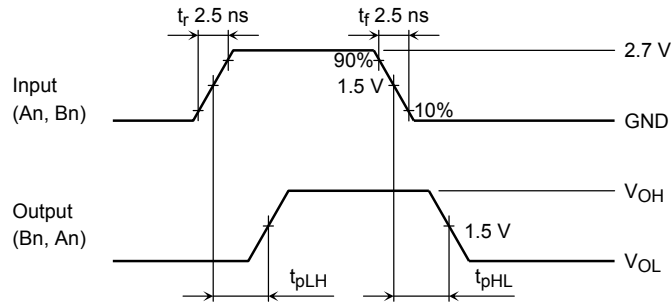
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

**AC Test Circuit**

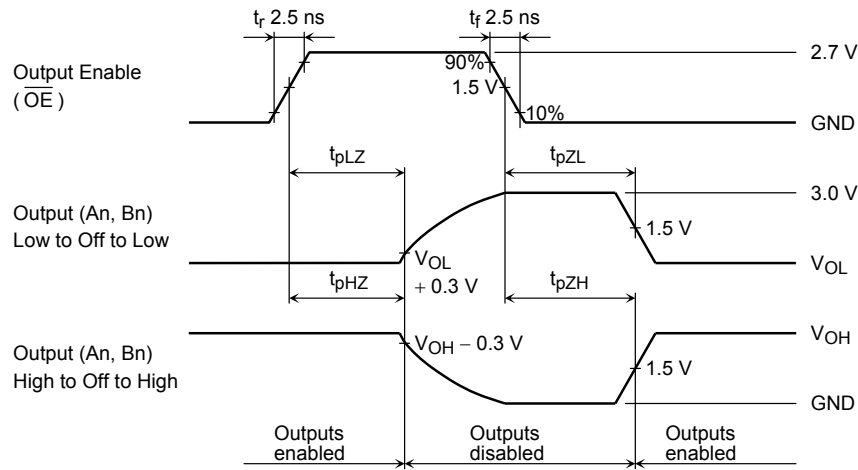


**Figure 1**

**AC Waveform**



**Figure 2  $t_{pLH}, t_{pHL}$**

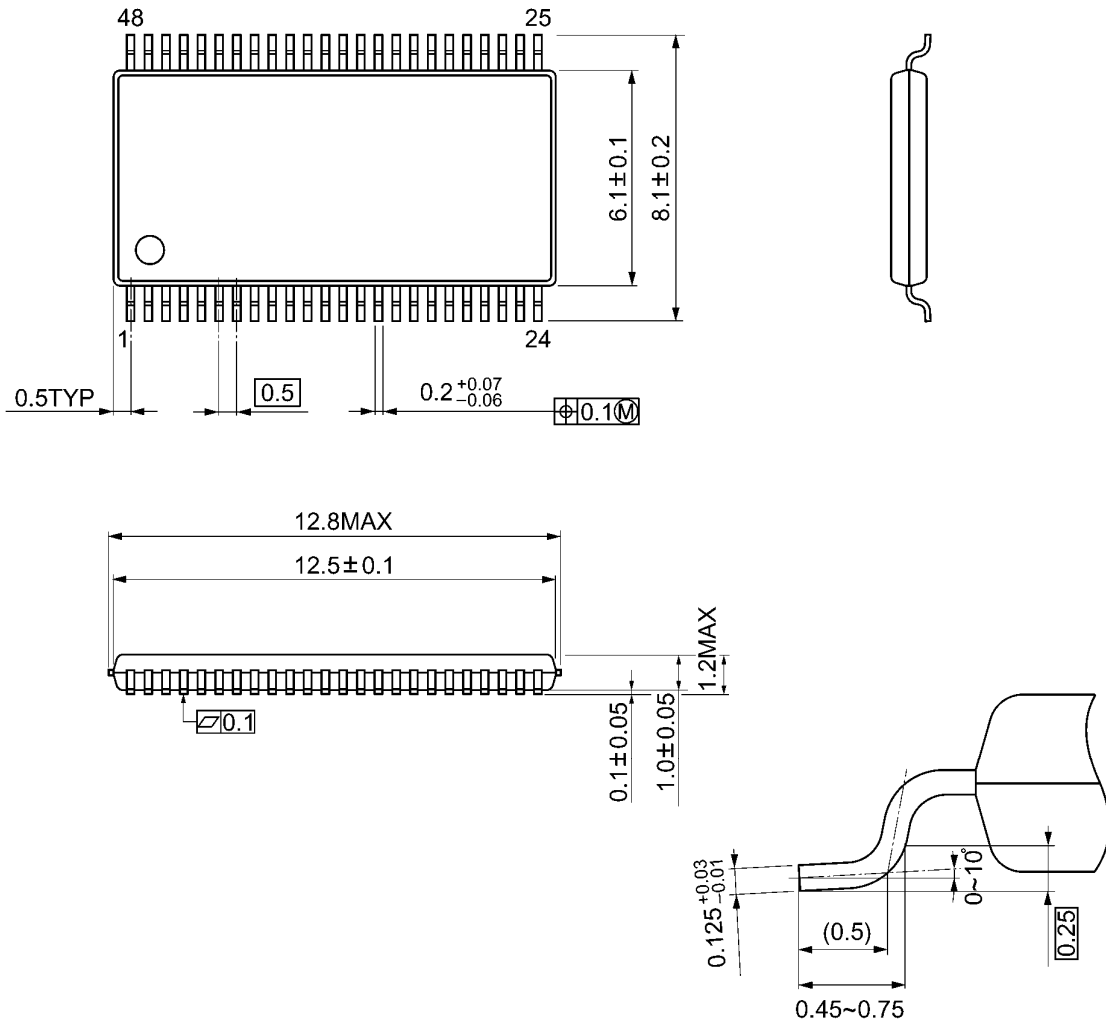


**Figure 3  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$**

## Package Dimensions

TSSOP48-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)



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20070701-EN GENERAL

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