Data Sheet

VSC7125

1.0625 Gbits/sec Fibre Channel Transceiver

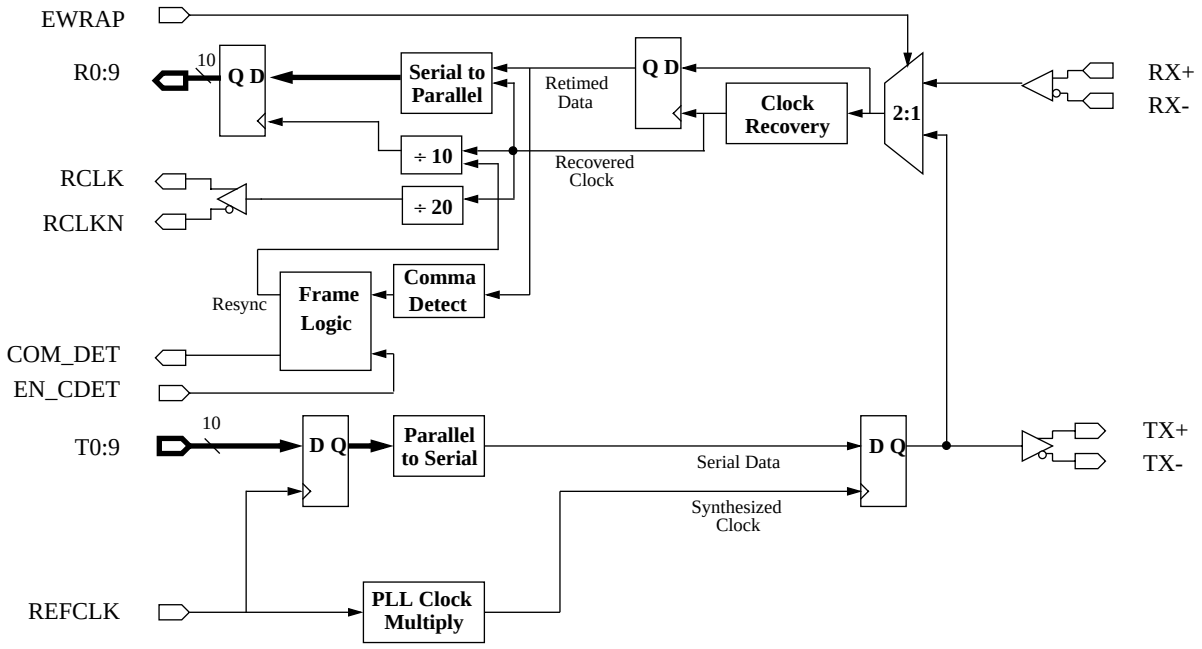
Features

- ANSI X3T11 Fibre Channel Compatible 1.0625 Gbps Full-duplex Transceiver
- 10 Bit TTL Interface for Transmit and Receive Data
- Monolithic Clock Synthesis and Clock Recovery - No External Components
- 106.25 MHz TTL Reference Clock
- Low Power Operation - 650 mW
- Suitable for Both Coaxial and Optical Link Applications
- 64 Pin, 10mm or 14mm PQFP
- Single +3.3V Power Supply

General Description

The VSC7125 is a full-speed Fibre Channel Transceiver optimized for Disk Drive and other space constrained applications. It accepts 10-bit 8B/10B encoded transmit data, latches it on the rising edge of REFCLK and serializes it onto the TX PECL differential outputs at a baud rate which is ten times the REFCLK frequency. The VSC7125 also samples serial receive data on the RX PECL differential inputs, recovers the clock and data, deserializes it onto the 10-bit receive data bus, outputs two recovered clocks at one twentieth of the incoming baud rate and detects Fibre Channel "Comma" characters. The VSC7125 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components.

VSC7125 Block Diagram



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Functional Description

Clock Synthesizer

The VSC7125 clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock at nominally 1.0625 GHz. The clock synthesizer contains a fully monolithic PLL which does not require any external components.

Serializer

The VSC7125 accepts TTL input data as a parallel 10 bit character on the T0:9 bus which is latched into the input latch on the rising edge of REFCLK. This data will be serialized and transmitted on the TX PECL differential outputs at a baud rate of ten times the frequency of the REFCLK input, with bit T0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification, or an equivalent, edge rich, DC-balanced code.

Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. The 10 bit interface on the VSC7125 corresponds to a transmission character. This mapping is illustrated below.

Figure 1: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	X	X	X	1	1	1	1	1	0	0

Last Data Bit Transmitted — First Data Bit Transmitted

Clock Recovery

The VSC7125 accepts differential high speed serial inputs on the RX+/RX- pins, extracts the clock and retimes the data. The serial bit stream should be encoded to provide DC balance and limited run length by a Fibre Channel compatible 8B/10B transmitter or equivalent. The VSC7125 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 0.01% of ten times the REFCLK frequency. For example if the REFCLK used is 106.25MHz, then the incoming serial baud rate must be 1.0625 gigabaud $\pm$0.01%.

Deserializer

The retimed serial bit stream is converted into a 10-bit parallel output character. The VSC7125 provides complementary TTL recovered clocks, RCLK and RCLKN, which are at one twentieth of the serial baud rate. This architecture is designed to simplify demultiplexing of the 10-bit data characters into a 20-bit halfword in the downstream controller chip. The clocks are generated by dividing down the high-speed clock which is phase locked to the serial data. The serial data is retimed by the internal high-speed clock, and deserialized. The

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resulting parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN. In order to maximize the setup and hold times available at this interface, the parallel data is loaded into the output register at a point nominally midway between the transition edges of RCLK and RCLKN.

If serial input data is not present, or does not meet the required baud rate, the VSC7125 will continue to produce a recovered clock so that downstream logic may continue to function. The RCLK and RCLKN output frequency under these circumstances may differ from their expected frequency by no more than ±1%.

Word Alignment

The VSC7125 provides 7-bit Fibre Channel comma character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the VSC7125 constantly examines the serial data for the presence of the Fibre Channel “comma” character. This pattern is “0011111XXX”, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which is defined specifically for synchronization in Fibre Channel systems. Improper alignment of the comma character is defined as any of the following conditions:

1) The comma is not aligned within the 10-bit transmission character such that T0...T6 = “0011111”
2) The comma straddles the boundary between two 10-bit transmission characters.
3) The comma is properly aligned but occurs in the received character presented during the rising edge of RCLK rather than RCLKN.

When EN_CDET is HIGH and an improperly aligned comma is encountered, the internal data is shifted in such a manner that the comma character is aligned properly in R0:9. This results in proper character and half-word alignment. When the parallel data alignment changes in response to an improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. However, the synchronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 2 and Figure 3. Figure 2 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the comma character on R0:9. Figure 3 shows the case where the K28.5 is detected, but it is out of phase and a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

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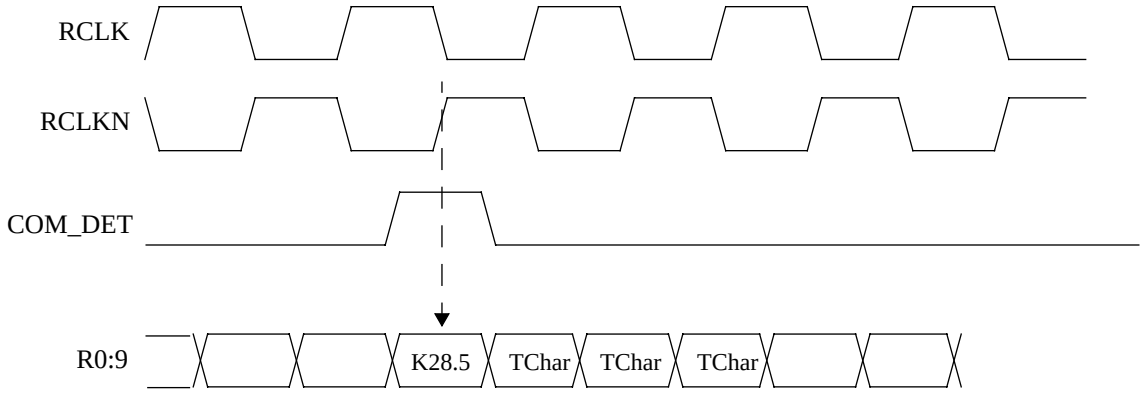
Figure 2: Detection of a Properly Aligned Comma Character



TChar: 10 bit Transmission Character

Figure 3: Detection and Resynchronization of an Improperly Aligned Comma

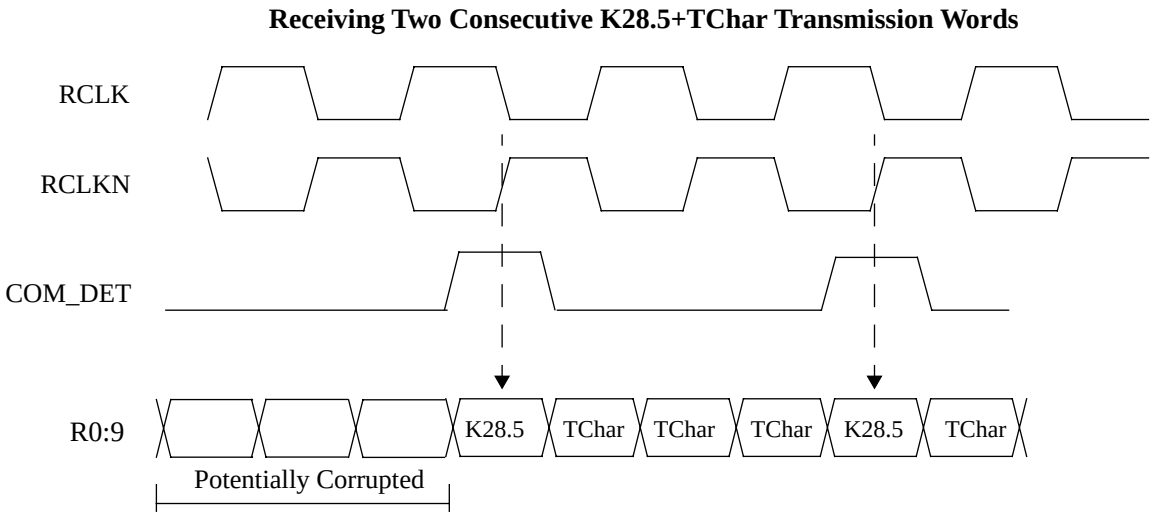


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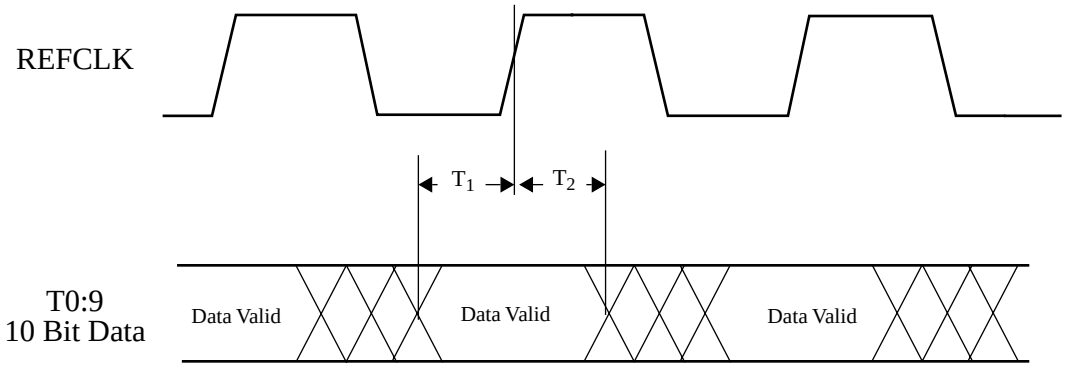
Figure 4: Transmit Timing Waveforms



AC Characteristics

Table 1: Transmit AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	T0:9 Setup time to the rising edge of REFCLK	1.5	—	ns.	Measured between the valid data level of T0:9 to the 1.4V point of REFCLK
T_2	T0:9 hold time after the rising edge of REFCLK	1.0	—	ns.	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—	300	ps.	20% to 80%, 75 Ohm load to Vss, Tested on a sample basis
T_{LAT}	Latency from rising edge of REFCLK to T0 appearing on TX+/TX-	11bc - 1ns		ns.	bc = Bit clocks ns = Nano second
Transmitter Output Jitter Allocation					
T_{rj}	Serial data output random jitter (RMS)	—	20	ps.	RMS, tested on a sample basis (refer to Figure 8)
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps.	Peak to peak, tested on a sample basis (refer to Figure 8)

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Table 2: Receive AC Characteristics

Parameters	Description	Min.	Max.	Units	Conditions
T_1	Data or COM_DET Valid prior to RCLK/RCLKN rise	4.0	—	ns.	Measured between the 1.4V point of RCLK or RCLKN and a valid level of R0:9. All outputs driving 10pF load.
T_2	Data or COM_DET Valid after RCLK or RCLKN rise	3.0	—	ns.	
T_3	Deviation of RCLK rising edge to RCLKN rising edge delay from nominal. $delay = \frac{f_{baud}}{10} \pm T_3$	-500	500	ps.	Nominal delay is 10 bit times. Tested on sample basis
T_4	Deviation of RCLK, RCLKN frequency from nominal. $f_{RCLK} = \frac{f_{REFCLK}}{2} \pm T_4$	-1.0	1.0	%	Whether or not locked to serial data
T_R, T_F	R0:9, COM_DET, RCLK, RCLKN rise and fall time	—	2.4	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$, into 10 pf. load.
R_{lat}	Latency from RX to R0:9	15bc + 2ns	34bc + 2ns		bc = Bit clock ns = Nano second
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs.	8B/10B IDLE pattern. Tested on a sample basis
Receive Data Jitter	Receive Data Jitter Power $\int_{100KHz}^{\frac{1}{2 \times BitTime}} PhaseNoise$	—	40	ps.	dBc, RMS for 10^{-12} Bit Error Ratio Tested on a sample basis

Note: Probability of recovery for data acquisition is 95% per section 5.3 of the FC-PH rev. 4.3.

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Figure 5: Receive Timing Waveforms

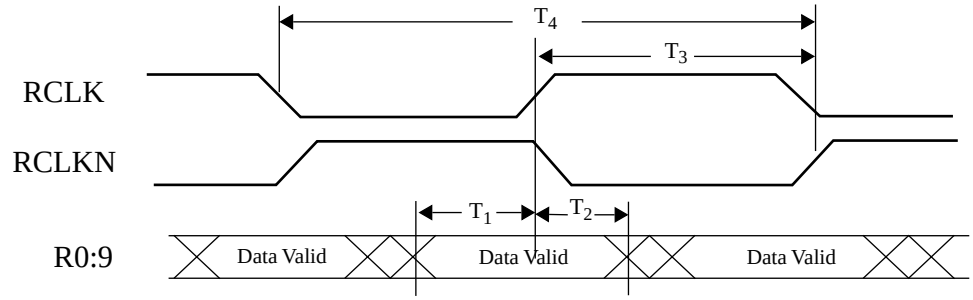

Figure 6: REFCLK Timing Waveforms

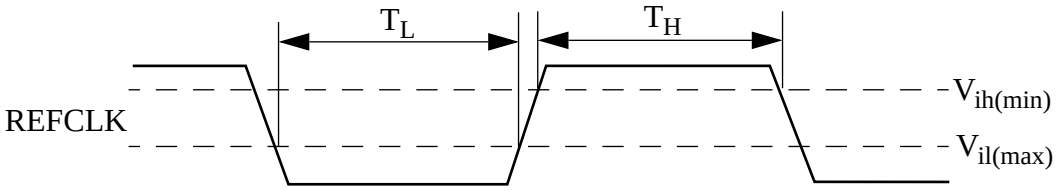

Table 3: Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FR	Frequency Range	100	110	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	200	ppm.	Maximum frequency offset between transmit and receive reference clocks on one link
DC	REFCLK duty cycle	30	70	%	Measured at 1.5V
T_{RCR},T_{RCF}	REFCLK rise and fall time	—	2.0	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	2	ps.	dbc, RMS for FC compliant output data jitter
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	40	ps.	dbc, RMS for 10^{-12} Bit Error Ratio with zero length external path. Tested on a sample basis

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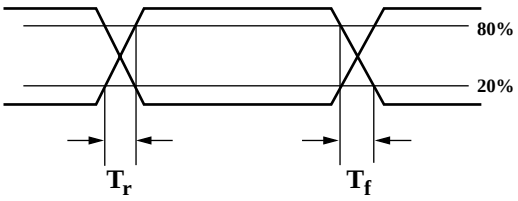
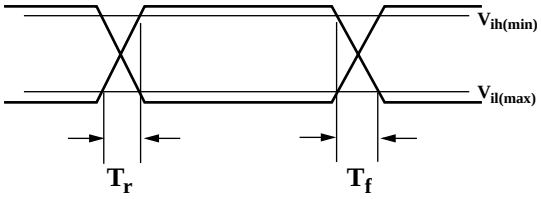
Figure 7: Parametric Measurement Information

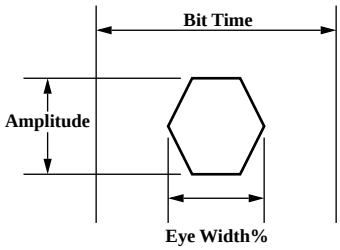
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

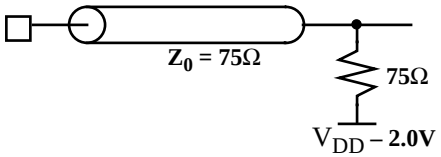


Receiver Input Eye Diagram Jitter Tolerance Mask



Parametric Test Load Circuit

Serial Output Load



TTL A.C. Output Load

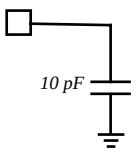


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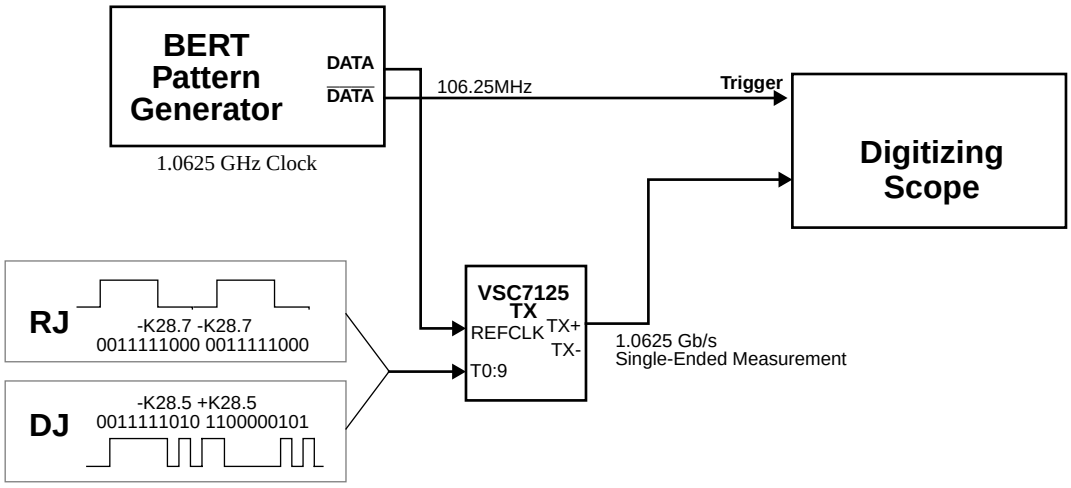
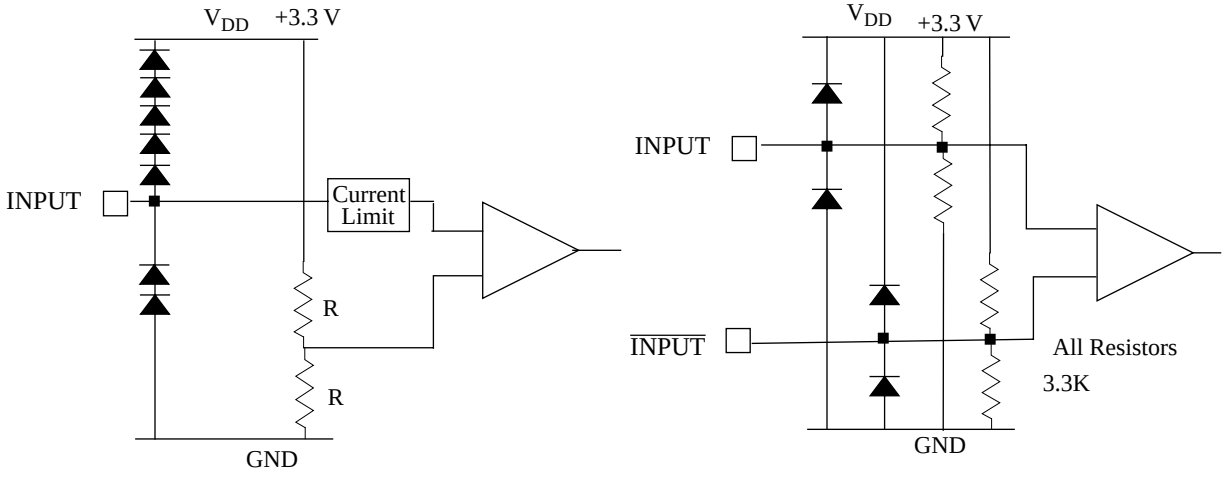
Figure 8: Transmitter Jitter Measurement Method



Random jitter (RJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ± 7 sigma of distribution.

Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variations.

Figure 9: Input Structures



REFCLK and TTL Inputs

A

High Speed Differential Input (RX+/RX-)

B

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DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT75}[1]	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V (TX+ - TX-)
ΔV_{OUT50}[1]	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V (TX+ - TX-)
ΔV_{IN}[1]	Receiver differential peak-to-peak Input Sensitivity RX	300	—	2600	mVp-p	Internally biased to Vdd/2 (RX+ - RX-)
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} =0.5V
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	625	900	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply Current	—	190	260	mA	Outputs open, V_{DD} = V_{DD} max

Note: (1) Refer to Application Note, AN-37, for differential measurement techniques.

Absolute Maximum Ratings *(1)*

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +100°C Case Temperature

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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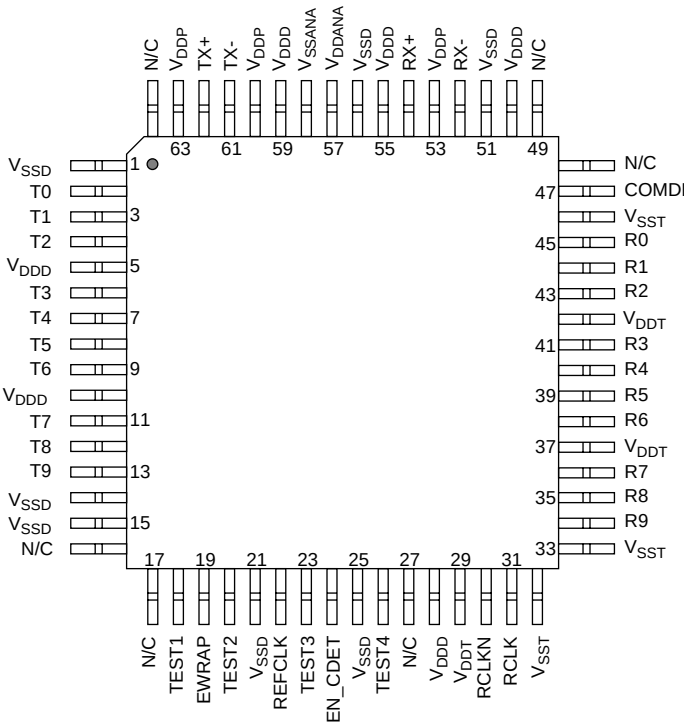
Package Pin Descriptions

Figure 10: Pin Diagram



(Top View)

Table 4: Pin Identification

Pin #	Name	Description
2-4, 6-9, 11-13	T0:9	INPUTS - TTL 10-bit transmit character. Parallel data on this bus is clocked in on the rising edge of REFCLK. The data bit corresponding to T0 is transmitted first.
22	REFCLK	INPUT - TTL This rising edge of this clock latches T0:9 into the input register. It also provides the reference clock, at one tenth the baud rate to the PLL.
62, 61	TX+, TX-	OUTPUTS - Differential PECL (AC Coupling recommended) These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW.
45-43, 41-38, 36-34	R0:9	OUTPUTS - TTL 10-bit received character. Parallel data on this bus is clocked out on the rising edges of RCLK and RCLKN. R0 is the first bit received on RX+/RX-.

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Table 4: Pin Identification

Pin #	Name	Description
19	EWRAP	INPUT - TTL LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled and the TX outputs are held HIGH.
54, 52	RX+, RX-	INPUTS - Differential PECL (AC Coupling recommended) The serial receive data inputs selected when EWRAP is LOW. Internally biased tot VDD/2, with 3.3KΩ resistors from each input pin to VDD and GND.
31, 30	RCLK, RCLKN	OUTPUT - Complementary TTL Recovered clocks derived from one twentieth of the RX+/- data stream. Each rising transition of RCLK or RCLKN corresponds to a new word on R0:9.
24	EN_CDET	INPUT - TTL Enables COMDET and word resynchronization when HIGH. When LOW, keeps current word alignment and disables COMDET.
47	COMDET	OUTPUT - TTL This output goes HIGH for half of an RCLK period to indicate that R0:9 contains a Comma Character (‘0011111XXX’). COMDET will go HIGH only during a cycle when RCLKN is rising. COMDET is enabled by EN_CDET being HIGH.
18,20,23	TEST1 TEST2 TEST3	INPUT These signals are used for factory test. For normal operation, tie to VDD.
26	TEST_4	OUTPUT This signal is used for factory test. For normal operation, leave open.
57	VDDANA	Analog Power Supply
58	VSSANA	Analog Ground
5, 10, 28, 50, 55, 59	VDDD	Digital Logic Power Supply
1, 14, 15, 21, 25, 51, 56	VSSD	Digital Logic Ground
29, 37, 42	VDDT	TTL Output Power Supply
32, 33, 46	VSST	TTL Output Ground
53, 60, 63	VDDP	PECL I/O Power Supply
16,17,27, 48,49,64	N/C	No Connection. These pins are not internally connected.

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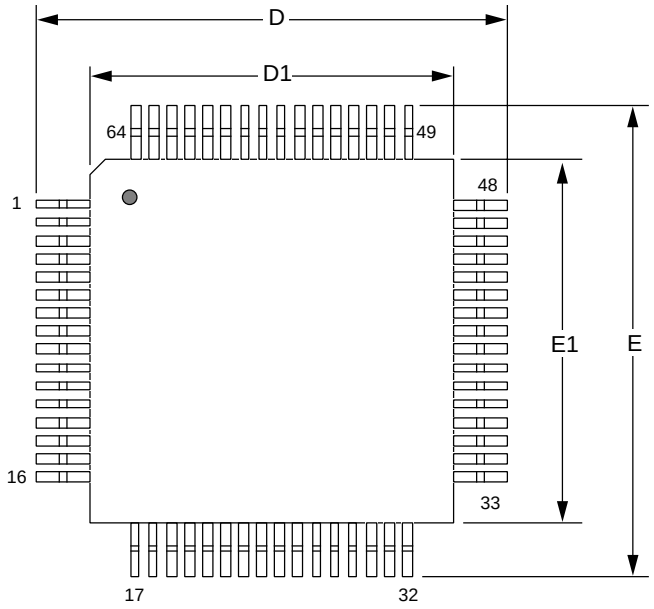
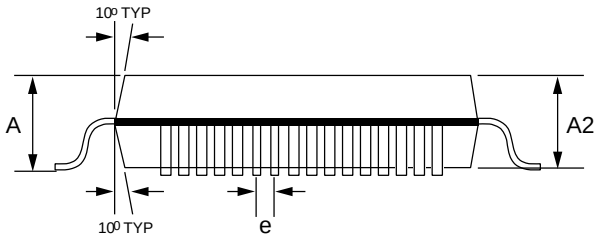
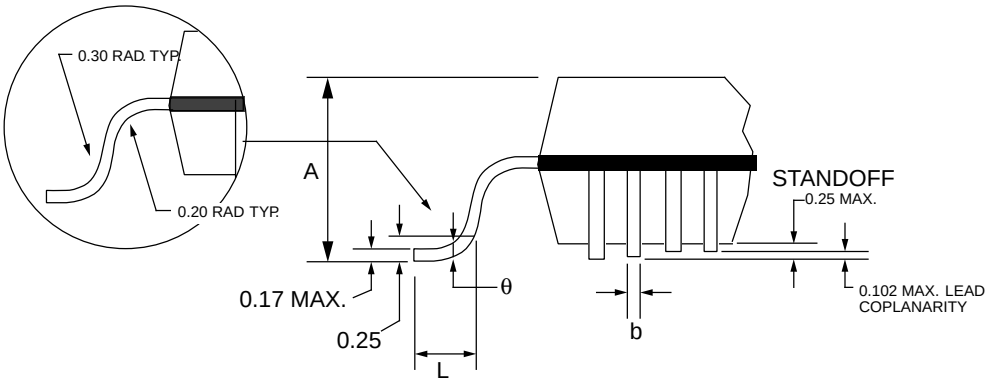
Package Information

64-pin PQFP Package Dimensions



Item	10 mm	14 mm	Tolerance
A	2.45	2.35	MAX
A2	2.00	2.00	+.10/-.05
D	13.20	17.20	±.25
D1	10.00	14.00	±.10
E	13.20	17.20	±.25
E1	10.00	14.00	±.10
b	0.22	0.35	±.05
e	0.50	0.80	BASIC
L	0.88	0.88	±.15/-.10
θ	0° - 7°		





NOTES:

All drawings not to scale
All units in mm unless otherwise noted.
10 x 10 mm Package # 101-266-1
14 x 14 mm Package # 101-262-1

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Package Thermal Considerations

The VSC7125 is packaged in either a 10 mm PQFP or a 14 mm PQFP with internal heat spreaders. These packages use industry-standard EIAJ footprints, but have been enhanced to improve thermal dissipation. The construction of the packages is as shown in Figure 11.

Figure 11: Package Cross Section

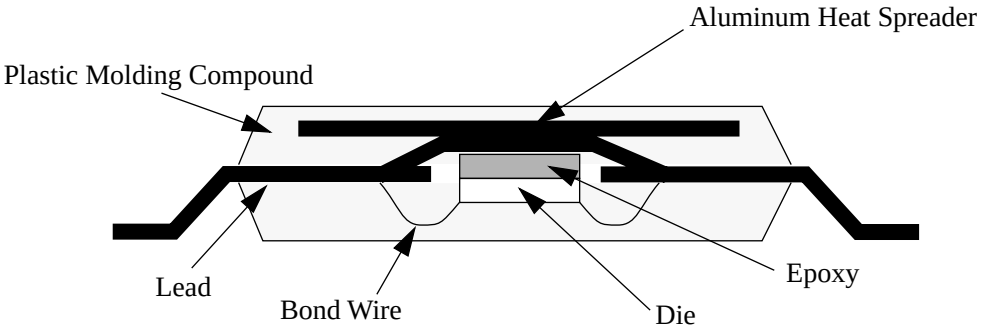

Table 5: Thermal Resistance

Symbol	*Description*	*10mm Value*	*14mm Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	10.5	10	^{o}C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	53	32	^{o}C/W
θ_{ca-100}	Thermal resistance from case to ambient with 100 LFM airflow	44	28	^{o}C/W
θ_{ca-200}	Thermal resistance from case to ambient with200 LFM airflow	39	25	^{o}C/W
θ_{ca-400}	Thermal resistance from case to ambient with 400 LFM airflow	34	22	^{o}C/W
θ_{ca-600}	Thermal resistance from case to ambient with 600 LFM airflow	31	20	^{o}C/W

The VSC7125 is designed to operate with a junction temperature up to 110^{o}C. The user must guarantee that the temperature specification is not violated. With the Thermal Resistances shown above, the 10x10mm PQFP can operate in still air ambient temperatures of 53^{o}C [53^{o}C=110^{o}C-0.9W*(10.5^{o}C/W+53^{o}C/W)] while the 14x14 PQFP can operate in still air ambient temperatures of 73^{o}C [73^{o}C=110^{o}C-0.9W*(10^{o}C/W+32^{o}C/W)]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7125xx

Device Type:

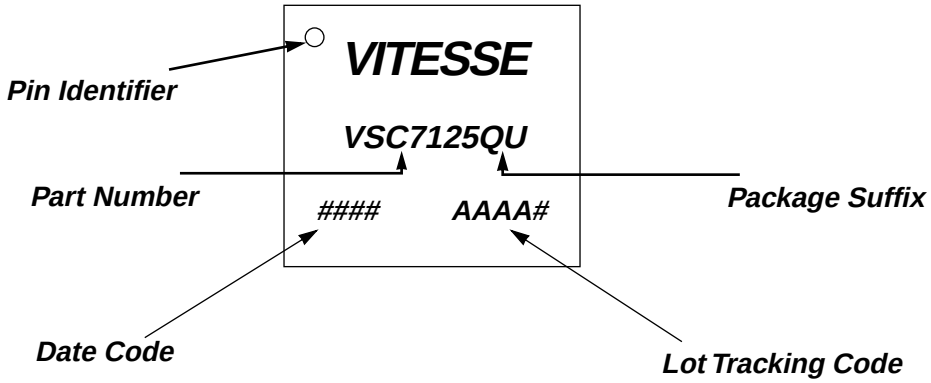
VSC7125: 1.0625 Gbps Transceiver

Package Style (64-pin)

QN: 14x14mm PQFP
QU: 10x10mm PQFP

Marking Information

The package is marked with three lines of text as shown below (QU Package):



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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