

# DATA SHEET

**TDA8580J**

**Multi-purpose power amplifier**

Preliminary specification  
Supersedes data of 1998 Feb 25  
File under Integrated Circuits, IC01

2000 Apr 18

**Multi-purpose power amplifier****TDA8580J****FEATURES****General**

- Supply voltage range from 8 to 24 V
- Low distortion
- Few external components, fixed gain
- High output power
- Can be used as a stereo amplifier in Bridge-Tied Load (BTL) or quad Single-Ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode with one- or two-pin operation
- Diagnostic information for Dynamic Distortion Detector (DDD), high temperature (145 °C) and short-circuit
- No switch on/off pops when switching between standby and mute or mute and on; an external RC-network is prescribed to ensure pop-free operation
- Low offset variation at outputs between mute and on
- Fast mute on supply voltage drops.

**Protection**

- Short-circuit proof to ground, positive supply voltage and across load; the supply voltage ranges where the different short circuit conditions are guaranteed are given in Chapter "Limiting values"
- ESD protected on all pins
- Thermal protection against temperatures exceeding 150 °C.

**GENERAL DESCRIPTION**

The TDA8580J is a stereo Bridge-Tied Load (BTL) or a quad Single-Ended (SE) amplifier that operates over a wide supply voltage range from 8 to 24 V. This makes it suitable for applications such as television, home-sound systems and active speakers.

Because of an internal voltage buffer, this device can be used without a capacitor connected in series with the load (SE application). A combined BTL and 2 × SE application can also be configured (one chip stereo and subwoofer application).

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8580J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

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## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	operating supply voltage		8.0	14.4	24	V
$I_{q(\text{tot})}$	total quiescent current	$V_P = 14.4 \text{ V}$	–	140	170	mA
$I_{\text{stb}}$	standby supply current	$V_P = 14.4 \text{ V}$	–	1	50	$\mu\text{A}$
<b>Bridge-tied load application</b>						
$G_V$	voltage gain		31	32	33	dB
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	14	15	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$ ; $R_L = 8 \Omega$	21	23	–	W
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$ ; $P_o = 1 \text{ W}$ ; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 1 \text{ kHz}$ ; $P_o = 10 \text{ W}$ ; $V_P = 24 \text{ V}$ ; $R_L = 8 \Omega$	–	0.02	0.05	%
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$ ; mute condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$ ; on condition	–	0	140	mV
$V_{\text{no}}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$	–	100	150	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ ; on or mute condition; $R_S = 0 \Omega$	50	60	–	dB
<b>Single-ended application</b>						
$G_V$	voltage gain		25	26	27	dB
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	3.8	4.0	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$ ; $R_L = 4 \Omega$	10.5	11.5	–	W
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$ ; mute condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$ ; on condition	–	0	100	mV
$V_{\text{no}}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$	–	80	120	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ ; on or mute condition; $R_S = 0 \Omega$	40	45	–	dB

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BLOCK DIAGRAM

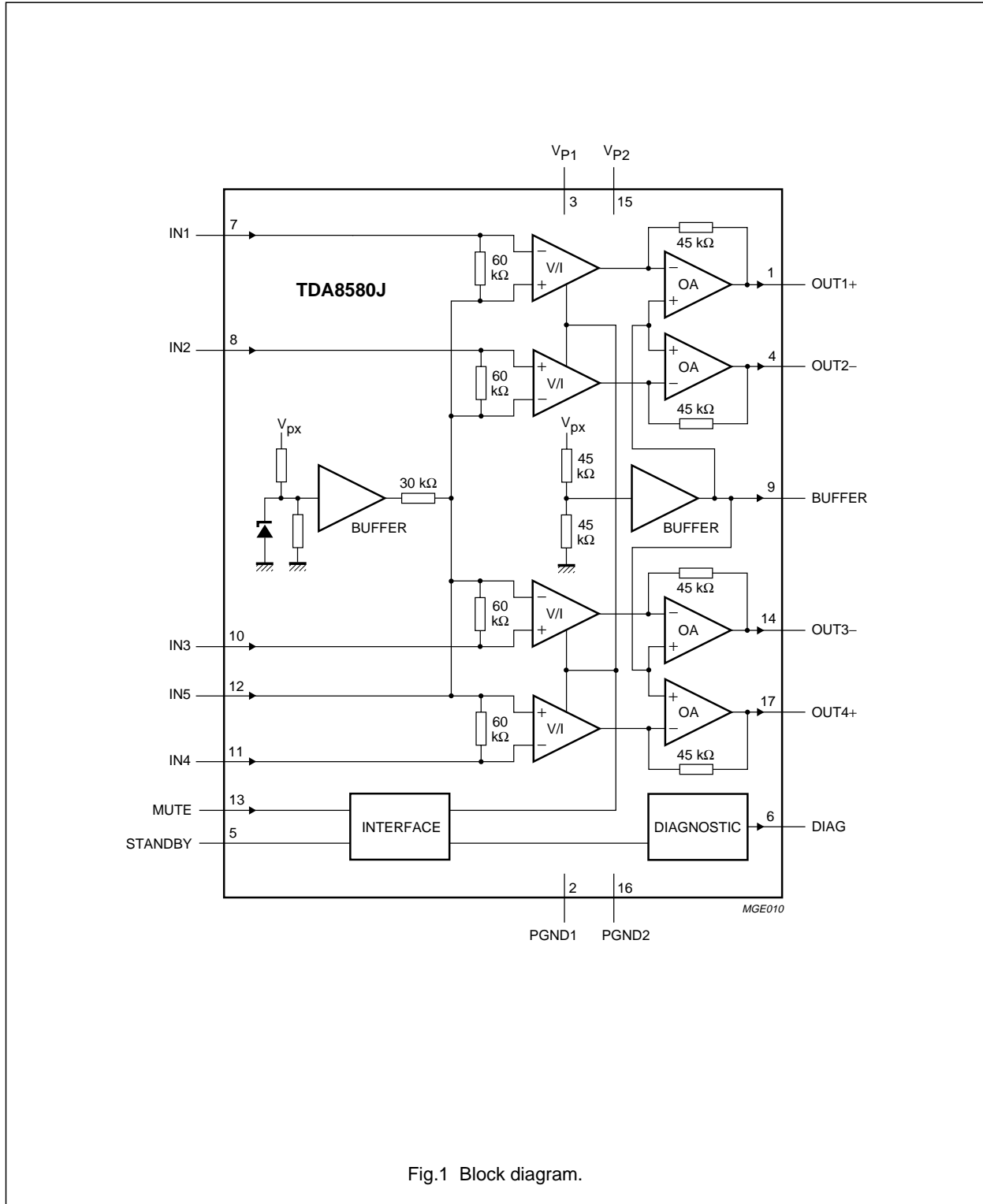


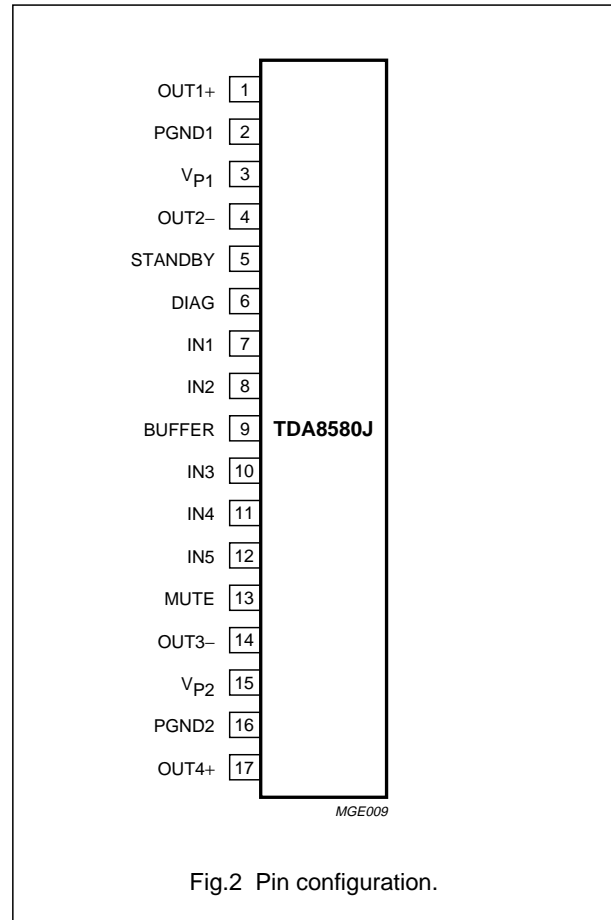
Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
OUT1+	1	non-inverting output 1
PGND1	2	power ground 1
V <sub>P1</sub>	3	supply voltage 1
OUT2-	4	inverting output 2
STANDBY	5	standby/mute/on selection input
DIAG	6	diagnostic output
IN1	7	input 1
IN2	8	input 2
BUFFER	9	single-ended buffer output
IN3	10	input 3
IN4	11	input 4
IN5	12	input 5; signal ground capacitor connection
MUTE	13	mute/on selection input
OUT3-	14	inverting output 3
V <sub>P2</sub>	15	supply voltage 2
PGND2	16	power ground 2
OUT4+	17	non-inverting output 4



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**FUNCTIONAL DESCRIPTION**

The TDA8580J is a multi-purpose power amplifier with four amplifiers which can be connected in the following configurations with high output power and low distortion (at minimum quiescent current):

- Dual bridge-tied load amplifiers
- Quad single-ended amplifiers
- Dual single-ended amplifiers and one bridge-tied load amplifier.

The amplifier can be switched in on, mute and off (standby) by the MUTE and STANDBY pins (for interfacing directly with a microcontroller). One-pin operation is also possible by applying a voltage greater than 8 V to the STANDBY pin to switch the amplifier in on mode.

Special attention is given to the dynamic behaviour as follows:

- Slow offset change between mute and on (controlled by MUTE and STANDBY pins)

- Low noise levels, which are independent of the supply voltage.

Protections are included to avoid the IC being damaged at:

- Over temperature:  $T_j > 150\text{ °C}$
- Short-circuit of the output pin(s) to ground or supply rail; when short-circuited, the power dissipation is limited
- ESD protection (Human Body Model 3000 V, Machine Model 300 V)
- Energy handling. A DC voltage of 6 V can be connected to the output of any amplifier while the supply pins are short-circuited to ground.

Diagnostics are available for the following conditions (see Figs 3, 4 and 5):

- Chip temperature above 145 °C
- Distortion over 2% due to clipping
- Short-circuit protection active.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage	operating	–	24	V
		no signal condition	–	28	V
V <sub>DIAG</sub>	voltage on pin DIAG		–	18	V
I <sub>OSM</sub>	non-repetitive peak output current		–	6	A
I <sub>ORM</sub>	repetitive peak output current		–	4.5	A
V <sub>P(scol)</sub>	supply voltage with short-circuit across load		–	28	V
V <sub>P(scg)</sub>	supply voltage with short-circuit from output to ground		–	26	V
V <sub>P(scs)</sub>	supply voltage with short-circuit from output to supply		–	16	V
V <sub>P(rp)</sub>	reverse polarity		–	6	V
P <sub>tot</sub>	total power dissipation		–	75	W
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>stg</sub>	storage temperature		–55	+150	°C
T <sub>amb</sub>	ambient temperature		–40	+85	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	40	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case		1.5	K/W

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**CHARACTERISTICS**

$V_P = 14.4\text{ V}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ;  $f_i = 1\text{ kHz}$ ;  $R_L = \infty$ ; measured in test circuit of Fig.28; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_P$	operating supply voltage		8.0	14.4	24	V
$I_{q(\text{tot})}$	total quiescent current		–	140	170	mA
$I_{\text{stb}}$	standby current		–	1	50	$\mu\text{A}$
$V_O$	DC output voltage		–	7.0	–	V
$V_{P(\text{mute})}$	low supply voltage mute		6.0	7.0	8.0	V
$V_I$	DC input voltage		–	4.0	–	V
<b>Control pins</b>						
STANDBY PIN (see Table 1)						
$V_{5(\text{stb})}$	voltage at STANDBY pin for standby condition		0	–	0.8	V
$V_{\text{hys}(5)(\text{stb})}$	hysteresis voltage at STANDBY pin for standby condition	note 1	–	0.2	–	V
$V_{5(\text{mute})}$	voltage at STANDBY pin for mute condition	$V_{13} < 0.8\text{ V}$	2.0	–	5.3	V
$V_{5(\text{on})}$	voltage at STANDBY pin for on condition	$V_P > 9\text{ V}$ ; note 2	8.0	–	18	V
MUTE PIN (see Table 1)						
$V_{13(\text{mute})}$	voltage at MUTE pin for mute condition	$V_5 = 5\text{ V}$	0	–	0.8	V
$V_{13(\text{on})}$	voltage at MUTE pin for on condition	$V_5 = 5\text{ V}$	2.5	–	5.3	V
<b>Diagnostic; output buffer (open-collector);</b> see Figs 3, 4 and 5						
$V_{\text{OL}}$	LOW-level output voltage	$I_{\text{sink}} = 1\text{ mA}$	–	0.2	0.8	V
$I_{\text{LI}}$	leakage current	$V_{\text{DIAG}} = 14.4\text{ V}$	–	–	1	$\mu\text{A}$
CD	clip detector	$V_{\text{DIAG}} < 0.8\text{ V}$	1	2	4	%
$T_{j(\text{diag})}$	junction temperature for high temperature warning	$V_{\text{DIAG}} < 0.8\text{ V}$	–	145	–	$^{\circ}\text{C}$
<b>Stereo BTL application;</b> see Figs 6, 7, 10, 11, 14, 15, 18, 19, 21, 22, 23, 24, 26 and 28						
THD	total harmonic distortion	$f_i = 10\text{ kHz}$ ; $P_o = 1\text{ W}$ ; $R_L = 4\ \Omega$ ; filter: $22\text{ Hz} < f < 30\text{ kHz}$	–	0.2	0.3	%
		$f_i = 1\text{ kHz}$ ; $P_o = 1\text{ W}$ ; $V_P = 14.4\text{ V}$ ; $R_L = 4\ \Omega$	–	0.05	0.1	%
		$f_i = 1\text{ kHz}$ ; $P_o = 10\text{ W}$ ; $V_P = 24\text{ V}$ ; $R_L = 8\ \Omega$	–	0.02	0.05	%
$P_o$	output power	THD = 0.5%; $V_P = 14.4\text{ V}$ ; $R_L = 4\ \Omega$	14	15	–	W
		THD = 0.5%; $V_P = 24\text{ V}$ ; $R_L = 8\ \Omega$	21	23	–	W
		THD = 10%; $V_P = 14.4\text{ V}$ ; $R_L = 4\ \Omega$	18	20	–	W
		THD = 10%; $V_P = 24\text{ V}$ ; $R_L = 8\ \Omega$	28	30	–	W
$G_v$	voltage gain	$V_{o(\text{rms})} = 3\text{ V}$	31	32	33	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{cs}$	channel separation	$P_o = 2 \text{ W}$ ; $f_i = 1 \text{ kHz}$ ; $R_L = 4 \Omega$	60	65	–	dB
$ \Delta G_V $	channel unbalance		–	–	1	dB
$V_{\text{offset(DC)}}$	DC output offset voltage	on condition	–	0	140	mV
		mute condition; $R_L = 4 \Omega$	–	10	20	mV
$V_{no}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$ ; note 3	–	100	150	$\mu\text{V}$
$V_{no(\text{mute})}$	noise output voltage mute	note 3	–	0	20	$\mu\text{V}$
$V_{o(\text{mute})}$	output voltage mute	$V_{i(\text{rms})} = 1 \text{ V}$	–	3	500	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$R_S = 0 \Omega$ ; $f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ ; on or mute condition	50	60	–	dB
$Z_i$	input impedance		23	30	37	$\text{k}\Omega$
CMRR	common mode rejection ratio	$R_S = 0 \Omega$ ; $V_{i(\text{rms})} = 0.5 \text{ V}$ ; $f_i = 1 \text{ kHz}$	–	60	–	dB
<b>Quad SE application; see Figs 8, 9, 12, 13, 16, 17, 20, 25, 27 and 29</b>						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$ ; $P_o = 1 \text{ W}$ ; $R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 10 \text{ kHz}$ ; $P_o = 1 \text{ W}$ ; $R_L = 4 \Omega$ ; filter: $22 \text{ Hz} < f < 30 \text{ kHz}$	–	0.2	0.3	%
		$f_i = 1 \text{ kHz}$ ; $P_o = 1 \text{ W}$ ; $V_P = 24 \text{ V}$ ; $R_L = 4 \Omega$ ; filter: $22 \text{ Hz} < f < 30 \text{ kHz}$	–	0.05	0.1	%
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	3.8	4.0	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$ ; $R_L = 4 \Omega$	10.5	11.5	–	W
		THD = 10%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	4.9	5.2	–	W
		THD = 10%; $V_P = 24 \text{ V}$ ; $R_L = 4 \Omega$	14	15	–	W
$G_V$	voltage gain	$V_{o(\text{rms})} = 3 \text{ V}$	25	26	27	dB
$\alpha_{cs}$	channel separation	$P_o = 2 \text{ W}$ ; $f_i = 1 \text{ kHz}$ ; $R_L = 4 \Omega$	40	46	–	dB
$ \Delta G_V $	channel unbalance		–	–	1	dB
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$ ; on condition	–	0	100	mV
		$V_P = 14.4 \text{ V}$ ; mute condition; $R_L = 4 \Omega$	–	10	20	mV
$V_{no}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$ ; note 3	–	80	120	$\mu\text{V}$
$V_{no(\text{mute})}$	noise output voltage mute	note 3	–	0	20	$\mu\text{V}$
$V_{o(\text{mute})}$	output voltage mute	$V_{i(\text{rms})} = 1 \text{ V}$	–	3	500	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ , on or mute condition; $R_S = 0 \Omega$	40	45	–	dB
$Z_i$	input impedance		46	60	74	$\text{k}\Omega$
CMRR	common mode rejection ratio	$V_{i(\text{rms})} = 0.5 \text{ V}$ ; $f_i = 1 \text{ kHz}$ ; $R_S = 0 \Omega$	–	60	–	dB

**Notes**

1. Hysteresis between the rise and fall voltage when pin STANDBY is controlled with low ohmic voltage source.
2. At lower  $V_P$  the voltage at the STANDBY pin for on condition will be adjusted automatically to maintain an on condition at low battery voltage (down to 8 V) when using one-pin operation.
3. The noise output is measured in a bandwidth of 20 Hz to 20 kHz.

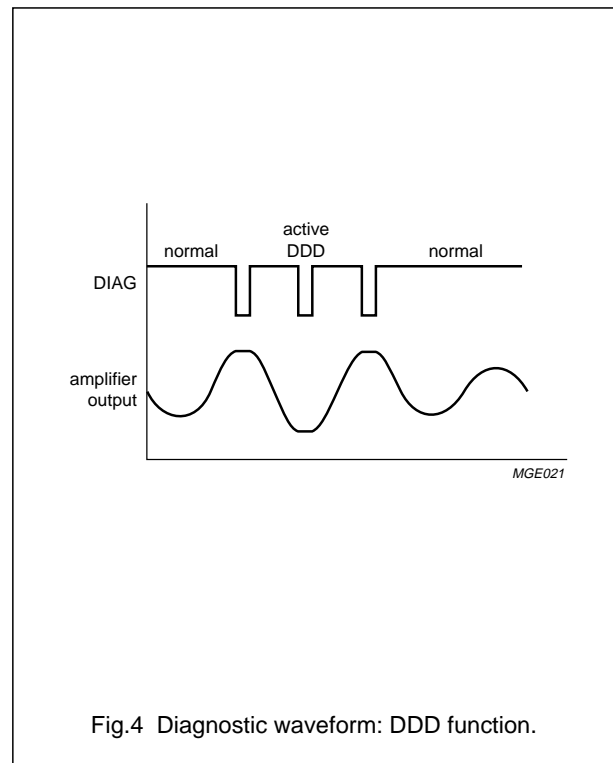
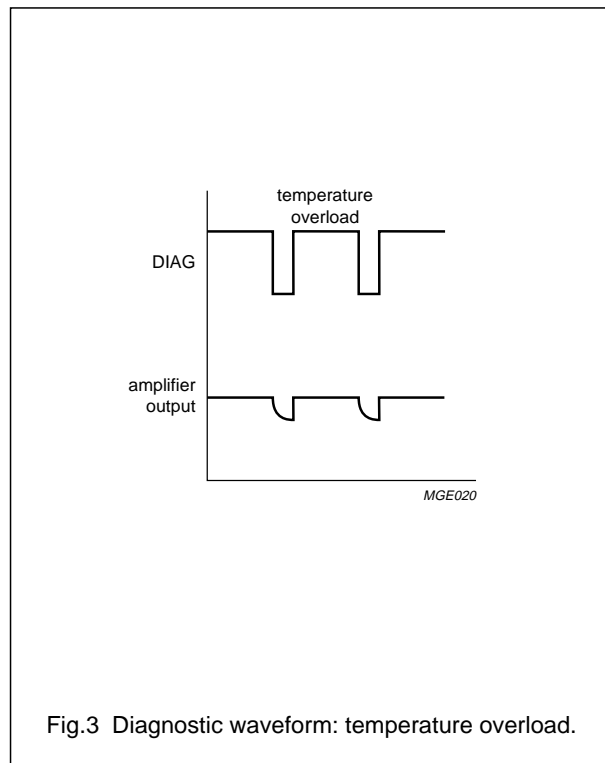


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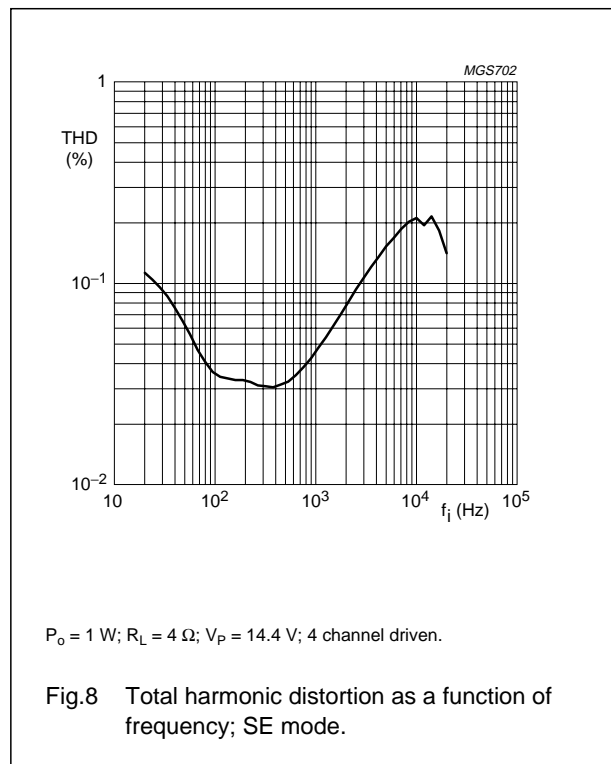
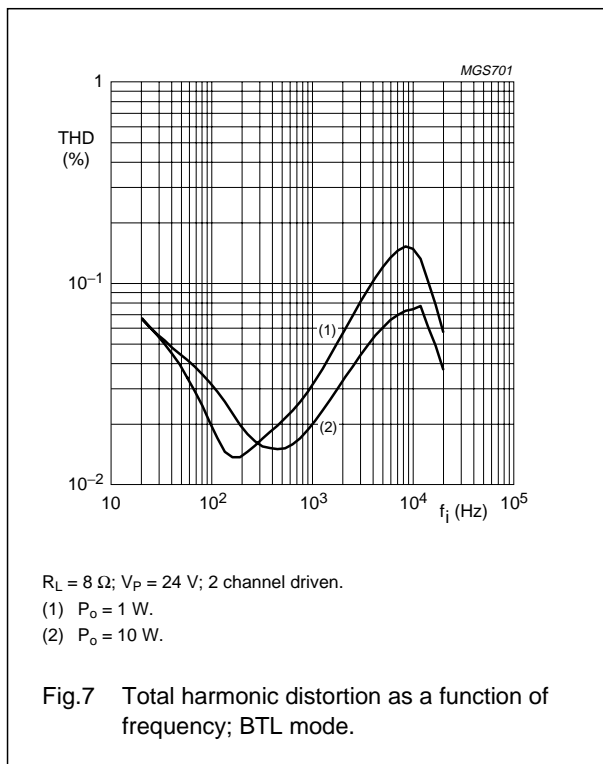
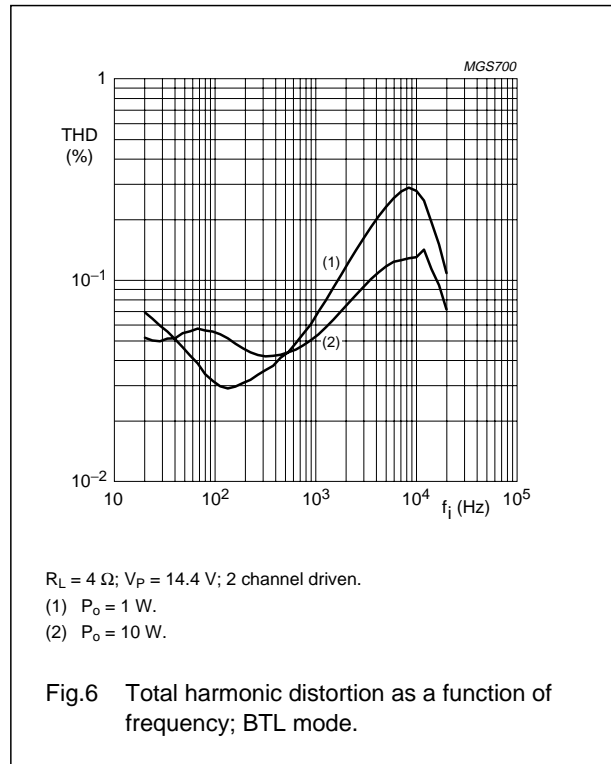
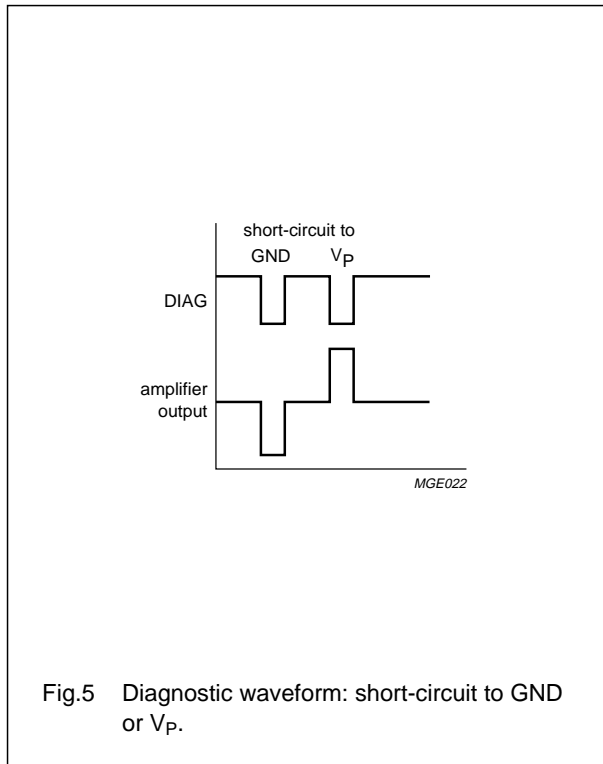
**Table 1** Selection of standby, mute and on

VOLTAGE AT PIN STANDBY	VOLTAGE AT PIN MUTE	FUNCTION
< 0.8 V	don't care	standby (off)
2 to 5.3 V	< 0.8 V	mute (DC settled)
2 to 5.3 V	2.5 to 5.3 V	on (AC operating)
$\geq 8.0$ V	don't care	on (AC operating)



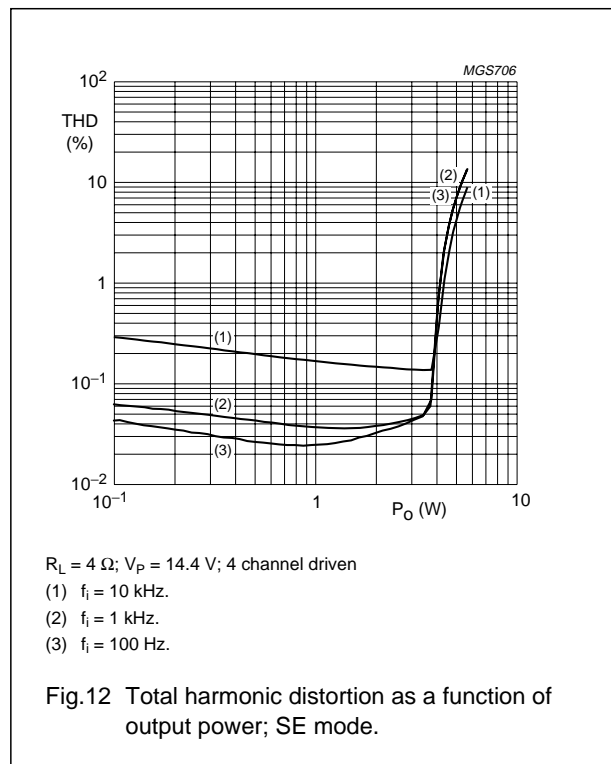
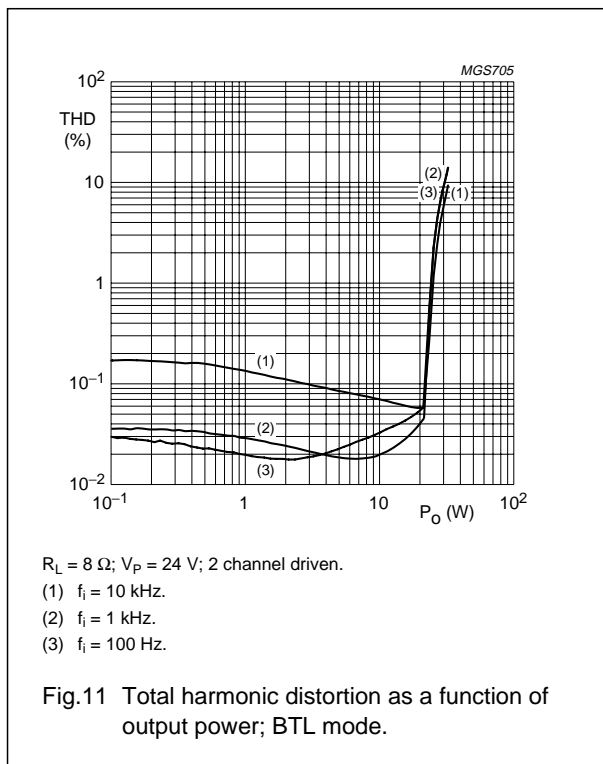
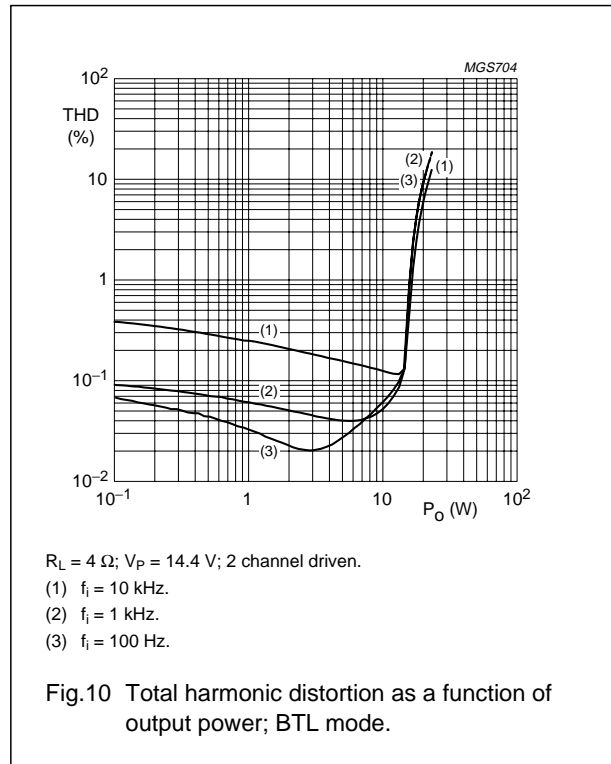
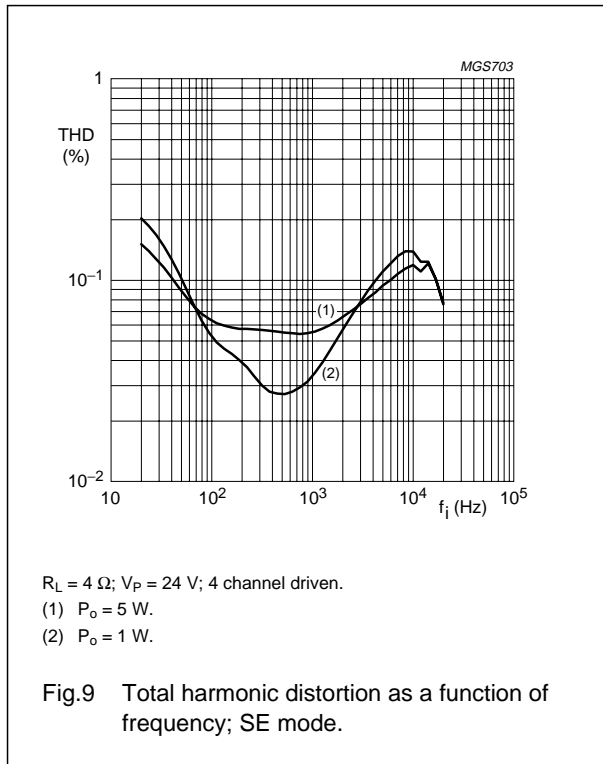
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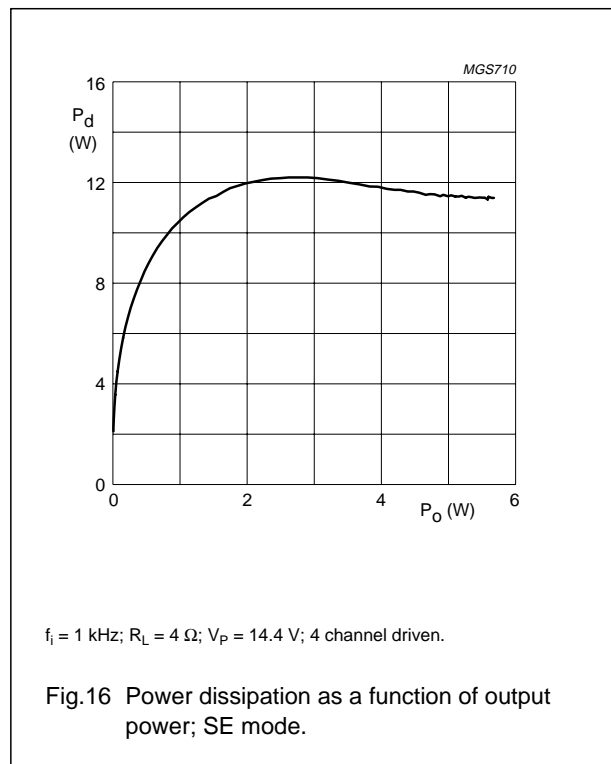
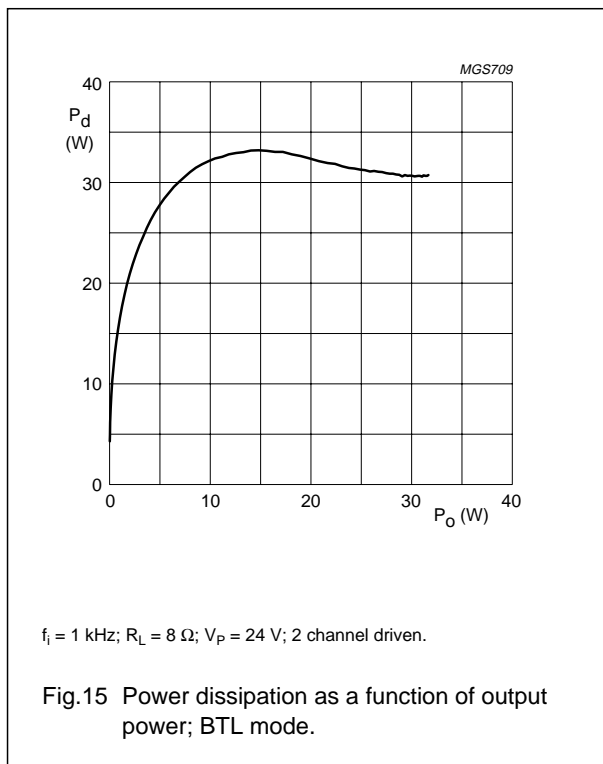
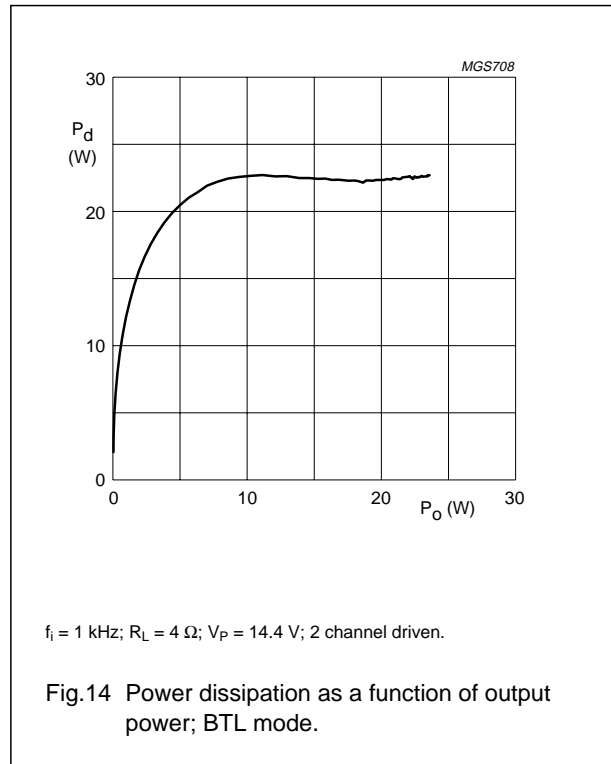
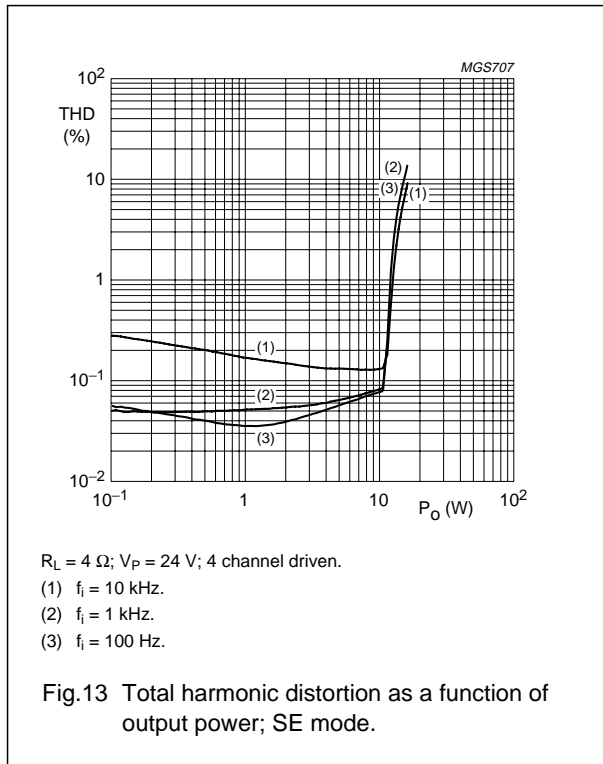
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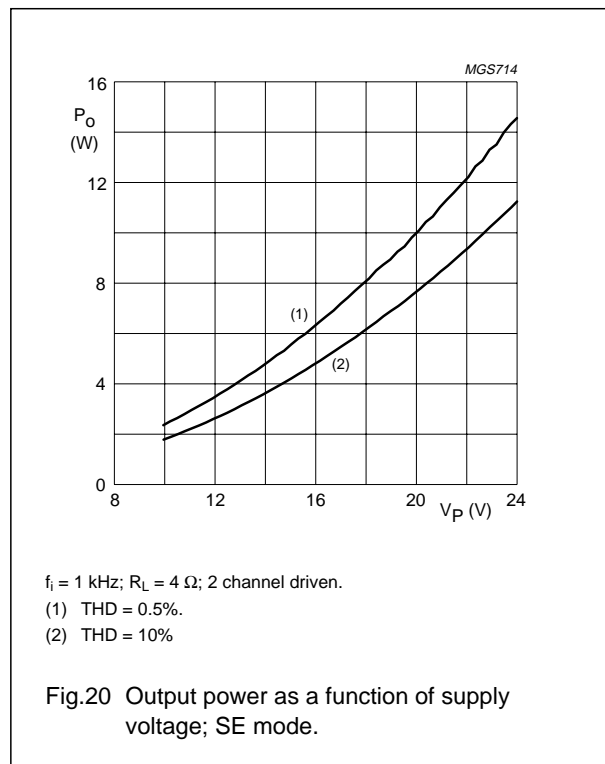
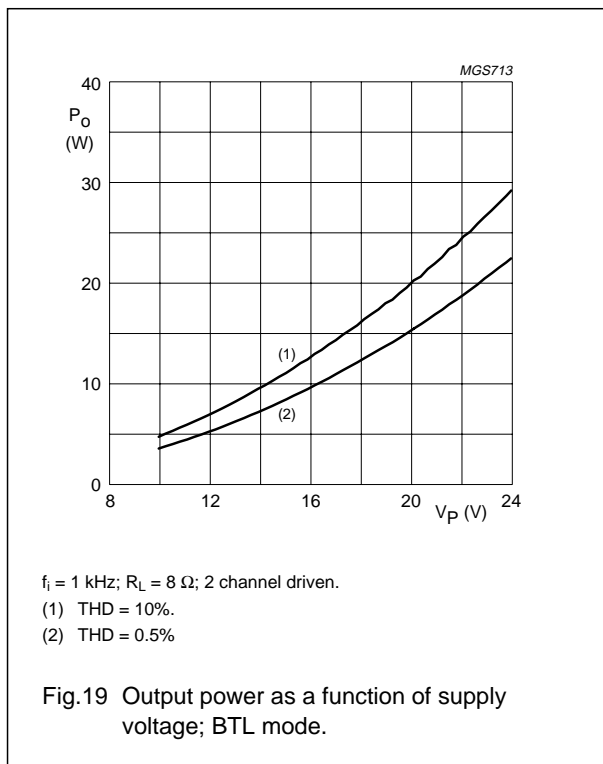
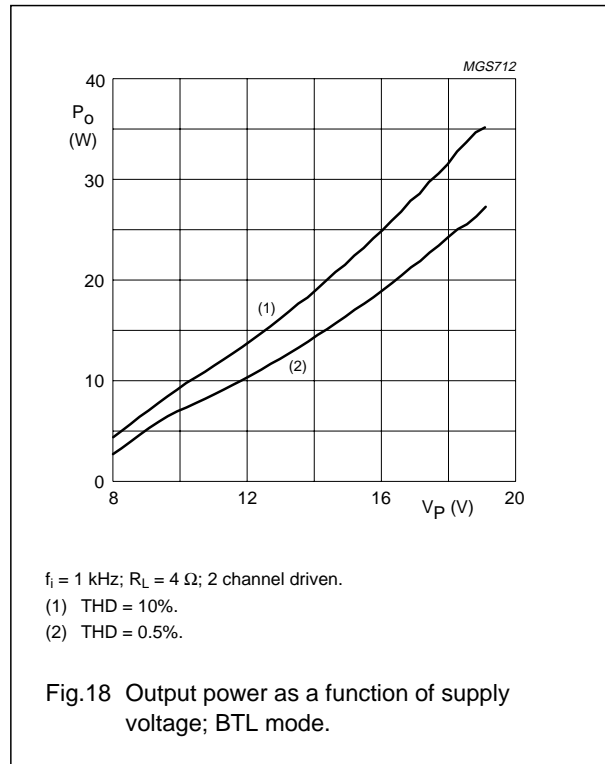
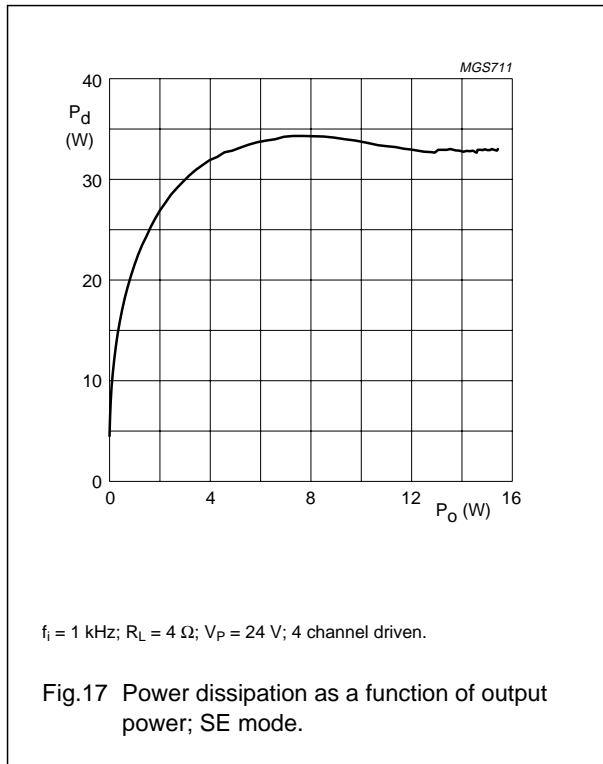
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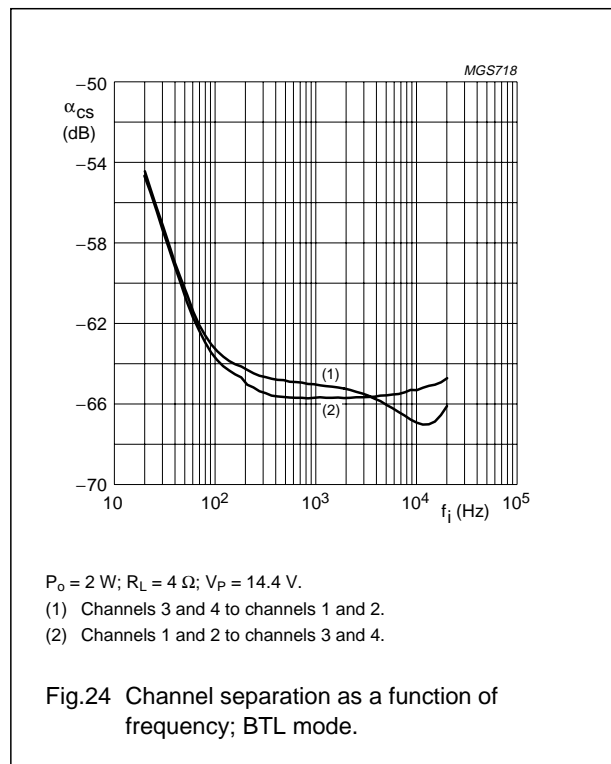
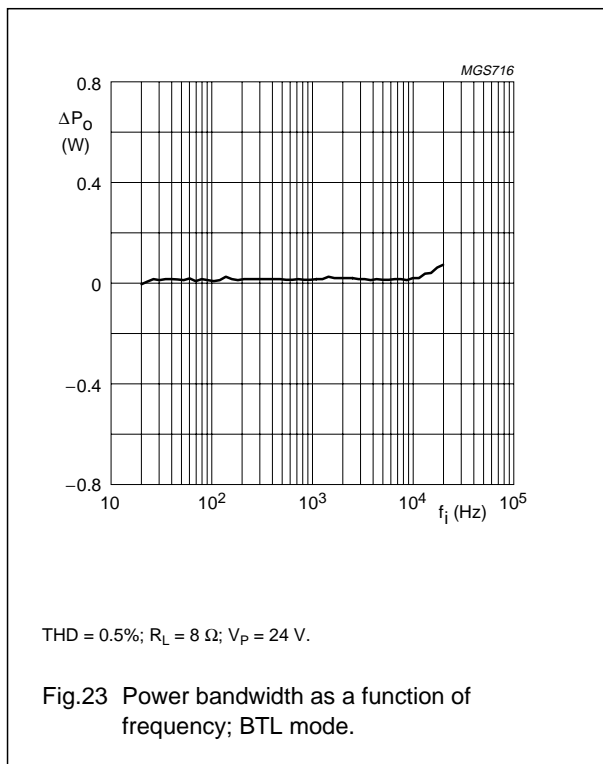
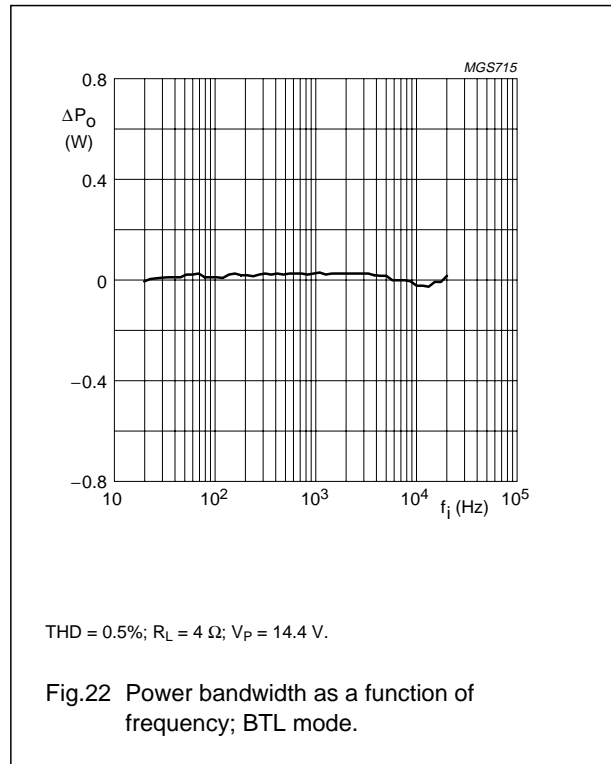
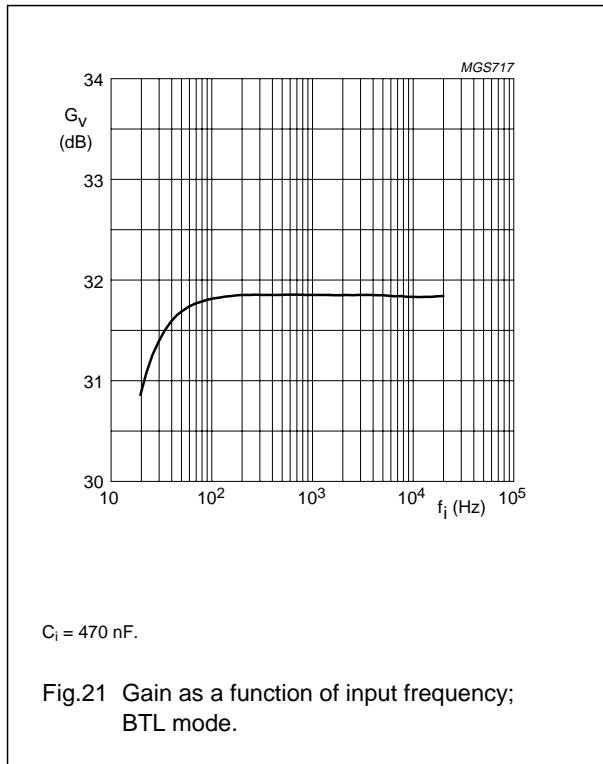
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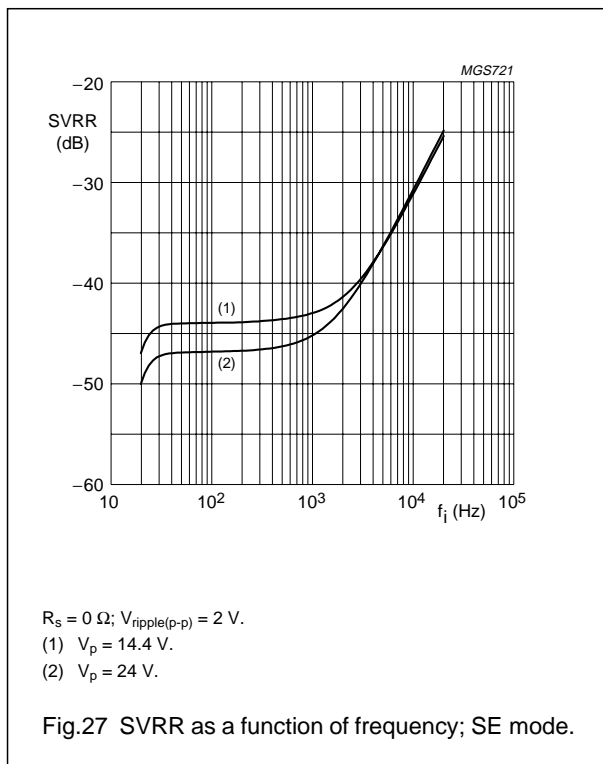
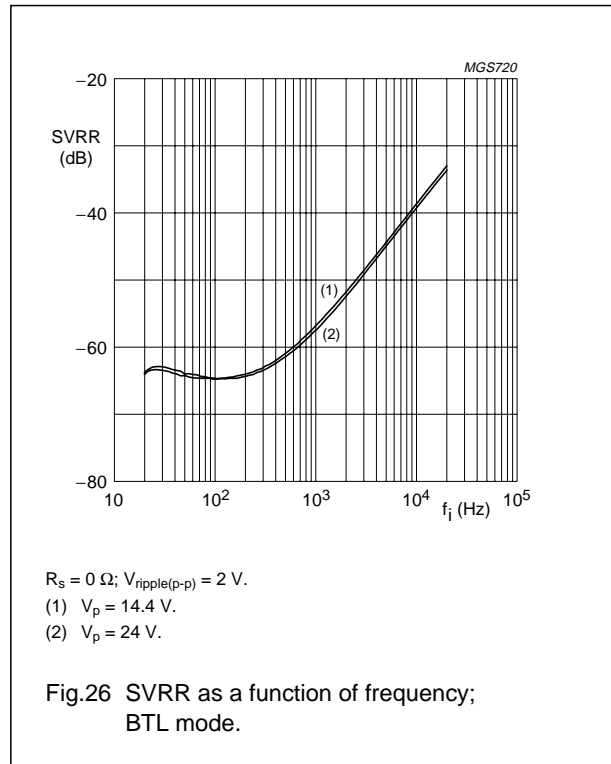
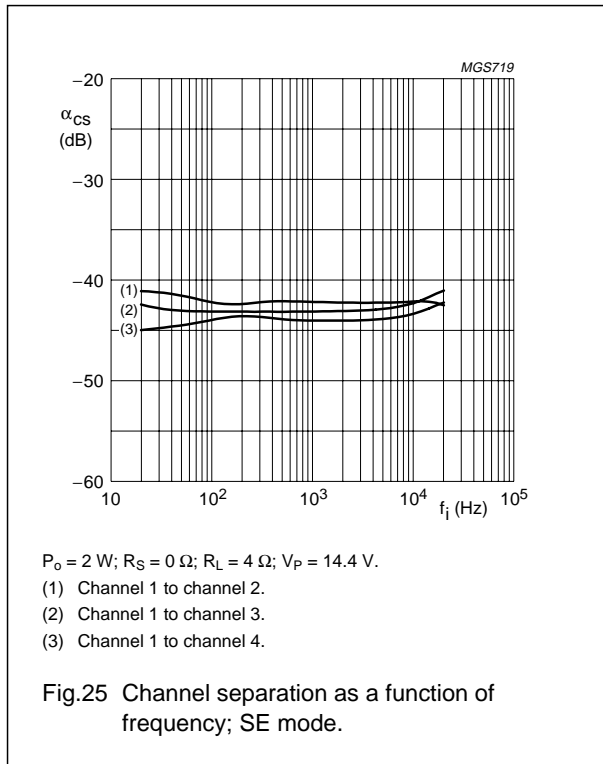
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### APPLICATION INFORMATION

The application circuit depends on the supply voltage used. For supply voltages below 18 V the application circuits are shown in Figs 28, 29 and 30.

The typical application circuits for the different supply voltage ranges are shown in Figs 31, 32 and 33.

#### Additional information for the applications shown in Figs 28, 29 and 30

The RC-network connected to pin 5 determines the amplifier switch on/off behaviour as follows;

- Switched from STANDBY to MUTE when  $V_{\text{switching}}$  (typically 9 V) is enabled and the switch SW1 is closed. During MUTE there is no output noise and no offset.
- Switched from MUTE to ON when the switch SW1 is opened. During switching ON the offset and noise are gradually built up. The time constant is fixed by  $R1 \times C1$ .

The inputs can be tied together and connected to one input capacitor. Because the input resistance is decreased by a factor of 2, the low frequency roll-off is shifted to a higher frequency when  $C_i$  is kept the same value.

The low frequency cut-off is determined by;

$$f_{-3\text{dB}} = 1 / (2\pi \times R_i \times C_i)$$

$$= \frac{1}{2\pi \times 60 \times 10^3 \times 220 \times 10^{-9}} = 12 \text{ Hz.}$$

The Boucherot network connected to the buffer (pin 9) is necessary to guarantee a low output resistance at high frequencies when the buffer is loaded (only in SE applications).

#### Additional information for the applications shown in Figs 31, 32 and 33

Short circuit behaviour at high supply voltages ( $V_p > 18 \text{ V}$ ):

- When  $V_p > 18 \text{ V}$  it is advisable to use the applications given in Figs 32 and 33. In these applications the diagnostics output is tied to pin 5 (one pin operation) or pin 13 (two pin operation). During a fault condition the amplifier is soft-muted and the amplitude of the output signal is reduced at:
  - over temperature (still large dynamic range)
  - short to ground and over load (output current reduced)

- The 4.7  $\mu\text{F}$  capacitor and the 10 k $\Omega$  resistor connected to pin 5 or to pin 13 are used to:
  - provide a stable loop
  - control the switch on/off behaviour
  - minimize the effect due to clip detection.

#### Use of common buffer

In SE applications the buffer output is used in place of a SE capacitor. To minimize the crosstalk (high channel separation) and distortion it is advised to connect the speaker wires as closely as possible to pin 9 without using a shared wire. Internally in the IC all the efforts have been taken to minimize the crosstalk by locating the feedback loops as close as possible to pin 9.

If a common wire is shared by all the speakers, the series resistance of this shared wire will introduce added signal voltages resulting from the currents flowing through this wire when a connected amplifier is driven by a signal.

#### Optimize the THD performance

The TDA8580J application can be optimized to gain the lowest THD possible by applying the following guidelines:

- SE application: minimize the shared wires to pin 9 (see section "Use of common buffer").
- Because the inputs are quasi differential, ground loops can be avoided by connecting the negative terminal of the 100  $\mu\text{F}$  signal ground capacitor (connected to pin 12) to the ground pin of the signal processor.
 

Note: do not leave the inputs in the open condition to prevent HF oscillation.
- Increase the value of electrolytic supply capacitor (typical value 1000  $\mu\text{F}$ ) to the maximum possible to minimize cross talk and distortion at low signal frequencies, due to the PSRR (power supply rejection ratio). For suppressing high frequency transients on the supply line a capacitor (typical value 100 nF) with a low ESR is required to be connected in parallel with the electrolytic capacitor. The capacitor combination must be placed as close as possible to the IC (using short interconnection tracks).

#### Headroom

A typical CD requires at least 12 dB dynamic headroom (a factor of 15.85), compared with the average power output, for passing the loudest parts without distortion.



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For BTL application at  $V_p = 24\text{ V}$ ,  $R_L = 8\ \Omega$  and  $P_o$  at THD = 0.5% (see Fig.15), the Average Listening Level (ALL) for music power without distortion yields:

$$P_{o(ALL)} = \frac{23}{15.85} = 1.45\text{ W.}$$

**Table 2**  $P_d$  as a function of headroom (music signals) for  $P_o = 2 \times 23\text{ W}$  (THD = 0.5%).

HEADROOM	$P_d$
0 dB	32 W
12 dB	16 W

So for the average music listening level a total power dissipation of 16 W can be used for calculating the optimum heat sink thermal resistance.

**Heatsink calculation**

The measured thermal resistance of this package  $R_{th(j-c)}$  is a maximum of 1.5 K/W. For a maximum ambient temperature of 60°C the required heatsink thermal resistance can be calculated as shown in the following example.

**EXAMPLE**

Measured or given values:

$$V_p = 24\text{ V}$$

$$R_L = 8\ \Omega\ (2 \times \text{BTL})$$

$$\text{Measured worst case } P_d\ (\text{sine wave}) = 32\text{ W}$$

$$T_{j(max)} = 150^\circ\text{C}$$

$$T_{amb(max)} = 60^\circ\text{C}$$

$$R_{th(j-c)} = 1.5\text{ K/W}$$

$$R_{th(hs)} = \frac{T_{j(max)} - T_{amb(max)}}{P_d} - R_{th(j-c)}$$

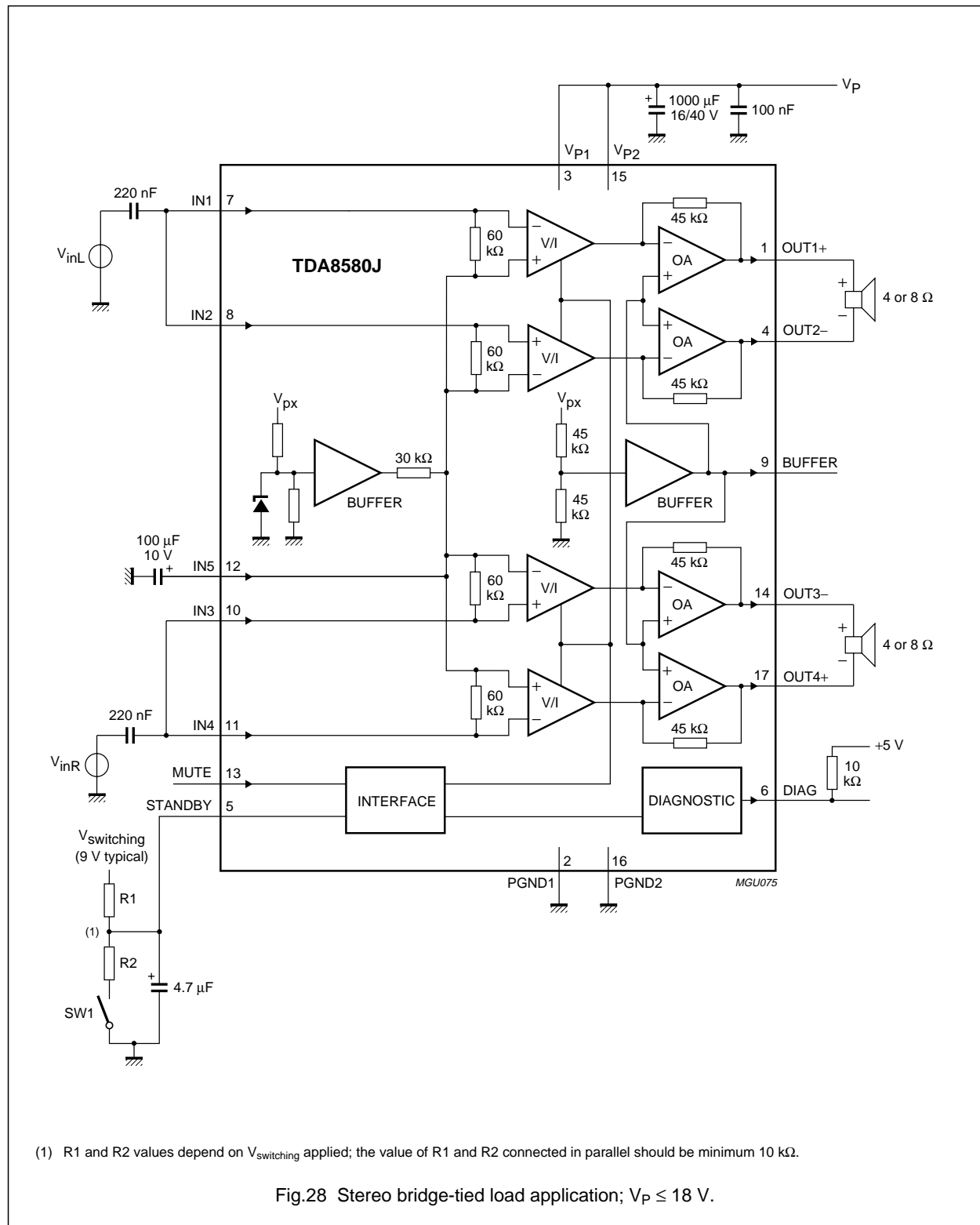
$$= \frac{150 - 60}{32} - 1.5 = 1.3\text{ K/W}$$

**Table 3** Heatsink thermal resistance as a function of headroom for  $P_o = 2 \times 23\text{ W}$  (THD = 0.5%).

HEAD ROOM	$P_d$	$R_{th(hs)}$
0 dB	32 W	1.3 K/W
12 dB	16 W	4.12 K/W

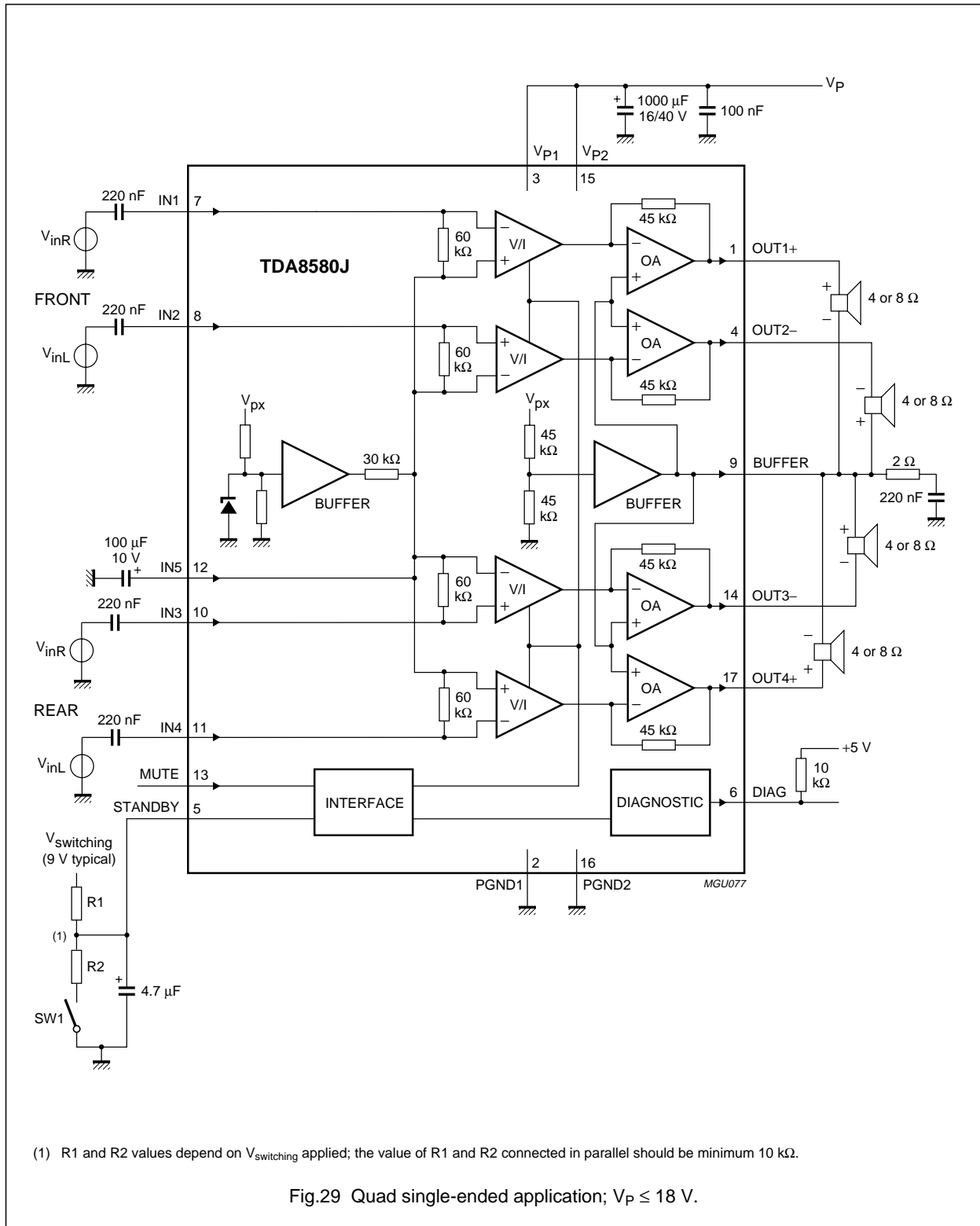
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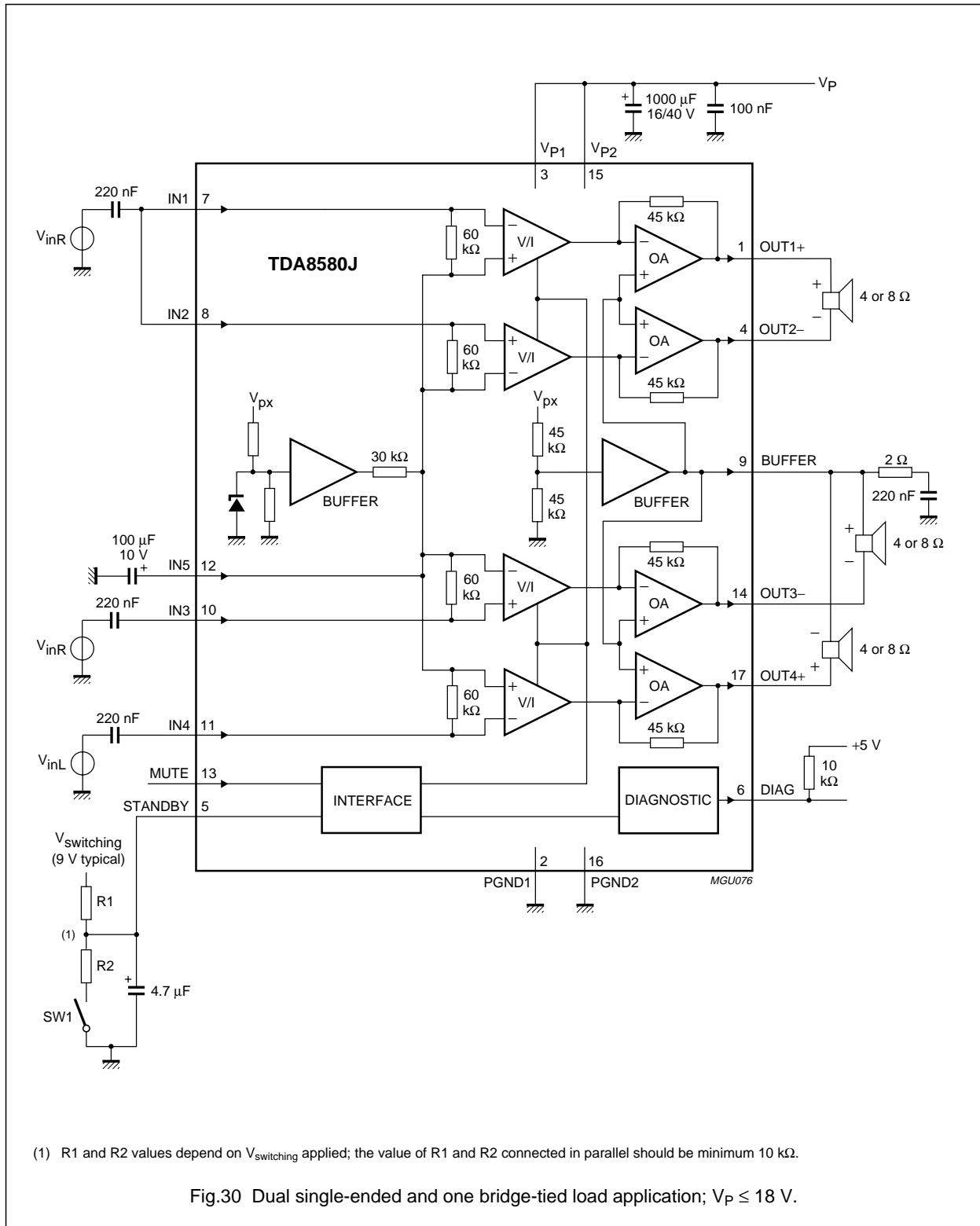
Multi-purpose power amplifier

TDA8580J



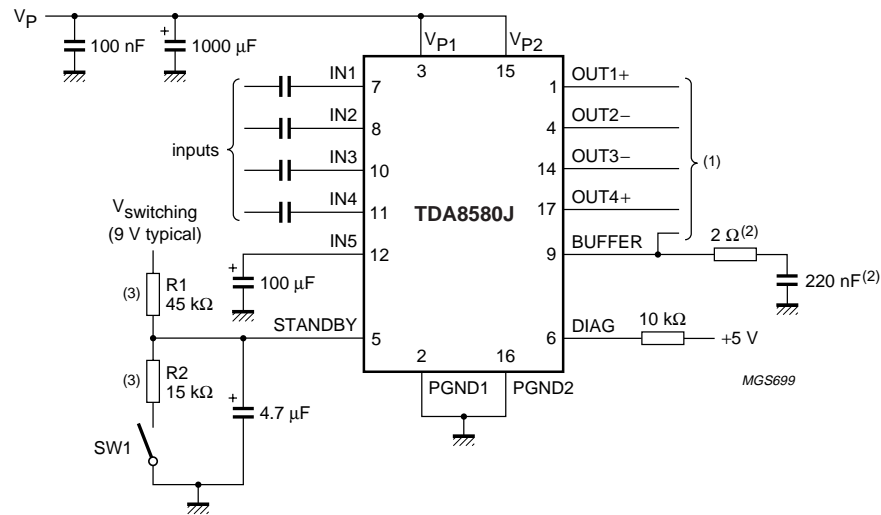
Multi-purpose power amplifier

TDA8580J



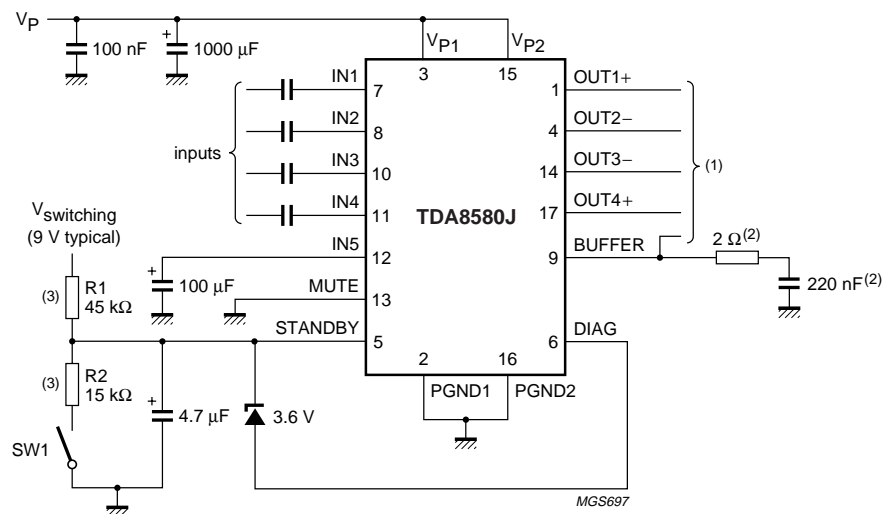
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- (1) Load conditions: quad SE (4 x 4 Ω), or dual BTL (2 x 8 Ω), or dual SE (2 x 4 Ω) and one BTL (1 x 8 Ω).  
 (2) RC combination not required in BTL mode.  
 (3) R1 and R2 values depend on  $V_{switching}$  applied; the value of R1 and R2 connected in parallel should be minimum 10 kΩ.

Fig.31 Application 1; supply voltage range  $8\text{ V} < V_P \leq 18\text{ V}$ ; 1-pin and 2-pin operation.

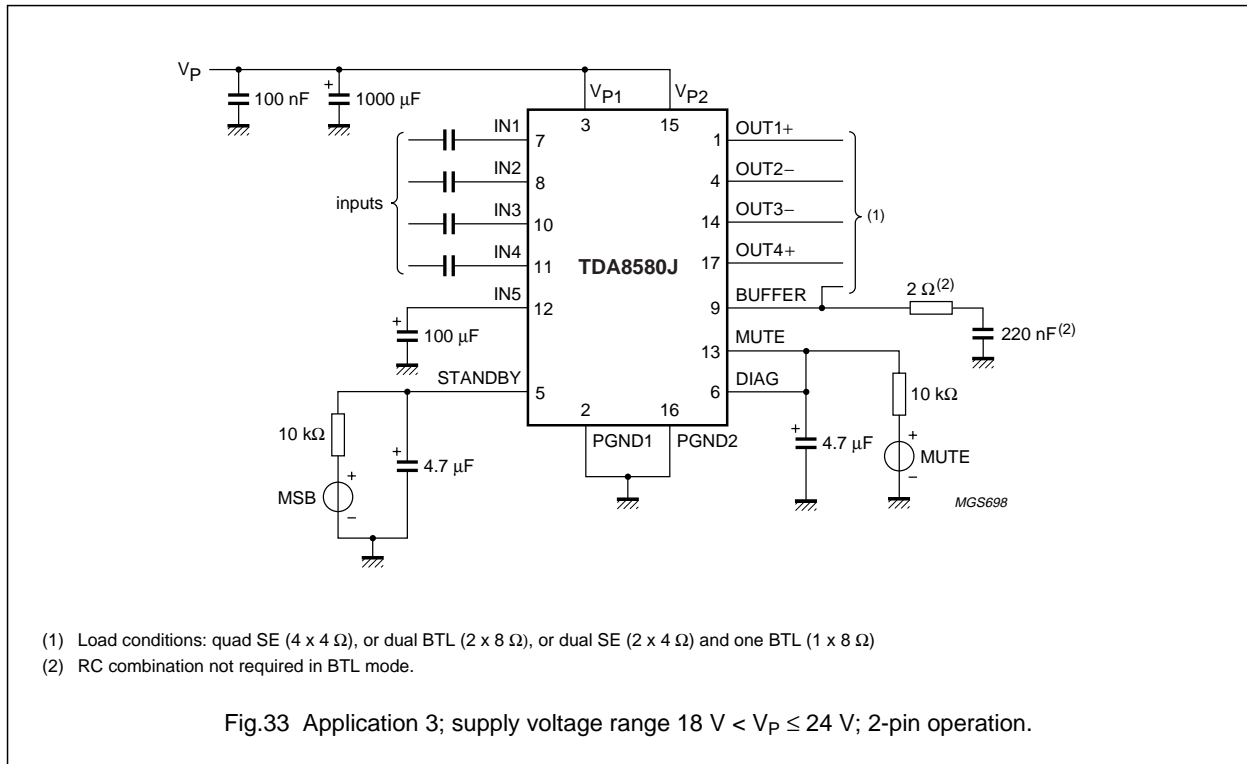


- (1) Load conditions: quad SE (4 x 4 Ω), or dual BTL (2 x 8 Ω), or dual SE (2 x 4 Ω) and one BTL (1 x 8 Ω).  
 (2) RC combination not required in BTL mode.  
 (3) R1 and R2 values depend on  $V_{switching}$  applied; the value of R1 and R2 connected in parallel should be minimum 10 kΩ.

Fig.32 Application 2; supply voltage range  $18\text{ V} < V_P \leq 24\text{ V}$ ; 1-pin operation.

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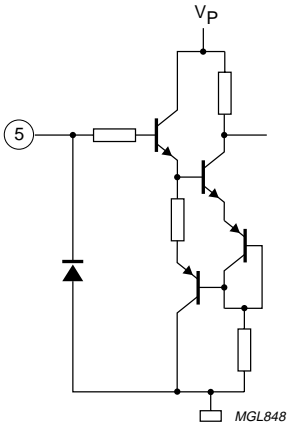
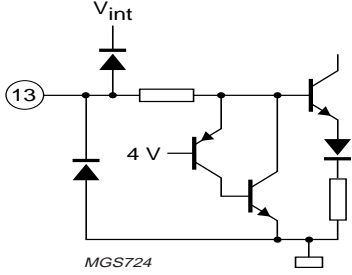
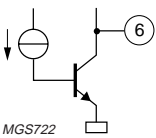


INTERNAL PIN CONFIGURATION

PIN	NAME	EQUIVALENT CIRCUIT
7, 8, 10, 11 and 12	Inputs	
1, 4, 9, 14 and 17	Outputs	

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PIN	NAME	EQUIVALENT CIRCUIT
5	STANDBY	
13	MUTE	
6	DIAG	

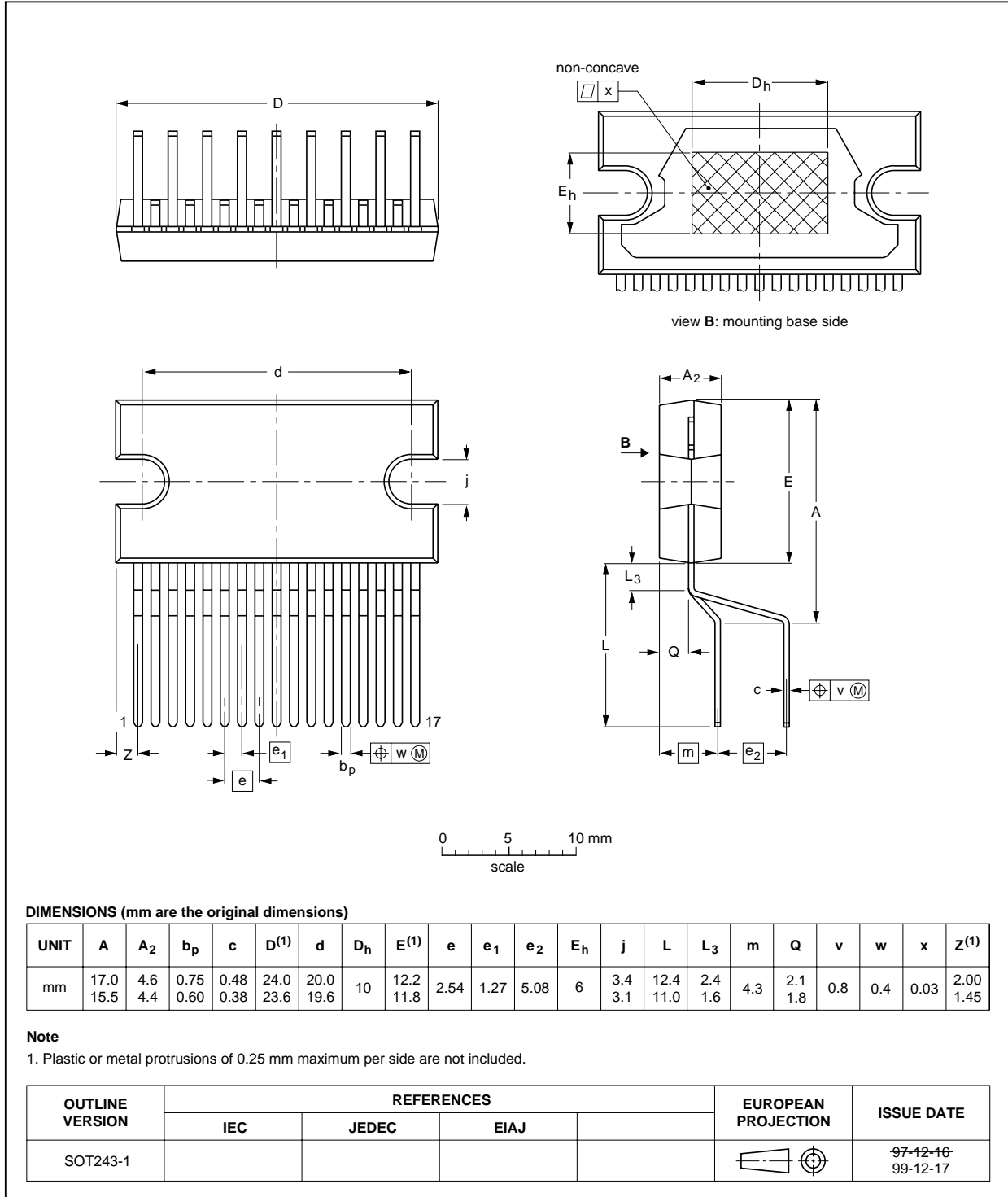
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## PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1





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**SOLDERING****Introduction to soldering through-hole mount packages**

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

**Soldering by dipping or by solder wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Manual soldering**

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**Suitability of through-hole mount IC packages for dipping and wave soldering methods**

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable <sup>(1)</sup>

**Note**

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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## DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS <sup>(1)</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

## Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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