M54975P/FP

Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M54975 is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains a serial input to serial/parallel output 8-bit CMOS shift register and CMOS latch as well as bipolar 8-bit parallel-output driver.

FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Latch circuit included for each stage
- Enable input for output control
- Low supply current ..... $I_{CC} \geq 10\mu A$ at standby
- Serial input/output level is compatible with standard CMOS
- Driver : Withstand voltage ..... $BV_{CEO} \geq 30V$
  Large drive current ..... ($I_{O(max)}$=300mA)
- Wide operating temperature range ..... T_a=-20 – +75°C

APPLICATION

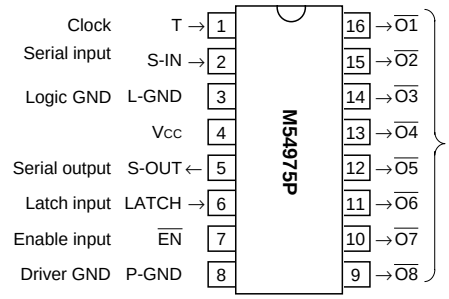
Thermal printer head dot driver, Serial-to parallel conversion, Relay and Solenoid driver

FUNCTION

The M54975 consists of an 8-bit D-type flip-flop, the output of which is connected to 8 latches.

When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an “L” to “H” change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4(P)
16P2N-A(FP)

Using a number of M54975 units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54975.

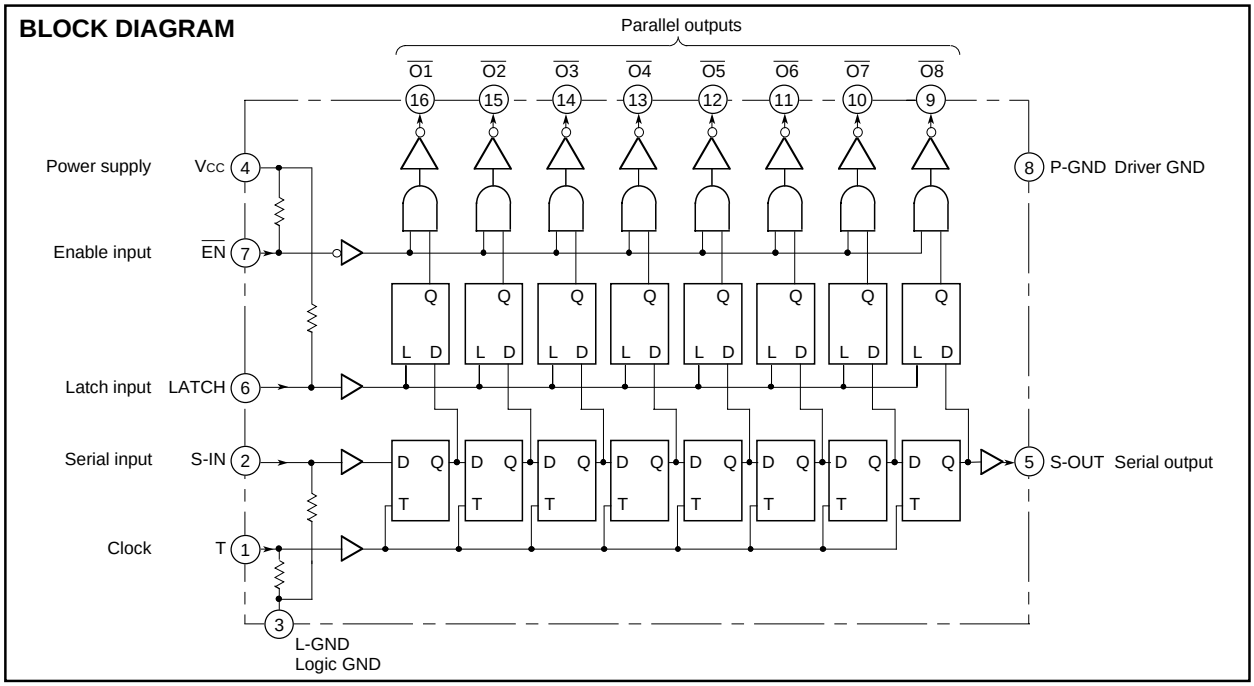
In parallel output, when the latch input is set to “H” and the output-control input (enable input $\overline{EN}$) is “L”, a clock pulse changing from “L” to “H” will cause the serial data input signal to appear at output $\overline{O1}$, and the data will be shifted in order at outputs $\overline{O2}$ – $\overline{O8}$.

The parallel output will yield a signal that is inverted with respect to the serial data input.

Setting the LATCH input to “L” will prevent data from entering the latch.

When the $\overline{EN}$ input is set to “H”, all outputs ($\overline{O1}$ – $\overline{O8}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the $\overline{EN}$ input to “H” (and outputs $\overline{O1}$ – $\overline{O8}$ will set to

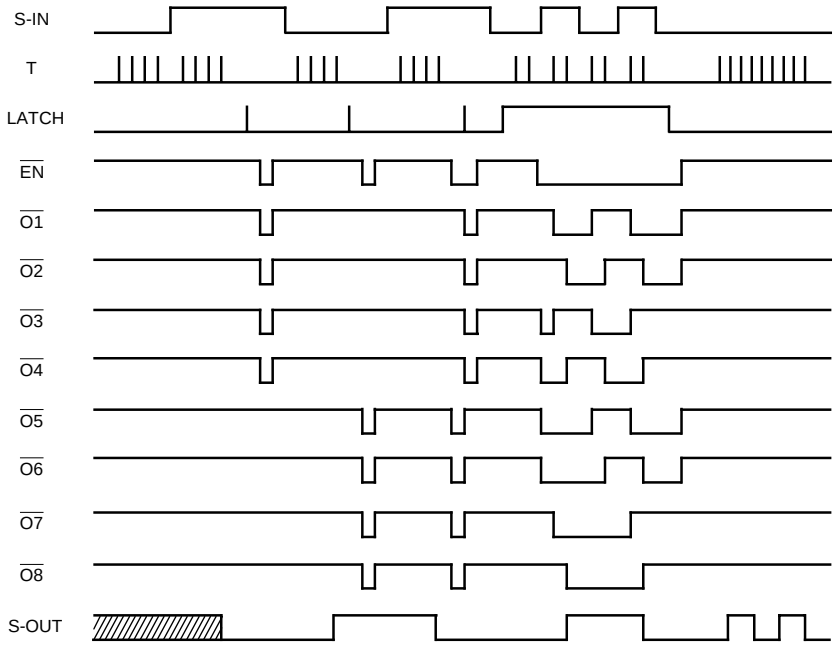
BLOCK DIAGRAM



OFF) until the input data is set and the internal logic state has been determined.

L-GND is the ground of the CMOS logic circuit section and P-GND is the ground for the output driver section ($\overline{O1}$ – $\overline{O8}$), which is made up of bipolar transistors that are capable of driving large currents.

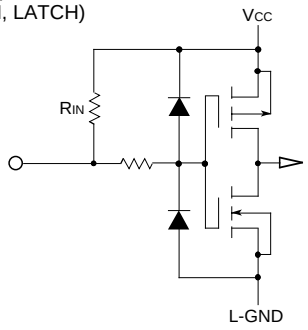
TIMING CHART



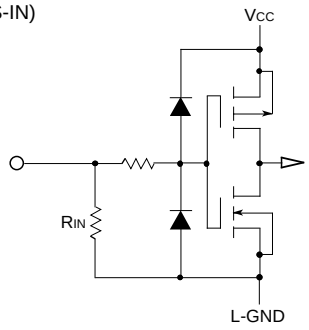
* The state of the shaded part is unstable.

INPUT/OUTPUT CIRCUIT DIAGRAM

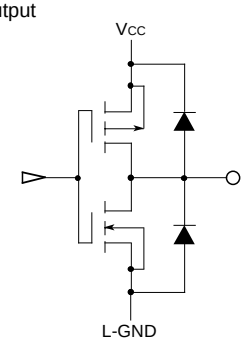
1 Inputs with pullup resistor ($\overline{EN}$, LATCH)



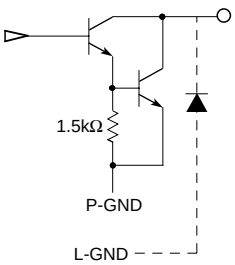
2 Inputs with pulldown resistor (T, S-IN)



3 Serial output (S-OUT)



4 Parallel outputs ($\overline{O1}$ – $\overline{O8}$)



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			-0.5 – +8	V
V_I	Input voltage			-0.5 – V_{CC}+0.5	V
V_O	Output voltage	S-OUT		-0.5 – V_{CC}+0.5	V
		$\overline{O1}$ – $\overline{O8}$: OFF		-0.5 – +30	
I_O	Output current	$\overline{O1}$ – $\overline{O8}$: ON		350	mA
P_d	Power dissipation	T_a=25°C	M54975P	1.25	W
			M54975FP	0.8	
T_{opr}	Operating temperature			-20 – 75	°C
T_{stg}	Storage temperature			-55 – 125	°C

RECOMMENDED OPERATING DONDITION

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	$\overline{O1}$ – $\overline{O8}$: OFF			30	V
I_O	Output current (per circuit)	M54975P			300	mA
		M54975FP			100	

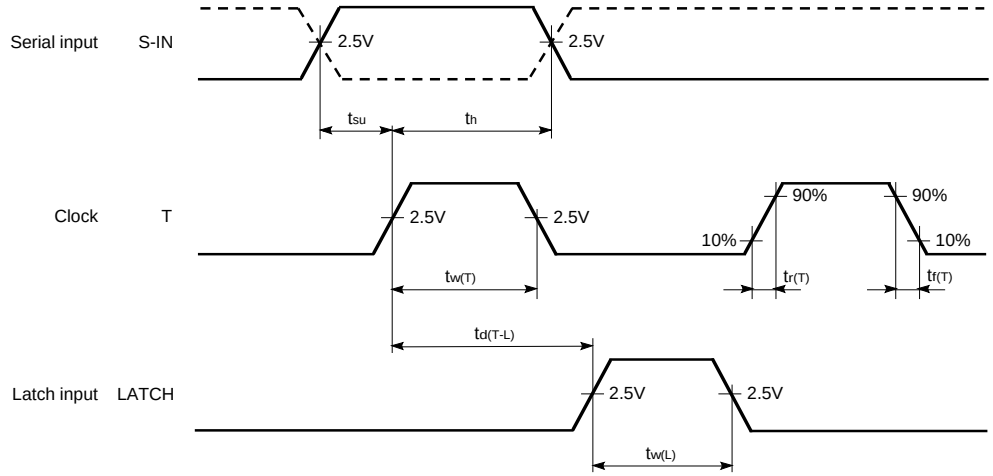
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage		T_a=-20 – 75°C	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	Input resistance			50		—	kΩ
V_{OH}	High-level output voltage	S-OUT	|I_O|≤1μA	4.9		—	V
V_{OL}	Low-level output voltage	S-OUT		—		0.1	V
I_{OH}	High-level output current	S-OUT	V_{OH}=4.5V	-100		—	μA
I_{OL}	Low-level output current	S-OUT	V_{OL}=0.4V	400		—	μA
V_{OL1}	Low-level output voltage	$\overline{O1}$ – $\overline{O8}$	I_{OL}=100mA	—		1.2	V
V_{OL2}			I_{OL}=200mA	—		1.4	V
V_{OL3}			I_{OL}=300mA	—		1.6	V
I_{OLK}	Output leak current	$\overline{O1}$ – $\overline{O8}$	V_O=30V	—		50	μA
I_{CC1}	Supply current		Input: open, All driver outputs: OFF	—		10	μA
I_{CC2}			One driver output is ON.	—		1.7	mA

TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f_{(T)}$	Clock frequency	Input duty: 40 – 60%			2	MHz
$t_{w(T)}$	Clock pulse width		200			ns
$t_{w(L)}$	Latch pulse width		200			ns
t_{su}	Data setup time		100			ns
t_h	Data hold time		100			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Clock pulse rise time				500	ns
$t_{f(T)}$	Clock pulse fall time				500	ns

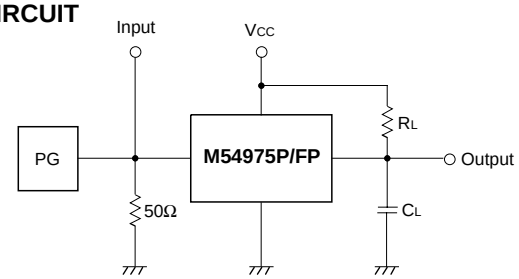
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, unless otherwise noted)

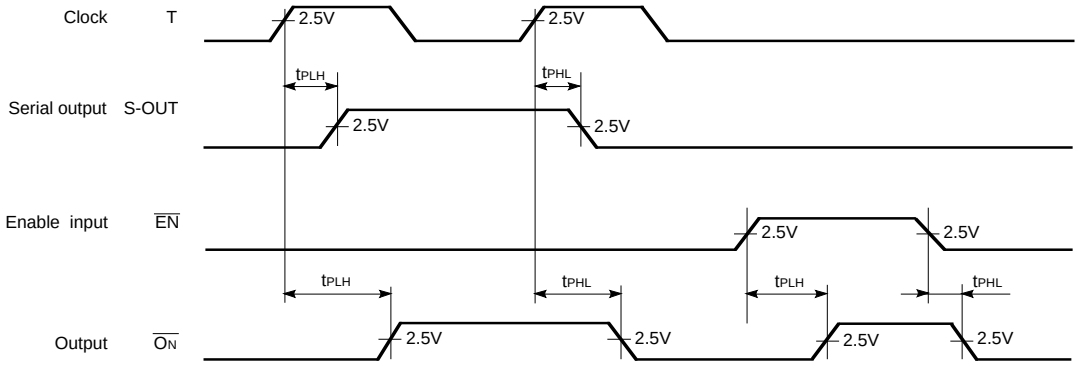
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tPLH	Low-to-high-level output propagation time From input T to output S-OUT	VIH=5V VIL=0V RL(S-OUT)=∞ RL($\overline{ON}$)=100Ω (N=1–8) CL=15pF			0.3	µs
tPHL	High-to-low-level output propagation time From input T to output S-OUT				0.3	µs
tPLH	Low-to-high-level output propagation time From input T to output $\overline{ON}$				10	µs
tPHL	High-to-low-level output propagation time From input T to output $\overline{ON}$				2	µs
tPLH	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{ON}$				10	µs
tPHL	High-to-low-level output propagation time From input $\overline{EN}$ to output $\overline{ON}$				2	µs

TEST CIRCUIT



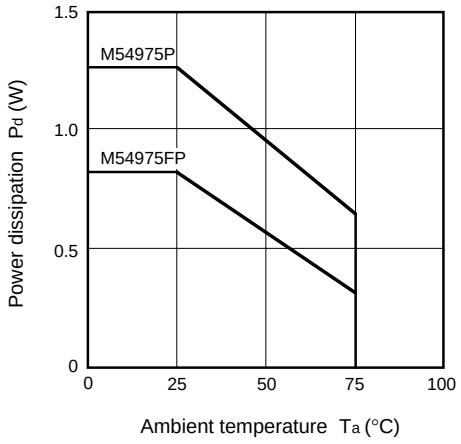
- The input waveform: tr ≤ 20ns, tf ≤ 20ns
- The capacitance CL includes the wiring stray capacitance and probe input capacitance.

TIMING CHART

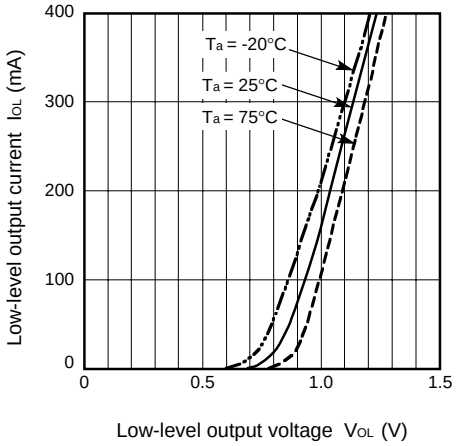


TYPICAL CHARACTERISTICS (V_{CC}=5V, unless otherwise noted)

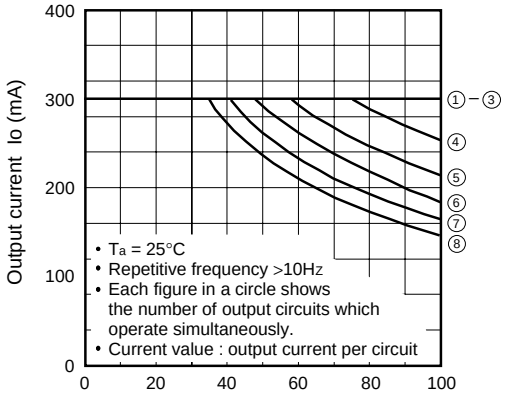
Thermal derating
(Absolute maximum rating)



Driver output V_{OL} vs. I_{OL}



Duty cycle vs. allowable output current
(M54975P)



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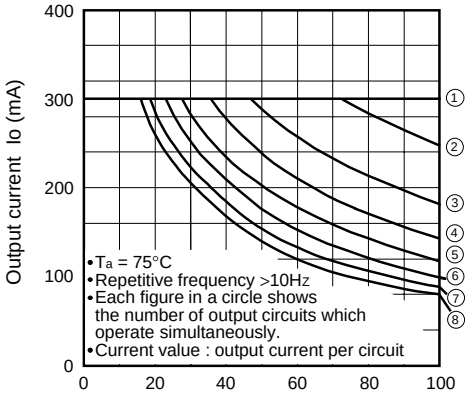
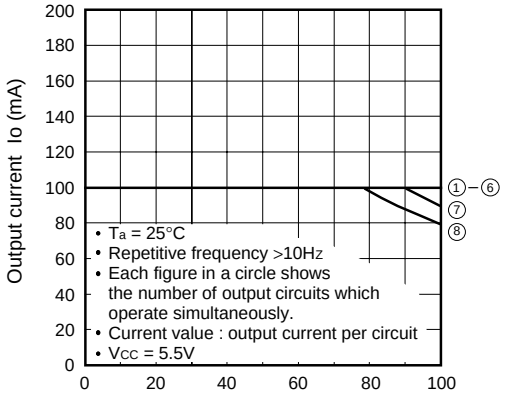


Duty cycle vs. allowable output current
(M54975FP)



Duty cycle vs. allowable output current
(M54975FP)