NEC

MOS INTEGRATED CIRCUIT

μPD17P236

4-BIT SINGLE-CHIP MICROCONTROLLER FOR SMALL GENERAL-PURPOSE INFRARED REMOTE CONTROLLER

The μPD17P236 is a model of the μPD17236 with a one-time PROM instead of an internal mask ROM.

Since the user can write programs to the μPD17P236, it is ideal for experimental production or small-scale production of the μPD17230, 17231, 17232, 17233, 17234, 17235, or 17236 systems.

When reading this document, also read the documents related to the μPD17230, 17231, 17232, 17233, 17234, 17235, and 17236.

Detailed functions are described in the following user's manual. Read this manual when designing your system.

μPD172×× Series User's Manual: U12795E

FEATURES

- Pin compatible with μPD17230, 17231, 17232, 17233, 17234, 17235, and 17236 (except PROM programming function)
- Carrier generator circuit for infrared remote controller (REM output)
- 17K architecture: General-purpose register method
- Program memory (one-time PROM): 32 Kbytes (16,384 × 16)
- Data memory (RAM): 223 × 4 bits
- Low-voltage detection circuit
- Input/output of $P1A_0$ pin, clock selection for carrier generation

	μPD17P236M1	μPD17P236M2	μPD17P236M3	μPD17P236M4
Input/output of $P1A_0$ pin	Output	Input	Output	Input
Clock (Rf_X) selection for carrier generation	$Rf_X = f_X/2$		$Rf_X = f_X$	

- Supply voltage: V_{DD} = 2.2 to 3.6 V (f_X = 4 MHz: high-speed mode, 4 μs)
  V_{DD} = 3.0 to 3.6 V (f_X = 8 MHz: high-speed mode, 2 μs)

APPLICATIONS

Preset remote controllers, toys, and portable systems

Document No. U14776EJ1V0DS00 (1st edition)
Date Published June 2000 J CP(K)
Printed in Japan

ORDERING INFORMATION

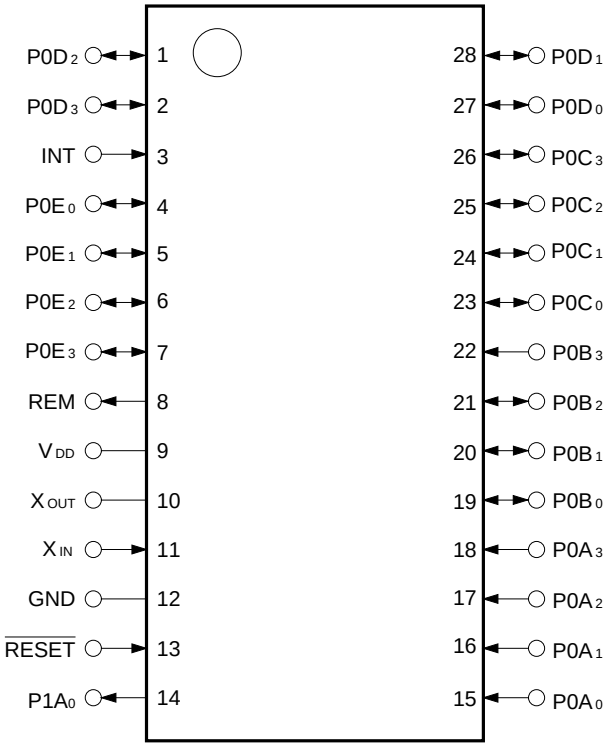
Part Number	Package
μPD17P236M1GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M1MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M2GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M2MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M3GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M3MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M4GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M4MC-5A4	30-pin plastic SSOP (7.62 mm (300))

PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode

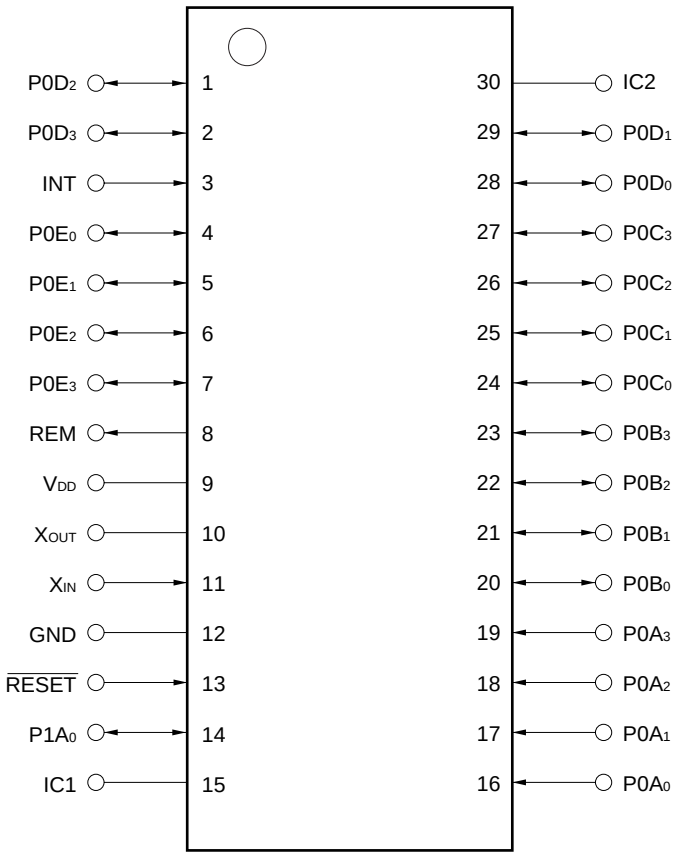
- **28-pin plastic SOP (9.53 mm (375))**

  μPD17P236M1GT, 17P236M2GT, 17P236M3GT, 17P236M4GT



• **30-pin plastic SSOP (7.62 mm (300))**

μPD17P236M1MC-5A4, 17P236M2MC-5A4, 17P236M3MC-5A4, 17P236M4MC-5A4



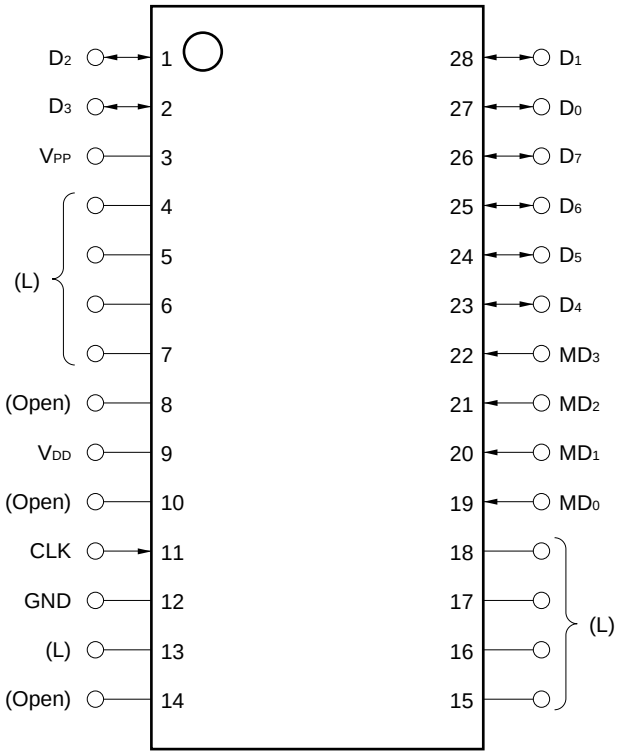
GND	:	Ground
IC1, IC2	:	Internally connected[Note 1]
INT	:	External interrupt request signal input
$P0A_0$-$P0A_3$	:	Input port (CMOS input)
$P0B_0$-$P0B_3$	:	Input/output port (CMOS input/N-ch open-drain output)
$P0C_0$-$P0C_3$	:	Input/output port (CMOS input/N-ch open-drain output)
$P0D_0$-$P0D_3$	:	Input/output port (CMOS input/N-ch open-drain output)
$P0E_0$-$P0E_3$	:	Input/output port (CMOS push-pull output)
$P1A_0$	:	Input port (CMOS input) or output port (N-ch open-drain output)[Note 2]
REM	:	Remote controller output (CMOS push-pull output)
$\overline{\text{RESET}}$	:	Reset input
V_{DD}	:	Power supply
X_{IN}, X_{OUT}	:	Resonator connection

Notes 1. This pin cannot be used. Leave open.

2. Input port or output port is selected depending on the product (see **2. PIN FUNCTIONS**).

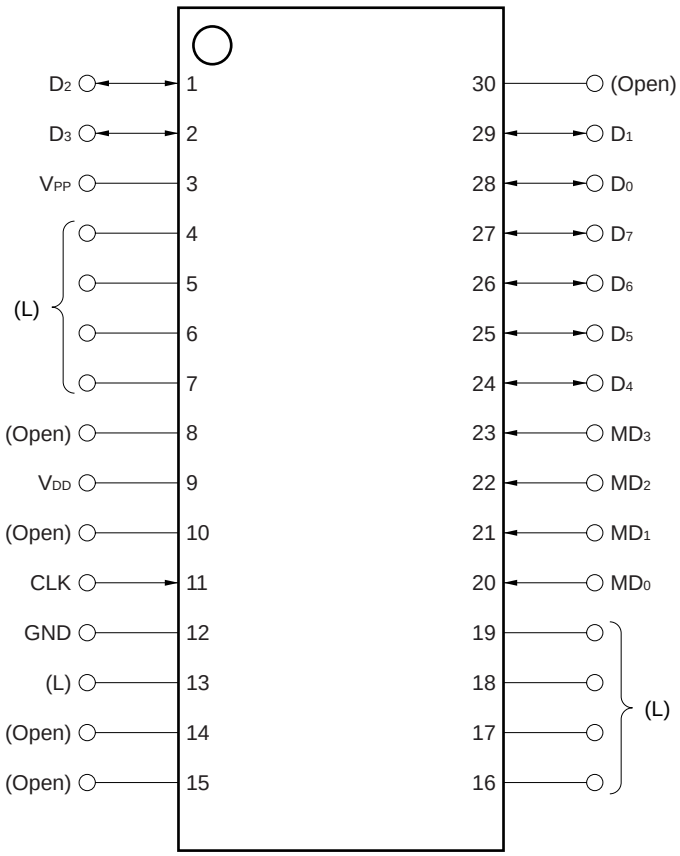
(2) PROM programming mode

• **28-pin plastic SOP (9.53 mm (375))**
μPD17P236M1GT, 17P236M2GT, 17P236M3GT, 17P236M4GT



• **30-pin plastic SSOP (7.62 mm (300))**

μPD17P236M1MC-5A4, 17P236M2MC-5A4, 17P236M3MC-5A4, 17P236M4MC-5A4



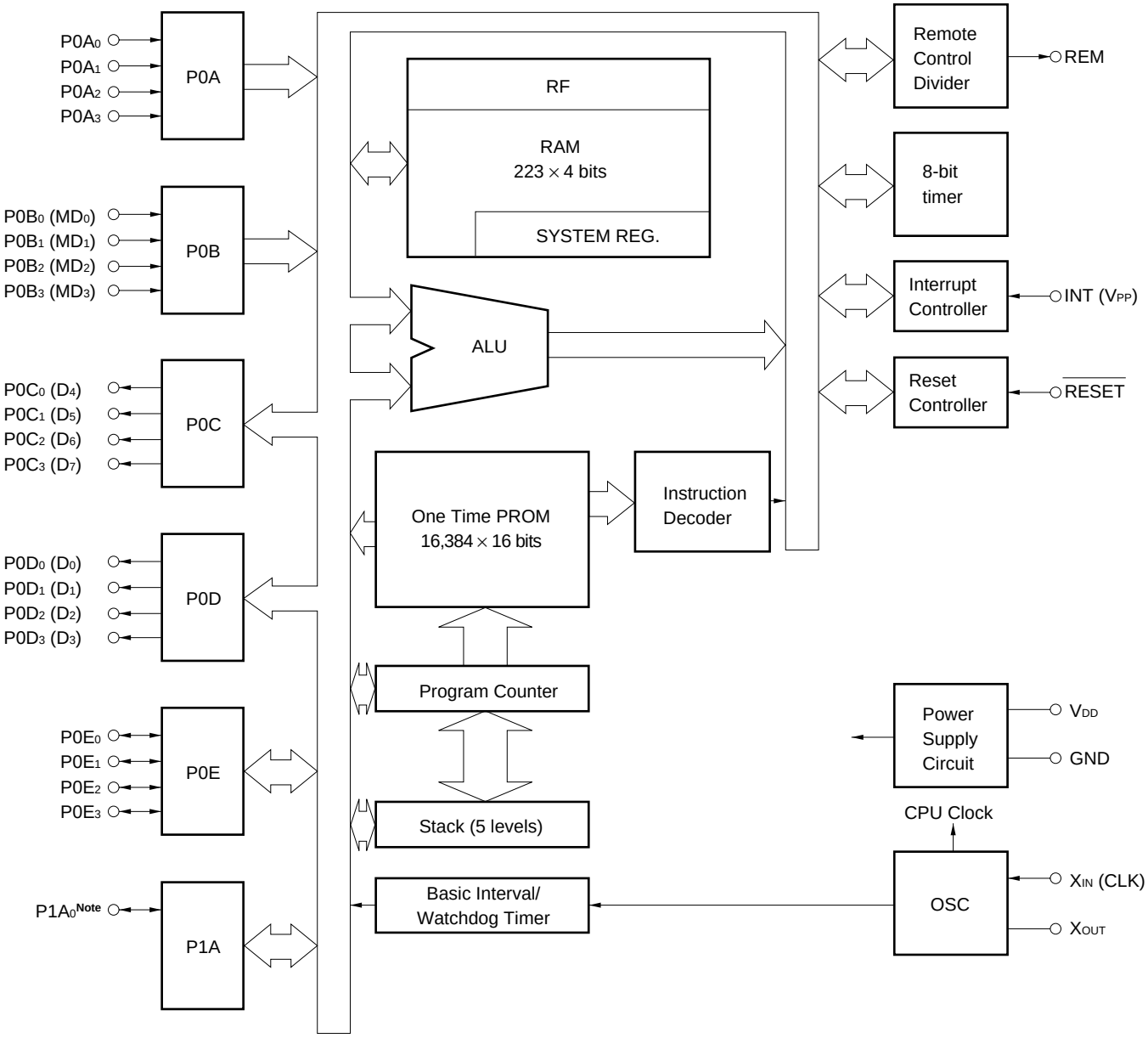
Caution Contents in parentheses indicate how to handle unused pins in PROM programming mode.

L : Connect to GND via a resistor (470 Ω) separately.

Open : Leave unconnected.

CLK	:	Clock input for PROM
D_0-D_7	:	Data input/output for PROM
GND	:	Ground
MD_0-MD_3	:	Mode select input for PROM
V_{DD}	:	Power supply
V_{PP}	:	Power supply for PROM writing

BLOCK DIAGRAM



Note Input port or output port is selected depending on the product (see **2. PIN FUNCTIONS**).

Remark ( ): During PROM programming mode

CONTENTS

1. DIFFERENCES BETWEEN μPD17236 AND μPD17P236

μPD17P236 is equipped with PROM to which data can be written by the user instead of the internal mask ROM (program memory) of the μPD17236.

Table 1-1 shows the differences between the μPD17236 and μPD17P236.

The CPU functions and internal hardware of the μPD17P236, 17230, 17231, 17232, 17233, 17234, 17235, and 17236 are identical. Therefore, the μPD17P236 can be used to evaluate the program developed for the μPD17230, 17231, 17232, 17233, 17234, 17235, and 17236 system. **Note, however, that some of the electrical specifications such as supply current and low-voltage detection voltage of the μPD17P236 are different from those of the μPD17230, 17231, 17232, 17233, 17234, 17235, and 17236.**

Table 1-1. Differences among μPD17236 and μPD17P236

Item \ Product Name	μPD17P236 (μPD17P236M1, 17P236M2, 17P236M3, 17P236M4)	μPD17236
Program memory	One-time PROM	Mask ROM
	32 Kbytes (16,384 × 16) (0000H-3FFFH)	
Data memory	223 × 4 bits	
Input/output of $P1A_0$ pin	• Input (μPD17P236M2, 17P236M4) • Output (μPD17P236M1, 17P236M3)	Any (mask option)
Clock (Rf_X) selection for carrier generation	• $Rf_X = f_X/2$ (μPD17P236M1, 17P236M2) • $Rf_X = f_X$ (μPD17P236M3, 17P236M4)	Any (mask option)
Low-voltage detection circuit[Note]	Provided	Any (mask option)
Instruction execution time	• 2 μs (V_{DD} = 3.0 to 3.6 V) • 4 μs (V_{DD} = 2.2 to 3.6 V)	• 2 μs (V_{DD} = 2.2 to 3.6 V) • 4 μs (V_{DD} = 2.0 to 3.6 V)
Supply voltage	V_{DD} = 2.2 to 3.6 V	V_{DD} = 2.0 to 3.6 V
Package	• 28-pin plastic SOP (9.53 mm (375)) • 30-pin plastic SSOP (7.62 mm (300))	

Note Although the circuit configuration is identical, its electrical characteristics differ depending on the product.

2. PIN FUNCTIONS

2.1 Normal Operation Mode (1/2)

Pin No.	Symbol	Function	Output Format	At Reset
27 (28) 28 (29) 1 (1) 2 (2)	$P0D_0$ $P0D_1$ $P0D_2$ $P0D_3$	These pins constitute a 4-bit I/O port which can be set in the input or output mode in 4-bit units (group I/O). In the input mode, these pins serve as CMOS input pins with a pull-up resistor, and can be used as key return input lines of a key matrix. The standby status must be released when at least one of the input lines goes low. In the output mode, these pins are used as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Low-level output
3 (3)	INT	External interrupt request signal. This signal releases the standby status if an external interrupt request signal is input to it when the INT pin interrupt enable flag (IP) is set.	–	Input
4 (4) 5 (5) 6 (6) 7 (7)	$P0E_0$ $P0E_1$ $P0E_2$ $P0E_3$	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units. In the output mode, this port functions as a high current CMOS output port. In the input mode, function as CMOS input and can be specified to connect pull-up resistor by program.	CMOS push-pull	Input
8 (8)	REM	Outputs transfer signal for infrared remote controller. Active-high output.	CMOS push-pull	Low-level output
9 (9)	V_{DD}	Power supply	–	–
10 (10) 11 (11)	X_{OUT} X_{IN}	Connects ceramic resonator for system clock oscillation	–	(Oscillation stops)
12 (12)	GND	Ground	–	–
13 (13)	$\overline{\text{RESET}}$	Turns ON pull down resistor if POC or watchdog timer overflows and if the stack pointer overflows or underflows, and resets the system. Usually, the pull-down resistor is ON.	–	Input
14 (14)	$P1A_0$	μPD17P136M1, μPD17P136M3: This pin is 1-bit output port (N-ch open-drain output) and can be used as the output lines of a key matrix.	N-ch open-drain	High-impedance output
		μPD17P136M2, μPD17P136M4: This pin is 1-bit input port (CMOS input). However, it cannot release the STOP mode.	–	Input
15 (16) 16 (17) 17 (18) 18 (19)	$P0A_0$ $P0A_1$ $P0A_2$ $P0A_3$	These pins are CMOS input pins with a 4-bit pull-up resistor. They can be used as the key return input lines of a key matrix. If any one of these pins goes low, the standby status is released.	–	Input
19 (20) 20 (21) 21 (22) 22 (23)	$P0B_0$ $P0B_1$ $P0B_2$ $P0B_3$	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units. In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low. In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Input

Remark The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

2.1 Normal Operation Mode (2/2)

Pin No.	Symbol	Function	Output Format	At Reset
23 (24) 24 (25) 25 (26) 26 (27)	$P0C_0$ $P0C_1$ $P0C_2$ $P0C_3$	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 4-bit units (group I/O). In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low. In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Low-level output
(15) (30)	IC1 IC2	These pins cannot be used. Leave open.	–	–

Remark The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

2.2 PROM Programming Mode

Pin No.	Symbol	Function	Output Format	At Reset
3	V_{PP}	Power supply for PROM programming. Apply +12.5 V to this pin as the program voltage when writing/verifying program memory.	–	–
9	V_{DD}	Power supply. Apply +6 V to this pin when writing/verifying program memory.	–	–
11	CLK	Inputs clock for PROM programming.	–	–
12	GND	Ground.	–	–
19 (20) | 22 (23)	MD_0 | MD_3	Input pins used to select operation mode when PROM is programmed.	–	Input
23 (24) | 26 (27) 27 (28) 28 (29) 1 2	D_4 | D_7 D_0 D_1 D_2 D_3	Input/output 8-bit data for PROM programming	CMOS push-pull	Input

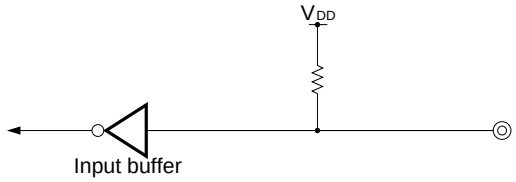
Remarks 1. The other pins are not used in the PROM programming mode. How to handle the other opins are described in **PIN CONFIGURATION (2) PROM programming mode**.

2. The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

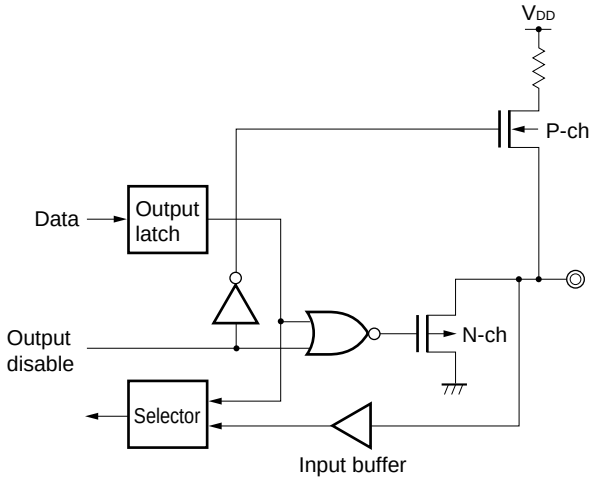
2.3 Input/Output Circuits

The equivalent input/output circuit for each μPD17P236 pin is shown below.

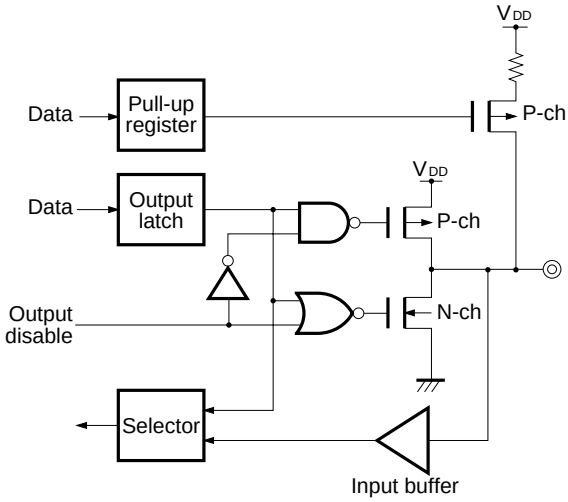
(1) P0A



(2) P0B, P0C, P0D

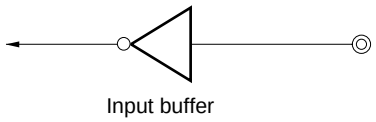


(3) P0E

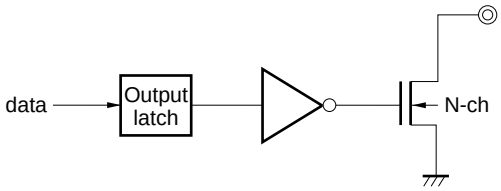


(4) P1A

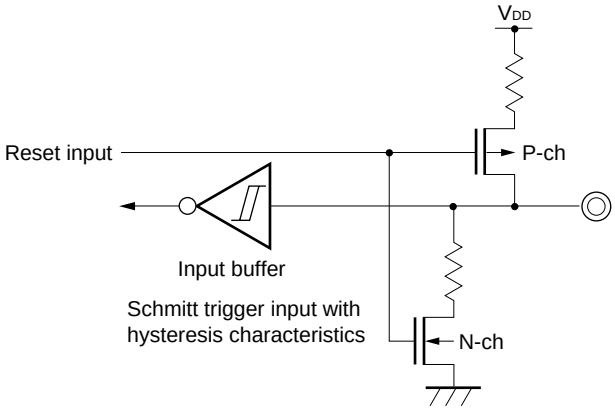
- Input mode (μPD17P236M2, 17P236M4)



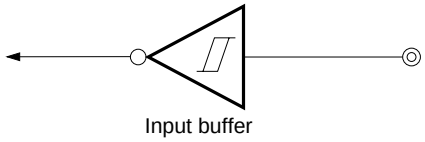
- Output mode (μPD17P236M1, 17P236M3)



(5) $\overline{\text{RESET}}$

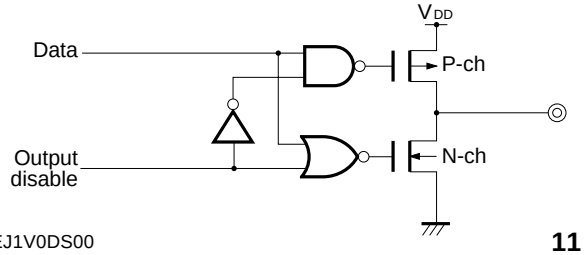


(6) INT



Schmitt trigger input with hysteresis characteristics

(7) REM



2.4 Processing of Unused Pins

Process the unused pins as follows:

Table 2-1. Processing of Unused Pins

Pin	Recommended Connection
$P0A_0$-$P0A_3$	Leave open.
$P0B_0$-$P0B_3$	
$P0C_0$-$P0C_3$	
$P0D_0$-$P0D_3$	
$P0E_0$-$P0E_3$	Input : Individually connect to V_{DD} or GND via resistor. Output : Leave open.
$P1A_0$	Connect to GND.
REM	Leave open.
INT	Connect to GND.
IC1, IC2	These pins cannot be used. Leave open.

2.5 Notes on Using the $\overline{\text{RESET}}$ and INT Pins

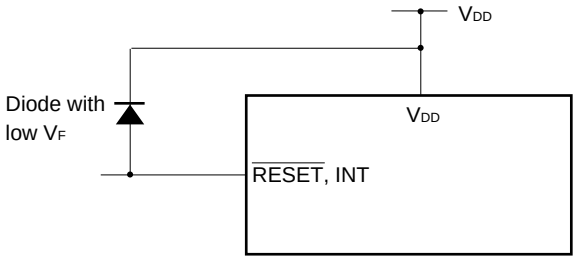
In addition to the functions shown in **2. PIN FUNCTIONS**, the $\overline{\text{RESET}}$ pin also has the function of setting a test mode (for IC testing) in which the internal operations of the μPD17P236 are tested.

When a voltage higher than V_{DD} is applied to either of these pins, the test mode is set. This means that, even during normal operation, the μPD17P236 may be set in the test mode if noise exceeding V_{DD} is applied.

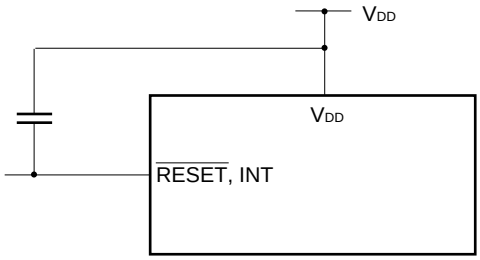
For example, if the wiring length of the $\overline{\text{RESET}}$ or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- **Connect diode with low V_F between V_{DD} and $\overline{\text{RESET}}$/INT pin**



- **Connect capacitor between V_{DD} and $\overline{\text{RESET}}$/INT pin**



3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD17P236 is a one-time PROM of 16,384 × 16 bits.

To write or verify this one-time PROM, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

Table 3-1. Pins Used to Write/Verify Program Memory

Pin Name	Function
V_{PP}	Supplies voltage when writing/verifying program memory. Apply +12.5 V to this pin.
V_{DD}	Power supply. Supply +6 V to this pin when writing/verifying program memory.
CLK	Inputs clock to update address when writing/verifying program memory. By inputting pulse four times to CLK pin, address of program memory is updated.
MD_0-MD_3	Input to select operation mode when writing/verifying program memory.
D_0-D_7	Inputs/outputs 8-bit data when writing/verifying program memory.

3.1 Operating Mode When Writing/Verifying Program Memory

The μPD17P236 is set in the program memory write/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after the μPD17P236 has been in the reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V) for a specific time. In this mode, the operating modes shown in Table 3-2 can be set by setting the MD_0 through MD_3 pins. Leave all the pins other than those shown in Table 3-1 unconnected or connect them to GND via pull-down resistor (470 Ω). (See **PIN CONFIGURATION (2) PROM programming mode.)**

Table 3-2. Setting Operation Mode

Setting of Operating Mode						Operating Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

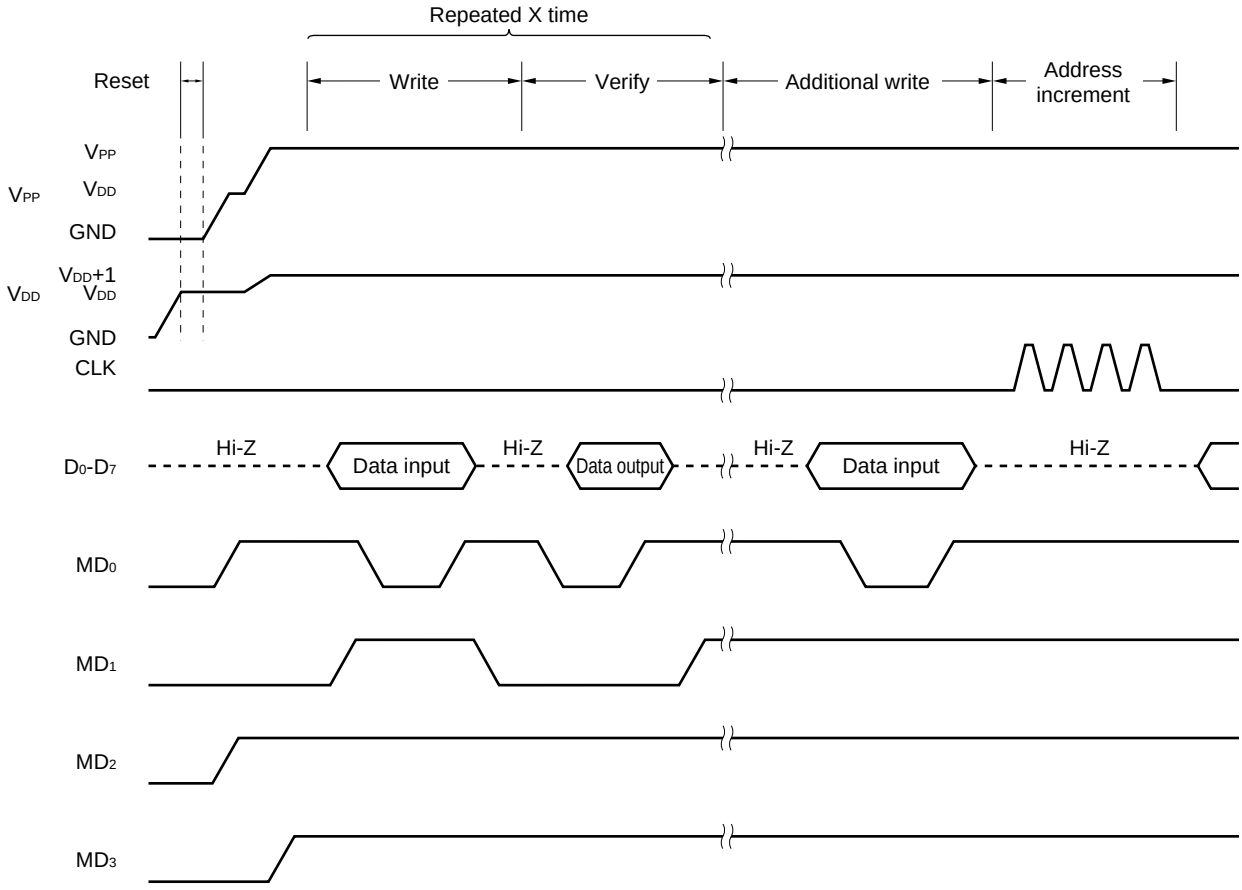
×: don't care (L or H)

3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

(1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
(2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
(3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
(4) Set the program memory address 0 clear mode by using the mode setting pins.
(5) Supply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Write data to the program memory in the 1-ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the data have been written to the program memory, proceed to (10). If not, repeat steps (7) through (9).
(10) Additional writing of (number of times of writing in (7) through (9): X) × 1 ms.
(11) Set the program inhibit mode.
(12) Input a pulse to the CLK pin four times to update the program memory address (+1).
(13) Repeat steps (7) through (12) up to the last address.
(14) Set the 0 clear mode of the program memory address.
(15) Change the voltages on the V_{DD} and V_{PP} pins to 5 V.
(16) Turn off power.

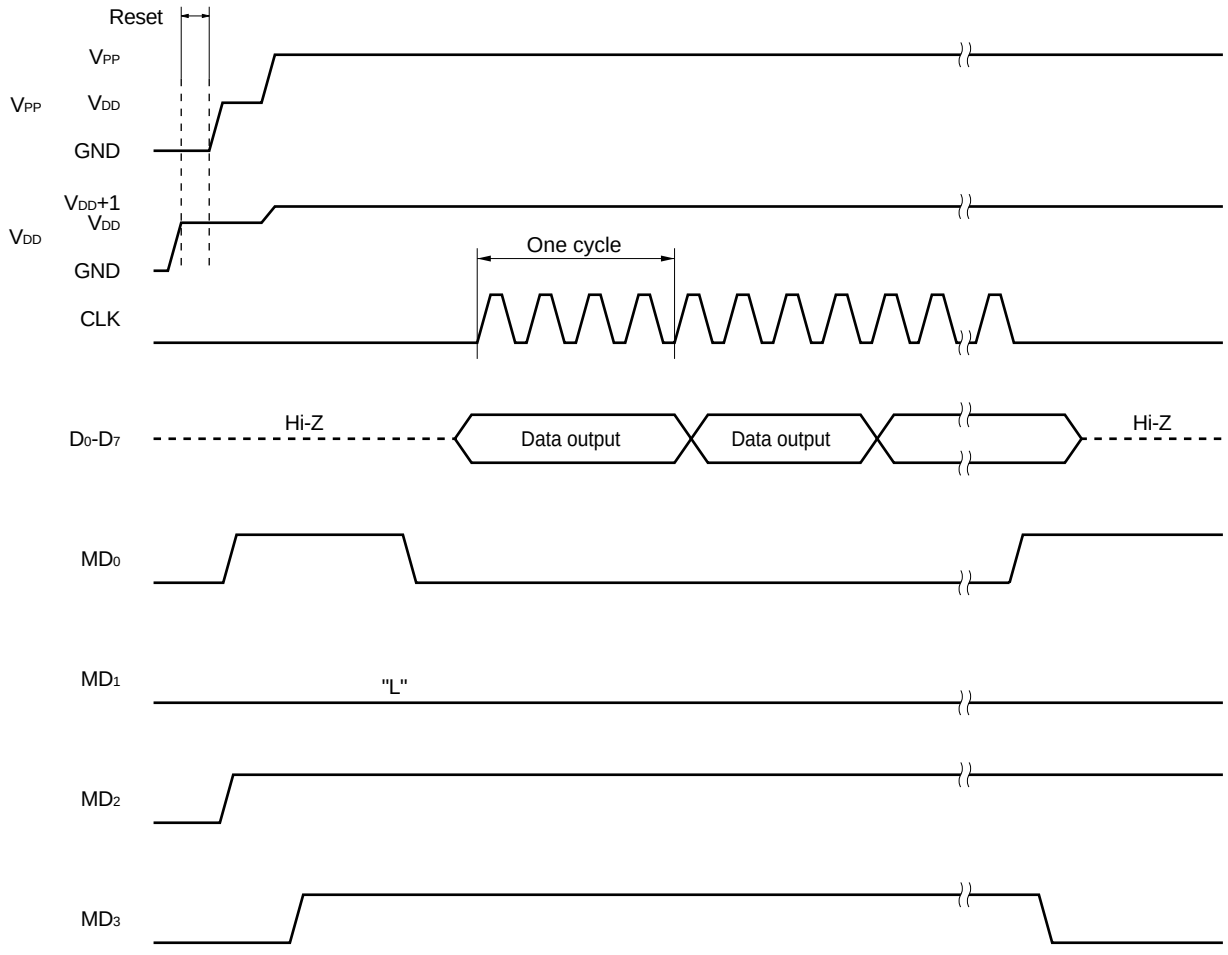
The following figure illustrates steps (2) through (12) above.



3.3 Program Memory Reading Procedure

(1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
(2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
(3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
(4) Set the program memory address 0 clear mode by using the mode setting pins.
(5) Supply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
(8) Set the program inhibit mode.
(9) Set the program memory address 0 clear mode.
(10) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
(11) Turn off power.

The following figure illustrates steps (2) through (9) above.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
PROM power supply	V_{PP}			–0.3 to +13.5	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current[Note]	I_{OH}	REM pin	Peak value	–36.0	mA
			rms value	–24.0	mA
		1 pin (P0E pin)	Peak value	–7.5	mA
			rms value	–5.0	mA
		Total of P0E pins	Peak value	–22.5	mA
			rms value	–15.0	mA
Low-level output current[Note]	I_{OL}	1 pin (P0B, P0C, P0D, P0E, $P1A_0$, or REM pin)	Peak value	7.5	mA
			rms value	5.0	mA
		Total of P0B, P0C, P0D, $P1A_0$, REM pins	Peak value	22.5	mA
			rms value	15.0	mA
		Total of P0E pins	Peak value	30.0	mA
			rms value	20.0	mA
Operating temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Power dissipation	P_d	T_A = 85°C		180	mW

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

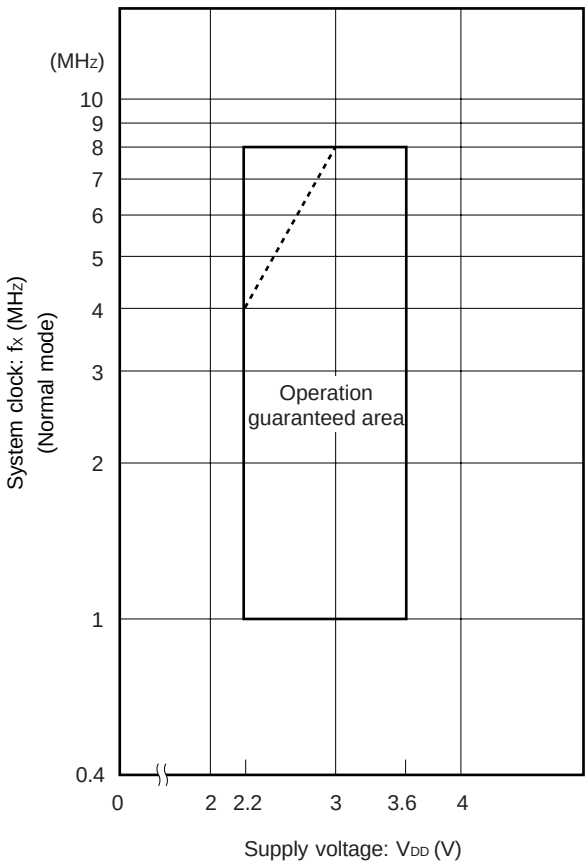
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Ranges (T_A = –40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	f_X = 1 MHz	High-speed mode (Instruction execution time: 16 μs)	2.2		3.6	V
	V_{DD2}	f_X = 4 MHz	High-speed mode (Instruction execution time: 4 μs)				
	V_{DD3}	f_X = 8 MHz	Ordinary mode (Instruction execution time: 4 μs)				
	V_{DD4}		High-speed mode (Instruction execution time: 2 μs)	3.0		3.6	V
Oscillation frequency	f_X			1.0	4.0	8.0	MHz
Operating temperature	T_A			–40	+25	+85	°C
Low-voltage detector circuit[Note]	t_{CY}			4		32	μs

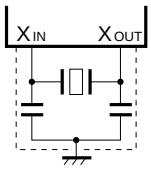
Note Reset if the status of V_{DD} = 2.05 V (TYP.) lasts for 1 ms or longer. Program hang-up does not occur even if the voltage drops, until the reset function is effected. Some oscillators stop oscillating before the reset function is effected.

f_X vs V_{DD}



Remark The region indicated by the broken line in the above figure is the guaranteed operating range in the high-speed mode.

System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

Resonator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]		1.0	4.0	8.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reached MIN. in oscillation voltage range			4	ms

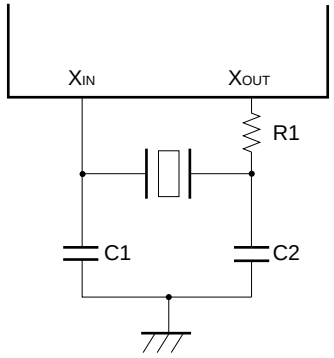
Notes 1. The oscillation frequency only indicates the oscillator characteristics.

2. The oscillation stabilization time is necessary for oscillation to be stabilized, after V_{DD} application or STOP mode release.

Caution To use a system clock oscillator circuit, perform the wiring in the area enclosed by the dotted line in the above figure as follows, to avoid adverse wiring capacitance influences:

- **Keep wiring length as short as possible.**
- **Do not cross a signal line with some other signal lines. Do not route the wiring in the vicinity of lines through which a large current flows.**
- **Always keep the oscillator capacitor ground at the same potential as GND. Do not ground the capacitor to a ground pattern, through which a large current flows.**
- **Do not extract signals from the oscillator.**

External circuit example



Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHI1}	P1A0 (input), $\overline{RESET}$, INT			0.8V_{DD}		V_{DD}	V
	V_{IH2}	P0A, P0B, P0C, P0D			0.7V_{DD}		V_{DD}	V
	V_{IH3}	P0E			0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P1A0 (input), $\overline{RESET}$, INT			0		0.2V_{DD}	V
	V_{IL2}	P0A, P0B, P0C, P0D			0		0.3V_{DD}	V
	V_{IL3}	P0E			0		0.35V_{DD}	V
High-level input leakage current	I_{LIH}	P0A, P0B, P0C, P0D, P0E, P1A0, $\overline{RESET}$, INT	V_{IH} = V_{DD}				3	μA
Low-level input leakage current	I_{LIL1}	INT, P1A0	V_{IL} = 0 V				–3	μA
	I_{LIL2}	P0E	V_{IL} = 0 V w/o pull-up resistor				–3	μA
Internal pull-up resistor	R_1	P0E, $\overline{RESET}$ (pulled up)			25	50	100	kΩ
	R_2	P0A, P0B, P0C, P0D			100	200	400	kΩ
Internal pull-down resistor	R_3	$\overline{RESET}$ (pulled down)			2.5	5	10	kΩ
High-level output current	I_{OH1}	REM	V_{OH} = 1.0 V, V_{DD} = 3 V		–6	–13	–24	mA
High-level output voltage	V_{OH}	P0E, REM	I_{OH} = –0.5 mA		V_{DD}–0.3		V_{DD}	V
Low-level output voltage	V_{OL1}	P0B, P0C, P0D, P1A0 (output), REM	I_{OL} = 0.5 mA		0		0.3	V
	V_{OL2}	P0E	I_{OL} = 1.5 mA		0		0.3	V
Low-voltage detection voltage	V_{DT}	$\overline{RESET}$ pin pulled down, V_{DT} = V_{DD}				2.05	2.2	V
Data retention voltage	V_{DDDR}	$\overline{RESET}$ = low level or STOP mode			1.3		3.6	V
Supply current	I_{DD1}	Operating mode (high-speed)	V_{DD} = 3 V ±10%	f_X = 1 MHz		0.55	1.1	mA
				f_X = 4 MHz		1.0	2.0	mA
				f_X = 8 MHz		1.3	2.6	mA
	I_{DD2}	Operating mode (low-speed)	V_{DD} = 3 V ±10%	f_X = 1 MHz		0.5	1.0	mA
				f_X = 4 MHz		0.75	1.5	mA
				f_X = 8 MHz		0.9	1.8	mA
	I_{DD3}	HALT mode	V_{DD} = 3 V ±10%	f_X = 1 MHz		0.4	0.8	mA
				f_X = 4 MHz		0.5	1.0	mA
				f_X = 8 MHz		0.6	1.2	mA
	I_{DD4}	STOP mode	V_{DD} = 3 V ±10% built-in POC			2.0	20.0	μA
				T_A = 25°C		2.0	5.0	μA

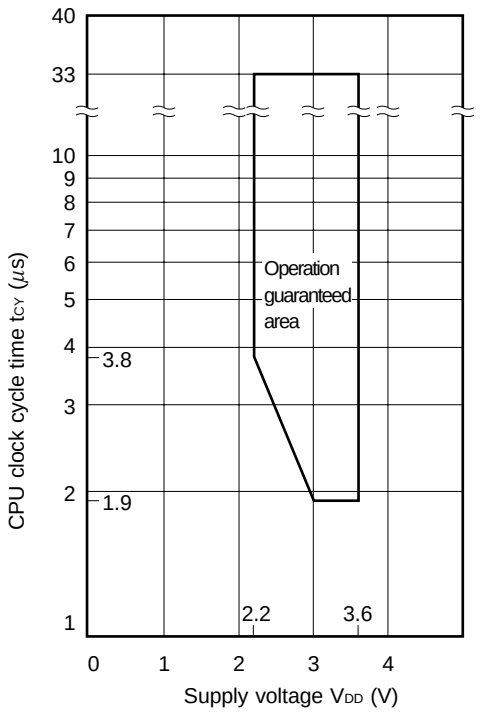
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU clock cycle time[Note] (instruction execution time)	t_{CY1}		3.8		33	μs
	t_{CY2}	V_{DD} = 3.0 to 3.6 V	1.9		33	μs
INT high/low level width	t_{INTH}, t_{INTL}		20			μs
$\overline{\text{RESET}}$ low level lwidth	t_{RSL}		10			μs

Note The CPU clock cycle time (instruction execution time) is determined by the oscillation frequency of the resonator connected and SYSCK (RF: address 02H) of the register file.

The figure on the right shows the CPU clock cycle time t_{CY} vs. supply voltage V_{DD} characteristics.

t_{CY} vs V_{DD}



DC Programming Characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Other than CLK	0.7V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Other than CLK	0		0.3V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD_0 = V_{IL}, MD_1 = V_{IH}			30	mA

Cautions 1. Keep V_{PP} to within +13.5 V including overshoot.

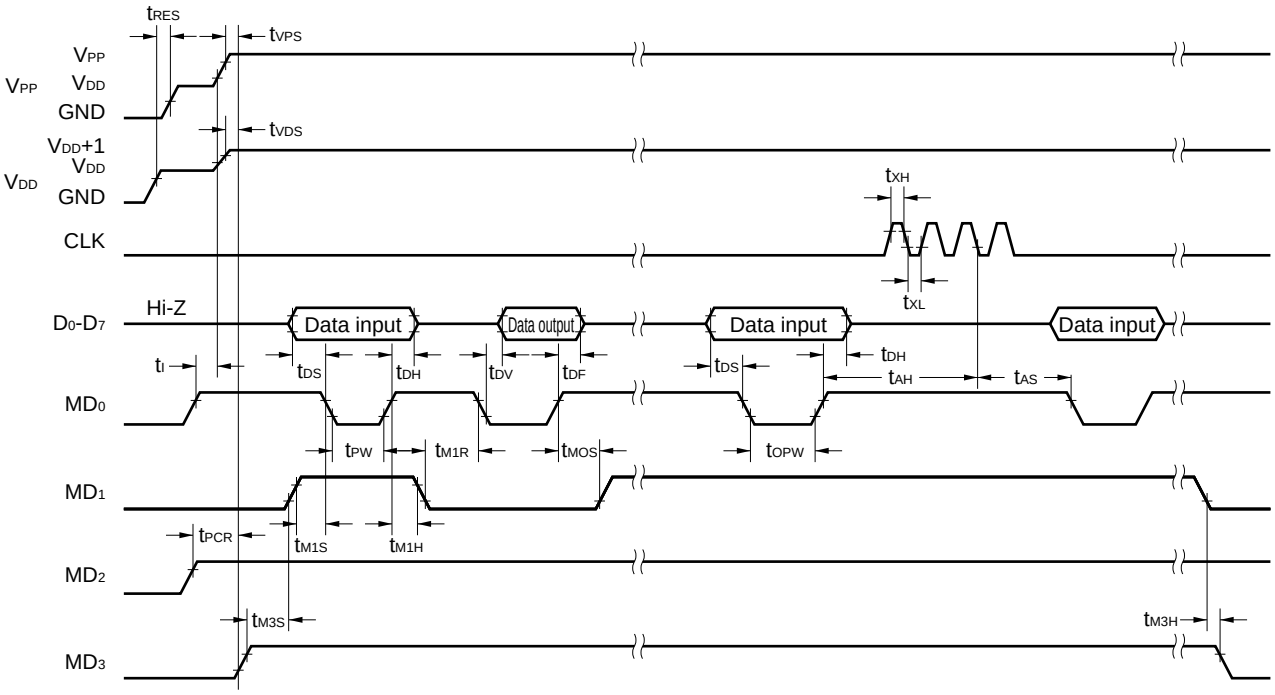
2. Apply V_{DD} before V_{PP} and turns it off after V_{PP}.

AC Programming Characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

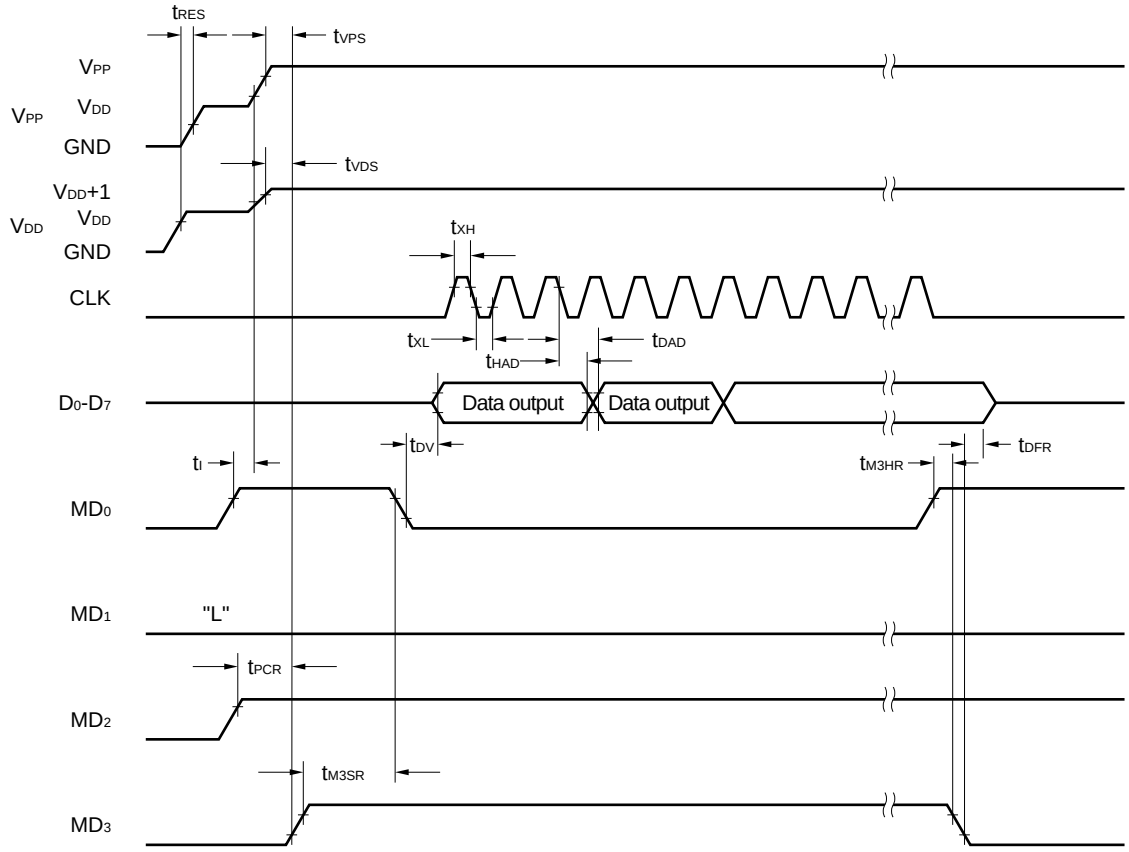
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note] (vs. MD_0↓)	t_{AS}		2			μs
MD_1 setup time (vs. MD_0↓)	t_{M1S}		2			μs
Data setup time (vs. MD_0↓)	t_{DS}		2			μs
Address hold time[Note] (vs. MD_0↑)	t_{AH}		2			μs
Data hold time (vs. MD_0↑)	t_{DH}		2			μs
MD_0↑→ data output float delay time	t_{DF}		0		130	ns
V_{PP} setup time (vs. MD_3↑)	t_{VPS}		2			μs
V_{DD} setup time (vs. MD_3↑)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD_0 setup time (vs. MD_1↑)	t_{MOS}		2			μs
MD_0↓→ data output delay time	t_{DV}	MD_0 = MD_1 = V_{IL}			1	μs
MD_1 hold time (vs. MD_0↑)	t_{M1H}	$t_{M1H}+t_{M1R} \geq 50$ μs	2			μs
MD_1 recovery time (vs. MD_0↓)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-, low-level width	t_{XH}, t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode set time	t_I		2			μs
MD_3 setup time (vs. MD_1↑)	t_{M3S}		2			μs
MD_3 hold time (vs. MD_1↓)	t_{M3H}		2			μs
MD_3 setup time (vs. MD_0↓)	t_{M3SR}	When program memory is read	2			μs
Address[Note] → data output delay time	t_{DAD}	When program memory is read			2	μs
Address[Note] → data output hold time	t_{HAD}	When program memory is read	0		130	ns
MD_3 hold time (vs. MD_0↑)	t_{M3HR}	When program memory is read	2			μs
MD_3↓→ data output float delay time	t_{DFR}	When program memory is read			2	μs
Reset setup time	t_{RES}		10			μs

Note The internal address increment (+1) is performed on the fall of the 3rd clock, where 4 clocks compreise one cycle. The internal clock is not connected to a pin.

Program Memory Write Timing

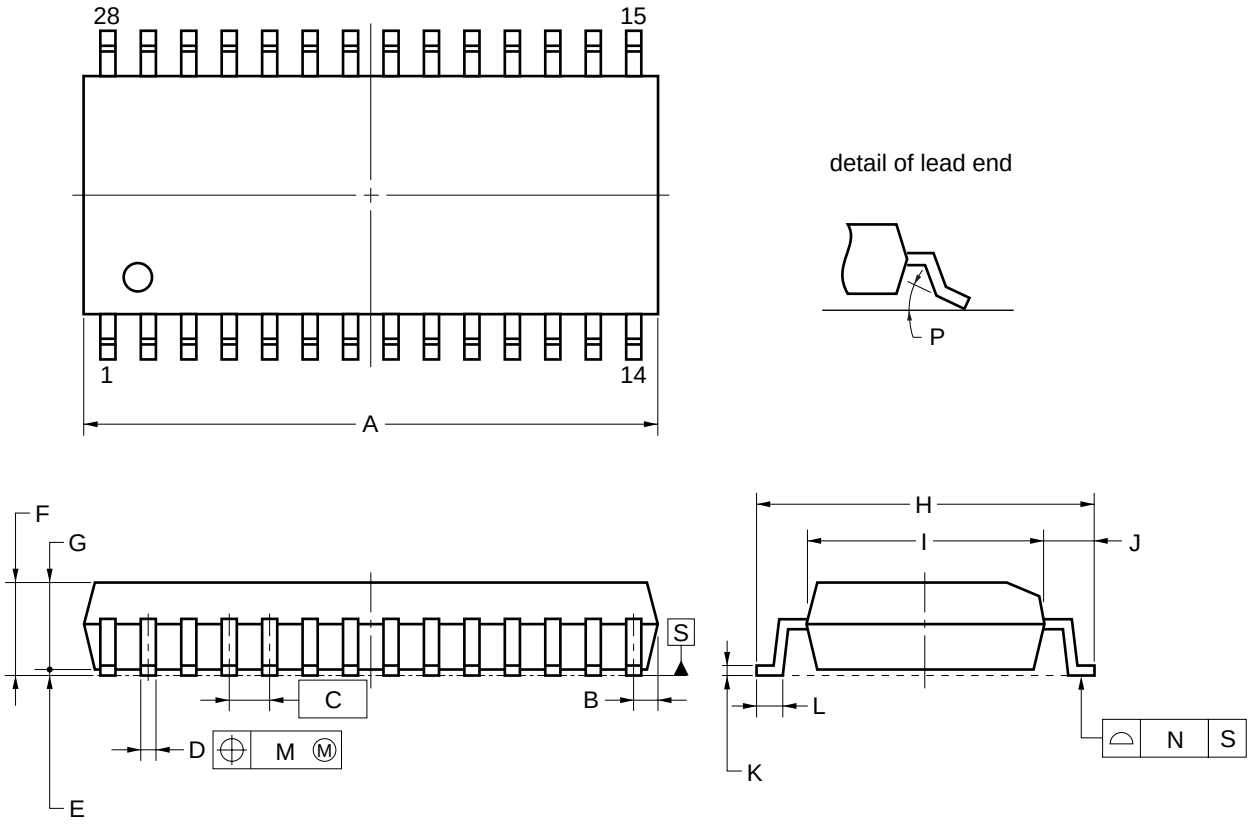


Program Memory Read Timing



5. PACKAGE DRAWING

28-PIN PLASTIC SOP (9.53 mm (375))



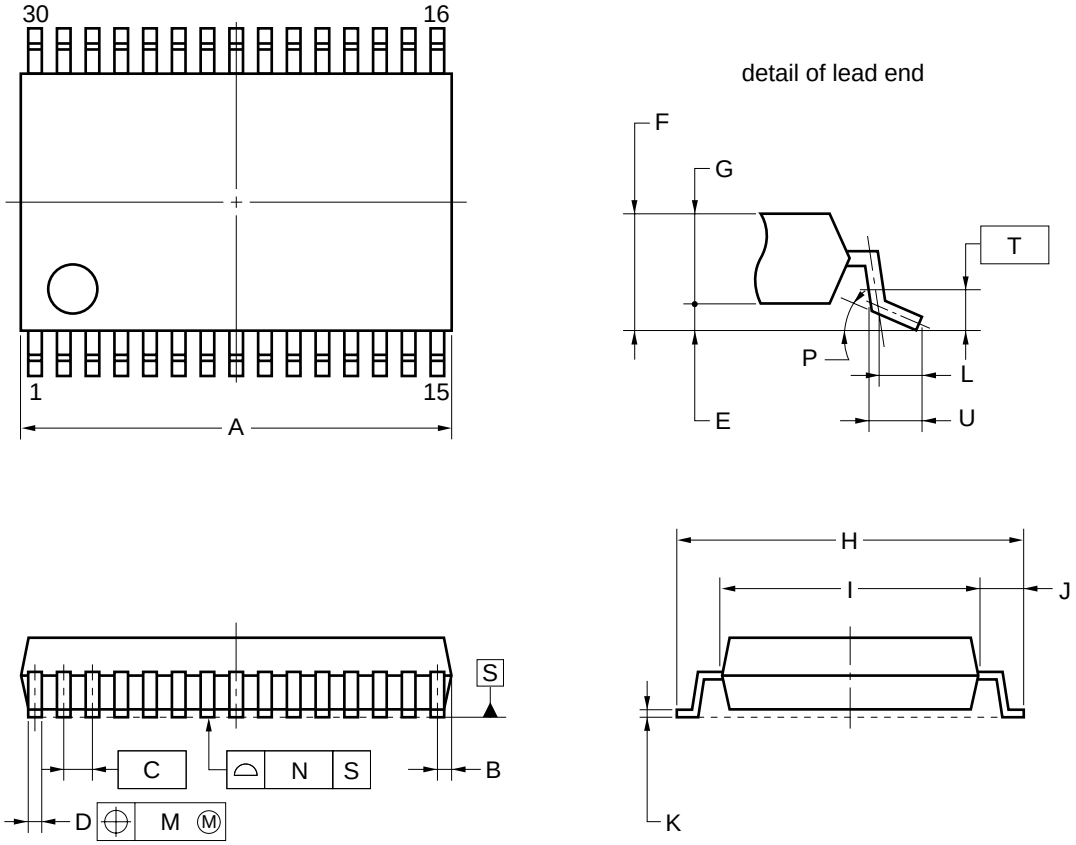
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.9±0.17
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	2.6±0.2
G	2.50
H	10.3±0.3
I	7.2±0.2
J	1.6±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.8±0.2
M	0.12
N	0.15
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GM-50-375B-5

30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

6. RECOMMENDED SOLDERING CONDITIONS

For the μPD17P236 soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For other soldering methods, please consult with NEC personnel.

Table 6-1. Soldering Conditions of Surface Mount Type

(1) μPD17P236M1GT: 28-pin plastic SOP (9.35 mm (375))
μPD17P236M2GT: 28-pin plastic SOP (9.35 mm (375))
μPD17P236M3GT: 28-pin plastic SOP (9.35 mm (375))
μPD17P236M4GT: 28-pin plastic SOP (9.35 mm (375))

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max. Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max, Time: 10 seconds max., Number of times: once, preheating temperature: 120°C max. (package surface temperature) Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	—

Note After opening the dry pack, store it at 25 °C or less and 6.5 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD17P236M1MC-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD17P236M2MC-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD17P236M3MC-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD17P236M4MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Symbol
Intrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max. Number of days: 3[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max. Number of days: 3[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max, Time: 10 seconds max., Number of times: once, preheating temperature: 120°C max. (package surface temperature) Number of days: 3[Note] (after that, prebaking is necessary at 125°C for 10 hours)	WS60-103-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	—

Note After opening the dry pack, store it at 25 °C or less and 6.5 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX. DEVELOPMENT TOOLS

To develop the programs for the μPD17P236 subseries, the following development tools are available:

Hardware

Name	Remarks
In-circuit emulator (IE-17K, IE-17K-ET[Note 1])	IE-17K and IE-17K-ET are the in-circuit emulators used in common with the 17K series microcontroller. IE-17K and IE-17K-ET are connected to a PC-9800 series or IBM PC/AT™ compatible machines as the host machine with RS-232C. By using these in-circuit emulators with a system evaluation board corresponding to the microcomputer, the emulators can emulate the microcomputer. A higher level debugging environment can be provided by using man-machine interface *SIMPLEHOST*™.
SE board (SE-17235)	This is an SE board for μPD17236 subseries. It can be used alone to evaluate a system or in combination with an in-circuit emulator for debugging.
Emulation probe (EP-17K28GT)	EP-17K28GT is an emulation probe for 17K series 28-pin SOP (GM-375B). When used with EV9500GT-28[Note 2], it connects an SE board to the target system.
Emulation probe (EP-17K30GS)	EP-17K30GS is an emulation probe for 17K series 30-pin SSOP (MC-5A4). When used with EV-9500GT-30[Note 3], it connects an SE board to the target system.
Conversion adapter (EV-9500GT-28[Note 2])	The EV-9500GT-28 is a conversion adapter for the 28-pin SOP (GM-375B). It is used to connect the EP-17K28GT and target system.
Conversion adapter (EV-9500GT-30[Note 3])	The EV-9500GT-30 is a conversion adapter for the 30-pin SSOP (MC-5A4). It is used to connect the EP-17K30GS and target system.
PROM programmer (AF-9706[Note 4], AF-9708[Note 4], AF-9709[Note 4])	AF-9706, AF-9708, and AF-9709 are PROM programmers corresponding to μPD17P236. By connecting program adapter PA-17P236 to this PROM programmer, μPD17P236 can be programmed.
Program adapter (PA-17P236)	PA-17P236 are adapters that is used to program μPD17P236, and is used in combination with AF-9706, AF-9708, or AF-9709.

Notes 1. Low-cost model: External power supply type

2. Two EV-9500GT-28 are supplied with the EP-17K28GT. Five EV-9500GT-28 are optionally available as a set.

3. Two EV-9500GT-30 are supplied with the EP-17K30GS. Five EV-9500GT-30 are optionally available as a set.

4. These are products from Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd. (Tel: 03-3733-1166).

Software

Name	Outline	Host Machine	OS	Supply	Order Code
17K assembler (RA17K)	The RA17K is an assembler common to the 17K series products. When developing the program of devices, RA17K is used in combination with a device file (AS17235).	PC-9800 series	Japanese Windows™	3.5" 2HD	μSAA13RA17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13RA17K
			English Windows		μSBB13RA17K
Device file (AS17235)	The AS17235 is a device file for μPD17230, 17231, 17232, 17233, 17234, 17235, and 17236 and is used in combination with an assembler for the 17K series (RA17K).	PC-9800 series	Japanese Windows	3.5" 2HD	μSAA13AS17235
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13AS17235
			English Windows		μSBB13AS17235
Support software (*SIMPLEHOST*)	*SIMPLEHOST* is a software package that enables man-machine interface on the Windows when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	Japanese Windows	3.5" 2HD	μSAA13ID17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μSAB13ID17K
			English Windows		μSBB13ID17K

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

SIMPLEHOST **is a trademark of NEC Corporation.**

Windows is either a registered trademark or a trademark of Microsoft Corporation in the United States and/or other countries.

PC/AT is a trademark of IBM Corporation.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

- **The information in this document is current as of June, 2000. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4