RECOMMENDED OPERATING CONDITIONS

The PJ34119 is a low power audio amplifier intergrated circuit intended （primarily）for telephone applications， such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply coltages(2.0V minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80dB , and the closed loop gain is set with two external resistors. A chip Disable pin permits powering down and/or muting the input signal. The PJ34119 is available in standard DIP-8, SOP-8 package.

DIP-8 SOP-8

Pin : 1.Cd 5.Vo1
2.Fc2 6.Vcc
3.Fc1 7.Gnd
4.Vin 8.Vo2

FEATURES

- Low Quiescent Supply Current(2.7mA Typ)for Battery powered Applications.
- Wide Operating Supply Voltage Range(2.0V to 16V), Allows Telephone Line Powered Applications.
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current(65 μ A Typ)
- Drives a Wide Range of Speaker Loads(8.0 Ω and Up)
- Output Power Exceeds 250mW with 32 Ω Speaker
- Low Total Harmonic Distortion(0.5% Typ)
- Gain Adjustable from <0 dB to >46dB for Voice Band
- Requires Few External Components.

ORDERING INFORMATION

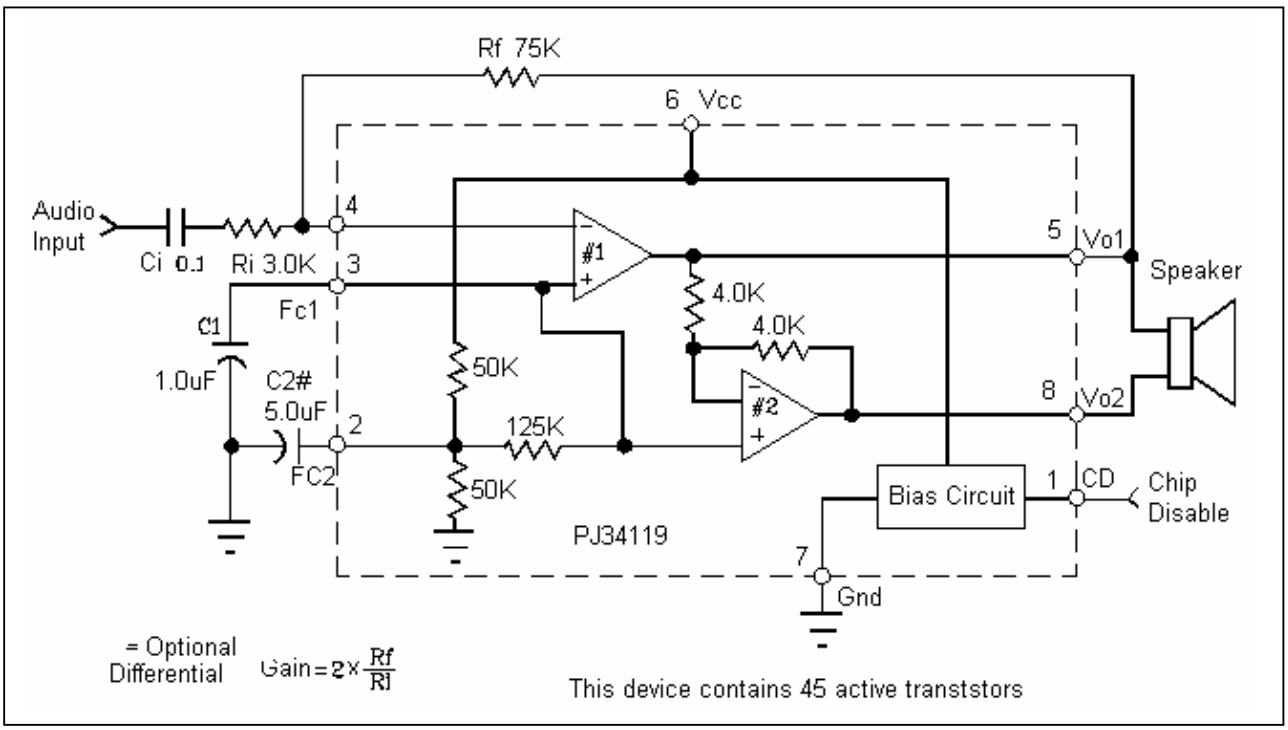
Device	Operating Temperature	Package
PJ34119CD	-20℃ to +85℃	DIP-8
PJ34119CS		SOP-8

ABSOLUTE MAXIMUM RATINGS (T_a = 25℃)

Characteristic	Value	Unit
Supply Voltage	-1.0 to 18	Vdc
Maximum Output Crrent at V_{O1},V_{O2}	±250	mA
Maximum Voltage @Vin,FC1,FC2,CD	-1.0,Vcc+1.0	Vdc
Applied Output Voltage to VO1,VO2 when disabled	-1.0,Vcc+1.0	
Junction Temperature	-55,+140	℃

NOTE:ESD data available upon request.

BLOCK DIAGRAM AND SIMPLIFIED APPLICATION



Characteristics	Symbol	Min	Max	Unit
Supply Voltage Voltage@CD(Pin 1)	V_{CC} V_{CD}	+2.0 0	+16 V_{CC}	Vdc Vdc
Load Impedance	R_L	8.0	-	Ω
Peak Load Current	I_L	-	±200	mA
Differential Gain (5.0KHz Bandwidth)	AVD	0	46	dB
Ambient Temperature	T_A	-20	+70	℃

ELECTRICAL CHARACTERISTICS (T_A=25℃,unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
AC Input Resistance(@ Vin)	Ri	-	>30	-	MΩ
Open Loop Gain(Amplifier #1, f<100Hz)	AVOL1	80	-	-	dB
Closed Loop Gain(Amplifier #2, Vcc=6.0V,f=1KHz, R_L=32Ω)	AV2	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	-	1.5	-	MHz
Output Power: Vcc=3.0V,R_L=16Ω,THD≤10% Vcc=6.0V,R_L=32Ω,THD≤10% Vcc=12V,R_L=100Ω,THD≤10%	 Pout3 Pout6 Pout12	 55 250 400	 - - -	 - - -	mW
Total Hamonic Distortion(f=1KHz) (Vcc=6.0V, R_L=32Ω, Pout=125mW) (Vcc≥3.0V, R_L=8.0Ω, Pout=20mW) (Vcc≥12V, R_L=32Ω, Pout=200mW)	THD	- - -	0.5 0.5 0.6	1.0 - -	%
Power Supply Rejection(Vcc=6.0V, ΔVcc=3.0V) (C1=∞, C2=0.01μF) (C1=0.1μF,C2=0,f=1.0KHz) (C1=1.0μF,C2=5.0μF,f=1.0KHz)	PSRR	50 - -	- 12 52	- - -	dB
Differential Muting (Vcc=6.0V,1.0KHz≤f≤20KHz,CD=2.0V)	GMT	-	>70	-	dB
AMPLIFIERS(DC CHARACTERISTICS)					
Output DC Level@V_{O1},V_{O2}, ,R_L=16(R_f=75K) V_{CC}=3.0V Vcc=6.0V Vcc=12V	 Vo(3) Vo(6) Vo(12)	 1.0 - -	 1.15 2.65 5.56	 1.25 - -	Vdc
Output Level High(Iout=-75mA,2.0≤Vcc≤16V) Low(Iout=75mA, 2.0≤Vcc≤16V)	 V_{OH} V_{OL}	 - -	 Vcc-1.0 0.16	 - -	Vdc
Output DC Offset Voltage(V_{O1}-V_{O2}) (Vcc=6.0V,RL=75KΩ, R_L=32Ω)	ΔVo	-30	0	+30	mV
Input Bias Current@Vin(Vcc=6.0V)	f_{IB}	-	-100	-200	nA
Equivalent Resistance @FC1(Vcc=6.0V) @FC2(Vcc=6.0V)	 R_{FC1} R_{FC2}	 100 18	 150 25	 220 40	KΩ
CHIP DISABLE(Pin1)					
Input Voltage Low High	 V_{IL} V_{IH}	 - 2.0	 - -	 0.8 -	Vdc
Input Resistance(Vcc=V_{CD}=16V)	R_{CD}	50	90	175	KΩ
POWER SUPPLY					
Power Supply Current (Vcc=3.0V,R_L=∞,CD=0.8V) (Vcc=16V,R_L=∞,CD=0.8V) (Vcc=3.0V,R_L=∞,CD=2.0V)	 I_{CC3} I_{CC16} I_{CCD}	 - - -	 2.7 3.3 65	 4.0 5.0 100	 mA mA μA

NOTE:Current into are positive,current out of a pin are negative.

PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Distable-Digital input. A Logic"0"(<0.8V) sets normal operation. A logic"I"（≥2.0V）sets the power down mode. Input impedance is nominally 90KΩ
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open it the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1.0μF capacitor at this pin(with a 5.0μF capacitor at Pin 2)provides(typically)52dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin.This pin can be used as an alternate input.
Vin	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and Vo1.
Vo1	5	Amplifier Output #1. The dc level is ≈(Vcc-0.7)/2
Vcc	6	DC supply voltage (+2.0V to +16V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
Vo2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out-of-phase with that at Vo1. The dc level is≈ (Vcc-0.7V)/2

TYPICAL TEMPERATURE PERFORMANCE (-20°C<T_A<+70°C)

Function	Typical Change	Units
Input Bias Current(@Vin)	±40	ρ A/℃
Total Harmonic Distortion (Vcc=6.0V, R_L=32Ω Pout=125mW, f=1KHz)	+0.003	%/ ℃
Power Supply Current (Vcc=3.0V, R_L=∞,CD=0V) (Vcc=3.0V, R_L=∞,CD=2.0V)	 -2.5 -0.03	μ A/℃

GENERAL

The PJ34119 is a low power audio amplifier capable of low voltage operation (Vcc=2.0V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (Vo1-Vo2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80dB(at f≤100Hz), and the closed loop gain is set by external resistor Rf and Rj. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5MHz. In order to adequately cover the telephone voice band (300Hz to 3400Hz), a maximum closed loop gain of 46 is recommended. Amplifier #2 is internally set to gain of –1.0(0dB).

The outputs of both amplifiers are capable of souring and sinking a peak current of 200mA.The outputs can typically swing to within≈0.4V above ground, and to within≈1.3V below Vcc, at the maximum current. See Figure 18 and 19 for V_{OH} and V_{OL} curves.

The output dc offset voltage (Vo1-Vo2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of Vin (pin 4) and through R_f, forcing Vo1 to shift negative by an amount equal to [$R_f \times I_{IB}$] Vo2 is shifted posited an equal amount. The output offset voltage, specified in the Electrical Characteristics is measured with the feedback the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as wells internal offset voltages of the amplifiers. The bias current is constant with respect to Vcc.

FC1 AND FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies , as shown in the graphs of Figure 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is function of the capacitors , and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50K and 125 KΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of Vcc of +6.0V. The turn-on time is ≈60% longer for Vcc=3.0V, and ≈20% less for Vcc=9.0V. Turn-off time is <10μs upon removal of Vcc.

CHIP DISABLE

The chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0V to 0.8V), the PJ34119 is enabled for normal operation. When Pin 1 is a Logic"1"(2.0V to Vcc V), the IC is disabled. If Pin 1 is open, that is equivalent to Logic "0" although good design proactive dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 KΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70dB.The turn-off time the audio output, from the application of the CD signal, is <2.0μs, and turn on-time is 12 ms-15ms. Both times are independent of C1,C2, and Vcc.

When the PJ34119 is disabled, the voltage at FC1 and FC2 do not change as they are powered from Vcc. The outputs, Vo1 and Vo2, change to high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of Vcc and Ground.

POWER DISSIPATION

Figure 8 to 10 indicate the device dissipation (within the IC) for various combinations of Vcc, R_L, and load power. The maximum power which can safely be dissipated within the PJ34119 is found from the following equation: $P_D=(140°C-T_A)/\theta_{JA}$

Where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.) The power dissipated within the PJ34119, in a given application, is found from the following equation:$P_D=(Vcc\times Icc)+(I_{RMS}\times Vcc)-(R_L\times I_{RMS}^2)$

Where Icc is obtained from Figure 15; and I_{RMS} is the RMS current at the load; and R_L is load resistance.Figure 8 to 10, along with Figure 11 to 13(distortion curves), and a peak working load current of ±200mA, define the operating range for the PJ34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0Ω,16Ω and 32Ω. The left(ascending portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the PJ34119. The right(descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the PJ34119, unlike many other audio amplifiers, However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than afew inches in length

Figure 1.Turn-On Time versus C1,C2 at Power-On

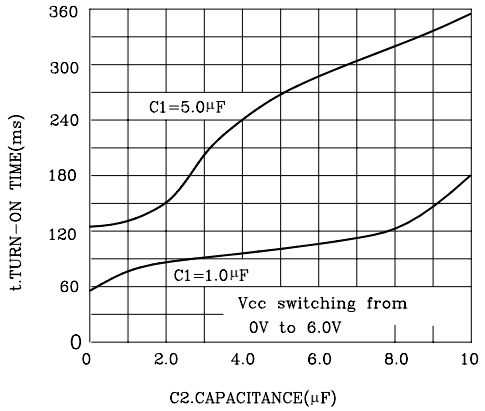


**FIGURE 2.AMPLIFIER #1
OPEN LOOP GAIN AND PHASE**

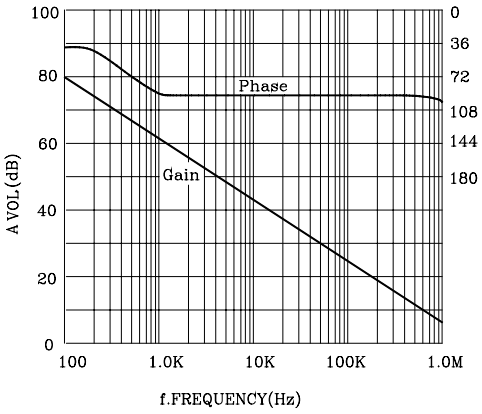


**FIGURE 3.DIFFERENTIAL GAIN
VERSUS FREQUENCY**

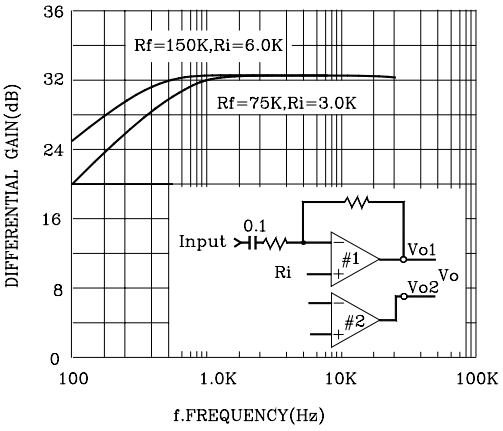


**FIGURE 4.POWER SUPPLY REJECTION versus
FREQUENCY(C2=10μF)**

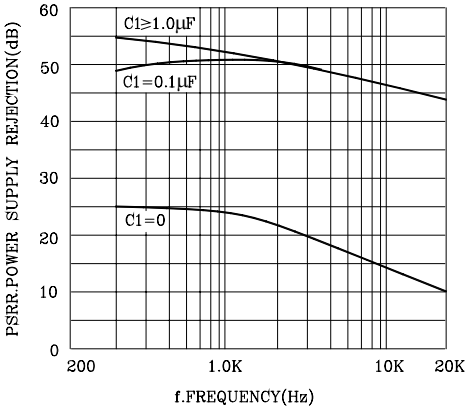


**FIGURE 5.POWER SUPPLY REJECTION versus
FREQUENCY(C2=5.0μF)**

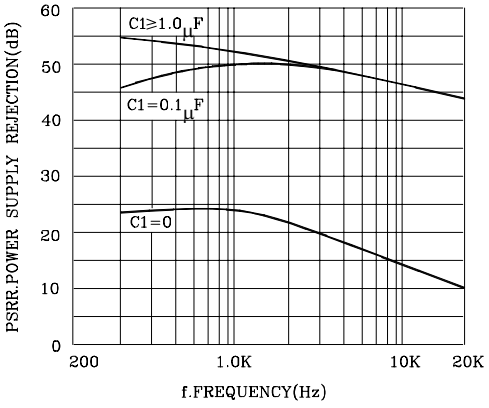


**FIGURE 6.Power SUPPLY REJECTION versus
FREQUENCY(C2=1.0μF)**

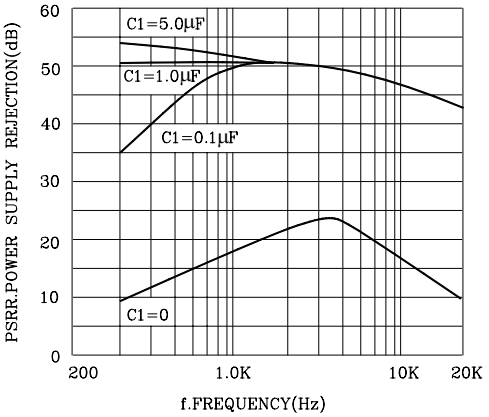


FIGURE 7.POWER SUPPLY REJECTION versus FREQUENCY(C2=0)

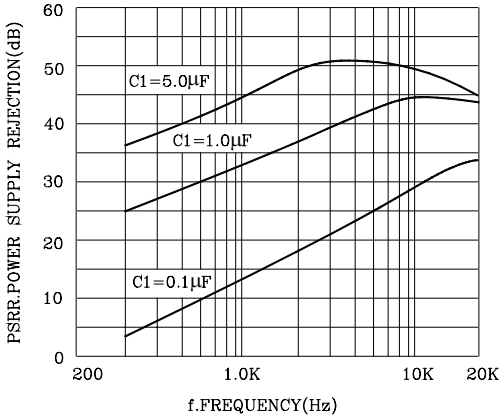


FIGURE 8.DEVICE DISSIPATION, 8.0Ω LOAD

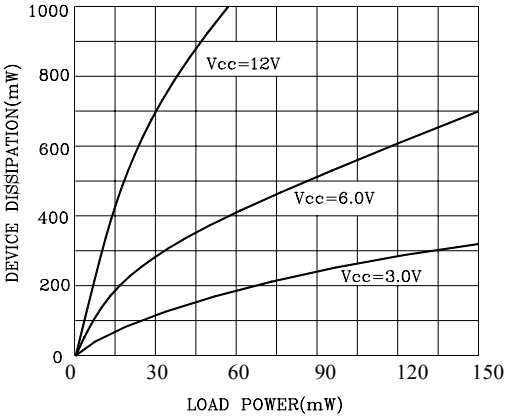


FIGURE 9.DEVICE DISSIPATION,16Ω LOAD

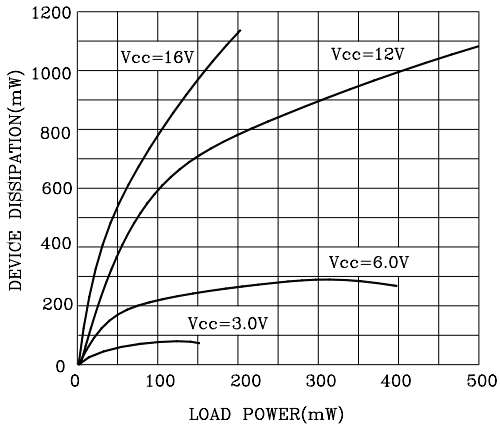


FIGURE 10.DEVIECE DISSIPATION, 32Ω LOAD

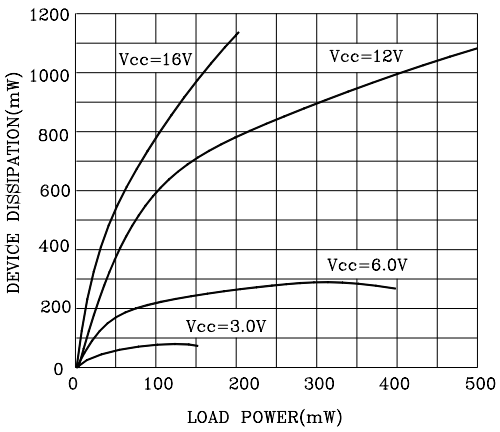


FIGURE 11.DISTORTION versus POWER (f=1.0KHz, AVD=34dB)

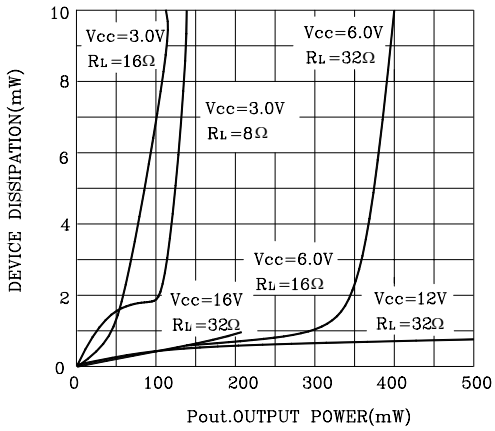


FIGURE 12.DISTORTION versus POWER (f=3.0KHz,AVD=34dB)

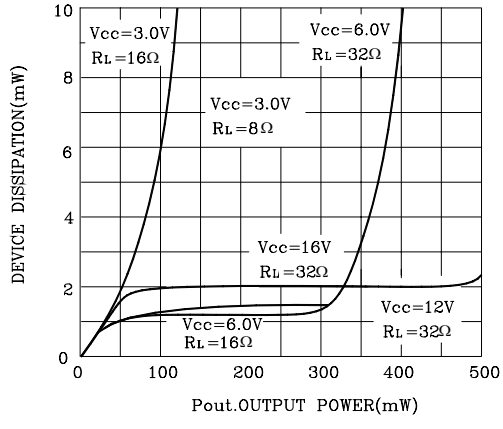


FIGURE 13.DISTORTION versus POWER (f=1,3.0KHz, AVD=12dB)

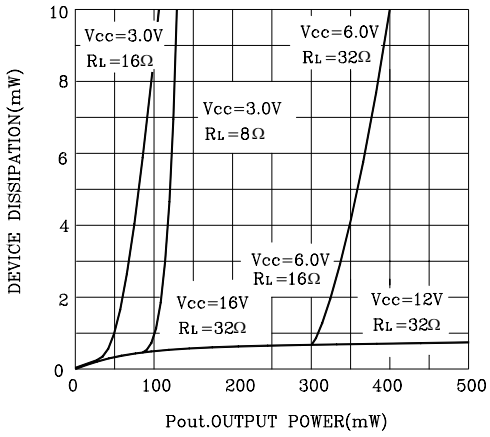


FIGURE 14.MAXIMUM ALLOWABLE LOAD POWER

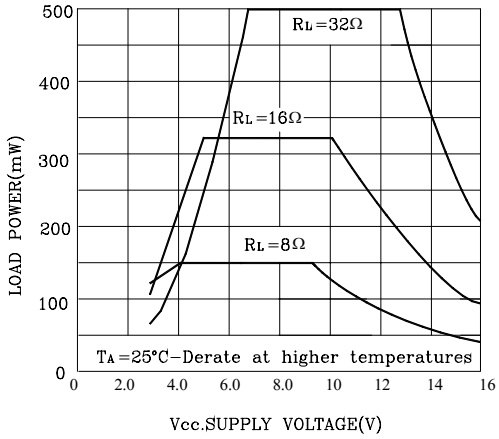


FIGURE 15.POWER SUPPLY CURRENT

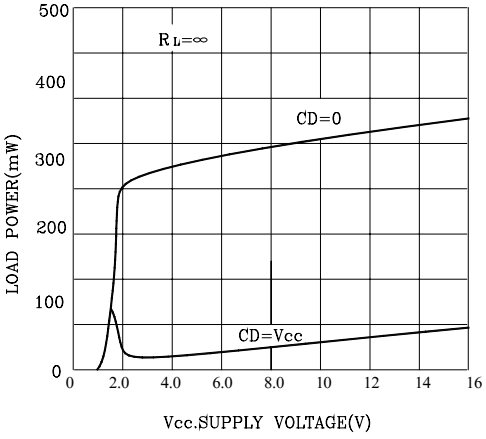


FIGURE 16.SMALL SIGNAL RESPONSE

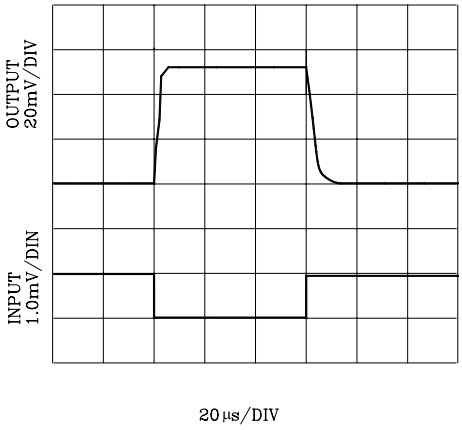


FIGURE 17.LARGE SIGNAL RESPONSE

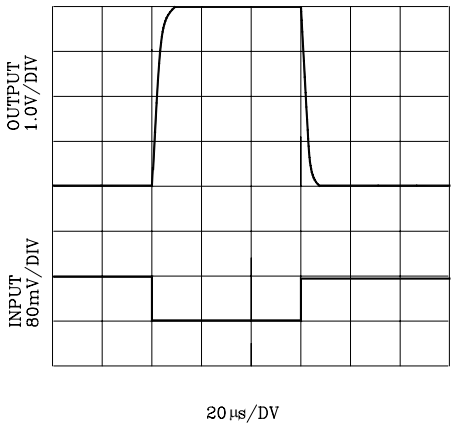


FIGURE 18.V_{CC}-V_{OH} @ V_{O1},V_{O2} versus LOAD CURRENT

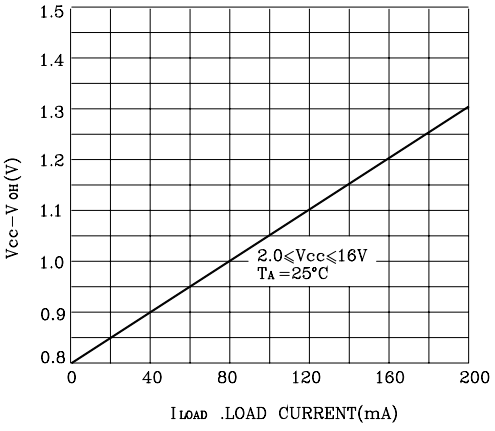


FIGURE 19.V_{OL} @ V_{O1},V_{O2} versus LOAD CURRENT

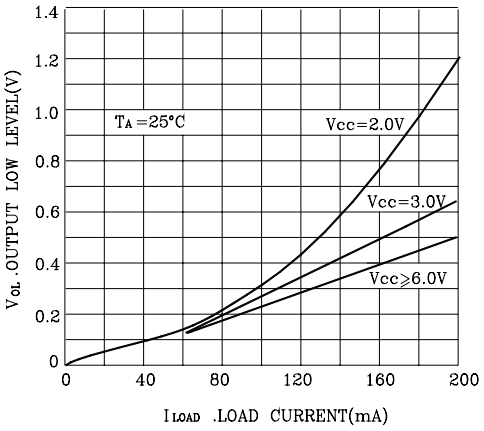


FIGURE 20.INPUT CHARACTERISTICE @ CD (PIN 1)

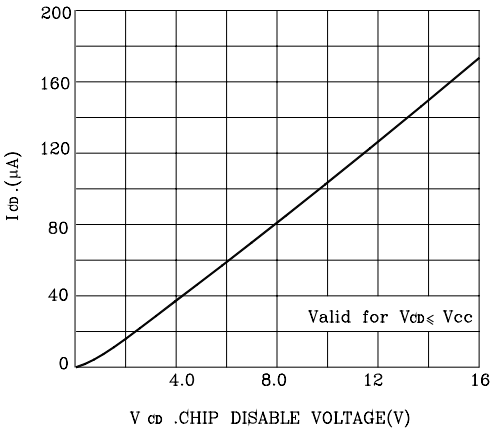


FIGURE 21.FREQUENCY RESPONSE OF FIGURE 22

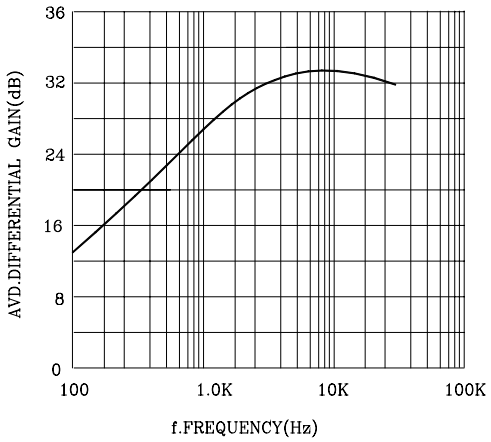
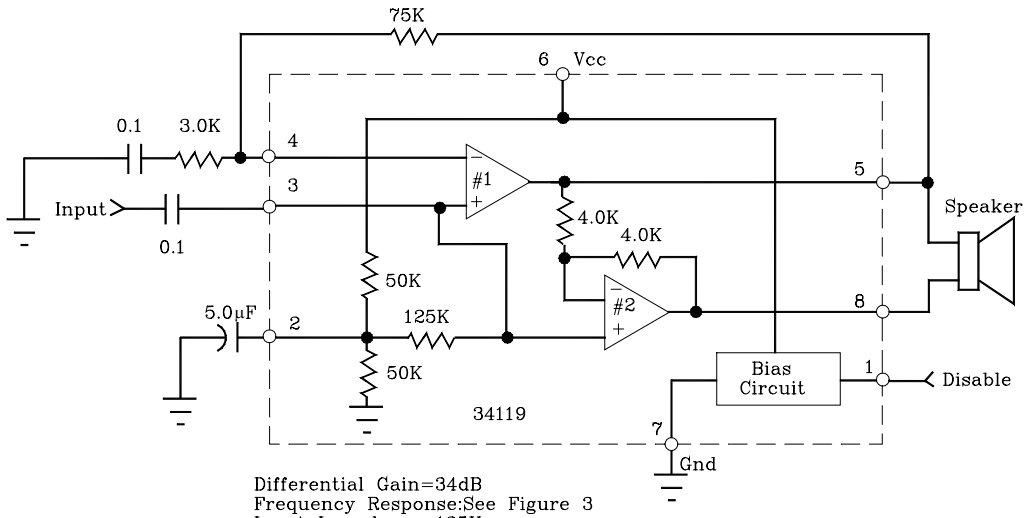


FIGURE 22.AUDIO AM[LIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain=34dB
Frequency Response:See Figure 3
Input Impedance≈125K
PSRR≈50dB

FIGURE 23.AUDIO AMPLIFIER WITH BASE SUPPRESSION

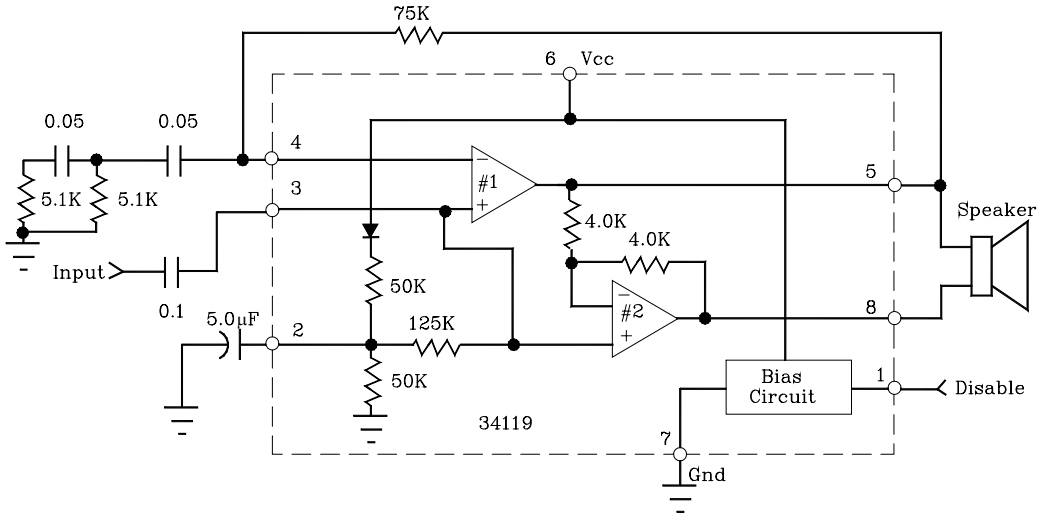
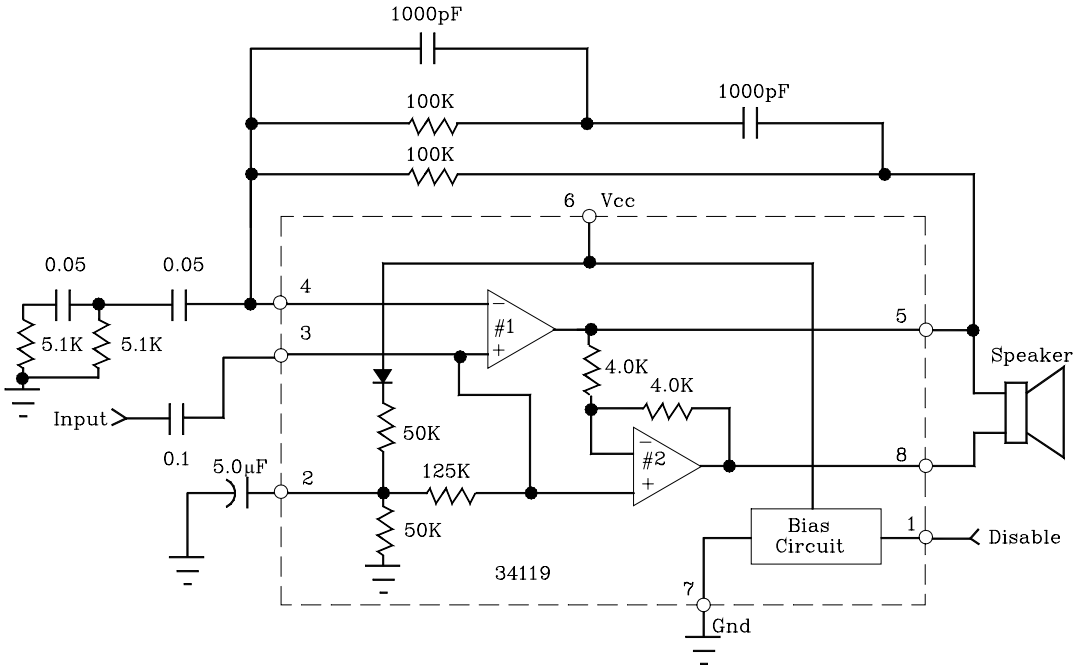
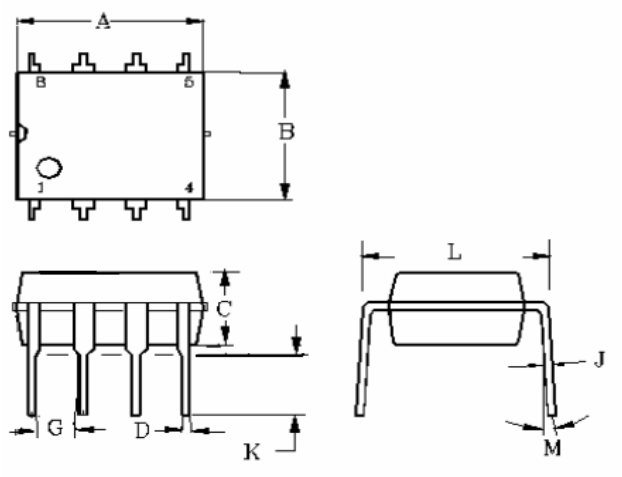


FIGURE 24.AUDIO AMPLIFIER WITH BANDPASS

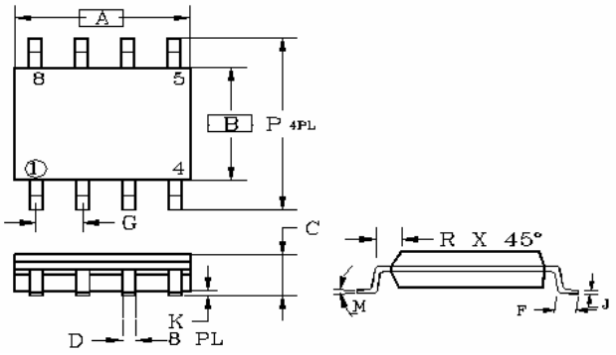


DIP-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.43	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54BSC		0.10BSC	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°

SOP-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019