S3098

DEVICE SPECIFICATION

SONET/SDH/ATM OC-192 1:16 Low Power Receiver w/CDR/Postamp

FEATURES

- Low power operation
- Silicon Germanium BiCMOS technology
- Complies with Telcordia and ITU-T specifications
- Supports G.709 and 10 Gigabit Ethernet rates
- Supports OC-192 to OC-192 with Forward Error Correction (FEC) rates
- Integrated phase lock loop
- Postamp on serial input
- VCO Tunable from 9.953 GHz to 10.709 GHz
- 155.52 MHz REFCLK input (or equivalent FEC rate)
- 16-bit parallel, 622.08 Mbps LVDS data path (or equivalent FEC rate)
- Lock detect indicator
- Low jitter CML differential or single-ended serial interface
- Recovered 622.08 MHz clock output (or equivalent FEC rate)
- Accepts Active High or Active Low signal detect inputs for loss of light (programmable)
- Accepts LVCMOS or LVPECL signal detect inputs
- Synthesizes parallel output clock during loss-of-signal conditions
- Power 1.3 W (typ)
- Compact 15 mm x 15 mm 148-pin CBGA package

APPLICATIONS

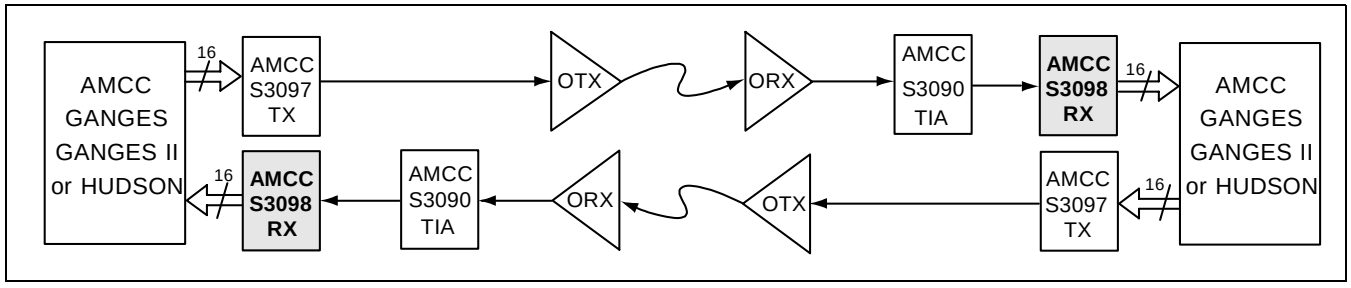
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3098 low power 1:16 receiver with Clock/Data Recovery (CDR) and integrated postamp is a fully integrated OC-192 deserialization/clock and data recovery device. The S3098 receives an OC-192 scrambled NRZ serial signal and recovers the clock. This recovered clock is then used to re-time and demultiplex the data into 16 parallel lines. If a loss-of-signal condition occurs (or LCKREFN is asserted Low), the internal Phase Lock Loop (PLL) will lock to the local 155.52 MHz Reference Clock (REFCLK) (or equivalent FEC rate) to provide a stable clock for down-stream purposes. The S3098 has a limiting postamp on the serial input for small signal gain.

The low jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia and ITU-T standards. Figure 1, *System Block Diagram,* shows a typical network application.

Figure 1. System Block Diagram



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S3098 OVERVIEW

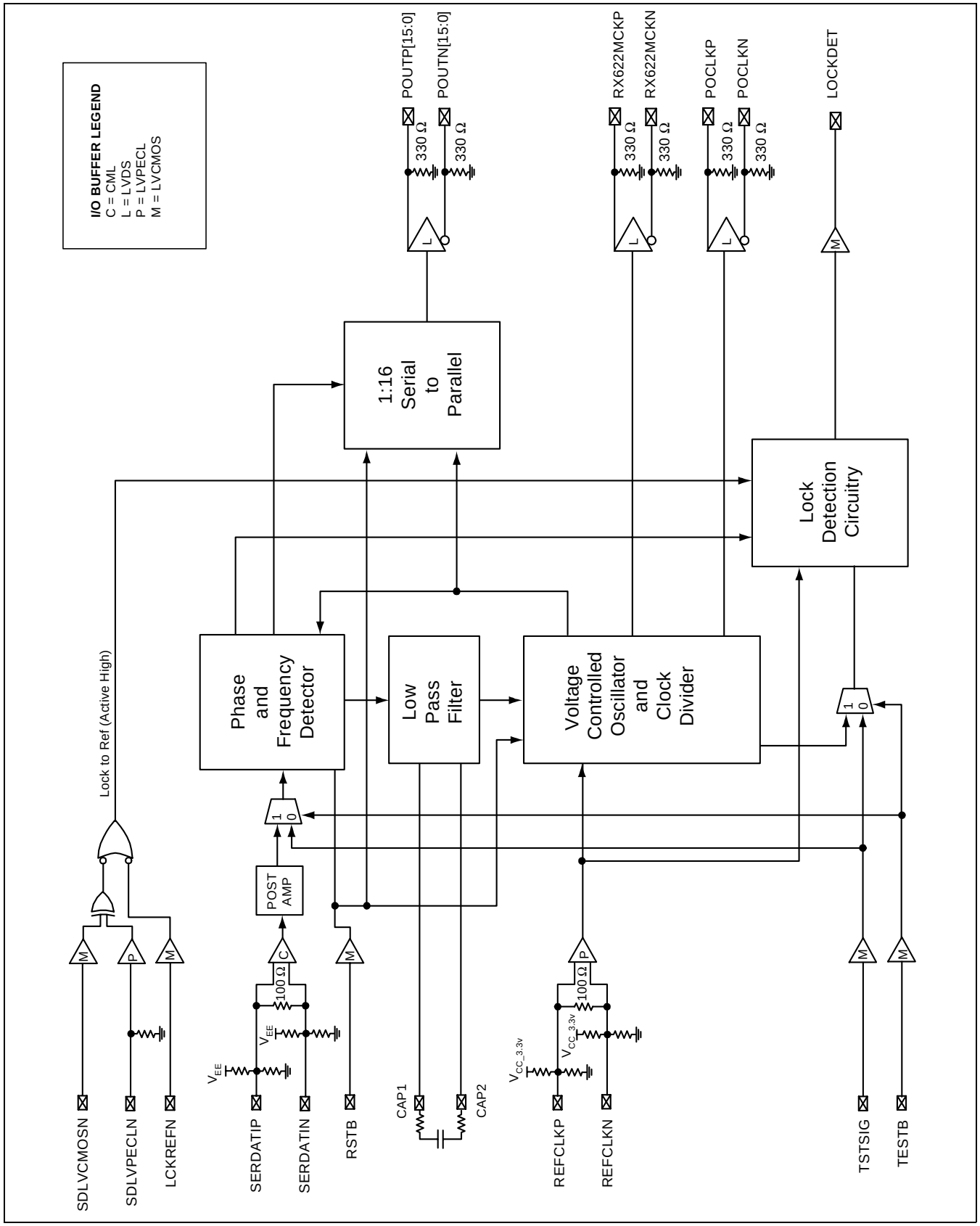
The S3098 Clock and Data Recovery Unit (CDR) with Demultiplexer (DeMUX) implements SONET/SDH deserialization functions. Figure 2, *Functional Block Diagram,* shows the basic operation of the chip. This chip can be used to implement the front end of the SONET equipment, which consists primarily of the parallel transmit interface and the serial receive interface. The chip includes clock and data recovery, serial-to-parallel conversion and system timing. The sequence of receiver operations of the S3098 is as follows:

1. Serial input to limiting postamp
2. Clock and data recovery
3. Serial-to-parallel conversion
4. 16-bit parallel output

Suggested Interface Devices

AMCC	GANGES (S19202)	OC-192 Mapper
AMCC	GANGES II (S19202CBI20)	OC-192 Mapper
AMCC	HUDSON (S19203)	Framer, Digital Wrapper
AMCC	MEKONG (S19204)	OC-192 Pointer Processor
AMCC	S2509	Quad backplane device
AMCC	S3090	10 Gbps TIA
AMCC	S3095	10 Gbps TIA with AGC
AMCC	S3097	OC-192 Transmitter
AMCC	S3196	10 Gbps Limiting Amp

Figure 2. Functional Block Diagram



S3098 PIN DESCRIPTION

Serial Data In (SERDATIP/N)

The Serial Data In (SERDATIP/N) pins are differential Current Mode Logic (CML) inputs. They receive inputs from an optics module or other upstream logic device. The S3098 extracts the clock from the SERDATIP/N inputs and provides a recovered clock (POCLKP/N) with re-timed parallel data. These pins are internally biased and terminated 100 Ω line-to-line.

Reference Clock (REFCLKP/N)

The Reference Clock (REFCLKP/N) pins are an LVPECL 155.52 MHz (or equivalent FEC rate) input used to establish the initial operating frequency of the clock recovery PLL. The REFCLKP/N is also used in the absence of data to maintain PLL lock. This input is internally biased and terminated 100 Ω line-to-line. Most implementations may require AC coupling. See Table 1, *Reference Frequency*, for REFCLK requirements.

Loop Filter (CAP1, CAP2)

The external loop filter capacitor and resistors are connected to the CAP1 and CAP2 pins. These devices should be surrounded by a ground shield. Component values should be as stated in Table 18, *External Loop Filter Components*.

Lock to Reference (LCKREFN)

The LVCMOS Lock to Reference (LCKREFN) signal, when asserted Low, will force the PLL to lock to the local Reference Clock (REFCLK) as well as de-assert LOCKDET.

Signal Detect (SDLVPECLN/SDLVCMOSN)

Two types of signal detect inputs (SDLVPECLN/SDLVCMOSN) are provided, LVPECL and LVCMOS. The LVPECL input should be driven by optical transceivers with an LVPECL signal detect output, and the LVCMOS input should be driven by optical transceivers with an LVCMOS signal detect output. The LVPECL input is internally pulled down. These inputs may be used with optics modules that are either active Low or active High for loss of light.

An optics module with an LVPECL output should be connected to the SDLVPECLN input. Connect SDLVCMOSN as shown in Table 2, *SDLVCMOSN Connections when using the SDLVPECLN Input*.

An optics module with an LVCMOS output should be connected to the SDLVCMOSN input. Connect SDLVPECLN as shown in Table 3, *SDLVPECLN Connections when using the SDLVCMOSN Input*.

Table 1. Reference Frequency

Input Data Rate (SERDATIP/N)	Required Reference Frequency (REFCLK)
9.953 Gbps	155.52 MHz
10.234 Gbps	159.91 MHz
10.317 Gbps	161.20 MHz
10.402 Gbps	162.53 MHz
10.488 Gbps	163.87 MHz
10.575 Gbps	165.23 MHz
10.664 Gbps	166.63 MHz
10.709 Gbps	167.33 MHz

Table 2. SDLVCMOSN Connections when using SDLVPECLN Input

	Optics Device Active Low for loss of light	Optics Device Active High for loss of light
SDLVCMOSN	Connect to GND	Connect to $V_{CC\_2.5V}$

Table 3. SDLVPECLN Connections when using SDLVCMOSN Input

	Optics Device Active Low for loss of light	Optics Device Active High for loss of light
SDLVPECLN	Connect to GND	Connect to $V_{CC\_3.3V}$[1]

1. Connecting to $V_{CC\_3.3\ V}$ is permitted under static conditions.

Reset (RSTB)

The master Reset (RSTB) LVCMOS pin, when asserted Low, asynchronously resets the device. For normal operation, connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor. This should be active for 100 ns to accurately reset the device.

Factory Test (TSTSIG, TESTB)

Two LVCMOS factory test (TSTSIG, TESTB) pins are for test factory purposes only. For normal operation, connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor.

Parallel Output Clock (POCLKP/N)

The Parallel Output Clock (POCLKP/N) LVDS output is an internally regenerated clock which is used to transfer demultiplexed data from an internal holding register to the output register, which drives POUTP/N [15:0]. This clock is synchronized with the parallel output data and must be inverted (cross traces on printed wire board) to be OIF compliant from the module perspective. The parallel outputs are internally terminated with 330 Ω to ground (GND).

Parallel Output Data (POUTP/N[15:0])

The Parallel Output Data (POUTP/N[15:0]) LVDS outputs are re-timed data, output from the Demultiplexer (Demux) at a rate of 622.08 Mbps (or equivalent FEC rate). Bit 15 is the most significant bit and is the first received. The data is re-timed and synchronized to the Parallel Output Clock (POCLKP/N). These outputs are internally terminated with 330 Ω to GND. This bus is typically connected to a framer, mapper or digital wrapper (e.g. GANGES II, GANGES, MEKONG, or HUDSON).

Lock Detect (LOCKDET)

When the LVCMOS output Lock Detect (LOCKDET) signal is inactive (Low), it indicates that the incoming data stream has failed the frequency test, as dictated by the PLL, or LCKREFN has been asserted Low, or SDLVCMOSN/SDLVPECL has been asserted. This test is used to determine whether or not serial input activity is valid data. When LOCKDET is active, the PLL is locked to the data stream.

Recovered 622.08 MHz Clock (RX622MCKP/N)

The LVDS 622.08 MHz Clock (or equivalent FEC rate) (RX622MCKP/N) is the clock which is recovered from the input data stream. During loss-of-signal conditions or when LCKREFN has been asserted, this output clock is derived from the Reference Clock Input (REFCLKP/N). This is internally terminated with 330 Ω to ground (GND).

S3098 FUNCTIONAL DESCRIPTION

Receiver Description

The S3098 receiver chip provides the first stage of the digital processing of a receive SONET OC-192 bit-serial stream. It converts the bit-serial 9.953 Gbps data stream into a 622.08 Mbps (or equivalent FEC rate) 16-bit parallel data format.

Postamp

The S3098 limiting postamp takes the differential serial data from the SERDATIP/N pins and provides 36 dB of small signal gain. The input to the postamp can be either AC or DC coupled.

Clock Recovery

The clock recovery circuitry generates a clock that is the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a Phase Lock Loop (PLL) so that it samples the data in the center of the data eye pattern.

The Clock and Data Recovery (CDR) extracts a synchronous signal from the serial data input using a PLL. The PLL consists of a Voltage Controlled Oscillator (VCO), Phase/Frequency Detectors (PFD), and a loop filter.

The frequency detector ensures predictable lock-up conditions. It is used during acquisition and serves as a means to pull the VCO into the range of the data rate at which the phase detector is capable of acquiring lock.

The phase detector used in the CDR is designed to give minimum static phase error of the PLL. When a transition has occurred, the value of the sample in the vicinity of the transition tells whether the VCO clock leads or lags the incoming data, and the phase detector produces a binary output accordingly.

When a loss-of-signal condition exists, Signal Detect (SDLVCMOSN or SDLVPECLN) will be de-asserted, and the PLL locks onto the Reference Clock (REFCLK) to provide a steady output clock. There are two pins (CAP1 and CAP2) to connect the external capacitor and resistors in order to adjust the PLL loop performance.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance proposed for SONET equipment by the Telcordia TA-NWT-000253 standard.

Lock Detect

The S3098 contains a lock detect circuit, which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than the typical value stated in Table 8, *Performance Specifications*, the PLL will be declared out of lock. The phase detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the typical value stated in Table 8, *Performance Specifications*, the PLL will be declared in lock, and the lock detect output will go active. A de-asserted signal detect (SDLVCMOSN or SDLVPECLN) will also cause an out-of-lock condition.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 16-bit registers. The first is a serial-in, parallel-out shift register, which performs the serial-to-parallel conversion. The second is a 16-bit internal holding register, which transfers data from the serial-to-parallel register on byte boundaries. On the falling edge of the Parallel Output Clock (POCLK), the data in the holding register is transferred to an output holding register, which drives Parallel Output Data (POUTP/N[15:0]).

Power Sequencing

In order to avoid latch up, the following power-up sequence is required. Apply GND first, next -5.2 V, then the positive supplies, +2.5 V and +3.3 V. These two positive supplies can be brought up simultaneously or in any order.

Table 4. Input Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff. CML	I	G1 J1	**Serial Data Input.** Differential high frequency serial data input to limiting postamp for small signal gain. Internally biased and terminated 100 Ω line-to-line.
REFCLKP REFCLKN	Diff. LVPECL	I	B1 C1	**Reference Clock.** Differential reference clock input at 155.52 MHz (or equivalent FEC rate). The PLL will lock onto this reference in the absence of serial input data. Internally biased and terminated 100 Ω line-to-line.
CAP1 CAP2	Analog	I	B4 C4	**Loop Filter.** The external loop filter capacitor and resistors are connected to these pins. Used to adjust the loop filter performance. See Figure 12, *External Loop Filter* and Table 18, *External Loop Filter Components.*
LCKREFN	LVCMOS	I	C14	**Lock to Reference.** Active Low. When active, the PLL will be forced to lock to the local reference clock input (REFCLK). If unused, connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor for normal operation.
RSTB	LVCMOS	I	A7	**Master Reset.** Active Low. Reset input for the device. For correct reset, this input must be asserted Low for 100 ns. Connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor if not used.
TESTB	LVCMOS	I	C6	**Test Enable.** Active Low. Used during production test to bypass the VCO in the PLL. Connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor for normal operation.
TSTSIG	LVCMOS	I	A6	**Test Input.** Active Low. Signal used for production test. Connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor for normal operation.
SDLVPECLN	Single-Ended LVPECL	I	A9	**Signal Detect.** A Single-Ended 10 K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. This input may be utilized by an optics module that is active Low or active High for loss of light. For an active High device, SDLVCMOSN must be connected to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor. For an active Low optics module, the SDLVCMOSN input must be connected to GND. The optics module LVPECL signal detect output may be directly connected to the SDLVPECLN input. This input is internally pulled Low. When a loss of light condition occurs, the internal PLL will be forced to lock to the REFCLK input signal.
SDLVCMOSN	LVCMOS	I	B13	**Signal Detect.** A LVCMOS input to be driven by the external optical receiver module to indicate a loss of received optical power. This input may be utilized by an optics module that is active Low or active High for loss of light. For an active Low device, SDLVPECLN must be connected to GND. For an active High optics module, the SDLVPECLN input must be connected to $V_{CC\_3.3\ V.}$ through a 10 kΩ resistor. The optics module LVCMOS signal detect output may be directly connected to the SDLVCMOSN input. When a loss of light condition occurs, the internal PLL will be forced to lock to the REFCLK input signal.

Table 5. Output Pin Descriptions and Assignment

Pin Name	Level	I/O	Pin #	Description
POCLKP POCLKN	LVDS	O	B10 B9	**Parallel Output Clock.** Regenerated 622.08 MHz (or equivalent FEC rate) differential output clock, synchronized to the parallel output data. (See Figure 5, *Parallel Data Output Delay from POCLK*). Internally terminated with 330 Ω to GND.
POUT0P POUT0N POUT1P POUT1N POUT2P POUT2N POUT3P POUT3N POUT4P POUT4N POUT5P POUT5N POUT6P POUT6N POUT7P POUT7N POUT8P POUT8N POUT9P POUT9N POUT10P POUT10N POUT11P POUT11N POUT12P POUT12N POUT13P POUT13N POUT14P POUT14N POUT15P POUT15N	LVDS	O	N2 N3 P3 P4 N4 N5 P5 P6 N6 N7 P7 P8 N8 N9 P9 P10 M11 M12 N12 N13 N14 M14 L13 K13 K14 J14 H14 G14 G13 F13 F14 E14	**Parallel Output Data.** Re-timed data from the Demultiplexer (DeMUX) at a rate of 622.08 Mbps (or equivalent FEC rate). POUTP/N15 is the most significant bit (corresponding to bit 1 of each word, the first bit received.) POUTP/N0 is the least significant bit corresponding to bit 16 of each word, the last bit received). Internally terminated with 330 Ω to GND.
LOCKDET	LVCMOS	O	A12	**Lock Detect.** Active High. Clock recovery indicator. Active when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.
RX622MCKP RX622MCKN	LVDS	O	B11 A11	**622.08 MHz Clock** (or equivalent FEC rate) derived from VCO clock. Internally terminated with 330 Ω to GND.

Table 6. Common Pin Descriptions and Assignment

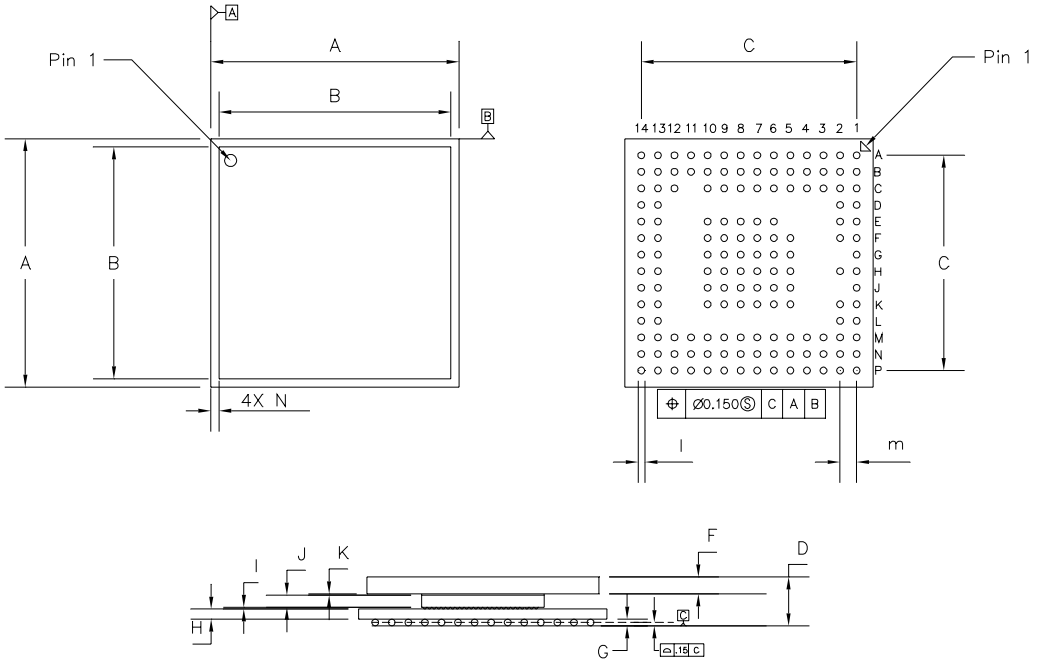
Pin Name	Level	I/O	Pin #	Description
COREVCC	+2.5 V	PWR	B8, C13, M2, M8, M9	Digital $V_{CC\_2.5\ V}$ + 2.5 V ± 5%
LVDSVCC	+2.5 V	PWR	C9, H13, M3, M6, M13	LVDS $V_{CC\_2.5\ V}$ + 2.5 V ± 5%
LVCMOSVCC	+2.5 V	PWR	C7	LVCMOS $V_{CC\_2.5\ V}$ + 2.5 V ± 5%
CMLVEE	-5.2 V	PWR	D1, E2, L2	CML V_{EE} -5.2 V ± 5%
SUBVEE	-5.2 V	PWR	B12, D13, J13, N11	Substrate V_{EE} -5.2 V ± 5%
ANALOG AVCC	+3.3 V	PWR	A3, A5	Analog $V_{CC\_3.3\ V}$ + 3.3 V ± 5%
DIGITALVCC	+3.3 V	PWR	C8	Digital $V_{CC\_3.3\ V}$ + 3.3 V ± 5%
GND	0 V	GND	A1, A2, A4, A8, A10, A13, A14, B2, B3, B5, B6, B7, B14, C2, C3, C5, C10, C12, D2, D14, E1, E13, F1, F2, H1, H2, K1, K2, L1, L14, M1, M4, M5, M7, M10, N1, N10, P1, P2, P11, P12, P13, P14	Analog/Digital Ground
THERMAL GND	0 V	GND	E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	Thermal Ground

Note: All digital, analog, and thermal grounds are connected together on the package.

Figure 3. S3098 Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	ANALOG GND	ANALOG GND	ANALOG AVCC +3.3V (FILTER)	ANALOG GND	ANALOG AVCC +3.3V (VCO)	TSTSIG	RSTB	DIGITAL GND	SDLV PECLN	DIGITAL GND	RX622 MCKN	LOCKDET	DIGITAL GND	DIGITAL GND
B	REFCLKP	ANALOG GND	ANALOG GND	CAP1	ANALOG GND	ANALOG GND	DIGITAL GND	CORE VCC +2.5V	POCLKN	POCLKP	RX622 MCKP	SUB VEE -5.2V	SDLV CMOSN	DIGITAL GND
C	REFCLKN	ANALOG GND	ANALOG GND	CAP2	ANALOG GND	TESTB	LVCMOS VCC +2.5V	DIGITAL VCC +3.3V (PD)	LVDS VCC +2.5V	DIGITAL GND		DIGITAL GND	CORE VCC +2.5V	LCKREFN
D	CML VEE -5.2V	ANALOG GND											SUB VEE -5.2V	DIGITAL GND
E	ANALOG GND	CML VEE -5.2V				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			DIGITAL GND	POUT15N
F	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT14N	POUT15P
G	SERDATIP				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT14P	POUT13N
H	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			LVDS VCC +2.5V	POUT13P
J	SERDATIN				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			SUB VEE -5.2V	POUT12N
K	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			POUT11N	POUT12P
L	ANALOG GND	CML VEE -5.2V				**PACKAGE TOP VIEW**							POUT11P	DIGITAL GND
M	ANALOG GND	CORE VCC +2.5V	LVDS VCC +2.5V	DIGITAL GND	DIGITAL GND	LVDS VCC +2.5V	DIGITAL GND	CORE VCC +2.5V	CORE VCC +2.5V	DIGITAL GND	POUT8P	POUT8N	LVDS VCC +2.5V	POUT10N
N	DIGITAL GND	POUT0P	POUT0N	POUT2P	POUT2N	POUT4P	POUT4N	POUT6P	POUT6N	DIGITAL GND	SUB VEE -5.2V	POUT9P	POUT9N	POUT10P
P	DIGITAL GND	DIGITAL GND	POUT1P	POUT1N	POUT3P	POUT3N	POUT5P	POUT5N	POUT7P	POUT7N	DIGITAL GND	DIGITAL GND	DIGITAL GND	DIGITAL GND

Figure 4. Compact 15 mm x 15 mm 148-pin CBGA Package



DIMENSIONS (millimeters)

UNIT	A	B	C	D	F	G	H	I	J	K	l	m	N
MIN	14.80	14.40	12.90	2.58	0.965	0.425 REF.	0.51	0.100 REF.	.730	0.025	0.33	1.00 REF.	0.05
NOM	15.00	14.50	13.00	2.97	1.016		0.61		.736	0.053	0.40		0.25
MAX	15.20	14.60	13.10	3.10	1.067		0.71		.743	0.080	0.47		0.45

Table 7. Package Thermals

Max Package Power (85°C Ambient) (Assuming 125°C Junction Temp)	**Θja**	**Θjc**
1.95 W	20.5°C/Watt	3.0°C/Watt

Table 8. Performance Specifications

Parameter	Min.	Typ	Max	Units	Conditions
Nominal VCO Center Frequency	9.953		10.709	GHz	
155.52 MHz (or equivalent FEC rate) Reference Clock Frequency Tolerance	-100		100	ppm	± 20 ppm is required to meet SONET output frequency specification.
155.52 MHz (or equivalent FEC rate) Reference Clock Input Duty Cycle	40		60	% of UI	
155.52 MHz (or equivalent FEC rate) Reference Clock Rise and Fall Times	0.080		0.8	ns	20% to 80% of amplitude.
SERDATIP/N Input Return Loss (S_{11}) (when driven differentially)			-10	dB	DC - 10 GHz
SERDATIP Input Return Loss (S_{11}) (when driven single-ended using the termination scheme in Figure 13)			-5	dB	DC - 10 GHz
Acquisition Lock Time (RSTB deassertion to LOCKDET assertion)		4.5		ms	Minimum transition density of 50%. Guaranteed, but not tested. With device already powered up and valid REFCLK.
Frequency difference at which the PLL goes out-of-lock (REFCLK compared to the divided down VCO clock).	±440	±600	±732	ppm	
Frequency difference at which receive PLL goes into lock (REFCLK compared to the divided down VCO clock).	±220	±300	±366	ppm	
J_{tol} Jitter Tolerance (SERDATIP/N)			15	$UI_{(p-p)}$	10 Hz-2.4 kHz (Sinusoidal)
			15/(f ÷ 2400)	$UI_{(p-p)}$	2.4 kHz-24 kHz (Sinusoidal)
			1.5	$UI_{(p-p)}$	24 kHz-400 kHz (Sinusoidal)
			$1.5/(f \div 400 \times 10^3)$	$UI_{(p-p)}$	400 kHz-4 MHz (Sinusoidal)
			0.15	$UI_{(p-p)}$	4 MHz-1 GHz (Sinusoidal)
L_{cid} Consecutive identical digits at Serial Data Input			80	bits	Number of bits with no transitions. (SONET spec is 75 bits max.)

Table 9. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S3098 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated or any other conditions beyond those indicated in the “Recommended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min.	Typ	Max	Units
Storage Temperature	-55		150	°C
$V_{CC\_2.5\ V}$ 2.5 V Supply	-0.5		2.7	V
$V_{CC\_3.3\ V}$ 3.3 V Supply	-0.5		3.6	V
V_{EE} -5.2 V Supply	-7.0		-0.5	V
LVCMOS Input Voltage	-0.5		$V_{CC\_2.5\ V}$ + 0.5	V
LVPECL Input Voltage	-0.5		$V_{CC\_3.3\ V}$ + 0.5	V
CML Input Voltage	V_{EE} -0.25		GND	V
LVDS Output Current Per Pin			5	mA
LVCMOS Output Current per pin (source/sink)			30/1000	uA
LVCMOS Input Current per pin (source/sink)			200/65	uA
LVDS Input Current Per Pin			7	mA
LVPECL Input Current Per Pin			13	mA
CML Input Current Per Pin			13	mA

Electrostatic Discharge (ESD) Ratings

The S3098 is rated to the following ESD voltages based on the human body model per JESD22-A114-B specification:

1. All pins are rated at 100 V.

Table 10. Recommended Operating Conditions

Parameter	Min.	Typ	Max	Units	Conditions
Ambient Temperature Under Bias	0		85	°C	Over process, voltage and temperature range.
Junction Temperature Under Bias	25		125	°C	Over process, voltage and temperature range.
Voltage on $V_{CC\_2.5\ V}$ with Respect to GND	2.375	2.5	2.625	V	Over process, voltage and temperature range.
Voltage on $V_{CC\_3.3\ V}$ with Respect to GND	3.135	3.3	3.465	V	Over process, voltage and temperature range.
Voltage on V_{EE} with Respect to GND	-4.94	-5.2	-5.46	V	Over process, voltage and temperature range.
$I_{CC\_2.5\ V}$ Supply Current			427	mA	Outputs terminated.
I_{EE_CML} Supply Current			44	mA	Outputs terminated.
$I_{CC\_3.3\ V\_AVCC/VCC}$ Supply Current			105	mA	Outputs terminated. 60% is AVCC 40% is VCC
Power Dissipation			1.72	W	Outputs terminated.
Power Supply Noise Rejection		35		mVpp	6 kHz to 2 MHz bandwidth

Table 11. Internally Biased Differential CML Input DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	GND -1.195		GND	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	GND -1.55		GND -0.305	V	Over process, voltage and temperature range.
V_{IDIFF}	Differential Input Voltage Swing	25		1400	mV	See Figure 6, *Differential Voltage Measurement*.
$V_{ISINGLE}$	Single-ended Input Voltage Swing (while driven differentially)	12.5		700	mV	See Figure 6, *Differential Voltage Measurement*.
$V_{ISINGLE}$	Single-ended Input Voltage Swing (while driven single-ended)	50*		700	mV	See Figure 7, *Single-ended Data Input Voltage Measurement*.
V_{ICM}	Input Common Mode Voltage	GND -1.2	GND -0.65	GND -0.3	V	Over process, voltage and temperature range.
R_{IDIFF}	Differential Input Resistance	70		100	Ω	Over process, voltage and temperature range. DC measurement.

* - Consult Single-Ended Termination Recommendation Application Note for improvement of input sensitivity.

Table 12. LVDS Output Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	1.25		1.8	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
V_{OL}	Output Low Voltage	0.85		1.45	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
V_{ODIFF}	Output Differential Voltage	500	740	1100	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range. See Figure 6, *Differential Voltage Measurement*
$V_{OSINGLE}$	Output Single-ended Voltage	250	370	550	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range. See Figure 6, *Differential Voltage Measurement*.
R_{ODIFF}	Differential Output Impedance			140	Ω	Over process, voltage and temperature range. Guaranteed by design.

Table 13. Internally Biased Differential LVPECL Input DC Characteristics (REFCLKP/N)

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	$V_{CC\_3.3\ V}$ -1.20		$V_{CC\_3.3\ V}$ -0.50	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	$V_{CC\_3.3\ V}$ -2.00		$V_{CC\_3.3\ V}$ -1.40	V	Over process, voltage and temperature range.
V_{IDIFF}	Differential Input Voltage Swing	300		1200	mV	Over process, voltage and temperature range. See Figure 6, *Differential Voltage Measurement*
$V_{ISINGLE}$	Single-ended Input Voltage Swing	150		600	mV	Over process, voltage and temperature range. See Figure 6, *Differential Voltage Measurement*
V_{ICM}	Input Common Mode Voltage	$V_{CC\_3.3\ V}$ -1.60		$V_{CC\_3.3\ V}$ -0.95	V	Over process, voltage and temperature range.
R_{IDIFF}	Differential Input Impedance	80	100	120	Ω	Over process, voltage and temperature range.

Table 14. Single-Ended LVPECL Input DC Characteristics (SDLVPECLN)

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	$V_{CC\_3.3\ V}$ -1.20		$V_{CC\_3.3\ V}$ -0.50	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	$V_{CC\_3.3\ V}$ -2.00		$V_{CC\_3.3\ V}$ -1.40	V	Over process, voltage and temperature range.
I_{IH}	Input High Current	50		300	µA	Over process, voltage and temperature range. $V_{IH} = V_{CC\_3.3\ V}$ - 0.5 V
I_{IL}	Input Low Current	-100		1.5	µA	Over process, voltage and temperature range. $V_{IL} = V_{CC\_3.3\ V}$ - 2 V

Table 15. LVCMOS Input DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	1.7		$V_{CC\_2.5\ V}$	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	0		0.7	V	Over process, voltage and temperature range.
I_{IH}	Input High Current			65	µA	V_{IH} min
I_{IL}	Input Low Current			200	µA	V_{IL} min

Table 16. LVCMOS Output DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.0		$V_{CC\_2.5\ V}$	V	Over process, voltage and temperature range. I_{OH} = 30 uA
V_{OL}	Output Low Voltage	0		0.4	V	Over process, voltage and temperature range. I_{OL} = 1 mA

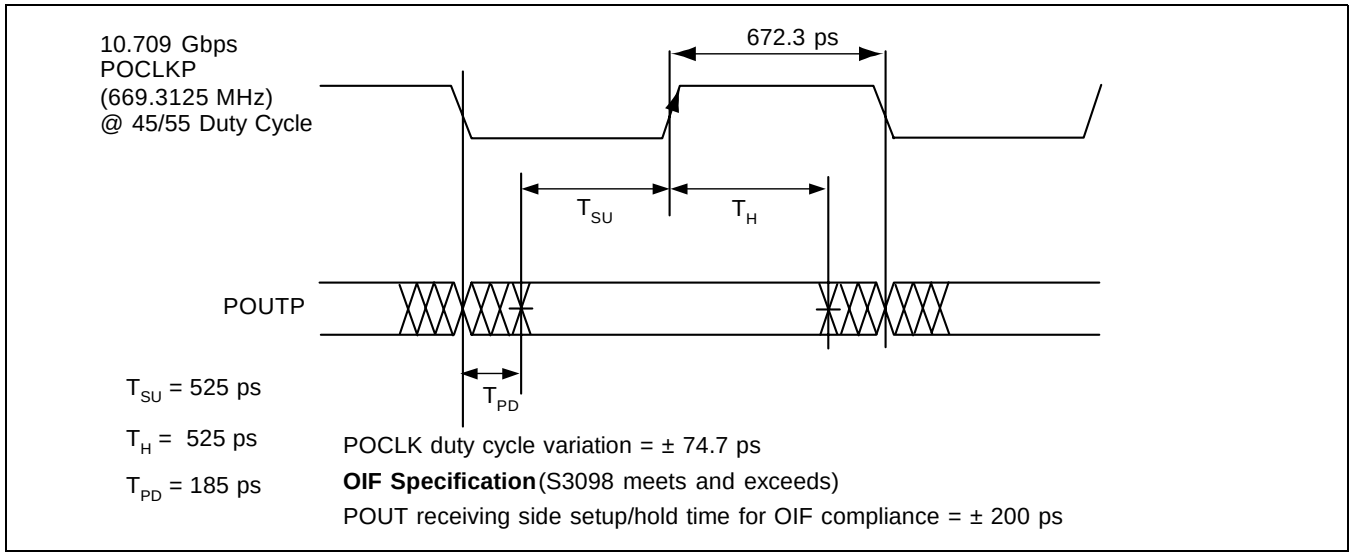
Table 17. AC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
C_{DUTY}	POCLKP/N / RX622MCKP/N Duty Cycle	45		55	%	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
T_{pd}	POUTP/N Delay from POCLKP/N			185	ps	Over process, voltage and temperature range. See Figure 5, *Parallel Data Output Delay from POCLK*
t_{SU}	POCLKP/N to POUTP/N	525			ps	Over process, voltage and temperature range. See Figure 5, *Parallel Data Output Delay from POCLK*
t_H	POCLKP/N to POUTP/N	525			ps	Over process, voltage and temperature range. See Figure 5, *Parallel Data Output Delay from POCLK*
$t_{r/f}$	LVPECL Input rise and fall time	80		800	ps	Over process, voltage and temperature range. 20% to 80%.
	LVDS Output rise and fall time	80		250	ps	Over process, voltage and temperature range. 20% to 80%.
	LVCMOS Output rise and fall time 5 pF load 15 pF load			 50 100	ns	Over process, voltage and temperature range. 20% to 80%. Guaranteed by design.
t_{PW}	RSTB Minimum Pulse Width	100			ns	Guaranteed by design.

Table 18. External Loop Filter Components (See Figure 12, External Loop Filter)

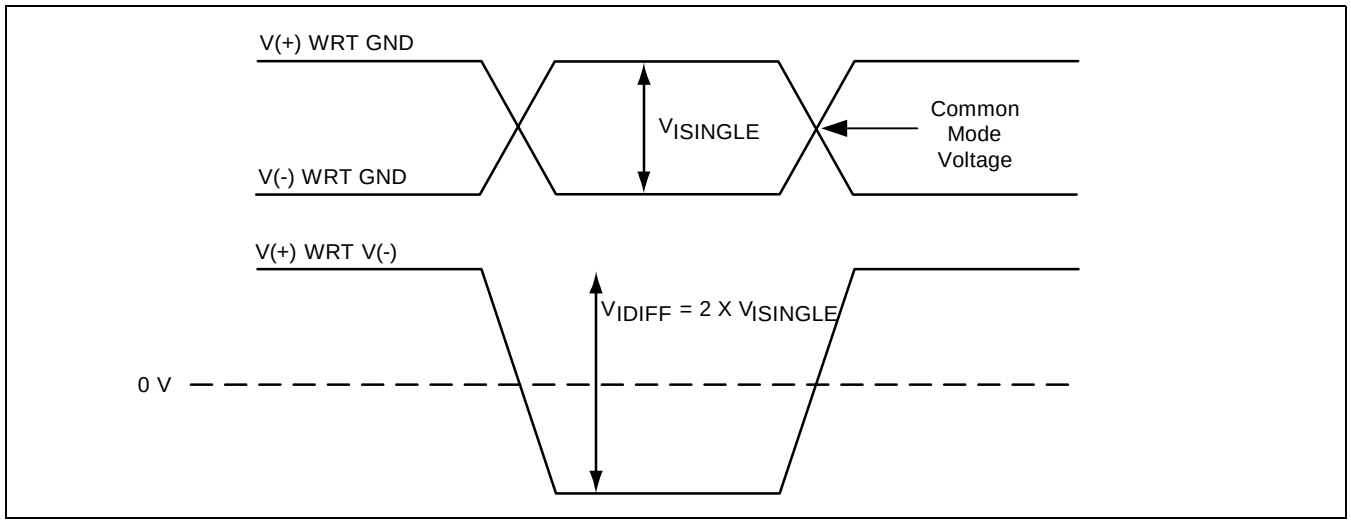
Symbol	Description	Value	Unit
R_1, R_2	Resistor, Surface Mount, 0402	15	Ω
C_1	Capacitor, Surface Mount, Non-polarized, 0603 or larger	1	µF

Figure 5. Parallel Data Output Delay from POCLK[1,2]



1. When a setup time is specified on LVDS signals between an input and a clock, the setup time in picoseconds, is from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time in picoseconds, is from the 50% point of the clock to the 50% point of the input.

Figure 6. Differential Voltage Measurement



Note: WRT = with respect to.

Figure 7. Single-Ended Data Input Voltage Measurement

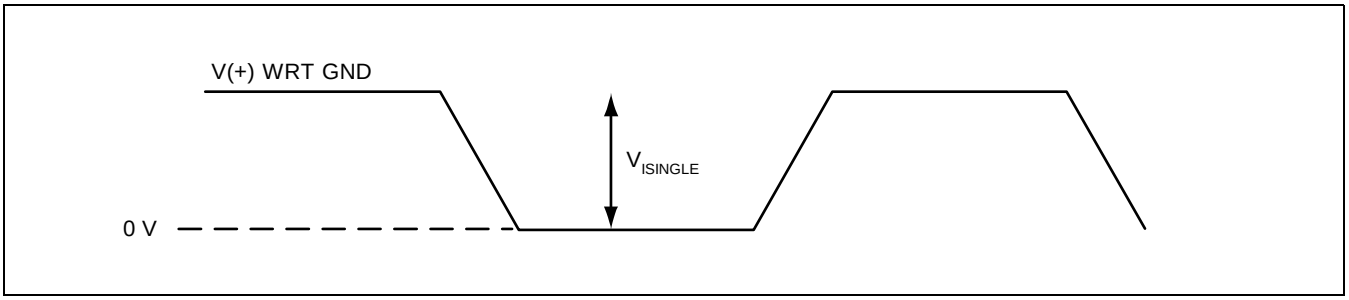


Figure 8. S3098 LVDS Output to LVDS Input

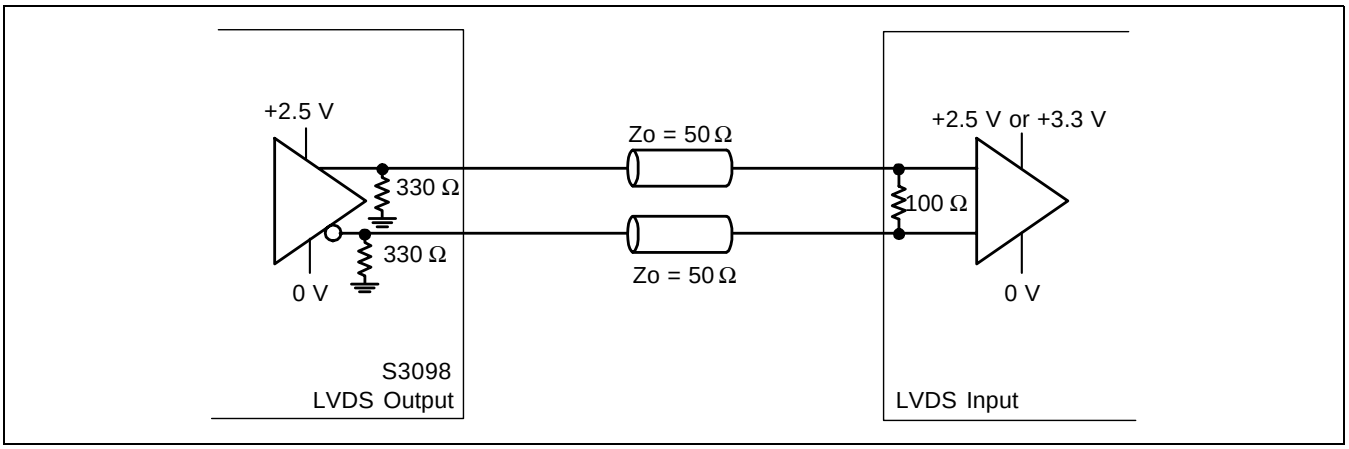


Figure 9. -5.2 V ECL Post Amp to S3098 Input DC Coupled Termination

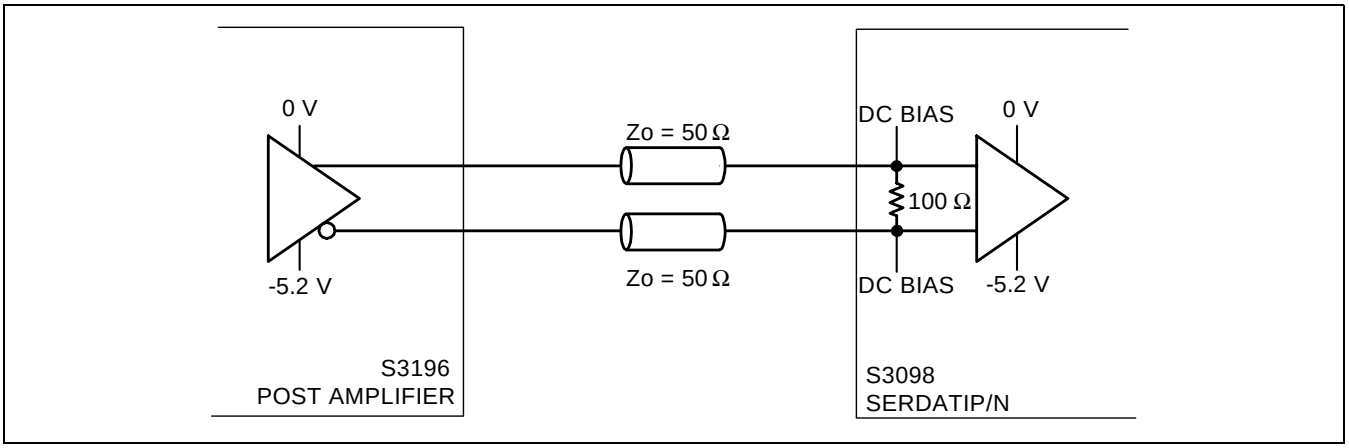


Figure 10. -5.2 V ECL TIA to S3098 DC Coupled Termination

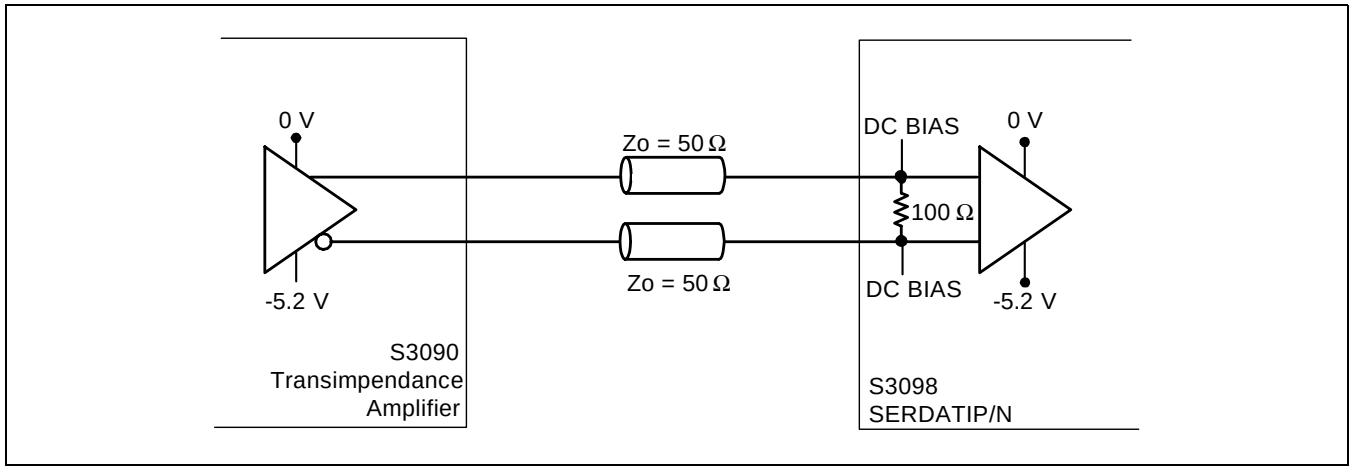


Figure 11. +3.3 V Differential LVPECL Driver to S3098 LVPECL Reference Clock Input, AC Coupled Termination

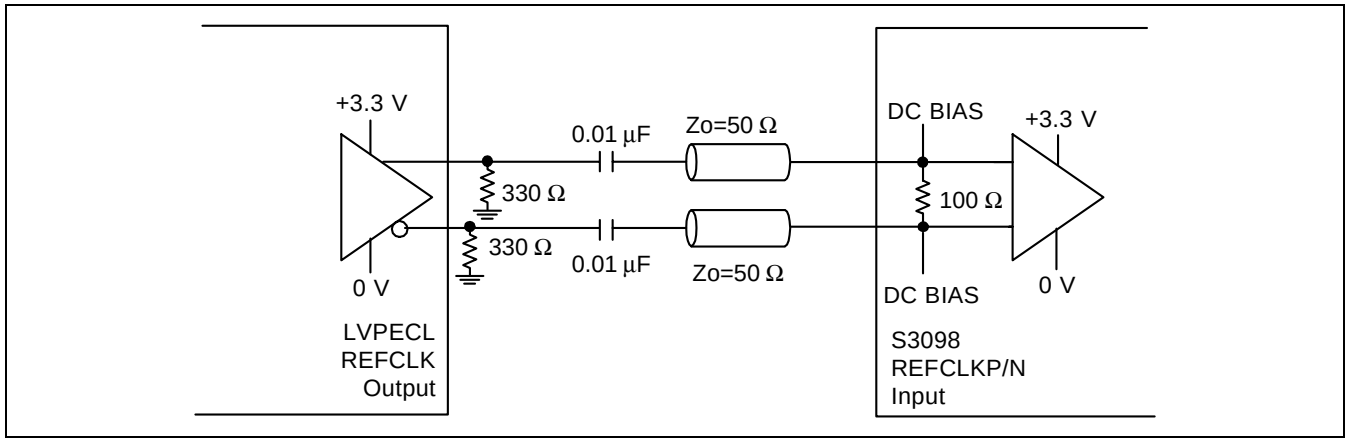


Figure 12. External Loop Filter (See Table 18, External Loop Filter Components)

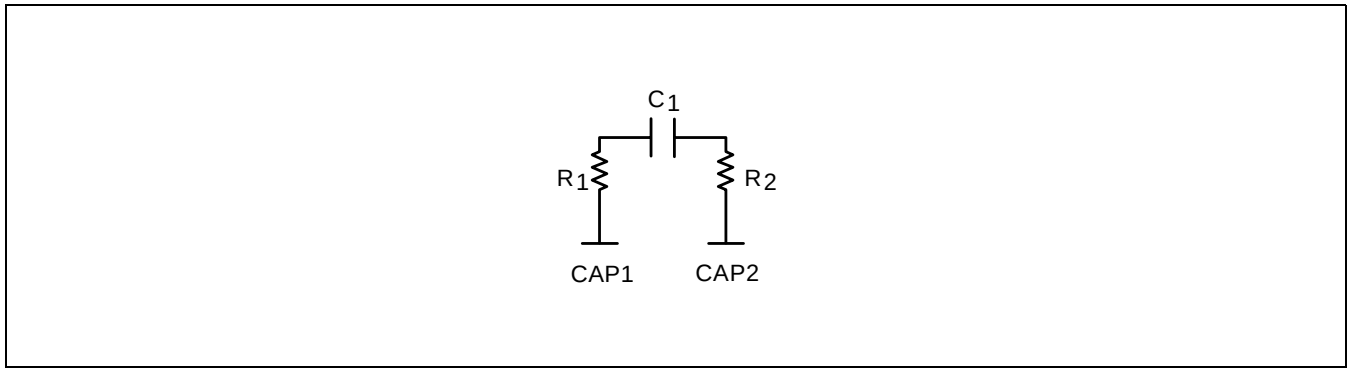
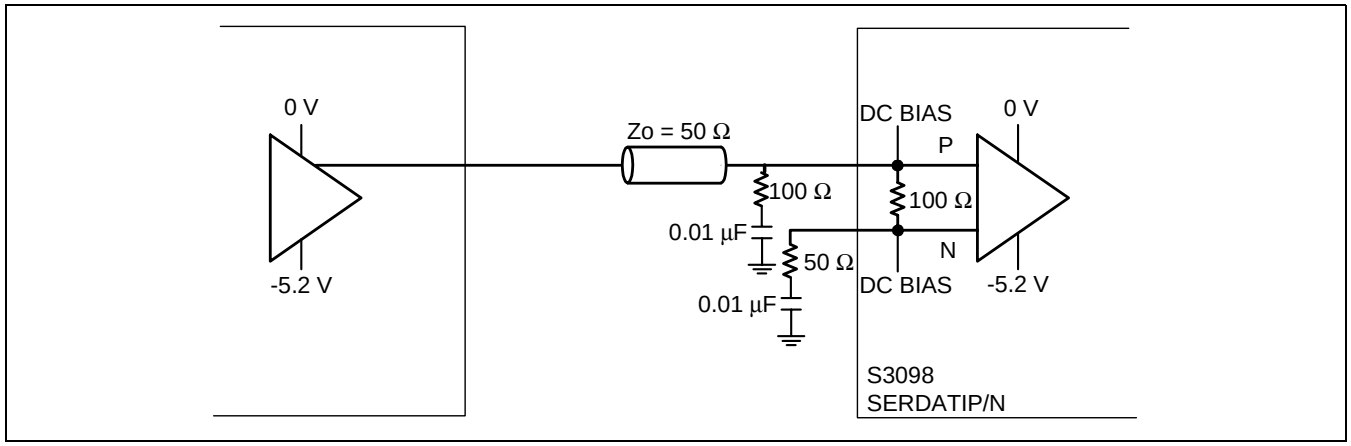


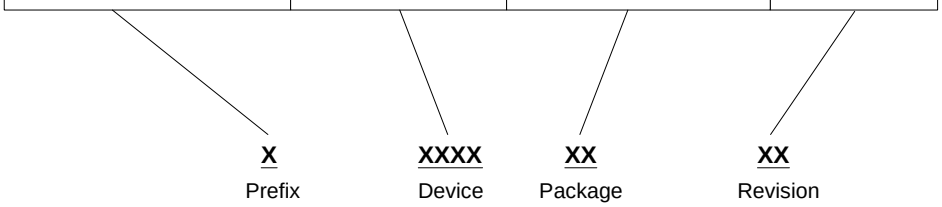
Figure 13. Single-Ended Termination Scheme (Termination Scheme that was characterized)[1]



1. See *S3098 Single-Ended Termination Recommendation* Application Note for more details and improvement of input sensitivity.

Ordering Information

Prefix	Device	Package	Revision
S – Integated Circuit	3098	CB – 148 CBGA	12



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