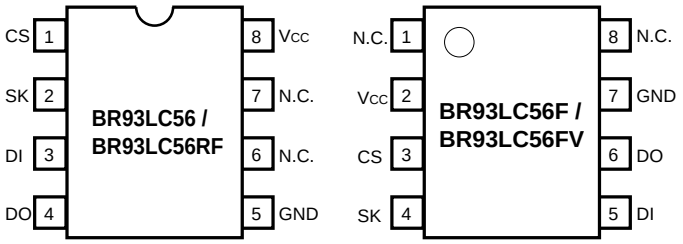
2,048-Bit Serial Electrically Erasable PROM

BR93LC56 / BR93LC56F / BR93LC56RF / BR93LC56FV

●Features

- Low power CMOS technology
- 128 × 16 bit configuration
- 2.7V to 5.5V operation
- Low power dissipation
  - 3mA (max.) active current: 5V
  - 5µA (max.) standby current: 5V
- Auto increment for efficient data bump
- Automatic erase-before-write
- Hardware and software write protection
  - Default to write-disabled state at power up
  - Software instructions for write-enable / disable
  - Vcc lock out inadvertent write protection
- 8-pin SOP / 8-pin SSOP-B / 8-pin DIP packages
- Device status signal during write cycle
- TTL compatible Input / Output
- 100,000 ERASE / write cycles
- 10 years Data Retention

●Pin assignments



●Pin descriptions

Pin name	Function
CS	Chip select input
SK	Serial clock input
DI	Start bit, operating code, address, and serial data input
DO	Serial data output, READY / $\overline{\text{BUSY}}$ internal status display output
GND	Ground
N.C.	Not connected
N.C.	Not connected
V_{CC}	Power supply

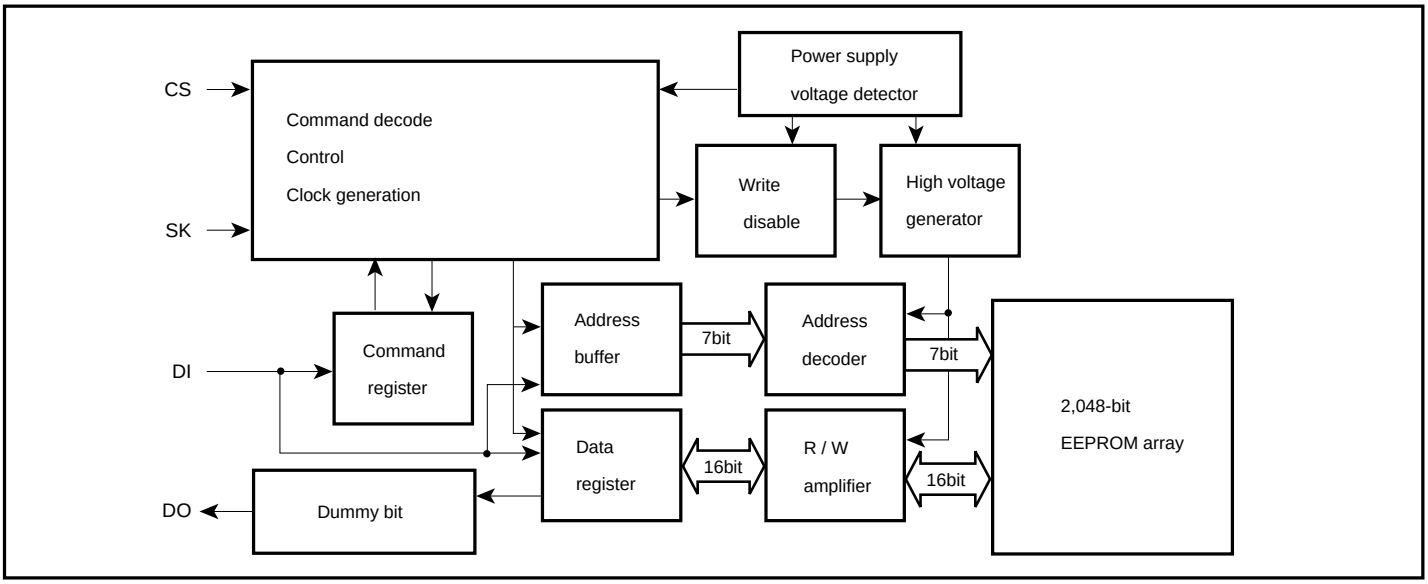
●Overview

The BR93LC56 is CMOS serial input / output-type memory circuits (EEPROMs) that can be programmed electrically. Each is configured of 128 words × 16 bits (2,048 bits), and each word can be accessed individually and data read from it and written to it.

Operation control is performed using five types of commands. The commands, addresses, and data are input through the DI pin under the control of the CS and SK pins. In a write operation, the internal status signal (READY or $\overline{\text{BUSY}}$) can be output from the DO pin.

The only difference between the BR93LC56 / F / RF / FV is the write disable voltage and its accompanying write enable voltage. All other functions and characteristics are the same.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Applied voltage		V_{CC}	– 0.3 ~ + 6.5	V
Power dissipation	BR93LC56	Pd	500*1	mW
	BR93LC56F / RF		350*2	
	BR93LC56FV		300*3	
Storage temperature		Tstg	– 65 ~ + 125	°C
Operating temperature		Topr	– 40 ~ + 85	°C
Terminal voltage		—	– 0.3 ~ V_{CC} + 0.3	V

∗1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.
∗2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.
∗3 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Writing	V_{CC}	2.7	—	5.5	V
	Reading		2.0	—	5.5	V
Input voltage		V_{IN}	0	—	V_{CC}	V

●Electrical characteristics (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage	V_{IL}	– 0.3	—	0.8	V	—
Input high level voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	—
Output low level voltage 1	V_{OL1}	—	—	0.4	V	I_{OL} = 2.1mA
Output high level voltage 1	V_{OH1}	2.4	—	—	V	I_{OH} = – 0.4mA
Output low level voltage 2	V_{OL2}	—	—	0.2	V	I_{OL} = 10µA
Output high level voltage 2	V_{OH2}	V_{CC} – 0.4	—	—	V	I_{OH} = – 10µA
Input leakage current	I_{LI}	– 1.0	—	1.0	µA	V_{IN} = 0V ~ V_{CC}
Output leakage current	I_{LO}	– 1.0	—	1.0	µA	V_{OUT} = 0V ~ V_{CC}, CS = GND
Operating current dissipation 1	I_{CC1}	—	1.5	3	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN f = 1MHz, WRITE
Operating current dissipation 2	I_{CC2}	—	0.7	1.5	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN f = 1MHz, READ
Standby current	I_{SB}	—	1.0	5	µA	CS = SK = DI = GND, DO = OPEN

(unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage	V_{IL}	– 0.3	—	0.15 × V_{CC}	V	—
Input high level voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
Output low level voltage	V_{OL}	—	—	0.2	V	I_{OL} = 10µA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = – 10µA
Input leakage current	I_{LI}	– 1.0	—	1.0	µA	V_{IN} = 0V ~ V_{CC}
Output leakage current	I_{LO}	– 1.0	—	1.0	µA	V_{OUT} = 0V ~ V_{CC}, CS = GND
Operating current dissipation 1	I_{CC1}	—	0.5	2	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 250kHz, WRITE
Operating current dissipation 2	I_{CC2}	—	0.2	1	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 250kHz, READ
Standby current	I_{SB}	—	0.4	3	µA	CS = SK = DI = GND, DO = OPEN

●Electrical characteristics (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 2.0V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage	V_{IL}	– 0.3	—	0.15 × V_{CC}	V	—
Input high level voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
Output low level voltage	V_{OL}	—	—	0.2	V	I_{OL} = 10µA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = – 10µA
Input leakage current	I_{LI}	– 1.0	—	1.0	µA	V_{IN} = 0V ~ V_{CC}
Output leakage current	I_{LO}	– 1.0	—	1.0	µA	V_{OUT} = 0V ~ V_{CC}, CS = 0V
Operating current dissipation 2	I_{CC2}	—	0.2	1	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN f = 200kHz, READ
Standby current	I_{SB}	—	0.4	3	µA	CS = SK = DI = 0V, DO = OPEN

●Circuit operation

(1) Command mode

With these ICs, commands are not recognized or acted upon until the start bit is received. The start bit is taken as the first “1” that is received after the CS pin rises.

∗1 After setting of the read command and input of the SK clock, data corresponding to the specified address is output, with data corresponding to upper addresses then output in sequence. (Auto increment function)

Command	Start bit	Operating code	Address	Data
Read (READ)∗1	1	10	0A6 ~ A0	—
Write enabled (WEN)	1	00	11XXXXXX	—
Write (WRITE)∗2	1	01	0A6 ~ A0	D15 ~ D0
Write all addresses (WRAL)∗2	1	00	01XXXXXX	D15 ~ D0
Write disabled (WDS)	1	00	00XXXXXX	—
Erase (ERASE)∗3	1	11	0A6 ~ A0	—
Chip erase (ERAL)∗3	1	00	10XXXXXX	—

X: Either V_{IH} or V_{IL}

∗2 When the write or write all addresses command is executed, all data in the selected memory cell is erased automatically, and the input data is written to the cell.

∗3 These modes are optional modes. Please contact Rohm for information on operation timing.

(2) Operation timing characteristics

(unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK clock frequency	f_{SK}	—	—	1	MHz
SK "H" time	t_{SKH}	450	—	—	ns
SK "L" time	t_{SKL}	450	—	—	ns
CS "L" time	t_{CS}	450	—	—	ns
CS setup time	t_{CSS}	50	—	—	ns
DI setup time	t_{DIS}	100	—	—	ns
CS hold time	t_{CSH}	0	—	—	ns
DI hold time	t_{DIH}	100	—	—	ns
Data "1" output delay time	t_{PD1}	—	—	500	ns
Data "0" output delay time	t_{PD0}	—	—	500	ns
Time from CS to output confirmation	t_{SV}	—	—	500	ns
Time from CS to output High impedance	t_{DF}	—	—	100	ns
Write cycle time	$t_{E/W}$	—	—	10	ms

For low voltage operation (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

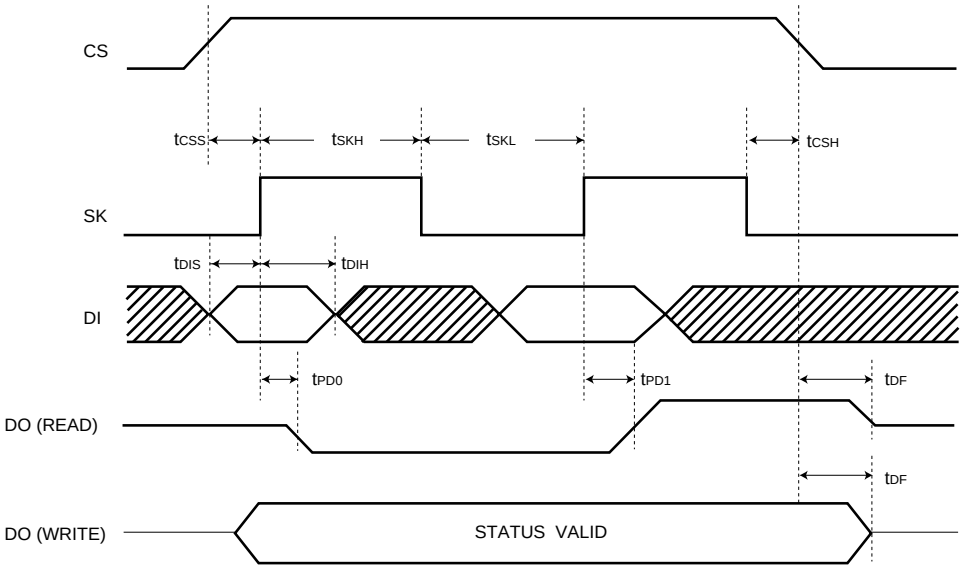
Parameter	Symbol	Min.	Typ.	Max.	Unit
SK clock frequency	f_{SK}	—	—	250	kHz
SK "H" time	t_{SKH}	1	—	—	µs
SK "L" time	t_{SKL}	1	—	—	µs
CS "L" time	t_{CS}	1	—	—	µs
CS setup time	t_{CSS}	200	—	—	ns
DI setup time	t_{DIS}	400	—	—	ns
CS hold time	t_{CSH}	0	—	—	ns
DI hold time	t_{DIH}	400	—	—	ns
Data "1" output delay time	t_{PD1}	—	—	2	µs
Data "0" output delay time	t_{PD0}	—	—	2	µs
Time from CS to output confirmation	t_{SV}	—	—	2	µs
Time from CS to output High impedance	t_{DF}	—	—	400	ns
Write cycle time	$t_{E/W}$	—	—	25	ms

When reading at low voltage (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 2.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK clock frequency	f_{SK}	—	—	200	kHz
SK "H" time	t_{SKH}	2	—	—	µs
SK "L" time	t_{SKL}	2	—	—	µs
CS "L" time	t_{CS}	2	—	—	µs
CS setup time	t_{CSS}	400	—	—	ns
DI setup time	t_{DIS}	800	—	—	ns
CS hold time	t_{CSH}	0	—	—	ns
DI hold time	t_{DIH}	800	—	—	ns
Data "1" output delay time	t_{PD1}	—	—	4	µs
Data "0" output delay time	t_{PD0}	—	—	4	µs
Time from CS to output High impedance	t_{DF}	—	—	800	ns

○ Not designed for radioactive rays.

(3) Timing chart



- Data is acquired from DI in synchronization with the SK rise.
- During a reading operation, data is output from DO in synchronization with the SK rise.
- During a writing operation, a Status Valid (READY or $\overline{\text{BUSY}}$) is valid from the time CS is HIGH until time t_{CS} after CS falls following the input of a write command and before the output of the next command start bit. Also, DO must be in a HIGH-Z state when CS is LOW.
- After the completion of each mode, make sure that CS is set to LOW, to reset the internal circuit, before changing modes.

Fig. 1 Synchronized data timing

(4) Reading (Figure 2)

When the read command is acknowledged, the data (16 bits) for the input address is output serially. The data is synchronized with the SK rise during A0 acquisition and a “0” (dummy bit) is output. All further data is output in synchronization with the SK pulse rises.

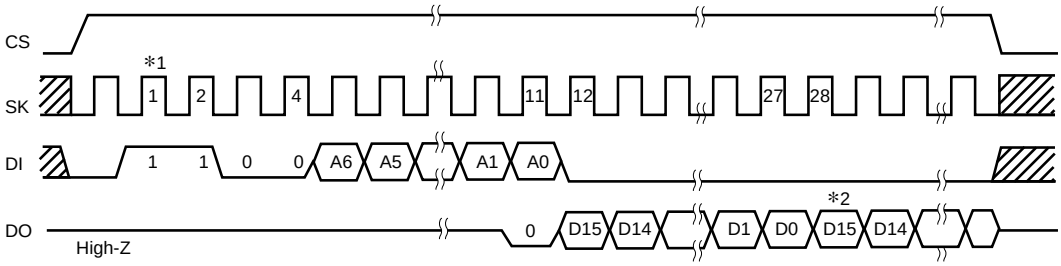
(5) Write enable (Figure 3)

These ICs are set to the write disabled state by the internal reset circuit when the power is turned on. Therefore, before performing a write command, the write enable command must be executed. When this command is executed, it remains valid until a write disable command is issued or the power supply is cut off. However, read commands can be used in either the write enable or write disable state.

(6) Write (Figure 4)

This command writes the input 16-bit data (D15 to D0) to the specified address (A6 to A0). Actual writing of the data begins after CS falls (following the 27th clock pulse after the start bit input), and the SK clock which reads D0 falls.

If STATUS is not detected (CS is fixed at LOW), or if STATUS is detected (CS = HIGH) at a maximum of 10 ms, in accordance with the time $t_{E/W}$, no commands are accepted while DO is LOW ($\overline{BUSY}$). Therefore, no commands should be input during this period.



∗1 If the first data input following the rise of the start bit CS is "1", the start bit is acknowledged. Also, if a "1" is input following several zeroes in succession, the "1" is recognized as the start bit, and subsequent operation commences. This applies also to all commands described subsequently.

∗2 Address auto increment function: These ICs are equipped with an address auto increment function which is effective only during reading operations. With this function, if the SK clock is input following execution of one of the above reading commands, data is read from upper addresses in succession. CS is held in HIGH state during automatic incrementing.

Fig. 2 Read cycle timing (READ)

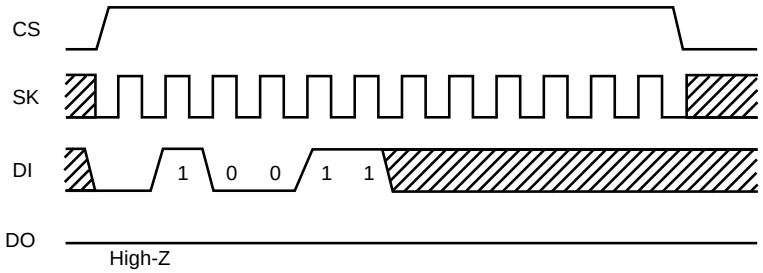


Fig. 3 Write enable cycle timing

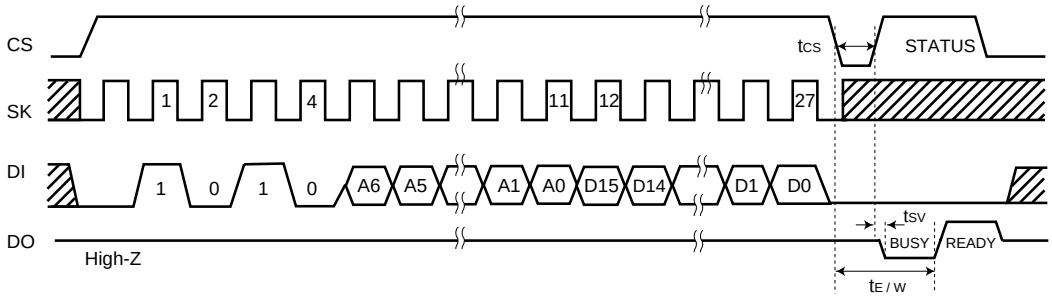


Fig. 4 Write cycle timing (WRITE)

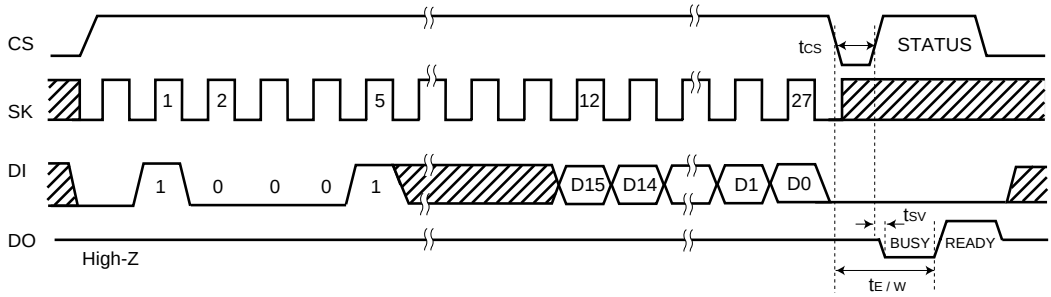


Fig. 5 Write all address cycle timing (WRAL)

(STATUS)

After time t_{CS} following the fall of CS, after input of the write command), if CS is set to HIGH, the write execute = BUSY (LOW) and the command wait status READY (HIGH) are output.

If in the command wait status (STATUS = READY), the next command can be performed within the time $t_{E/W}$. Thus, if data is input via SK and DI with CS = HIGH in the $t_{E/W}$ period, erroneous operations may be performed. To avoid this, make sure that DI = LOW when CS = HIGH. (Caution is especially important when common input ports are used.) This applies to all of the write commands.

(7) All address write (Figure 5)

With this command, the input 16-bit data is written simultaneously to all of the addresses (128 words).

Rather than writing one word at a time, in succession, data is written all at one time, enabling a write time of $t_{E/W}$.

(8) Write disable (Figure 6)

When the power supply is turned on, the IC enters the write disable status when a write enable command is issued. If a write disable command is issued at this point, however, the IC enters the write disabled status, just as when the power is first turned on. Subsequent write commands are cancelled by the software, but read commands may be executed. In the write enable status, writing begins even if a write command is entered accidentally. To prevent errors of this type, we recommend executing a write disable command after writing has been completed.

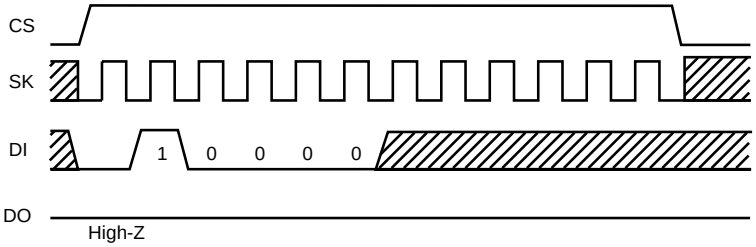
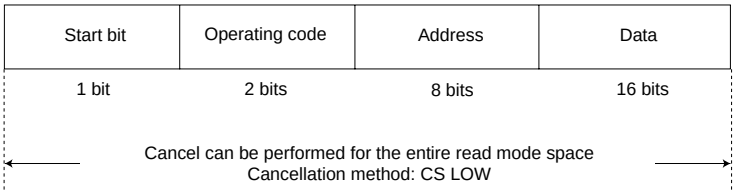


Fig. 6 Write disable cycle timing (WDS)

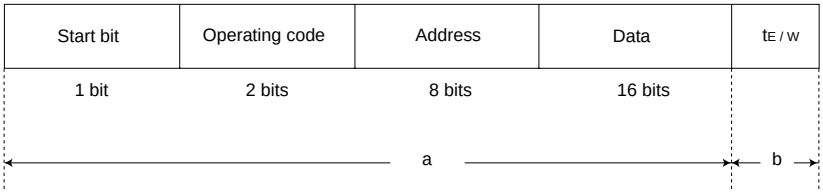
●Operation notes

(1) Cancelling modes

〈READ〉



〈WRITE, WRAL〉



a: Canceled by setting CS LOW or Vcc OFF (✻)
b: Cannot be canceled by any method. If Vcc is set to OFF during this time, the data in the designated address is not secured.
✻: Vcc OFF (Vcc is turned off after CS is set to LOW)

Fig.7

(2) Timing in the standby mode

As shown in Figure 8, during standby, if CS rises when SK is HIGH, the DI state may be read on the rising edge. If this happens, and DI is HIGH, this is taken to be the start bit, causing a bit error (see point “a” in Figure 8).

Make sure all inputs are LOW during standby or when turning the power supply on or off (see Figure 9).

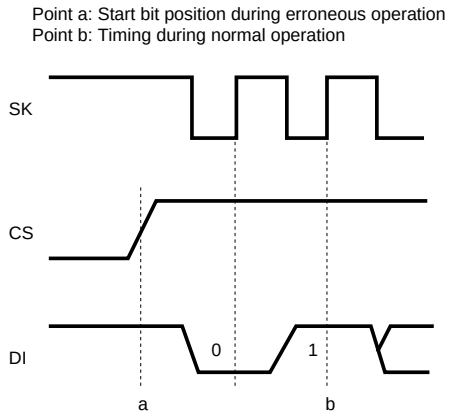


Fig. 8 Erroneous operation timing

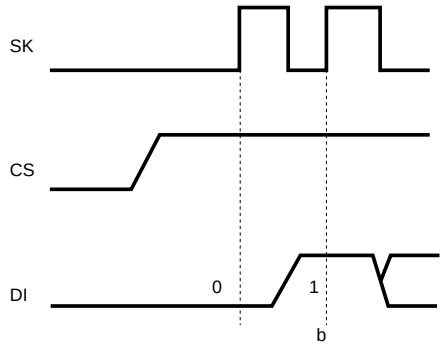


Fig. 9 Normal operation timing

(3) Precautions when turning power on and off

When turning the power supply on and off, make sure CS is set to LOW (see Figure 10).

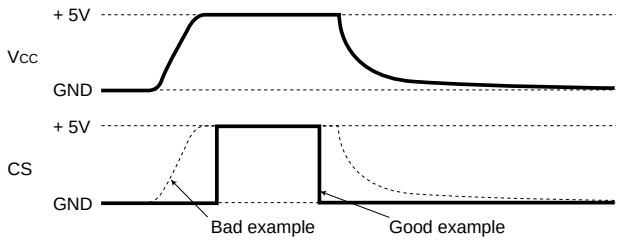
When CS is HIGH, the EEPROM enters the active state. To avoid this, make sure CS is set to LOW (disable mode) when turning on the power supply.

(When CS is LOW, all input is cancelled.)

When the power supply is turned off, the low power state can continue for a long time because of the capacity of the power supply line. Erroneous operations and erroneous writing can occur at such times for the same reasons as described above. To avoid this, make sure CS is set to LOW before turning off the power supply.

To prevent erroneous writing, these ICs are equipped with a POR (Power On Reset) circuit, but in order to achieve operation at a low power supply, V_{CC} is set to operate at approximately 1.3V. After the POR has been activated, writing is disabled, but if CS is set to HIGH, writing may be enabled because of noise or other factors. However, the POR circuit is effective only when the power supply is on, and will not operate when the power is off.

Also, to prevent erroneous writing at low voltages, these ICs are equipped with a built-in circuit (V_{CC}-lock-out circuit) which resets the write command if V_{CC} drops to approximately 2V or lower (typ.) (∗).



(Bad example) Here, the CS pin is pulled up to VCC. In this case, CS is HIGH (active state). Please be aware that the EEPROM may perform erroneous operations or write erroneous data because of noise or other factors. This can occur even if the CS input is high-Z.

(Good example) In this case, CS is LOW when the power supply is turned on or off.

Fig. 10

(4) Clock (SK) rise conditions

If the clock pin (SK) signal of the BR93LC56 / F / FV has a long rise time (tr) and if noise on the signal line exceeds a certain level, erroneous operation can occur due to erroneous counts in the clock. To prevent this, a Schmitt trigger is built into the SK input of the BR93-LC56 / F / FV. The hysteresis amplitude of this circuit is set to approximately 0.2V, so if the noise exceeds the SK input, the noise amplitude should be set to $0.2V_{P-P}$ or lower. Furthermore, rises and falls in the clock input should be accelerated as much as possible.

(5) Power supply noise

The BR93LC56 / F / FV discharge high volumes of high voltage when a write is completed. The power supply may fluctuate at such times. Therefore, make sure a capacitor of 1000pF or greater is connected between V_{CC} (Pin 8) and GND (Pin 5).

(6) Connecting DI and DO directly

The BR93LC56 / F / FV have an independent input pin (DI) and output pin (DO). These are treated as individual signals on the timing chart but can be controlled through one control line.Control can be initiated on a single control line by inserting a resistor R betweeen the [DI] pin and [DO] pin.

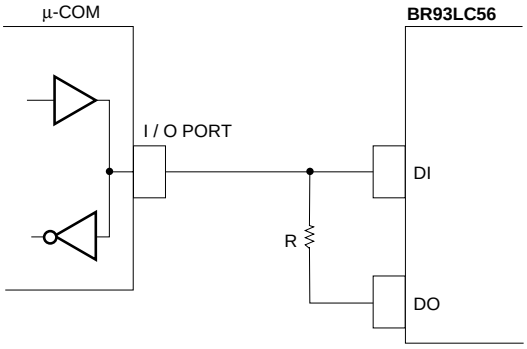


Fig. 11 Common connections for the DI and DO control line

1) Data collision between the μ-COM output and the DO output

Within the input and output timing of the BR93LC56 / F / FV, the drive from the μ-COM output to the DI input and a signal output from the DO output can be emitted at the same time. This happens only for the 1 clock cycle (a dummy bit “0” is output to the DO pin) which acquires the A0 address data during a read cycle. When the address data A0 = 1, the μ-COM output becomes a direct current source for the DO pin.

The resistor R is the only resistance which limits this current. Therefore, a resistor with a value which satisfies the μ-COM and the BR93LC56 / F / FV current capacity is required. When using a single control line, when a dummy bit “0” is output to the DO, the μ-COM I / O address data A0 is also output. Therefore, the dummy bit cannot be detected.

2) Feedback to the DI input from the DO output

Data is output from the DO pin and then feeds back into the DI input through the resistor R. This happens when:

· DO data is output during a read operation

· A READY / $\overline{\text{BUSY}}$ signal is output during WRITE or WRAL operation

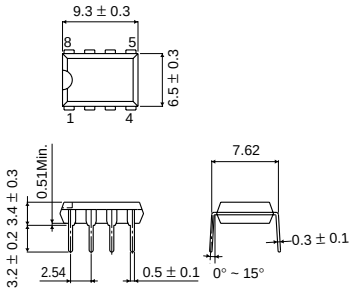
Such feedback does not cause problems in the basic operation of the BR93LC56 / F / FV.

The μ-COM input level must be adequately maintained for the voltage drop at R which is caused by the total input leakage current for the μ-COM and the BR93LC56 / F / FV.

In the state in which SK is input, when the READY / $\overline{\text{BUSY}}$ function is used, make sure that CS is dropped to LOW within four clock pulses of the output of the READY signal HIGH and the standby mode is restored. For input after the fifth clock pulse, the READY HIGH will be taken as the start bit and WDS or some other mode will be activated, depending on the DI state.

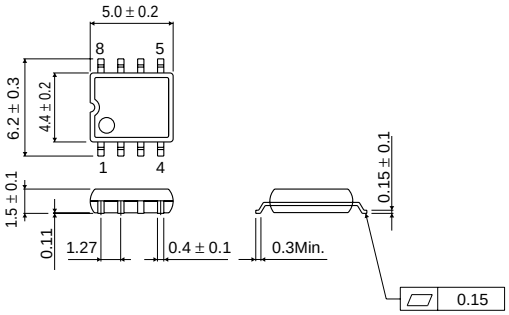
●External dimension (Units: mm)

BR93LC56



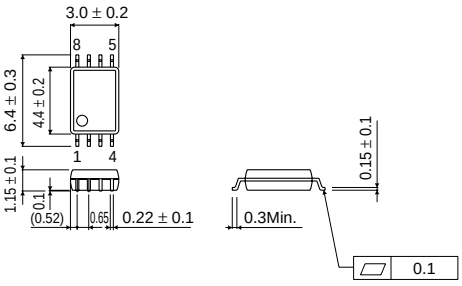
DIP8

BR93LC56F / RF



SOP8

BR93LC56FV



SSOP-B8