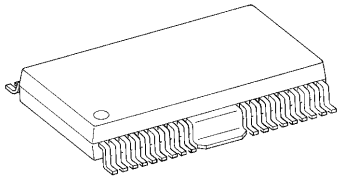
TOSHIBA Bi-CMOS PROCESSOR IC SILICON MONOLITHIC

TB62200AF

DUAL-STEPPING MOTOR DRIVER IC USING PWM CHOPPER TYPE

The TB62200AF is a dual-stepping motor driver driven by chopper micro-step pseudo sine wave.
To drive two-phase stepping motors, Two pairs of 16-bit latch and shift registers are built in the IC. The IC is optimal for driving stepping motors at high efficiency and with low-torque ripple.
The IC supports Mixed Decay mode for switching the attenuation ratio at chopping. The switching time for the attenuation ratio can be switched in two stages according to the load.



HSOP36-P-450-0.65

Weight : 0.79 g (Typ.)

FEATURES

- Chopping bipolar stepping motor driver
- Two stepping motors driven by micro-step pseudo sine wave are controlled by a single driver IC
- Monolithic Bi-CMOS IC
- Low ON-resistance of RDS (on) = 0.5 Ω (@T_j = 25°C, 1.0 A : Typ.)
- Two pairs of built-in 16-bit shift and latch registers
- Two pairs of built-in 4-bit D / A converters for micro steps
- Built-in TSD, V_{DD} & V_M power monitor (reset) circuit for protection
- Built-in charge pump circuit (two external capacitors)
- 36-pin power flat package (HSOP36-P-450-0.65)
- Output voltage : 30 V max
- Output current : 1.3 A / phase max
- Built-in Mixed Decay mode (Fast / Slow at 40 / 74% switchable) and Slow Decay mode
- Chopping frequency can be set by external resistors and capacitors. High-speed chopping possible at 100 kHz or higher.

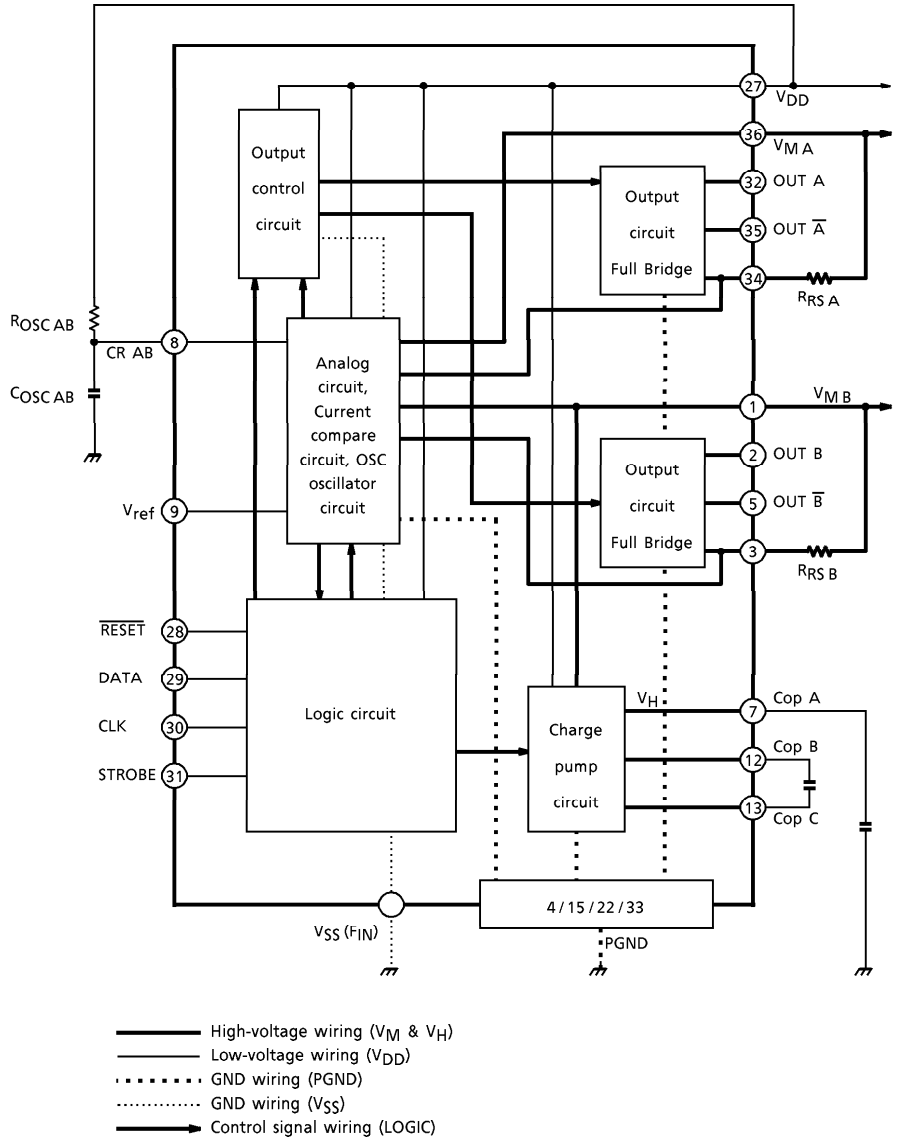
(Note 1) When using the IC, pay attention to thermal conditions.

(Note 2) These devices are easy damage by high static voltage.
In regards to this, please handle with care.

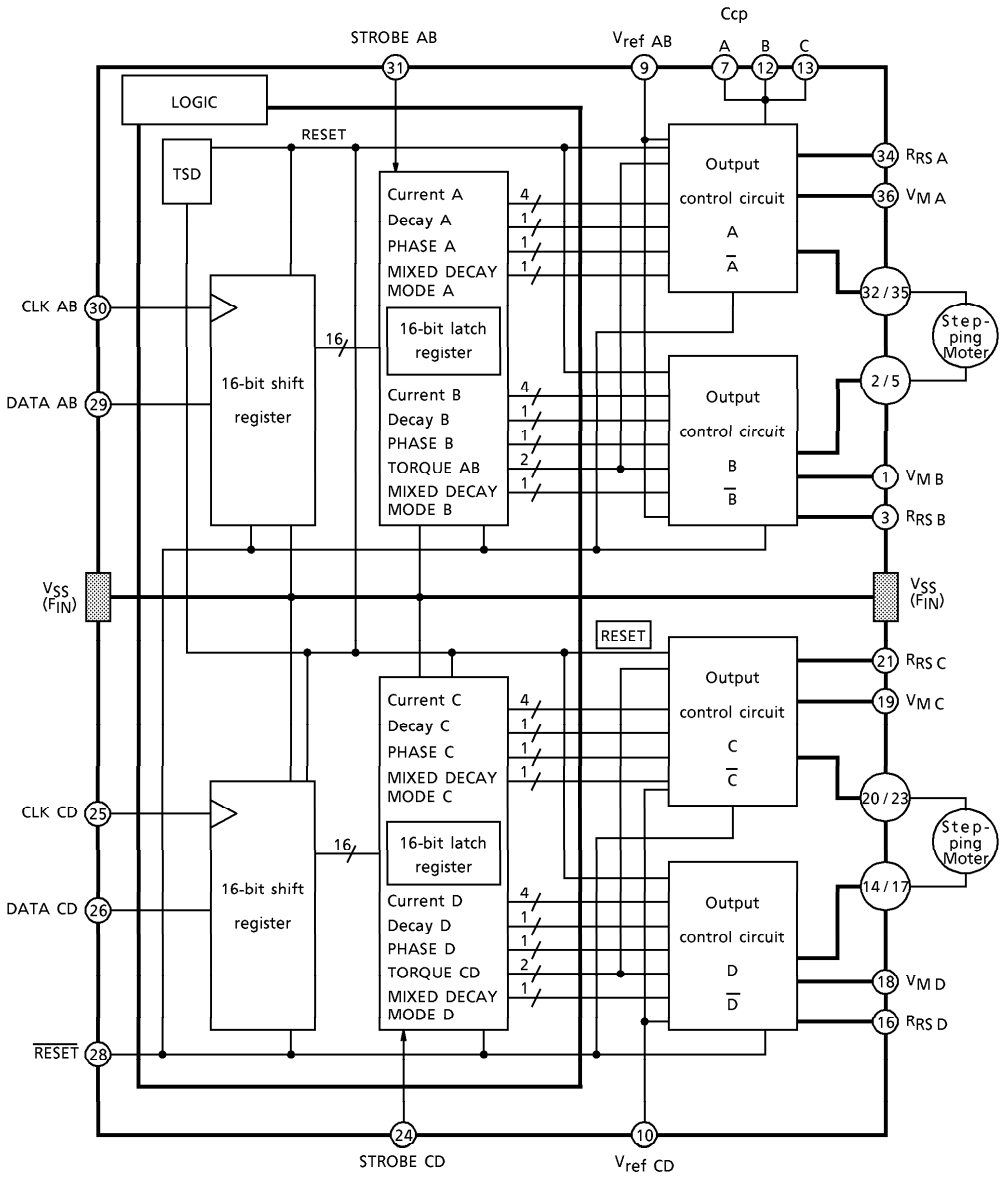
BLOCK DIAGRAM 1

Overview (Power lines : A / B unit (C / D unit is the same as A / B unit))

Block Diagram (Power lines)

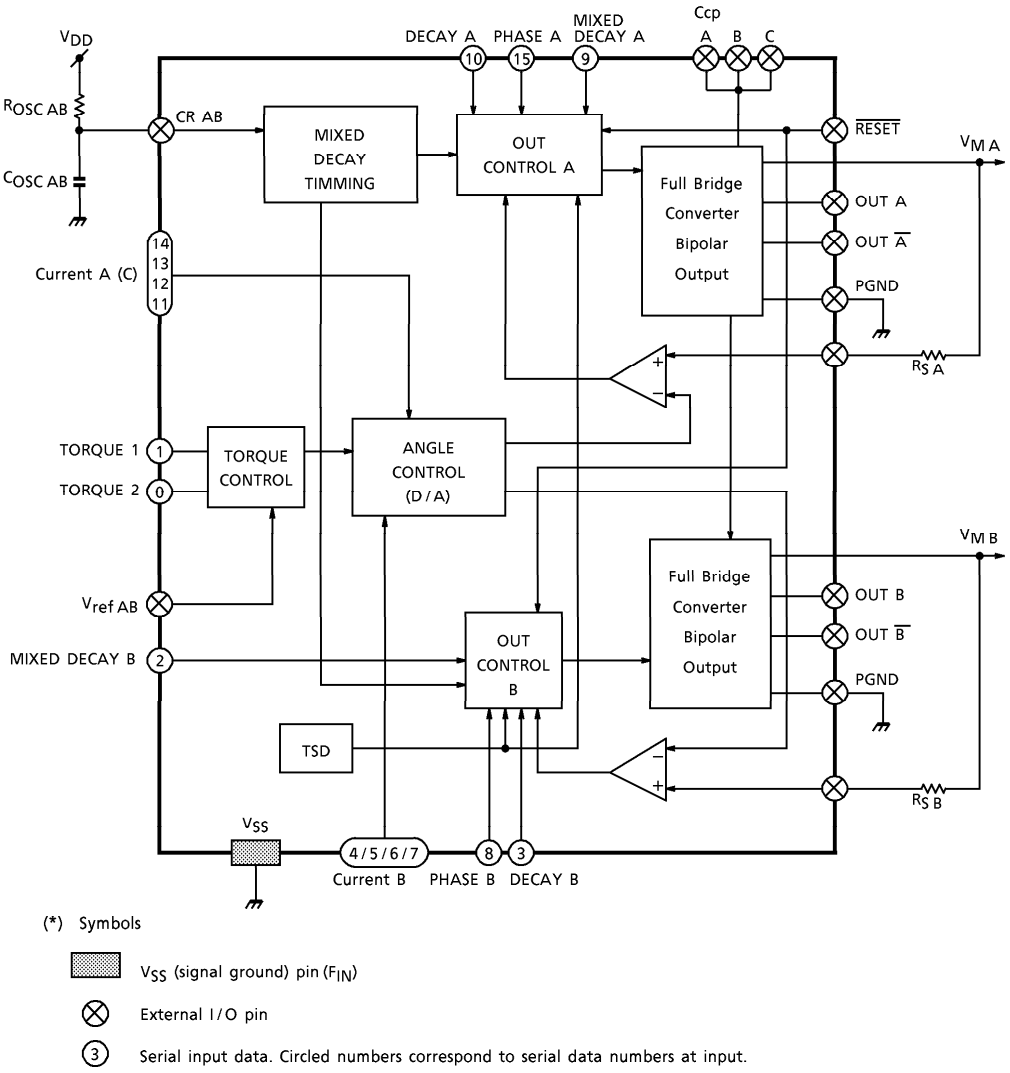


BLOCK DIAGRAM 2
Overview (Details)



BLOCK DIAGRAM 3

Output control circuit A / B unit (C / D unit is the same as A / B unit)



A chopping reference oscillation waveform (saw-tooth wave) is generated by the resistor and capacitor connected to the CR pin. Current path switching timing is generated for Mixed and Slow Decay modes according to the chopping waveform.

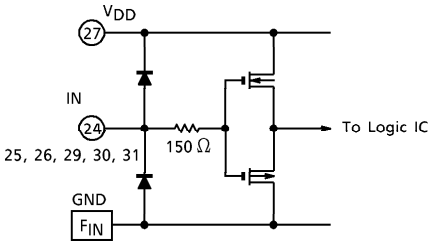
The reference voltage applied to the V_{ref} pin is attenuated by 100, 85, 70, or 50% according to the 2-bit torque data. A reference voltage is generated by the attenuated reference voltage and 4-bit current setting data.

When current flows through the sense resistor connected to the R_S pin, there is a potential difference between the V_M and R_S pins. The potential difference is compared by the comparator and the result fed back to the output control circuit. Then chopping takes place.

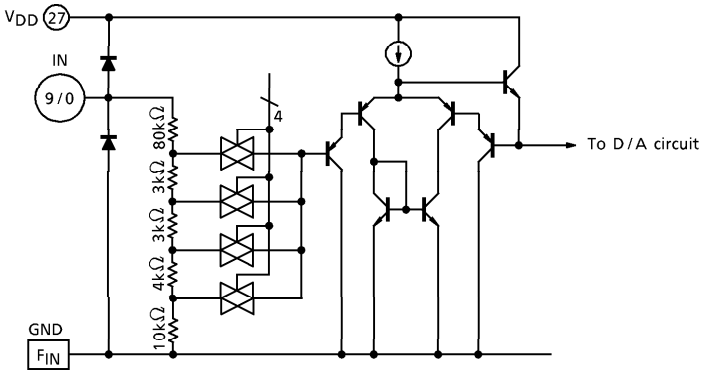
BLOCK DIAGRAM 4

Input A / B unit (C / D unit is the same as A / B unit)

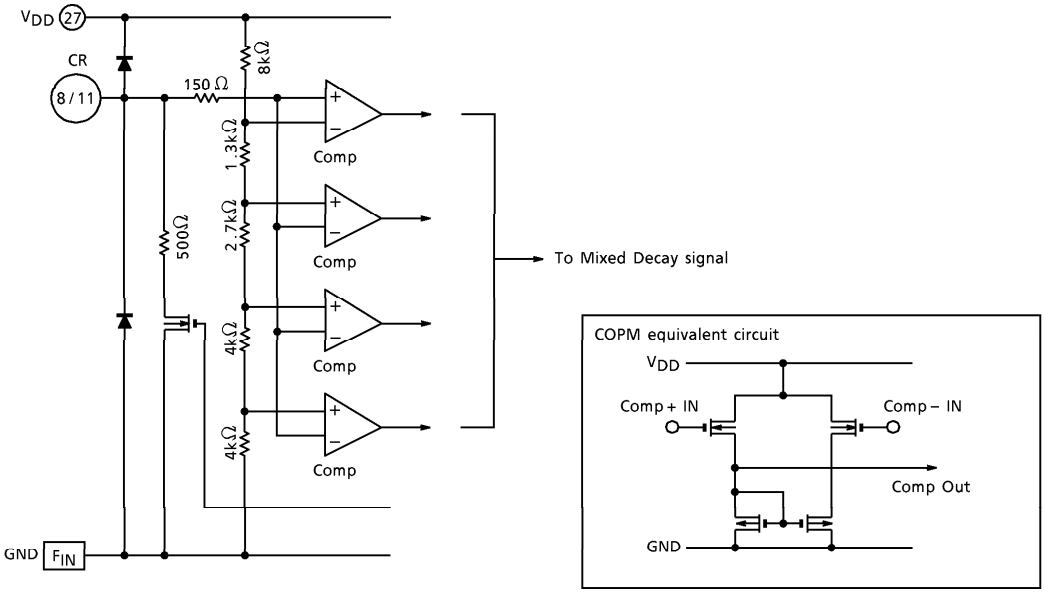
1. Logic input circuit (CLK, DATA, STROBE)



2. V_{ref} input circuit

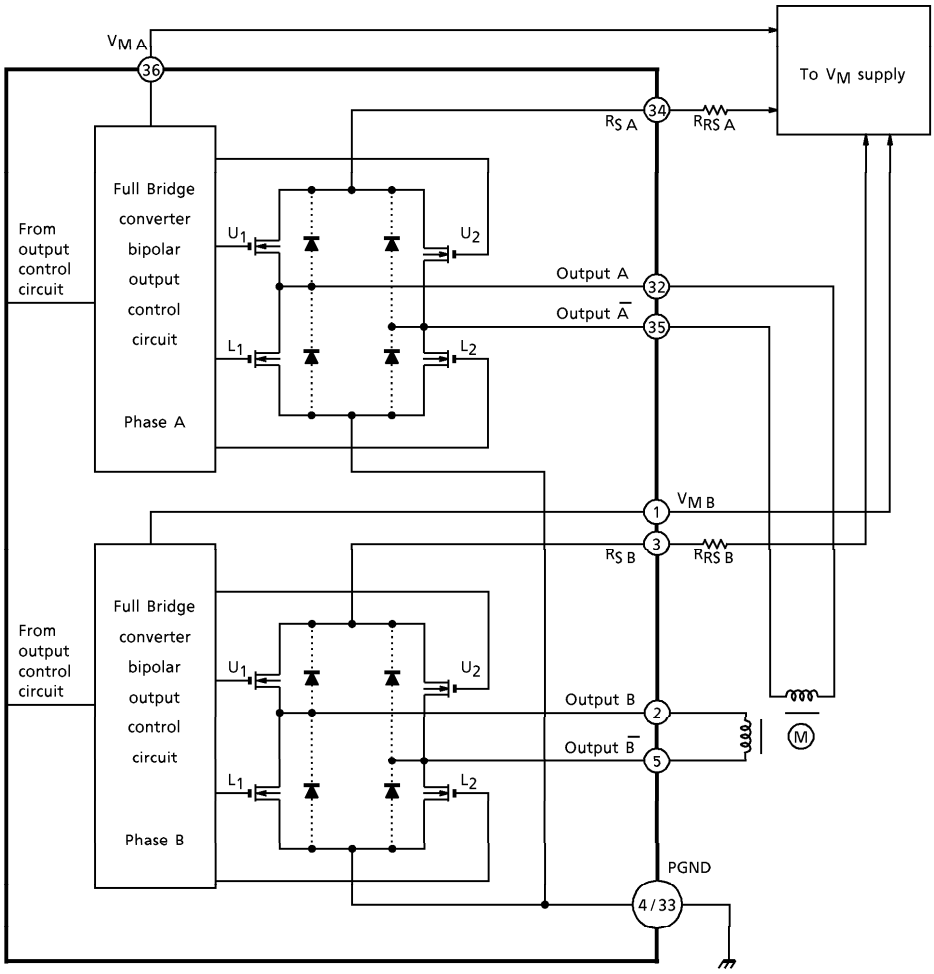


3. CR circuit block



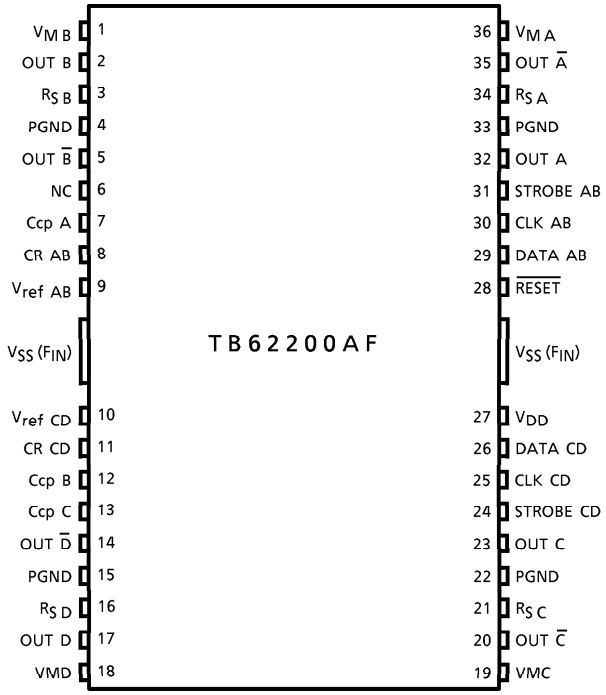
BLOCK DIAGRAM 5

Output A / B unit (C / D unit is the same as A / B unit)



PIN ASSIGNMENT

(TOP VIEW)



- $R_{S\,A\sim D}$: Current sense resistor connecting pins
- PGND : Power GND
- NC : Not connected

PIN DESCRIPTION

PIN No.	PIN SYMBOL	DESCRIPTION
1	$V_{M\,B}$	Power pin for output B block
2	OUT B	Output B pin
3	$R_{S\,B}$	Channel B current pin
4	PGND	Power GND pin (Note)
5	OUT $\overline{B}$	Output $\overline{B}$ pin
6	NC	Not connected
7	Ccp A	Capacitor pin for charge pump (Ccp1)
8	CR AB	External C / R (osc) pin AB (sets chopping frequency)
9	$V_{ref\,AB}$	V_{ref} input pin AB
F_{IN}	V_{SS}	F_{IN} (V_{SS}) : Logic GND pin (Note)
10	$V_{ref\,CD}$	V_{ref} input pin CD
11	CR CD	External C / R (osc) pin CD (sets chopping frequency)
12	Ccp B	Capacitor pin for charge pump (Ccp2)
13	Ccp C	Capacitor pin for charge pump (Ccp2)
14	OUT $\overline{D}$	Output $\overline{D}$ pin
15	PGND	Power GND pin (Note)
16	$R_{S\,D}$	Channel D current pin
17	OUT D	Output D pin
18	$V_{M\,D}$	Power pin for output D block
19	$V_{M\,C}$	Power pin for output C block
20	OUT $\overline{C}$	Output $\overline{C}$ pin
21	$R_{S\,C}$	Channel C current pin
22	PGND	Power GND pin (Note)
23	OUT C	Output C pin
24	STROBE CD	CD STROBE (latch) signal input pin ($\sqcap$: LATCH)
25	CLK CD	CD clock input pin
26	DATA CD	CD serial data signal input pin
27	V_{DD}	Power pin for logic block
F_{IN}	V_{SS}	F_{IN} (V_{SS}) : Logic GND pin (Note)
28	$\overline{RESET}$	Output reset signal input pin (L : RESET)
29	DATA AB	AB serial data signal input pin
30	CLK AB	AB clock input pin
31	STROBE AB	AB STROBE (latch) signal input pin ($\sqcap$: LATCH)
32	OUT A	Output A pin
33	PGND	Power GND pin (Note)
34	$R_{S\,A}$	Channel A current pin
35	OUT $\overline{A}$	Output $\overline{A}$ pin
36	$V_{M\,A}$	Power pin for output A block

(Note) How to handle GND pins
All power GND pins and F_{IN} (V_{SS} : signal GND) pins must be grounded.
Since F_{IN} also functions as a heat sink, take the heat dissipation into consideration when designing the board.

SIGNAL FUNCTIONS

1. Serial input signals (for A / B. C / D is the same as A / B)

DATA No.	NAME	FUNCTIONS
0	TORQUE 0	DATA No.0, 1 = HH : 100%, LH : 85%
1	TORQUE 1	HL : 70%, LL : 50%
2	MIXED DECAY MODE B	(H : 74% FAST DECAY, L : 40% FAST DECAY)
3	DECAY B	(H : SLOW DECAY, L : MIXED DECAY)
4	Current B_0	Used for setting current. (LLLL = Output ALL OFF MODE) 4-bit current B data (Steps can be divided into 16 by 4-bit data)
5	Current B_1	
6	Current B_2	
7	Current B_3	
8	PHASE B	Phase information (H : OUT B : H, OUT $\overline{B}$: L)
9	MIXED DECAY MODE A	(H : 74% FAST DECAY, L : 40% FAST DECAY)
10	DECAY A	(H : SLOW DECAY, L : MIXED DECAY)
11	Current A_0	Used for setting current. (LLLL = Output ALL OFF MODE) 4-bit current A data (Steps can be divided into 16 by 4-bit data)
12	Current A_1	
13	Current A_2	
14	Current A_3	
15	PHASE A	Phase information (H : OUT A : H, OUT $\overline{A}$: L)

(Note 1)

(Note 1) Serial data input order
Serial data are input in the order DATA 0 (TORQUE 0) → DATA 15 (PHASE A).

2. Serial input signal functions

		INPUT				Action
CLK	STROBE (LUTCH)	DATA	$\overline{RESET}$	V_{DDR} (Note 2) or V_{MR}	TSD OPERATION	
↑	×	×	H	H	L	No change in shift register.
↓	×	H	H	H	L	H level is input to shift register.
↓	×	L	H	H	L	L level is input to shift register.
×	↑	×	H	H	L	Shift register data are latched.
×	↓	×	H	H	L	Qn
×	×	×	L	×	L	Output off (shift register data clear)
×	×	×	×	L	L	Output off (shift register data clear)
×	×	×	H	H	H	Output off (shift register data hold) Charge pump in operation

× : Don't Care
Qn : Latched output level when STROBE is ↑.
H when TSD is in operation.
(Note 2) V_{DDR} and V_{MR}
H when the operable range (3 V typical) or higher and L when lower.

3. PHASE functions

INPUT	FUNCTION
H	Positive polarity (A : H, $\overline{A}$: L)
L	Negative polarity (A : L, $\overline{A}$: H)

4. DECAY functions

INPUT	FUNCTION
H	Slow Decay Mode
L	Mixed Decay Mode

5. Mixed Decay Mode functions

INPUT	FUNCTION
H	74% Mixed Decay Mode
L	40% Mixed Decay Mode

(Note) Valid only when DECAY signal is L (Mixed Decay Mode).

6. TORQUE functions

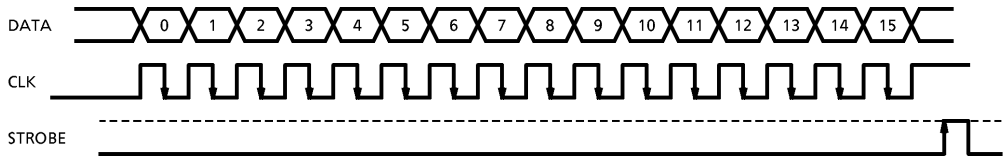
TORQUE 0	TORQUE 1	Comparator reference voltage
H	H	100%
L	H	85%
H	L	70%
L	L	50%

7. Current Ax (Bx) functions

STEP	SET ANGLE	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
16	90.0	H	H	H	H	L	L	L	L
15	84.4	H	H	H	H	L	L	L	H
14	78.8	H	H	H	L	L	L	H	L
13	73.1	H	H	L	H	L	L	H	H
12	67.5	H	H	L	L	L	H	L	L
11	61.2	H	L	H	H	L	H	L	H
10	56.3	H	L	H	L	L	H	H	L
9	50.6	H	L	L	H	L	H	H	H
8	45.0	H	L	L	L	H	L	L	L
7	39.4	L	H	H	H	H	L	L	H
6	33.8	L	H	H	L	H	L	H	L
5	28.1	L	H	L	H	H	L	H	H
4	22.5	L	H	L	L	H	H	L	L
3	16.9	L	L	H	H	H	H	L	H
2	11.3	L	L	H	L	H	H	H	L
1	5.6	L	L	L	H	H	H	H	H
0	0.0	L	L	L	L	H	H	H	H

By inputting the above current data (A : 4-bit, B : 4-bit), 17-microstep drive is possible. For 1 step fixed to 90 degrees, see the section on output current vector line (54 page).

8. Serial Data Input Setting



(*) Data input to the DATA pin are 16-bit serial data.
Data are transferred from DATA 0 (Torque 0) to DATA 15 (Phase A). Data are input and transferred at the following timings.

- At CLK falling edge : data input
- At CLK rising edge : data transfer

After data are transferred, all data are latched on the rising edge of the STROBE signal. As long as STROBE is not rising, the signal can be either Low or High during data transfer.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Logic Supply Voltage	V_{DD}	7	V
Output Voltage	V_M	30	V
Output Current	I_{out}	1.3 (Note 1)	A / phase
Current Detect Pin Voltage	V_{RS}	V_M − 1.0	V
Charge Pump Pin Maximum Voltage (CCP1 Pin)	V_H	V_M + 7.0	V
Logic Input Voltage	V_{IN}	~V_{DD} + 0.4	V
Power Dissipation	P_D	1.4 (Note 2)	W
		3.2 (Note 3)	W
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−50~150	°C

(Note 1) Perform thermal calculations for instantaneous current value and the maximum current value under normal conditions. Use the IC at 1.0 A or less per phase.
(Note 2) Measured for the IC only.
(Note 3) Measured when mounted on the board. (90 × 230 × 1.6 mm) (Ta = 25°C)

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Output Voltage	V_M	V_{DD} = 5.0 V	20	24	30	V
Output Current	I_{out}	Ta = 25°C, per phase	—	0.9	1.0	A
Logic Input Voltage	V_{IN}	—	GND	—	V_{DD}	V
Clock Frequency	f_{CLK}	V_{DD} = 5.0 V	1.0	—	25	MHz
Chopping Frequency	f_{chop}	V_{DD} = 5.0 V	32	100	150	MHz
Reference Voltage	V_{ref}	V_{DD} = 5.0 V, V_M = 24 V, Torque = 100%	2.0	3.0	V_{DD} − 1.0	V

ELECTRICAL CHARACTERISTICS 1 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	HIGH	V_{IN} (H)	1	CLK, $\overline{RESET}$, STROBE, DATA pins	2.0	—	V_{DD} + 0.4	V
	LOW	V_{IN} (L)			GND − 0.4	—	0.8	
Input Current		I_{IN} (H)	1	CLK, STROBE, $\overline{RESET}$, DATA pins	—	—	1.0	μA
		I_{IN} (L)			—	—	1.0	
Power Dissipation (V_{DD} pin)		I_{DD1}	1	V_{DD} = 5 V (STROBE, $\overline{RESET}$, DATA = L), $\overline{RESET}$ = L, Logic, output all off	—	4.0	6.0	mA
		I_{DD2}		Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, V_{DD} = 5 V, Charge Pump = charged	—	4.0	20	
Power Dissipation (V_M pin)		IM1	3	Output OPEN (STROBE, CLK, DATA = L), $\overline{RESET}$ = L, Logic, output all off Charge Pump = no operation	—	4.5	8	mA
		IM2		Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, V_{DD} = 5 V, V_M = 24 V, Output off Charge Pump = charged	—	12	20	
		IM3	4	Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, 100 kHz chopping (emulation), Output OPEN, Charge Pump = charged	—	30	40	
Output Standby Current	Upper	I_{OH}	2	V_{RS} = V_M = 24 V, V_{out} = 0 V, $\overline{RESET}$ = H DATA = ALL L	−400	—	—	μA
Output Bias Current	Upper	I_{OB}		V_{RS} = V_M = 24 V, V_{out} = 24 V, $\overline{RESET}$ = H, DATA = ALL L	−200	—	—	μA
Output Leakage Current	Lower	I_{OL}		V_{RS} = V_M = CcpA = V_{out} = 24 V, $\overline{RESET}$ = L	—	—	1.0	
Comparator Reference Voltage Ratio	HIGH (Reference)	V_{RS} (H)	5	V_{ref} = 3.0 V, V_{ref} (Gain) = 1 / 5.1 TORQUE = (H.H) = 100% set	—	100	—	%
	MID HIGH	V_{RS} (MH)		V_{ref} = 3.0 V, V_{ref} (Gain) = 1 / 5.1 TORQUE = (H.L) = 85% set	83	85	87	
	MID LOW	V_{RS} (ML)		V_{ref} = 3.0 V, V_{ref} (Gain) = 1 / 5.1 TORQUE = (L.H) = 70% set	68	70	72	
	LOW	V_{RS} (L)		V_{ref} = 3.0 V, V_{ref} (Gain) = 1 / 5.1 TORQUE = (L.L) = 50% set	48	50	52	
Output Current Differential		ΔI_{out1}	6	I_{out} = 900 mA	−5	—	5	%
Output Current Setting Differential		ΔI_{out2}	6	I_{out} = 900 mA	−10	—	10	%
RS Pin Current		IRS	7	V_{RS} = 24 V, V_M = 24 V, $\overline{RESET}$ = L (RESET status)	—	—	5	μA

ELECTRICAL CHARACTERISTICS 1 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transistor Drain-Source On-Resistance	R_{on} (D-S) 1	1	I_{out} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Drain-Source	—	0.5	0.6	Ω
	R_{on} (S-D) 1		I_{out} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Source-Drain	—	0.5	0.6	
	R_{on} (D-S) 2		I_{out} = 1.0 A, V_{DD} = 5 V, T_j = 105°C, Drain-Source	—	0.6	0.75	
	R_{on} (S-D) 2		I_{out} = 1.0 A, V_{DD} = 5 V, T_j = 105°C, Source-Drain		0.6	0.75	

ELECTRICAL CHARACTERISTICS 2 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{ref} Input Voltage	V_{ref}	11	V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = H, Output on	2	—	V_{DD} – 1.0	V
V_{ref} Input Current	I_{ref}	11	$\overline{RESET}$ = H, Output off V_M = 24 V, V_{DD} = 5 V, V_{ref} = 3.0 V	0	—	100	μA
V_{ref} Attenuation Ratio	V_{ref} (GAIN)	5	V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = H, Output on, V_{ref} = 2.0~V_{DD} – 1.0 V	1 / 4.9	1 / 5.1	1 / 5.3	—
TSD Temperature	T_jTSD (Note)	14	V_{DD} = 5 V, V_M = 24 V	130	—	170	°C
TSD Return Temperature Difference	ΔT_jTSD	14	T_jTSD = 130~170°C	—	T_jTSD – 20	—	°C
V_{DD} Return Voltage	V_{DDR}	12	V_M = 24 V, $\overline{RESET}$ = H	2	—	4	V
V_M Return Voltage	V_{MR}	13	V_{DD} = 5 V, $\overline{RESET}$ = H	2	—	4	V

(Note) Thermal Shut Down (TSD) circuit

When the IC junction temperature reaches the specified value, the TSD circuit turns off the output block for both unit (AB and CD).
The data latched at that time are held without change.
The TSD circuit operates in a range from 130 to 170°C. The circuit halts operation of the output circuits until the temperature drops by 20°C (typical) from the temperature at which the TSD circuit started operation.

ELECTRICAL CHARACTERISTICS 3 (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V, I_{out} = 0.9 A)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Chopper Current	Vector	—	θA = 90 (θ16)	—	—	100	—	%
			θA = 84 (θ15)		—	100	—	
			θA = 79 (θ14)		93	98	—	
			θA = 73 (θ13)		91	96	—	
			θA = 68 (θ12)		87	92	97	
			θA = 62 (θ11)		83	88	93	
			θA = 56 (θ10)		78	83	88	
			θA = 51 (θ9)		72	77	82	
			θA = 45 (θ8)		66	71	76	
			θA = 40 (θ7)		58	63	68	
			θA = 34 (θ6)		51	56	61	
			θA = 28 (θ5)		42	47	52	
			θA = 23 (θ4)		33	38	43	
			θA = 17 (θ3)		24	29	34	
			θA = 11 (θ2)		15	20	25	
			θA = 6 (θ1)		5	10	15	
			θA = 0 (θ0)		—	0	—	

ELECTRICAL CHARACTERISTICS 4 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Reference Voltage	ΔV_{RS}	—	θ = 16/16 – 15/16	V_{ref} = 3.0 V V_{ref} (gain) = 1/5.1	—	0	—	mV
			θ = 15/16 – 14/16		—	11	—	
			θ = 14/16 – 13/16		—	14	—	
			θ = 13/16 – 12/16		—	19	—	
			θ = 12/16 – 11/16		—	25	—	
			θ = 11/16 – 10/16		—	30	—	
			θ = 10/16 – 9/16		—	34	—	
			θ = 9/16 – 8/16		—	39	—	
			θ = 8/16 – 7/16		—	43	—	
			θ = 7/16 – 6/16		—	46	—	
			θ = 6/16 – 5/16		—	50	—	
			θ = 5/16 – 4/16		—	52	—	
			θ = 4/16 – 3/16		—	54	—	
			θ = 3/16 – 2/16		—	56	—	
			θ = 2/16 – 1/16		—	57	—	
			θ = 1/16 – 0/16		—	58	—	

AC CHARACTERISTICS
(Ta = 25°C, V_M = 24 V, V_{DD} = 5 V, output load condition of 6.8 mH / 5.7 Ω)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Frequency	f_{CLK}	15	—	1.0	—	25	MHz
Minimum Clock Pulse width	$t_{w\,(CLK)}$	15	See Figure 1.	40	—	—	ns
	$t_{wp\,(CLK)}$			20	—	—	
	$t_{wn\,(CLK)}$			20	—	—	
Minimum STROBE Pulse Width	t_{STROBE}	15	See Figure 1.	40	—	—	ns
	$t_{STROBE\,(H)}$			20	—	—	
	$t_{STROBE\,(L)}$			20	—	—	
Data Setup Time	$t_{suCLK-SIN}$	15	See Figure 1.	20	—	—	ns
	$t_{suST-CLK}$			20	—	—	
Data Hold Time	$t_{hCLK-SIN}$	15	See Figure 1.	20	—	—	ns
	$t_{hCLK-ST}$			20	—	—	
Output Switching Delay Time	OSC-Charge Delay	16	C_{osc} = 1000 pF, R_{osc} = 12 kΩ f_{chop} = 100 kHz, I_{out} = 0.9 A See Figure 2.	—	600	—	ns
	OSC-FAST Delay (Slow Decay Mode)			—	300	—	
Output Transistor Switching Characteristic	t_r	17	Output Load; 6.8 mH / 5.7 Ω See Figure 1.	—	70	—	ns
	t_f			—	50	—	
	$t_{pLH\,(ST)}$		STROBE (−)~OUT time Output Load; 6.8 mH / 5.7 Ω See Figure 1.	—	300	—	
	$t_{pHL\,(ST)}$			—	150	—	
Noise Rejection Dead Band Time	t_{BRNK}	18	I_{out} = 0.9 A, f_{chop} = 100 kHz C_{osc} = 1000 pF, R_{osc} = 12 kΩ	150	180	250	ns
Maximum Chopping Frequency	$f_{chop\,(MAX)}$	9	V_M = 24 V, V_{DD} = 5 V, Output active (I_{out} = 0.9 A) Step fixed, Ccp1 = 0.47 μF, Ccp2 = 0.02 μF	—	—	150	kHz
Minimum Chopping Frequency	$f_{chop\,(MIN)}$			32	—	—	
Chopping Frequency	f_{chop}	9	C_{osc} = 1000 pF, R_{osc} = 12 kΩ Output active (I_{out} = 0.9 A)	—	100	—	
Chopping Triangular-Wave High Value	H_{chop}	10	V_M = 24 V, V_{DD} = 5 V, I_{out} = 0.9 A, f_{chop} = 100 kHz Mixed Decay Mode	—	—	100	mA
Charge Pump Rise Time	t_{ONG}	19	Ccp1 = 0.47 μF, Ccp2 = 0.02 μF, V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = L → H	—	1	2	ms

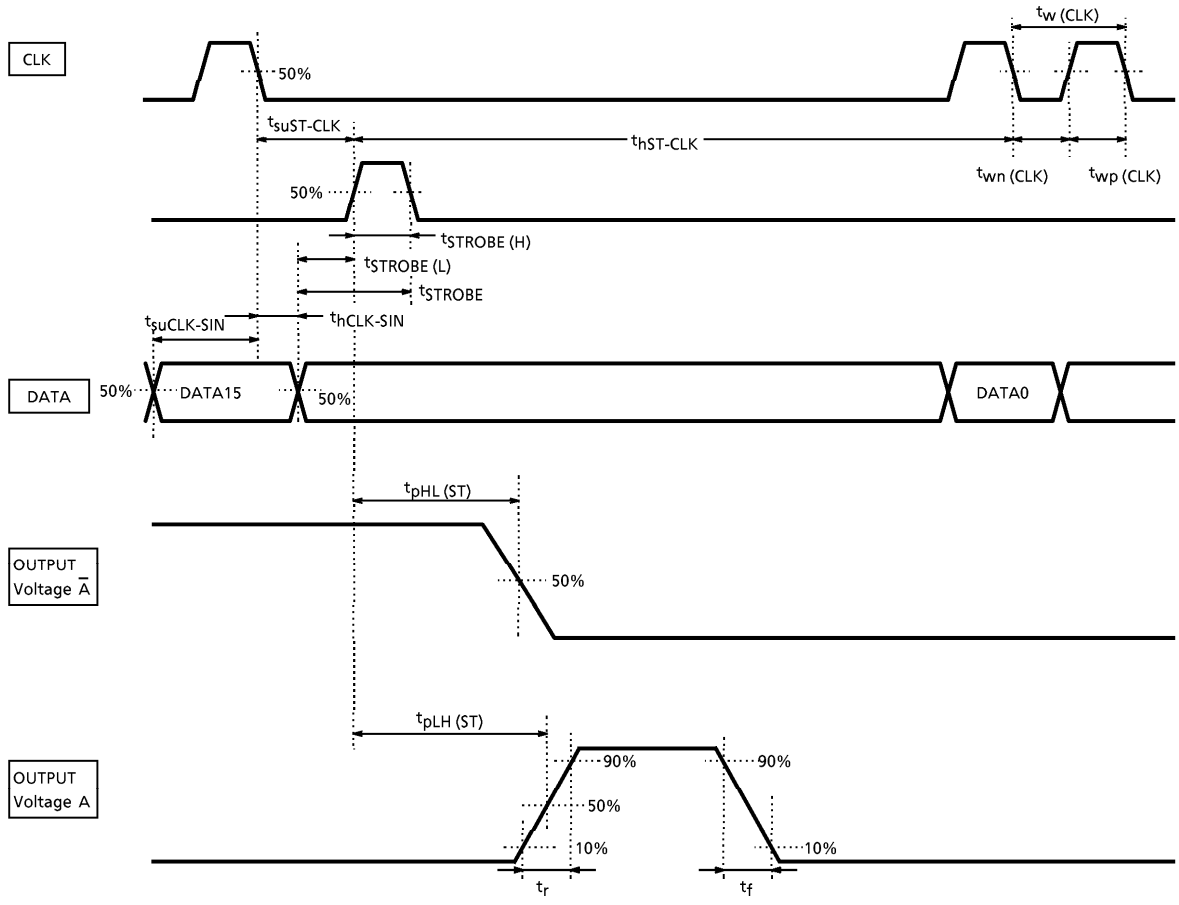


Figure 1 Test Waveforms (Timing Waveforms and Names)

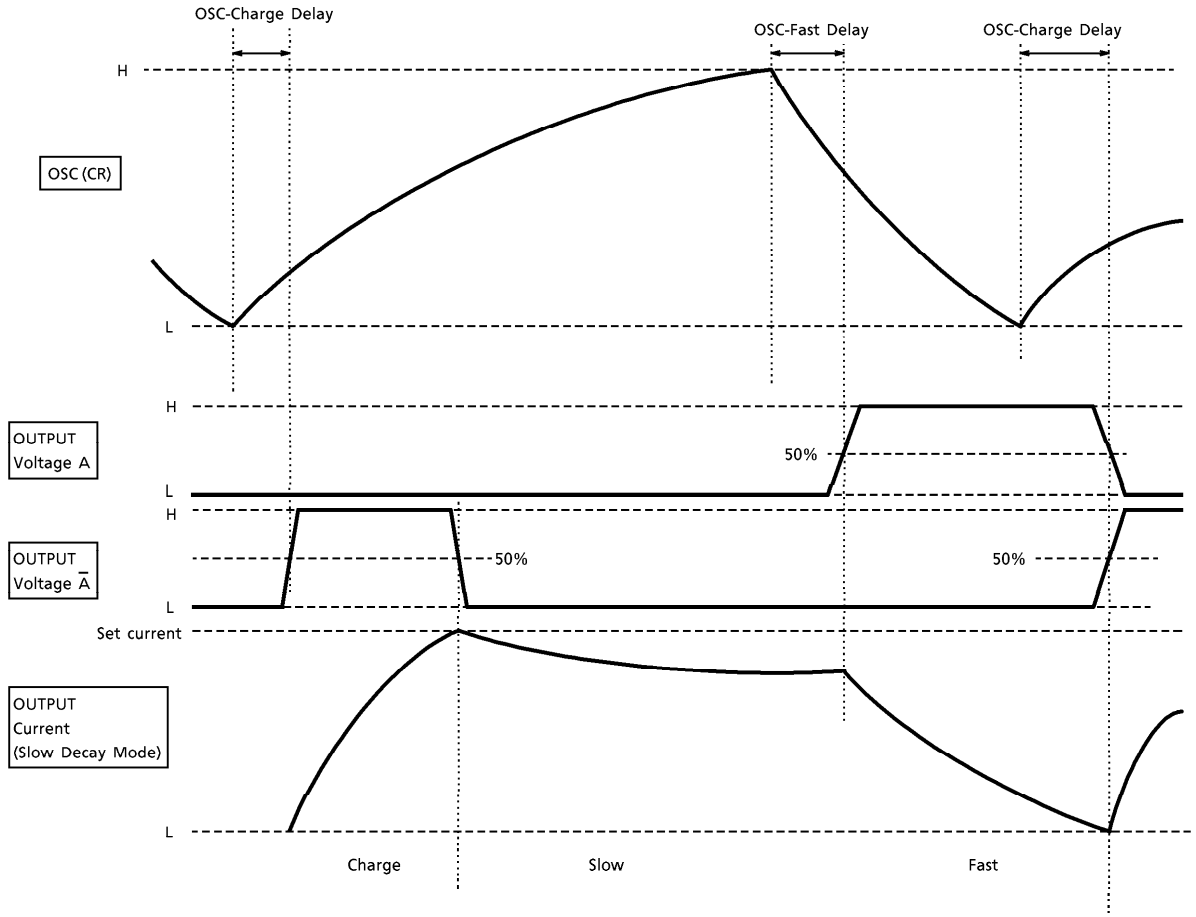
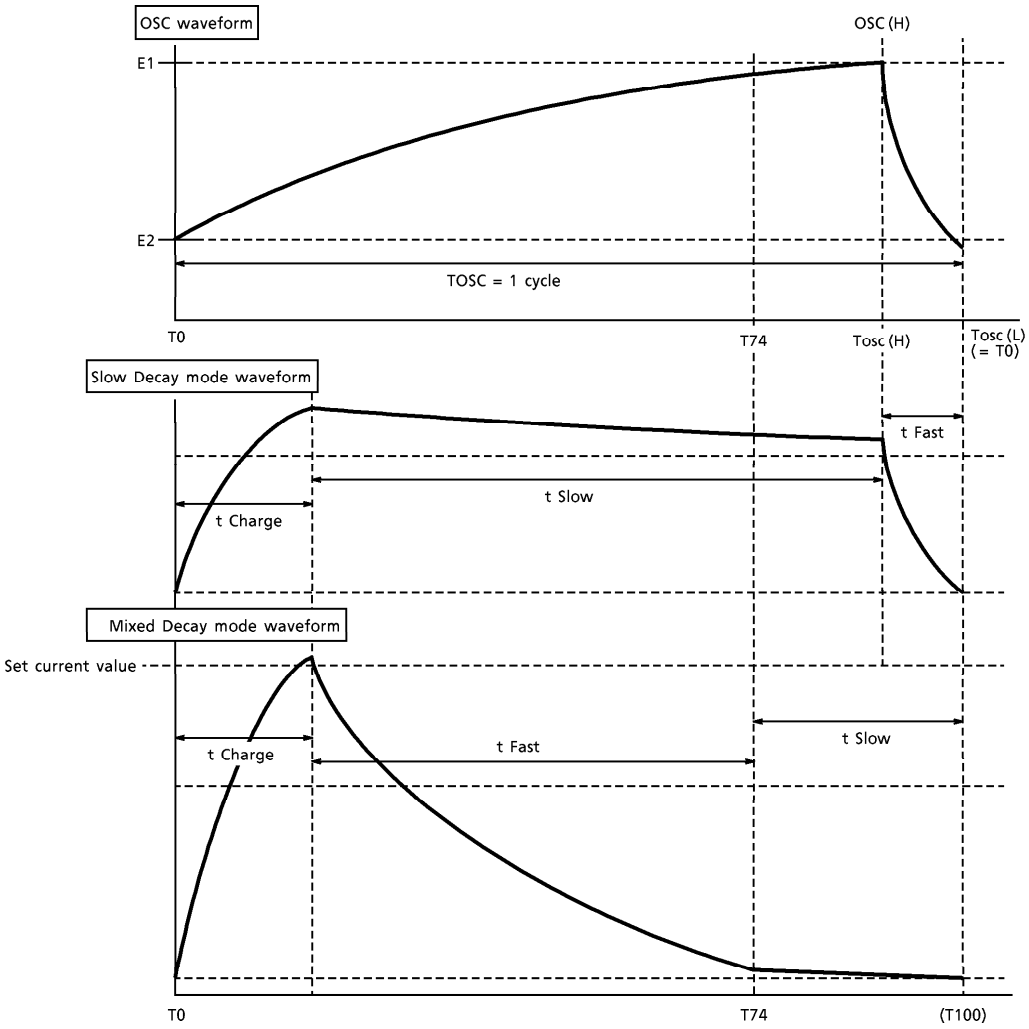


Figure 2 Test Waveforms (Timing Waveforms and Names)

OSC waveforms and output waveform timings

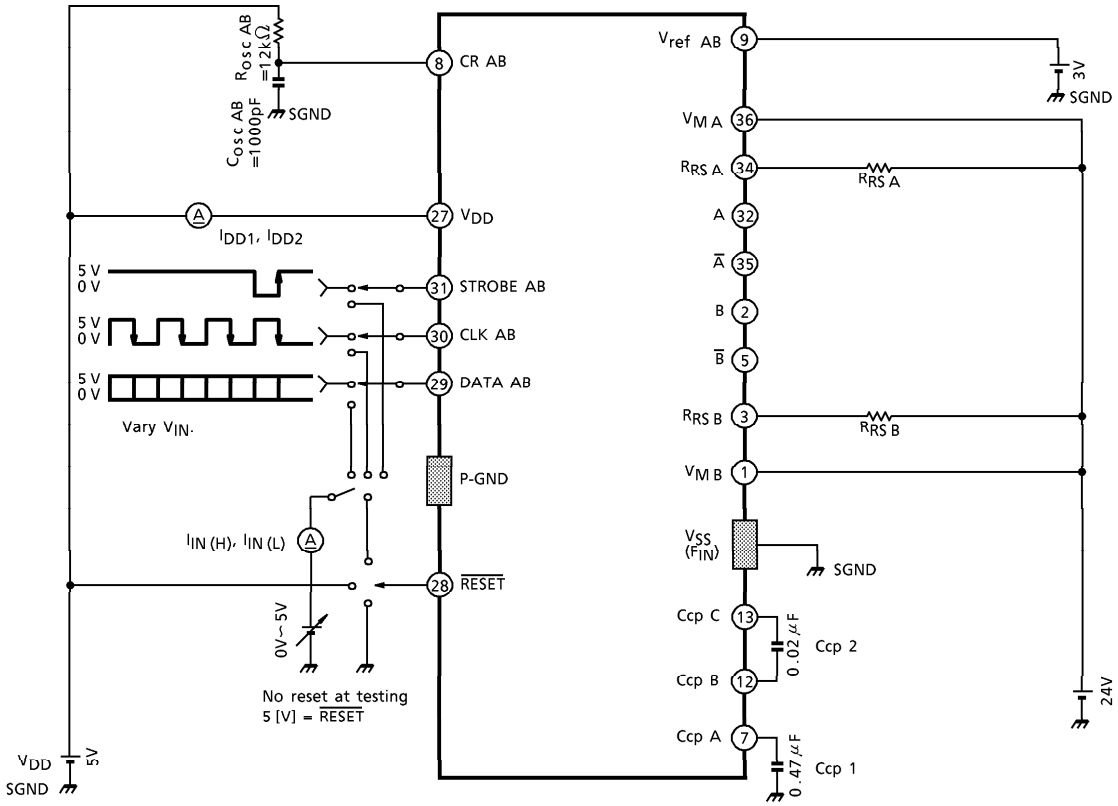


Slow Decay Mode : Mode changes from Charge → Slow → Fast.
In Charge mode, output starts. In Slow mode, output gradually attenuates.
In Fast mode, current is attenuated, dropping output instantly.
The output fall time is determined by the OSC signal fall time.
In Slow Decay mode, the advantage is that current ripple is small but attenuation capability is low. The mode is used to increase current (sine wave 0° to 90°) or to stabilize current (stabilize motor rotor).

Mixed Decay Mode : Mode changes from Charge → Fast → Slow.
Mode changes from Fast to Slow at 40% or 74% of the OSC cycle.
In Mixed Decay mode, current ripple is large but attenuation capability is high. The mode is used to attenuate current (sine wave 90° to 180°) or when current is unstable in Slow Decay mode.

TEST CIRCUIT (A / B unit only. C / D unit conforms to A / B unit.)

1. $V_{IN\,(H)}$, $V_{IN\,(L)}$, $I_{IN\,(H)}$, $I_{IN\,(L)}$, I_{DD1}, I_{DD2}



Test method

$V_{IN\,(H)}$: Set $\overline{RESET}$ to High and vary the logic input voltage from 0 to 7 V. Monitor I_{DD} and measure the change point (V_M = 24 V).

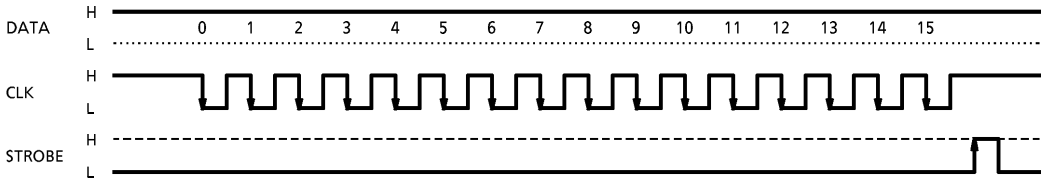
$V_{IN\,(L)}$: Set $\overline{RESET}$ to High and vary the logic input voltage from 5 to 0 V. Monitor I_{DD} and measure the change point.

$I_{IN\,(H)}$: Set $\overline{RESET}$ to High, set the the logic input voltage to 5 V, and measure the input current.

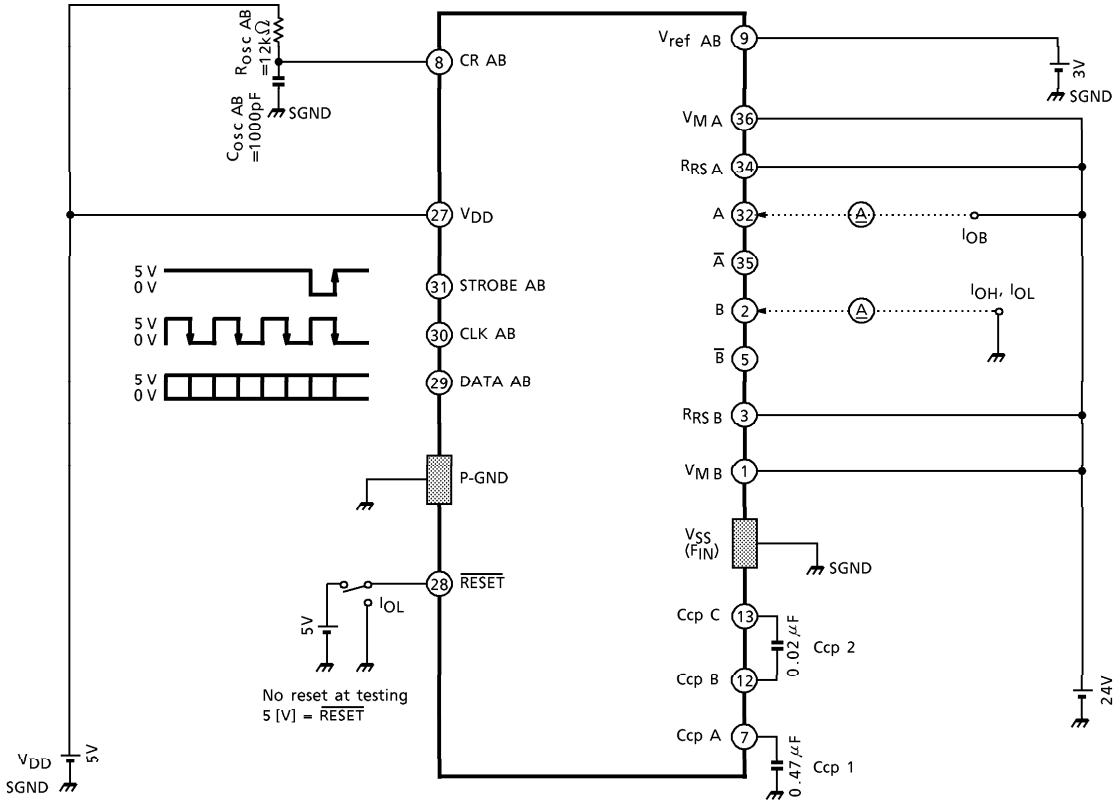
I_{DD1} : Apply V_{DD}, input $\overline{RESET}$, and measure I_{DD}.

I_{DD2} : Input 6.25 MHz clock and measure the current when the logic is operating. Set output to OPEN.

Setup data



2. I_{OB}, I_{OH}, I_{OL} (A / B unit only. C / D unit conforms to A / B unit.)



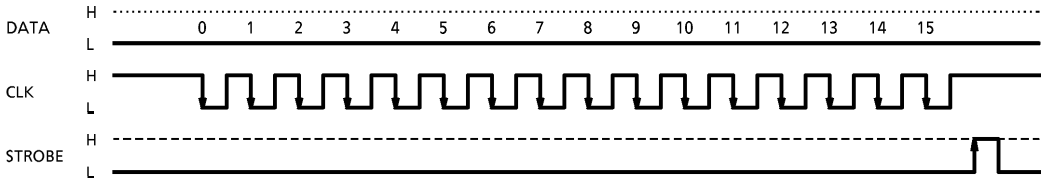
Test method

I_{OH} : With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = H, connect the output pins to GND, and measure the supply current.

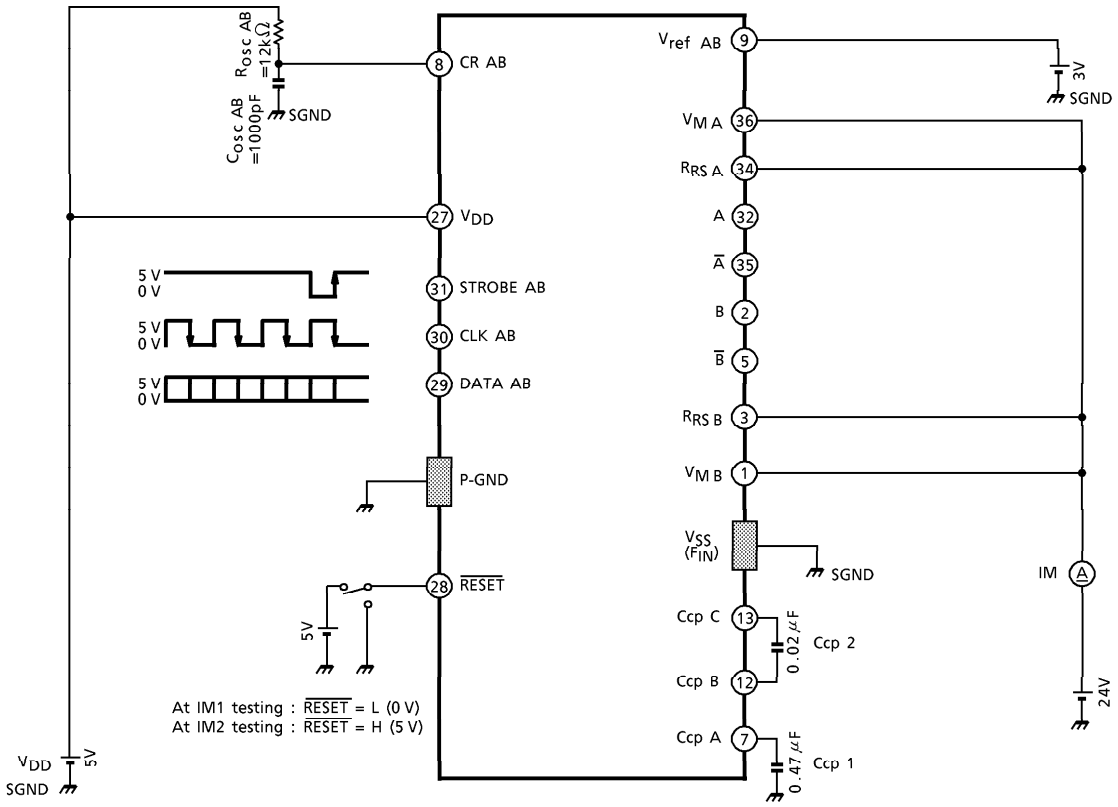
I_{OB} : With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = H, connect the output pins to V_M, and measure the supply current.

I_{OL} : With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = L, connect the output pins to GND, and measure the supply current.

Setup data



3. IM1, IM2 (A / B unit only. C / D unit conforms to A / B unit.)

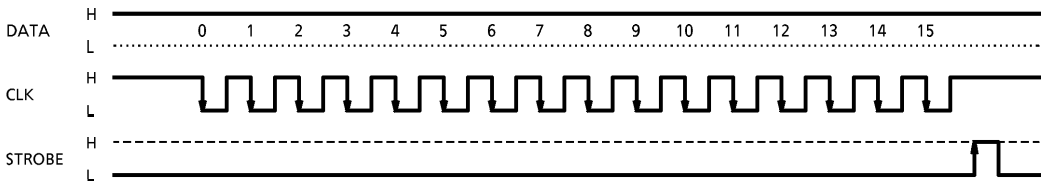


Test method

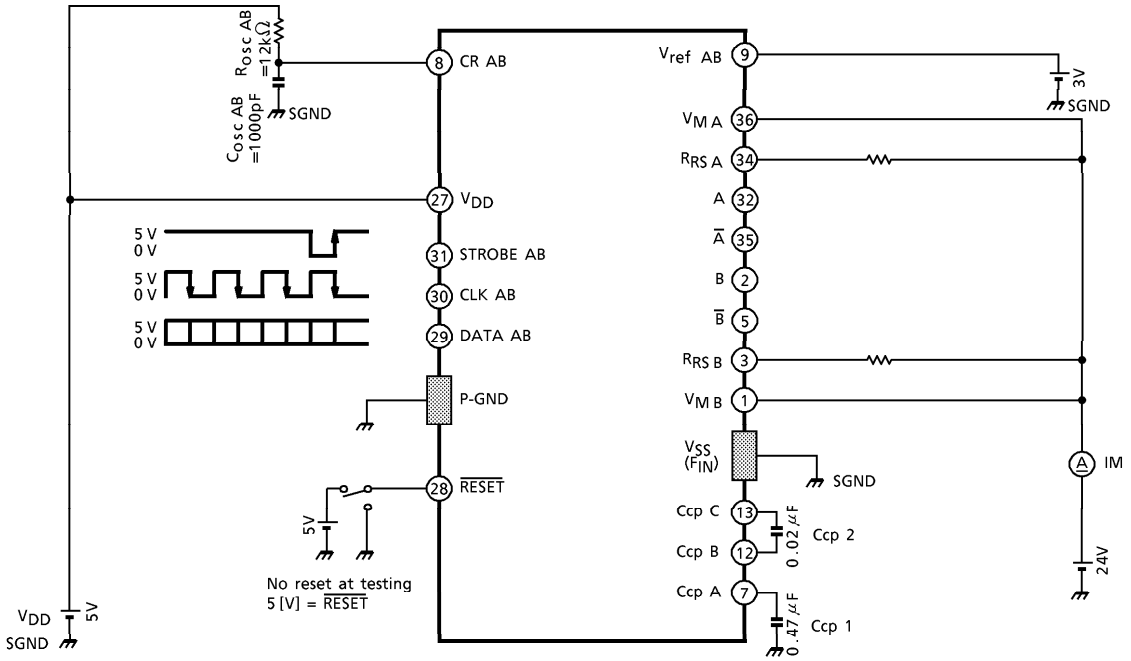
IM1 : Set the logic block to non-active (DATA = all 0), V_{DD} = 5 V, V_M = 24 V, and output to open. Measure the current input from V_M supply. $\overline{RESET}$ = L

IM2 : Set the logic block only to active (CLK = 6.25 MHz), V_M = 24 V, and output to open. Measure the current input from V_M supply. $\overline{RESET}$ = H

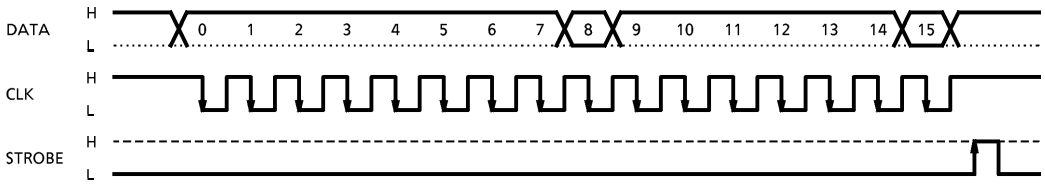
Setup data



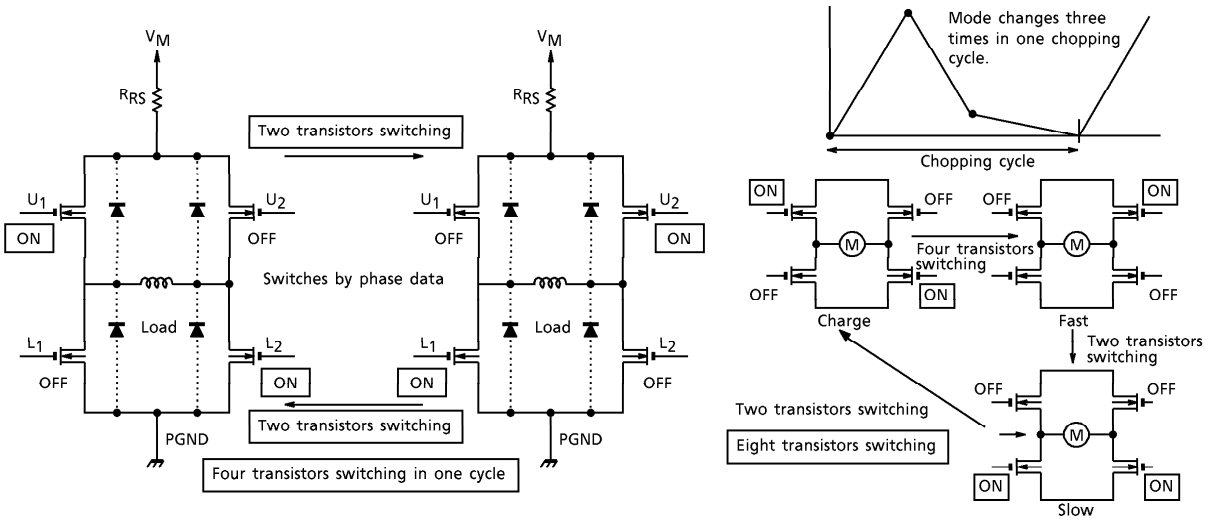
4. IM3 (A / B unit only. C / D unit conforms to A / B unit.)



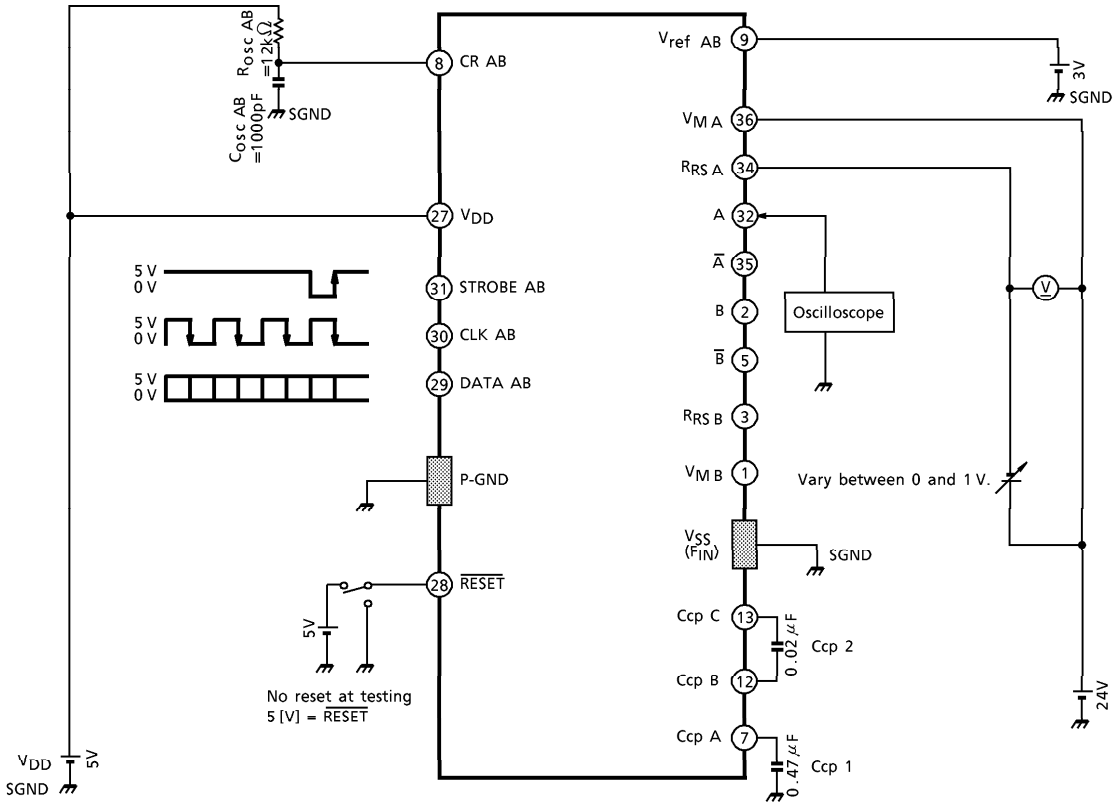
Setup data



Test method : Set output to open, change phase data from 1 → 0 → 1 → 0 and perform switching. When testing, input phase data at double the chopping frequency (if f_{chop} = 100 kHz, fDATA = 200 kHz) and measure the current value of V_M supply.



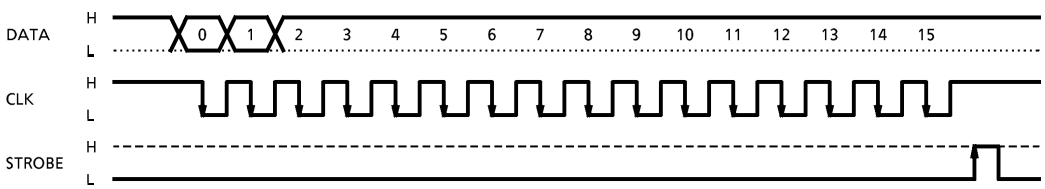
5. $V_{RS\,(H\sim L)}$, V_{ref} (GAIN) (when measuring phase A) after measurement (A / B unit only. C / D unit conforms to A / B unit.)



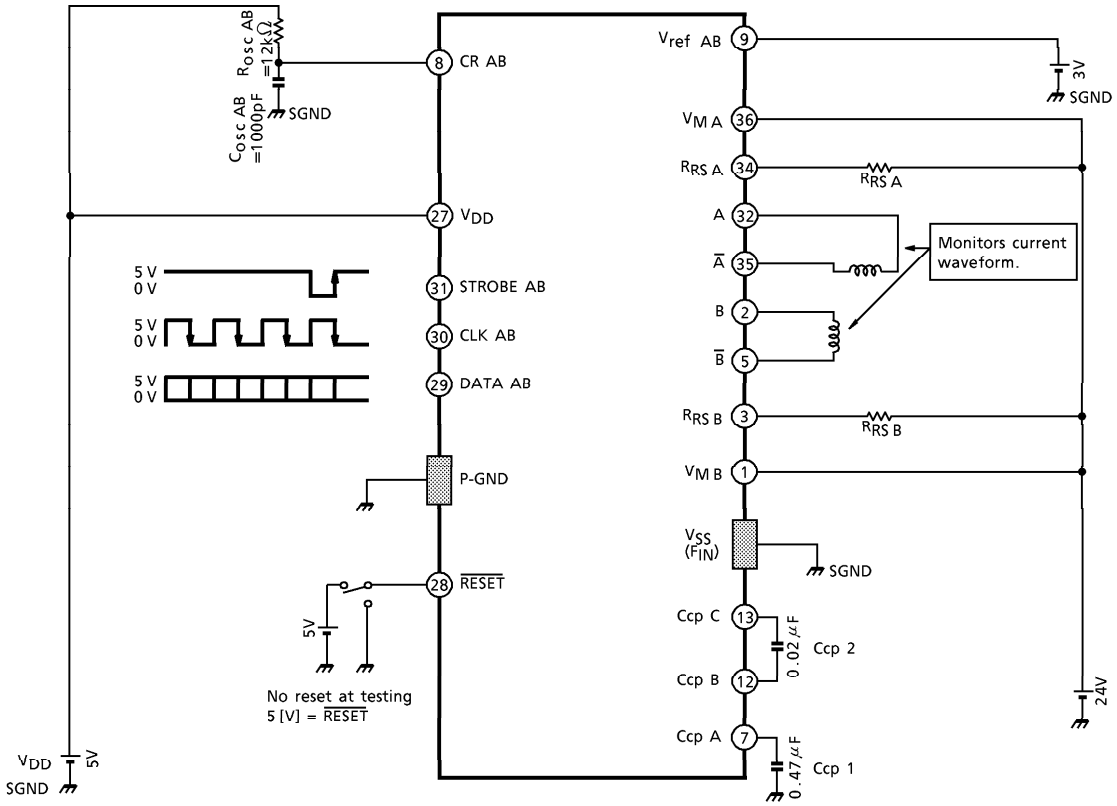
$V_{RS\,(H\sim L)}$: Input torque data = 100% (HH) and vary the voltage between V_M and R_S pins. Measure the voltage (V_{RS}) when output changes from fixed Charge mode to another mode.
Also measure V_{RS} when torque data = 85% (HL), 70% (LH), or 50% (LL) as above and calculate the ratio using V_{RS} value at 100% as reference.

$V_{ref\,(GAIN)}$: $V_{ref\,(GAIN)} = \dfrac{V_{RS\,(*)}}{V_{ref}}$ (*V_{RS} : when torque data = 100%)

Setup data

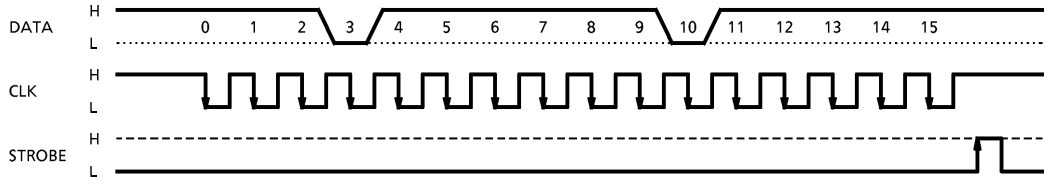


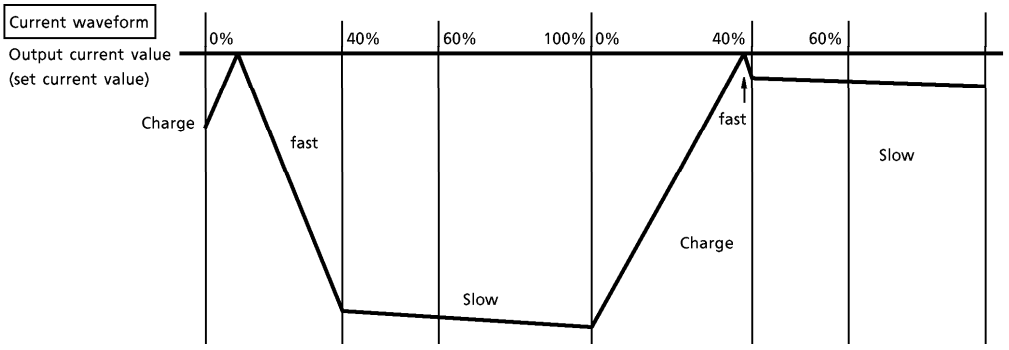
6. ΔI_{out1}, ΔI_{out2} (A / B unit only. C / D unit conforms to A / B unit.)



With L load, perform chopping in Mixed Decay mode. Monitor the output current waveform and measure the various output currents at constant current (@0.9 A) operation.

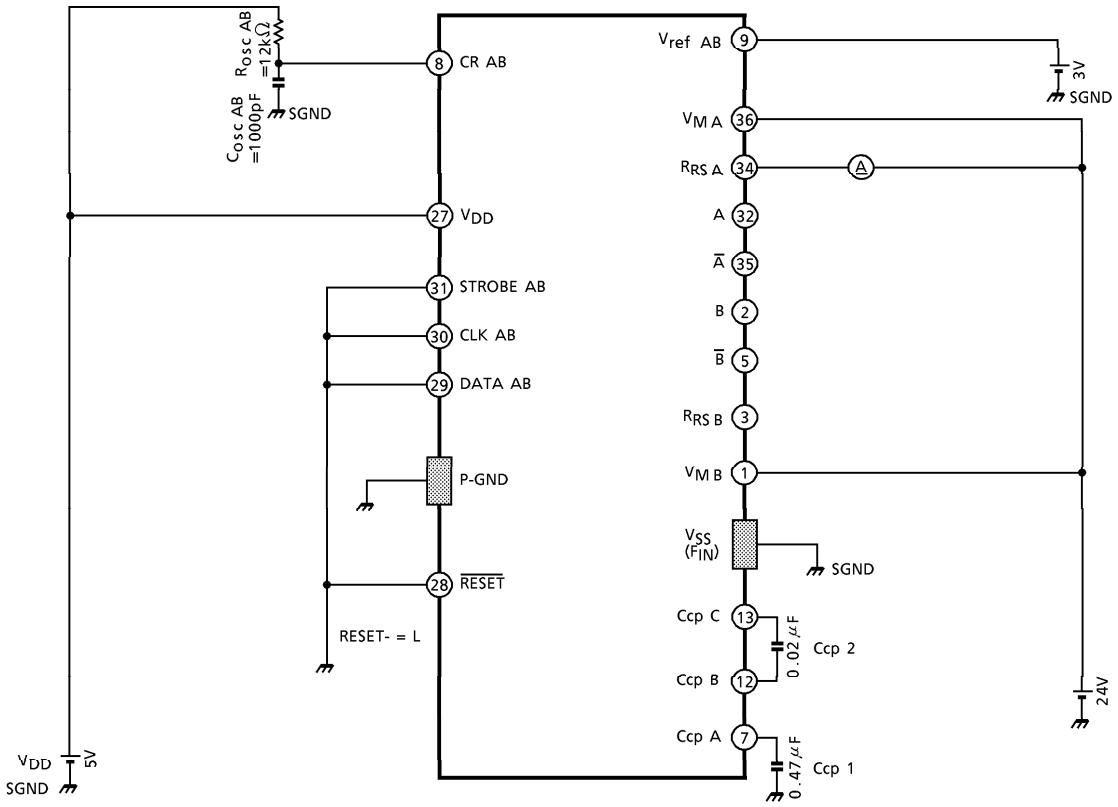
Setup data





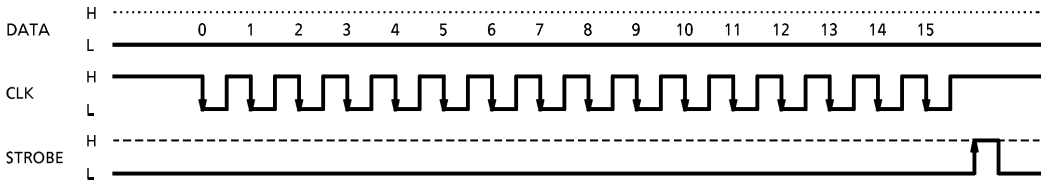
7. IRS (A unit only. B / C / D unit conforms to A unit.)

When measuring phase A

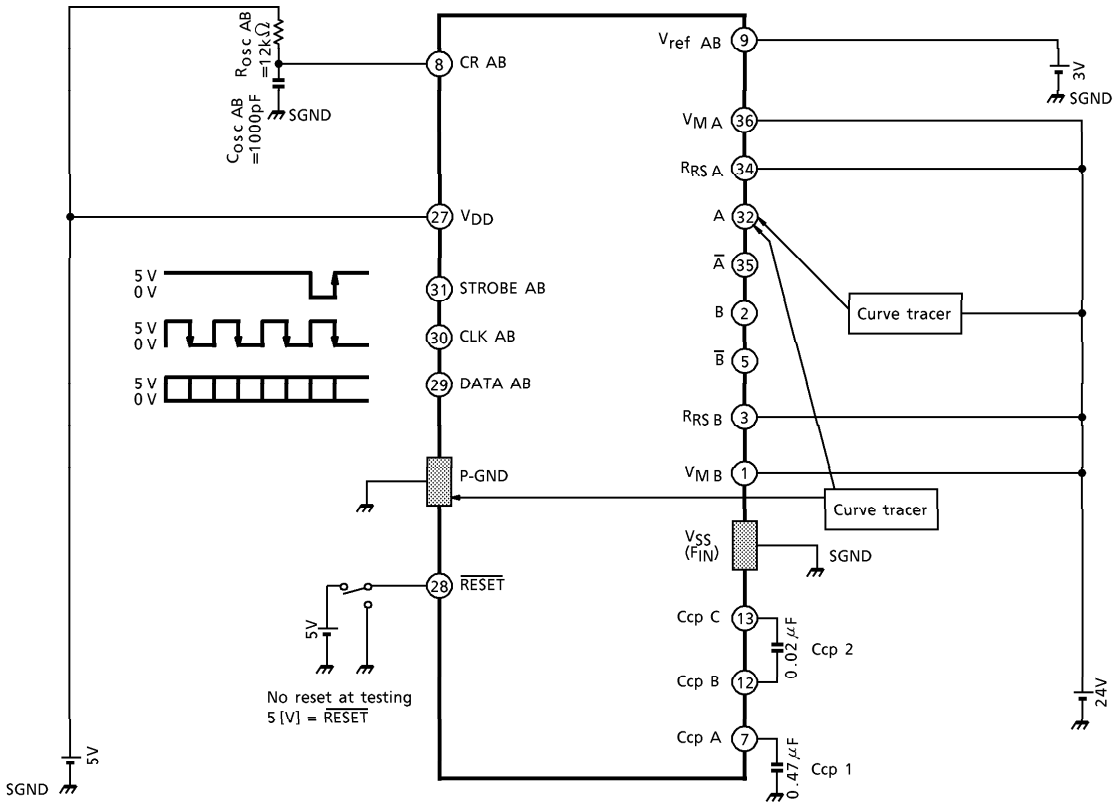


With L input to $\overline{\text{RESET}}$, connect V_M and R_{RS} to the power supply, and measure the current input to the R_S pin. (Either drop all the input pins to GND level or input all Low data to the DATA pin, then perform measurement. At that time, leave all other output pins open.)

Setup data

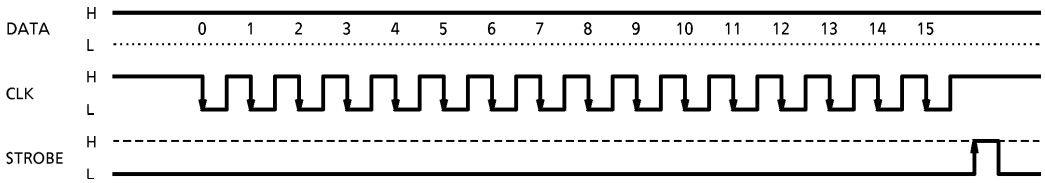


8. $R_{ON\,(D\text{-}S)}$, $R_{ON\,(S\text{-}D)}$ when measuring output A (A unit only. B / C / D unit conforms to A unit.)

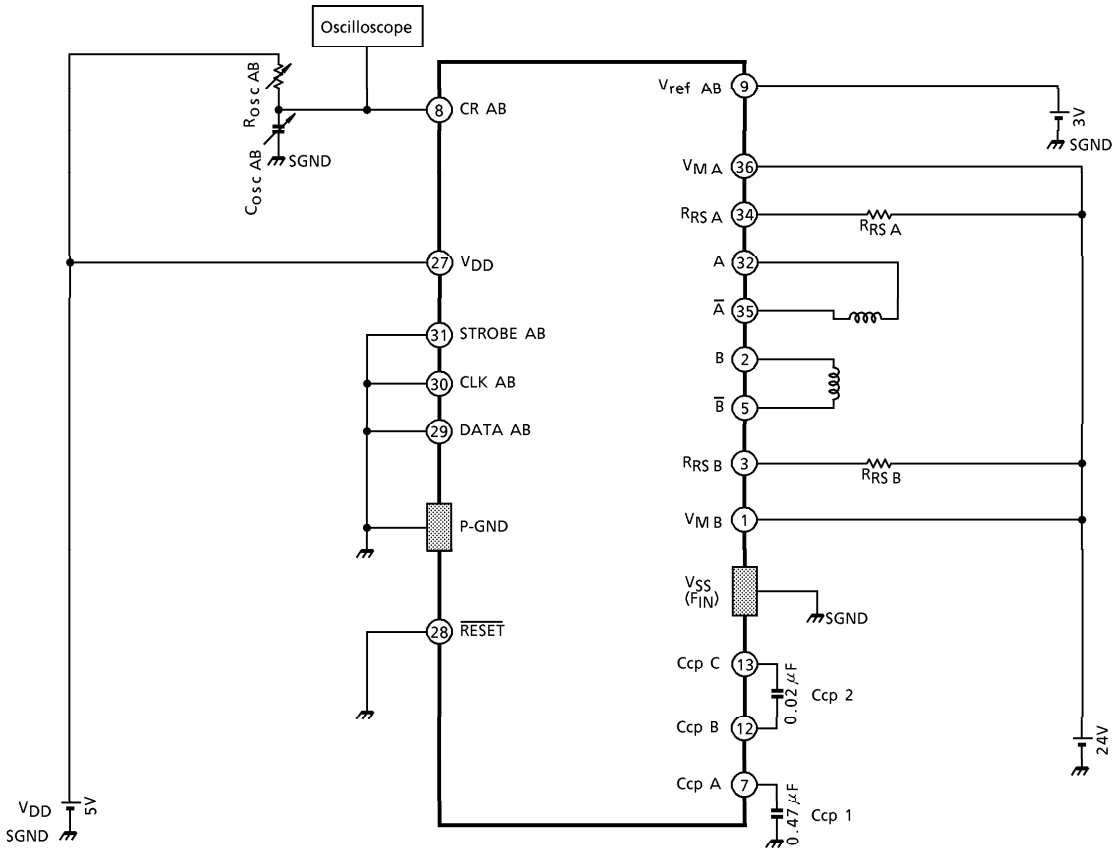


Input the current setting data (HHHH signal) to the DATA pin and measure the voltage between V_M and OUT when I_{OUT} = 1000 mA or the voltage between OUT and GND. Then, change the phase and repeat measurement. At that time, leave the output pins which are not measured open.

Setup data (Vary the phase data during testing.)

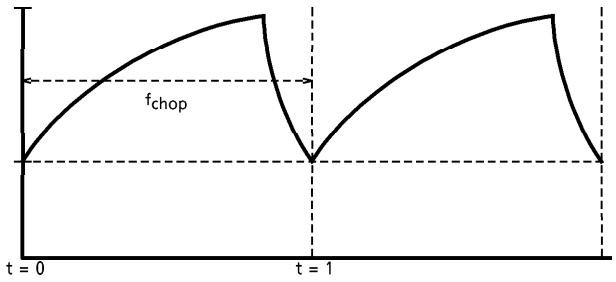


9. f_{chop} (f_{chop} (Min), f_{chop} (Max)) (A / B unit only. C / D unit conforms to A / B unit.)

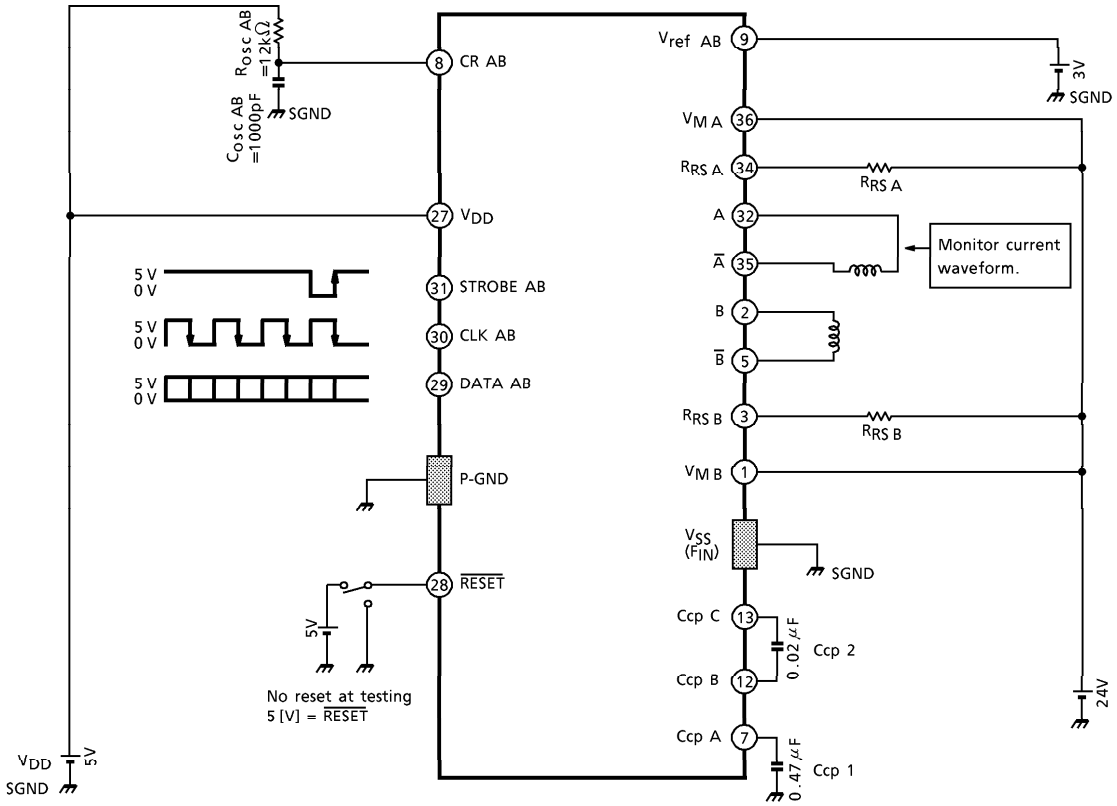


Change the R_{osc} and C_{osc} values and measure the frequency on the CR pin using the oscilloscope.

Oscilloscope waveform (example)

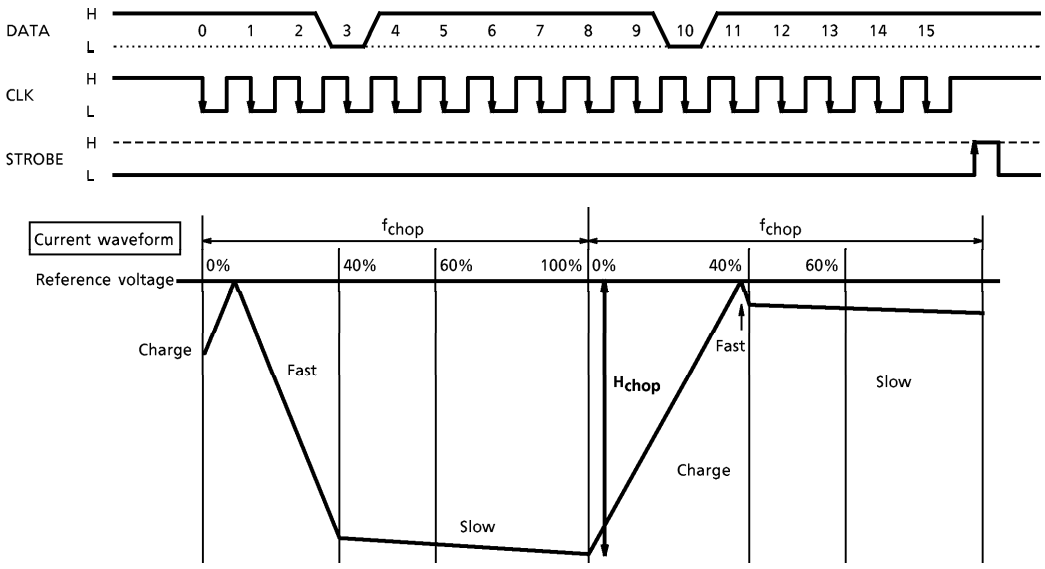


10. H_{chop} (Triangular wave high value) (A / B unit only. C / D unit conforms to A / B unit.)

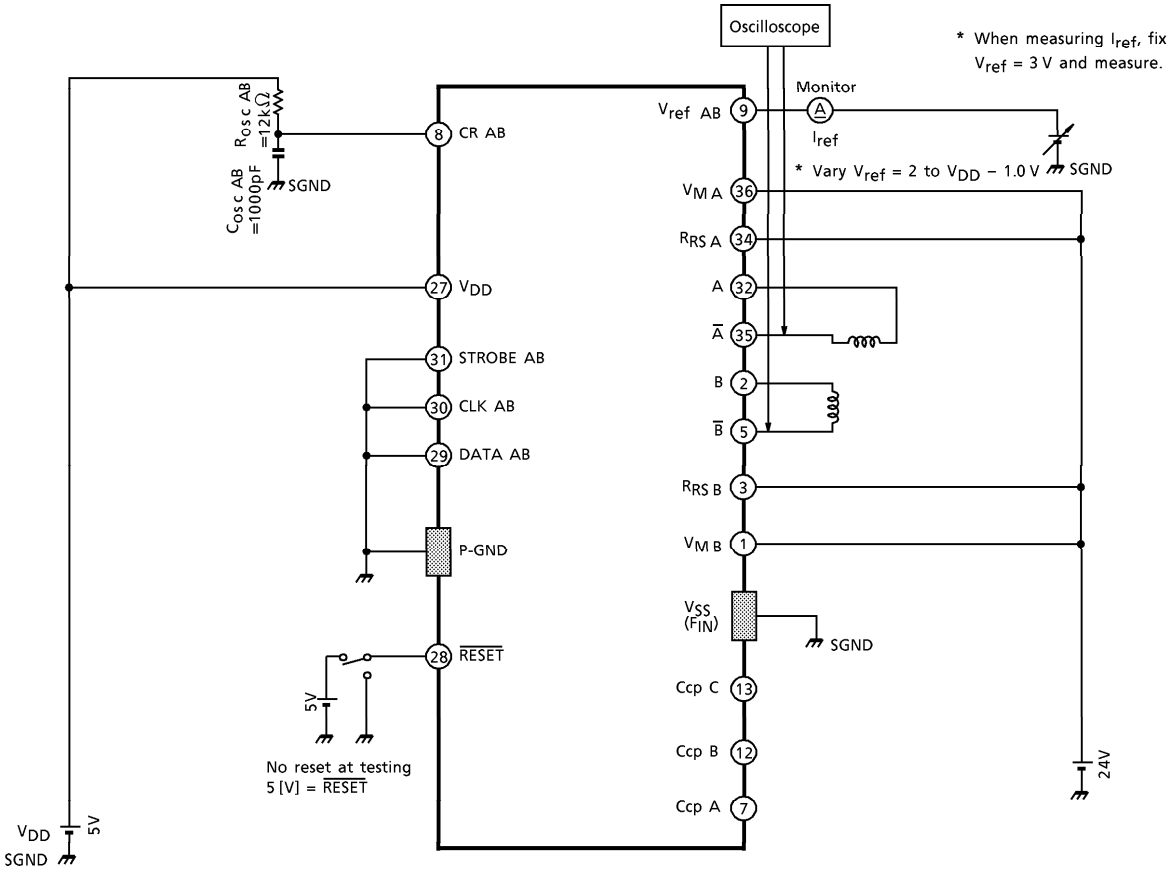


With L load, perform chopping in Mixed Decay mode. Monitor the output current waveform and measure the current ripple width (H_{chop}) at constant current (@0.9 A) operation. Input I_{out} = 0.9 A.

Setup data



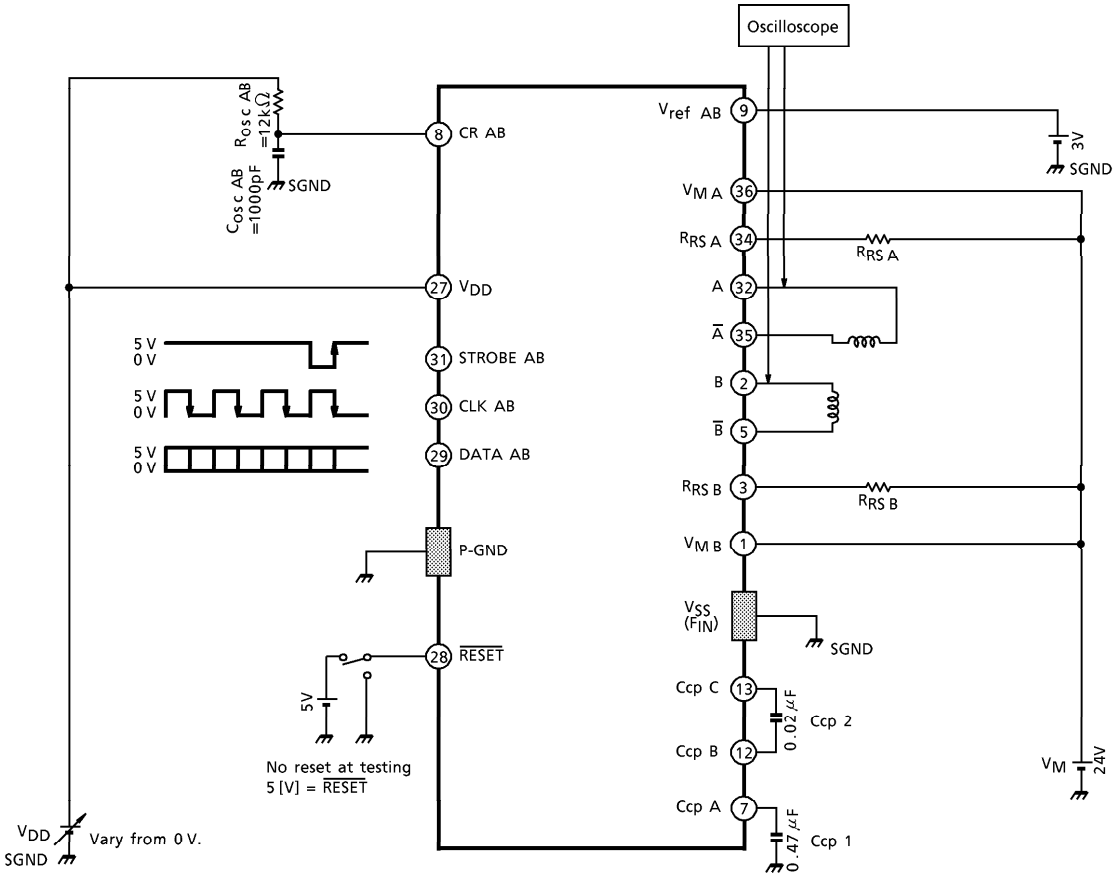
11. V_{ref}, I_{ref} (A / B unit only. C / D unit conforms to A / B unit.)



V_{ref} : Vary V_{ref} = 2 to V_{DD} − 1.0 V and confirm that output is on.

I_{ref} : When V_M = 24 V and V_{DD} = 5 V, apply the specified voltage of 3 V to the V_{ref} and monitor the current flow value.

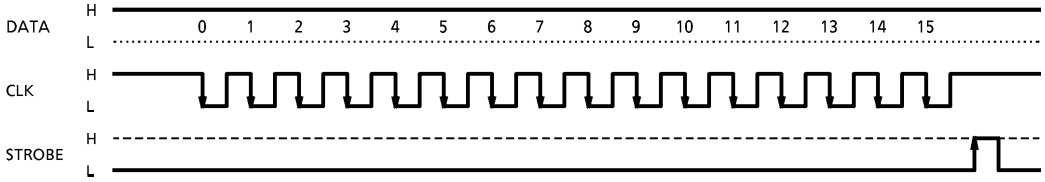
12. V_{DDR} (A / B unit only. C / D unit conforms to A / B unit.)



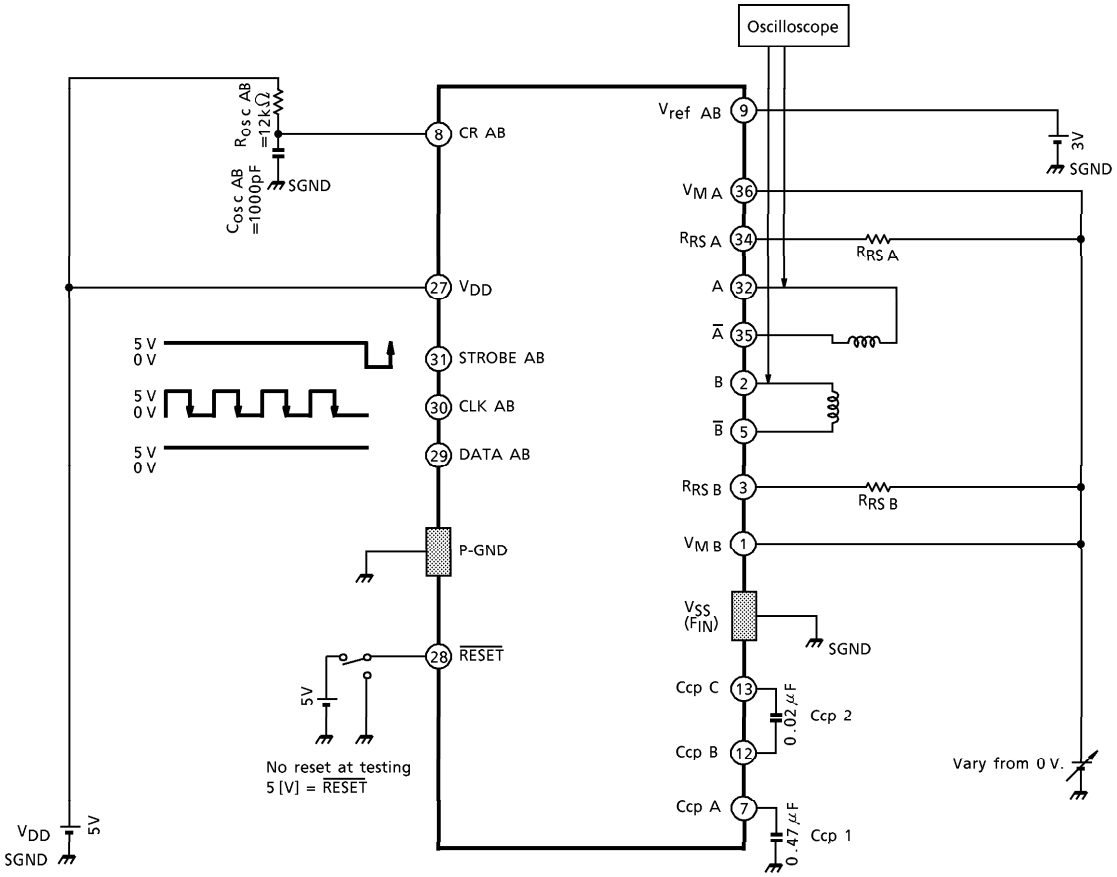
Monitor the output pins. Increase the V_{DD} voltage from 0. Measure the V_{DD} value when output starts.

Next, decrease the V_{DD} voltage and measure the V_{DD} value when output stops.

Setup data

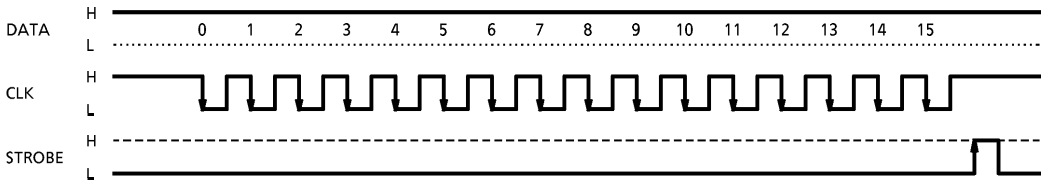


13. V_{MR} (A / B unit only. C / D unit conforms to A / B unit.)

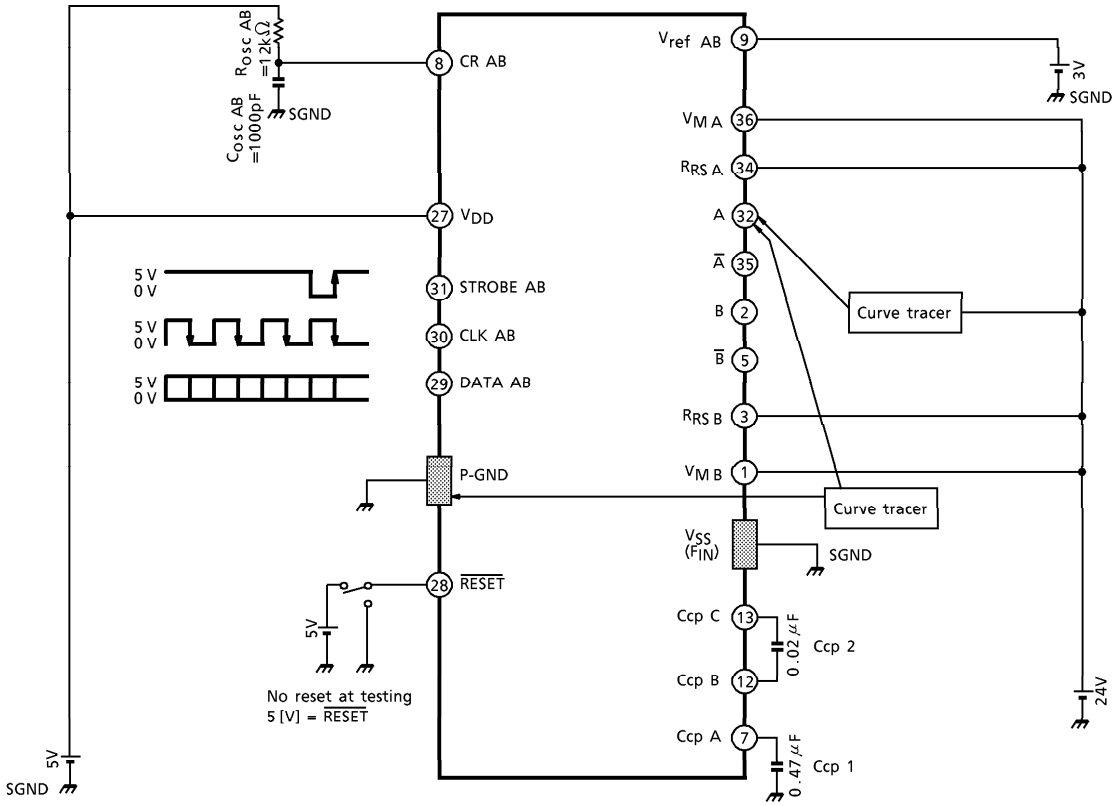


With the CLK signal and DATA (all High) input, increase the V_M voltage from 0.
Measure the V_M value when output starts.
Next, decrease the V_M voltage and measure the V_M value when output stops.

Setup data



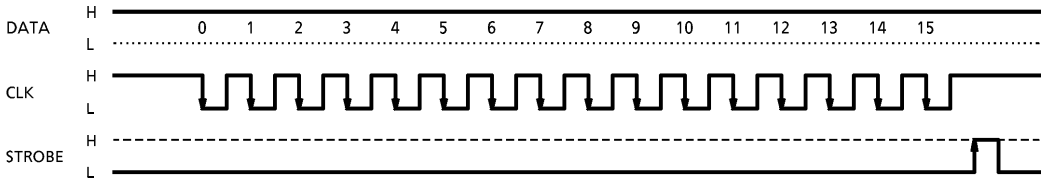
14. T_jTSD, ΔT_jTSD (Measure in an environment such as an constant temperature chamber where the temperature for the IC can be freely changed) (A / B unit only. C / D unit conforms to A / B unit.)



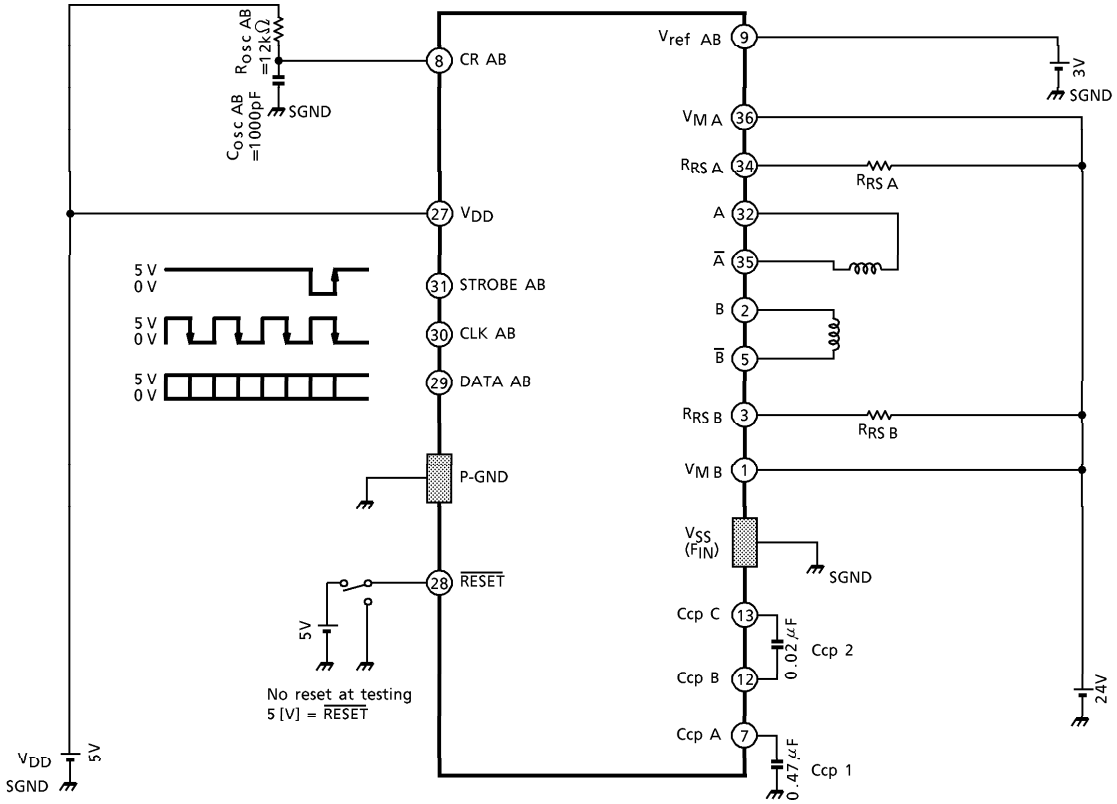
T_jTSD : Increase the ambient temperature. Measure the temperature when output stops.

ΔT_jTSD : Gradually decrease the temperature from that when the TSD circuit is turned off (output off). Measure the temperature when output restarts.

Setup data (Vary the phase data during testing.)

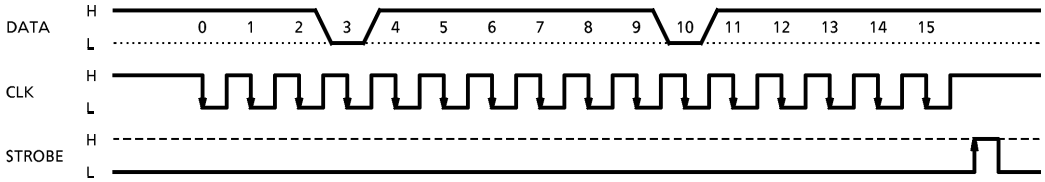


15. f_{CLK}, $t_{w\,(CLK)}$, $t_{wp\,(CLK)}$, $t_{wn\,(CLK)}$, t_{STROBE}, $t_{STROBE\,(H)}$, $t_{STOBE\,(L)}$, $t_{suCLK\text{-}SIN}$, $t_{suST\text{-}CLK}$, $t_{hCLK\text{-}SIN}$, $t_{hCLK\text{-}ST}$ (A / B unit only. C / D unit conforms to A / B unit.)

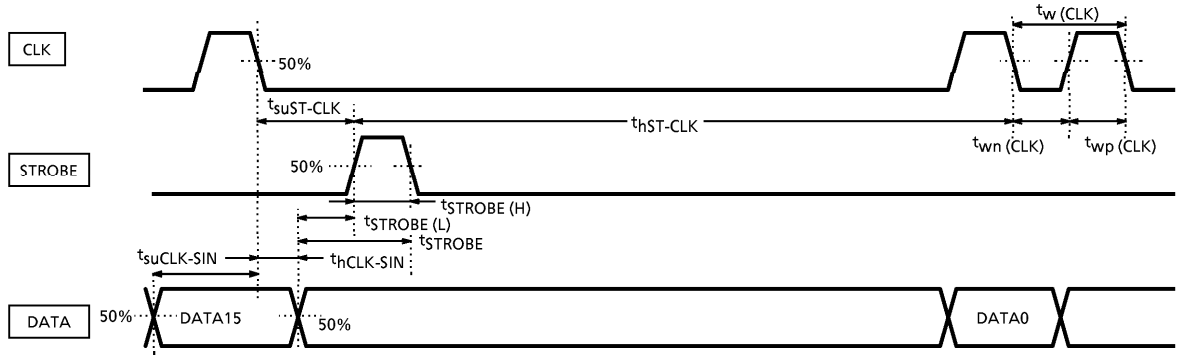


Input any data at f_{CLK} (max), perform chopping, and monitor the output waveform. For the measuring points, see the timing chart below.

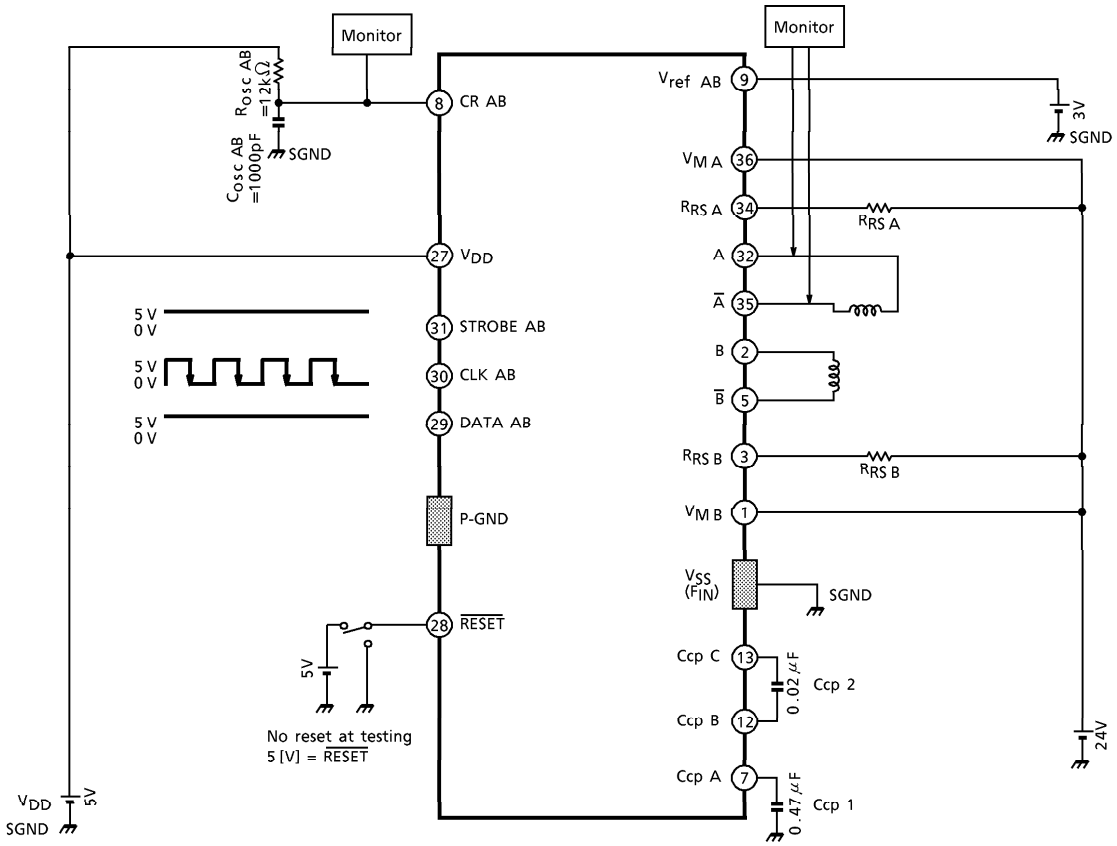
Setup data



Measuring points

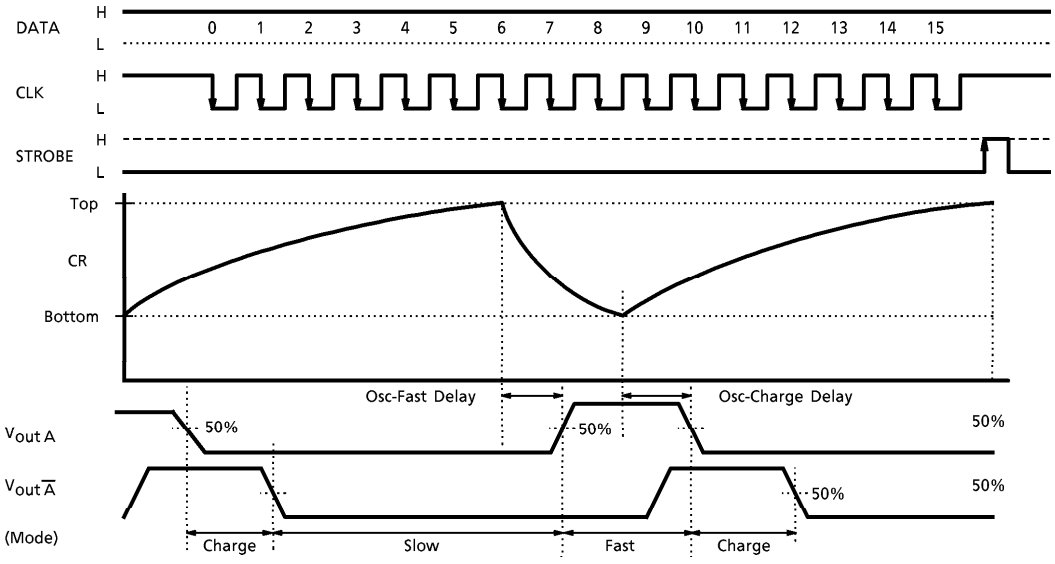


16. OSC-Fast Delay, OSC-Charge Delay (A / B unit only. C / D unit conforms to A / B unit.)

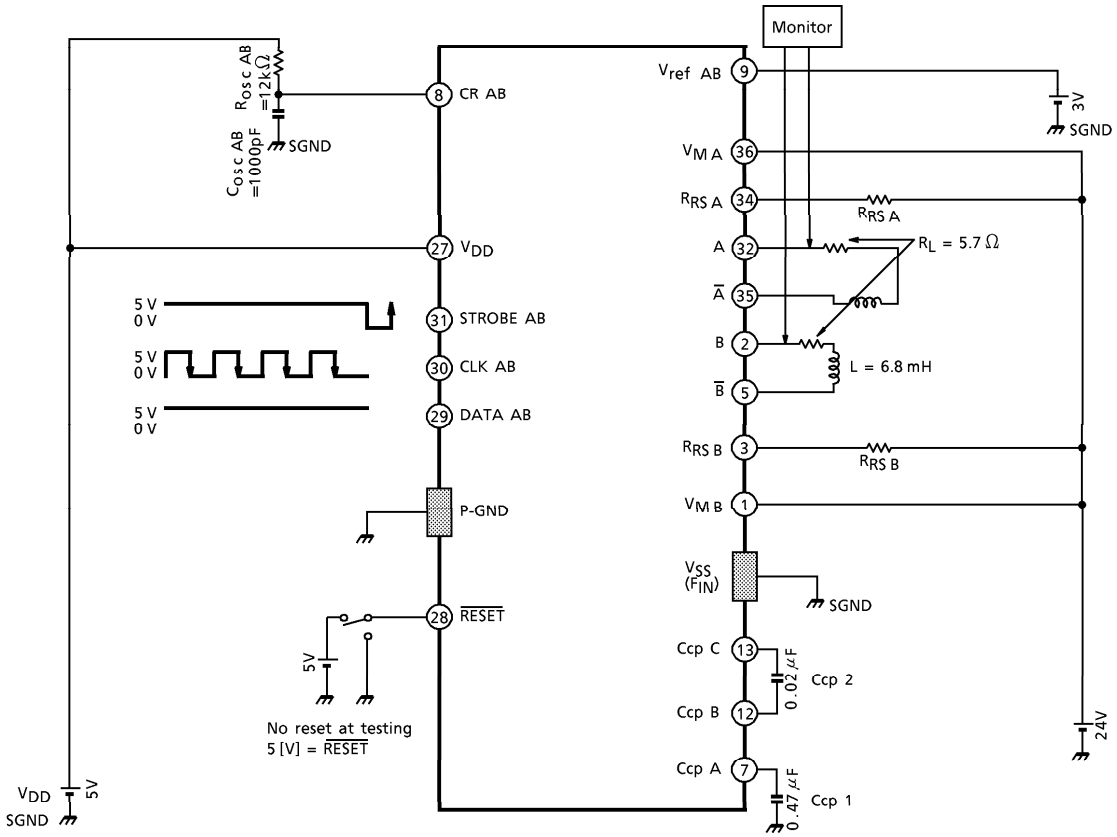


Fix the output current value in Slow Decay mode and turn the output on. Measure the time until the output switches from the CR pin waveform and the output voltage waveform.

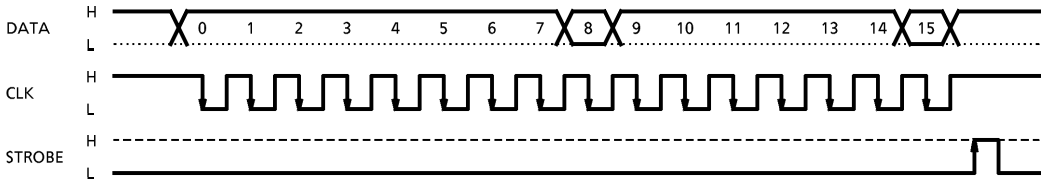
Setup data



17. $t_{pHL\,(ST)}$, $t_{pLH\,(ST)}$, t_r, t_f (A / B unit only. C / D unit conforms to A / B unit.)

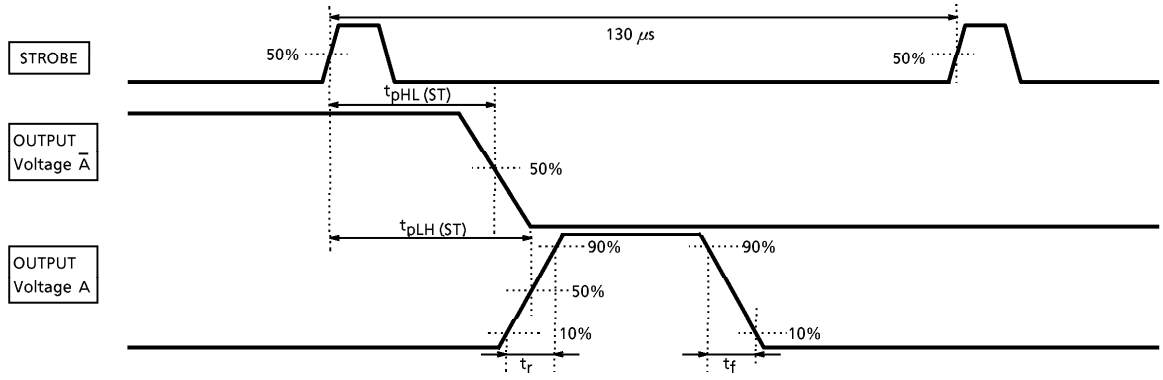


Setup data

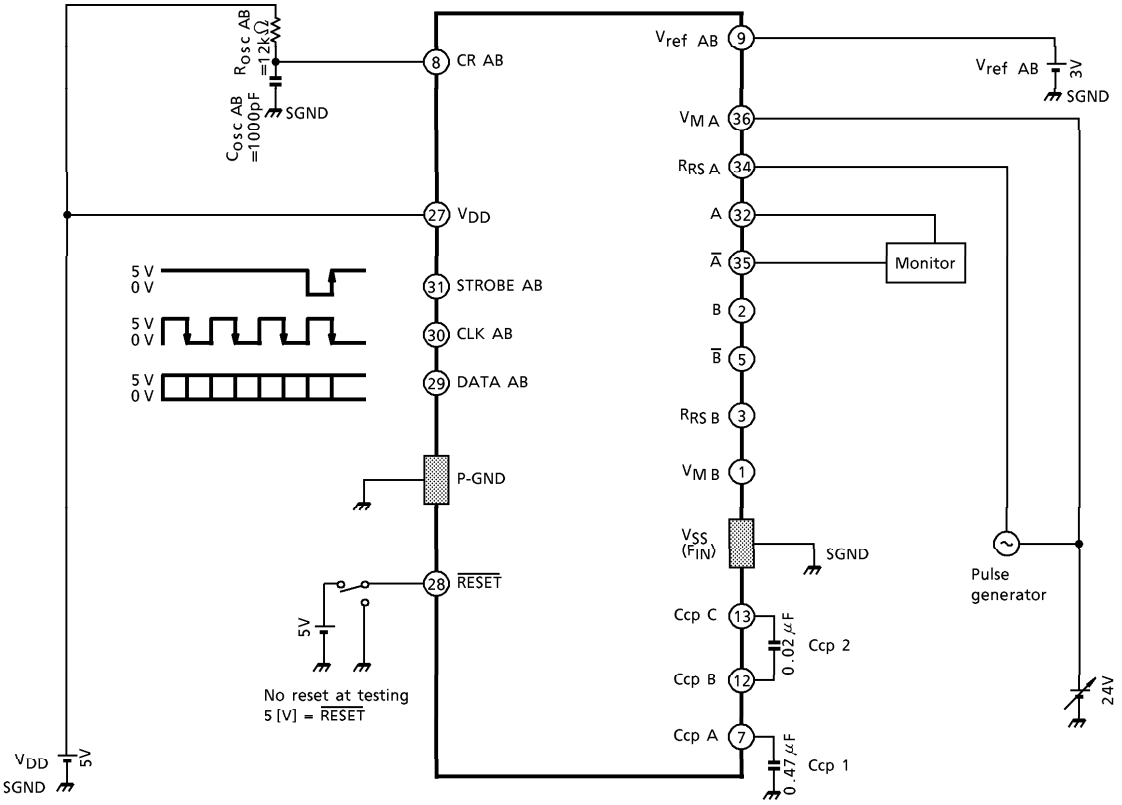


Switch PHASE every 130 μs and measure the output pin voltage and the STROBE signal.

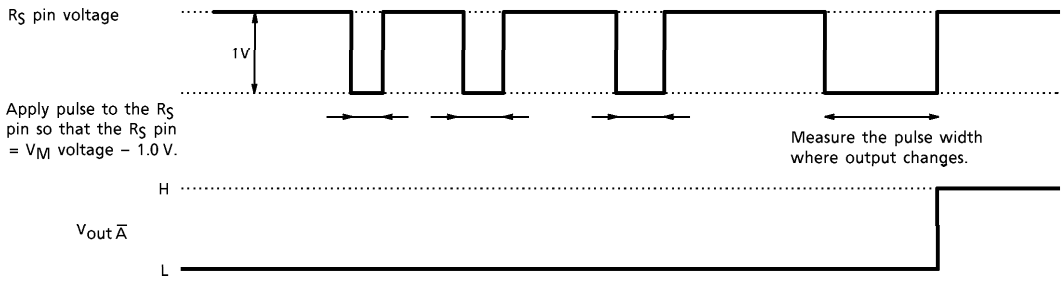
(Oscilloscope waveform (example))



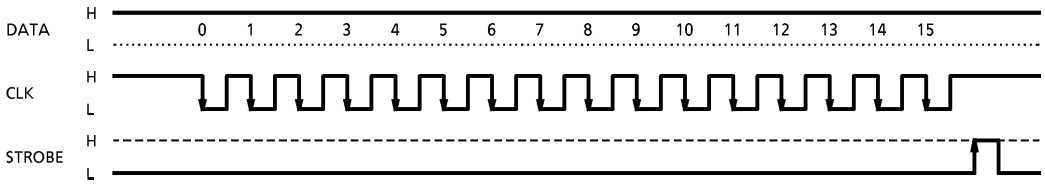
18. t_{BRANK} (A / B unit only. C / D unit conforms to A / B unit.)



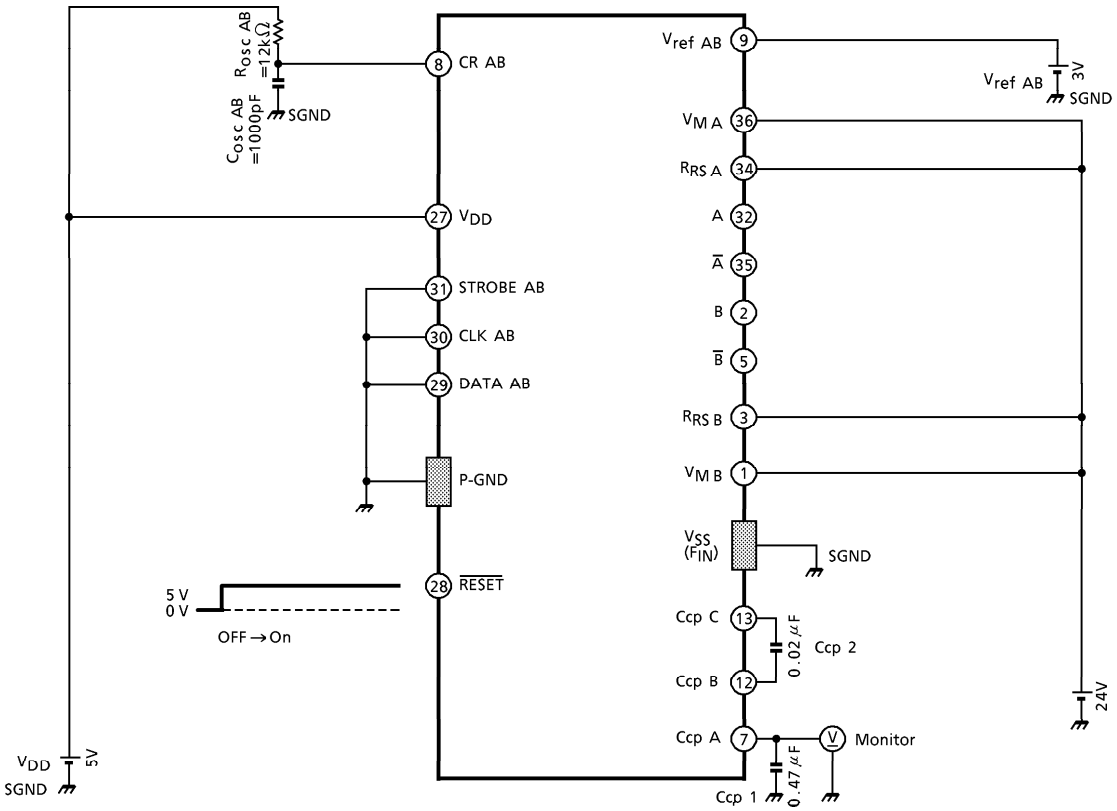
t_{BRANK} is the dead time band for avoiding malfunction caused by noise. Apply sufficient differential voltage (when V_{ref} = 3 V, 0.6 V or higher) to V_M-R_S and apply duty. When the pulse width reaches a certain value, triggering feedback and changing the output. Check the value.



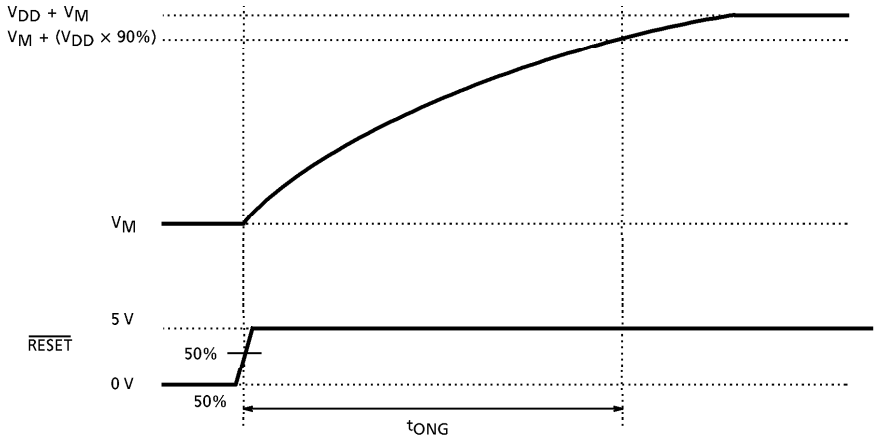
Setup data



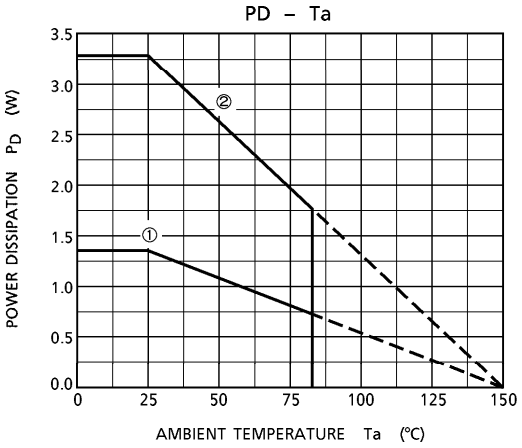
19. t_{ONG} (A / B unit only. C / D unit conforms to A / B unit.)



Apply V_M and V_{DD} and change $\overline{RESET}$ from L to H.
Measure the time until the CcpA pin becomes $V_M + V_{DD} \times 90\%$.



PD – Ta (Package power dissipation)



① $R_{th\ (j\text{-}a)}$ IC only (96°C / W)
② When mounted on the board (38.1°C / W)
Board size (90 × 230 × 1.6 mm)
※ $R_{th\ (j\text{-}c)}$: 8.5°C / W

How to calculate set current value

The set current value is calculated according to R_{RS} and V_{ref}.

$$I_{out}\ (Max) = V_{ref}\ (GAIN) \times V_{ref}\ (V) \times \frac{Torque}{(R_{RS} + R_{IC})}$$

V_{ref} (GAIN) = 1 / 5.1, R_{IC} (wiring resistance in IC) = 0.04 (Ω)

(Example)

V_{ref} = 3 (V)

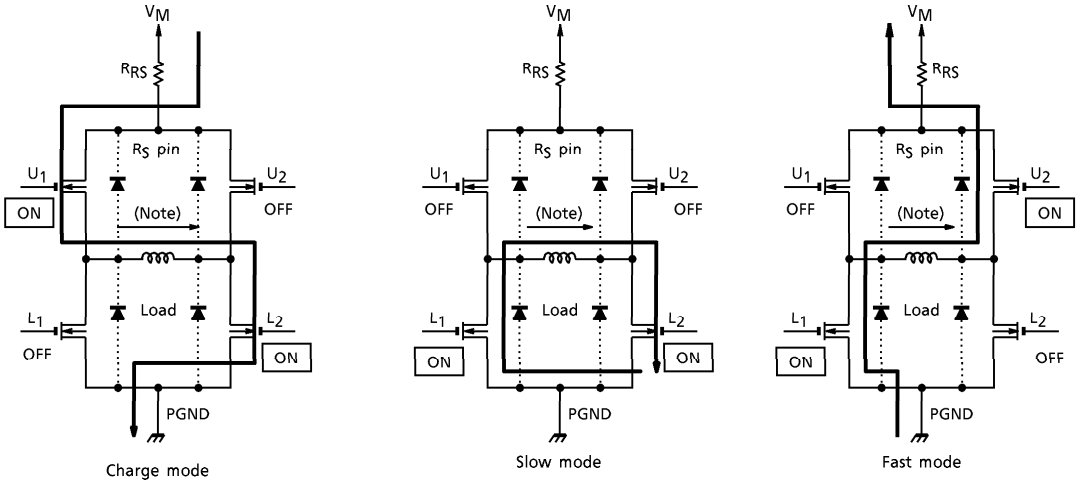
T_{orque} = 100 (%)

To output I_{out} = 0.8 (A),

$$0.8\ (A) = \frac{1}{5.1} \times 3\ (V) \times \frac{1}{R_{RS} + 0.04\ (\Omega)}$$

R_{RS} = 0.695 (Ω) (0.5 W or higher) is required.

Output transistor operating mode



(Remark) In Mixed Decay mode, mode changes from Fast to Slow at 40 or 74% of 1 f_{chop} cycle after charging is complete in Charge mode.

(Note) Although there are parasitic diodes on the dotted lines, they are not normally used in this IC.

Output transistor operation functions

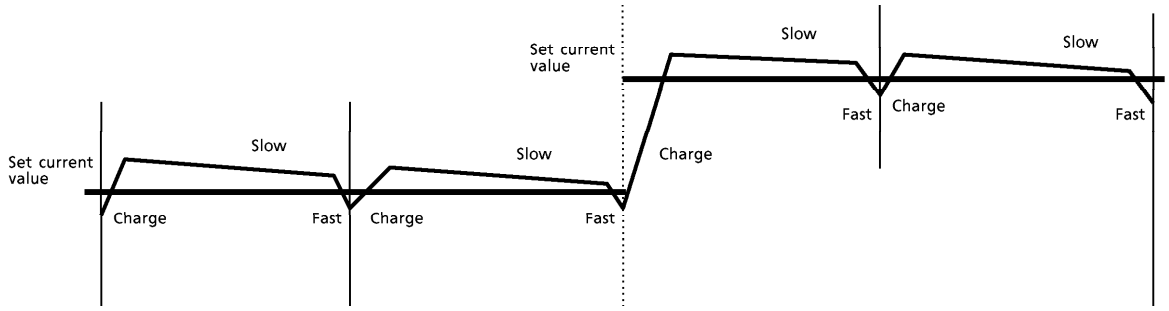
CLK	U_1	U_2	L_1	L_2
Charge	ON	OFF	OFF	ON
Slow	OFF	OFF	ON	ON
Fast	OFF	ON	ON	OFF

(Note) The above table is an example where current flows in the direction of the arrows in the above figures.
When the current flows in the opposite direction of the arrows, see the table below.

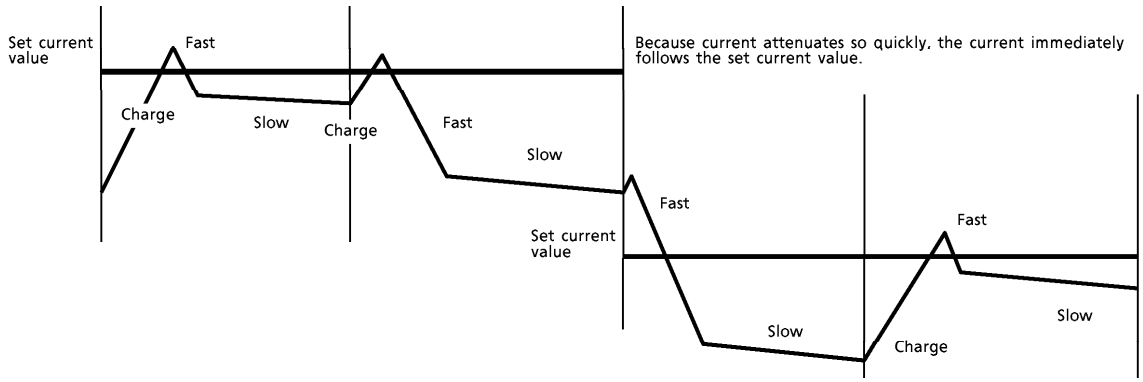
CLK	U_1	U_2	L_1	L_2
Charge	OFF	ON	ON	OFF
Slow	OFF	OFF	ON	ON
Fast	ON	OFF	OFF	ON

Current modes

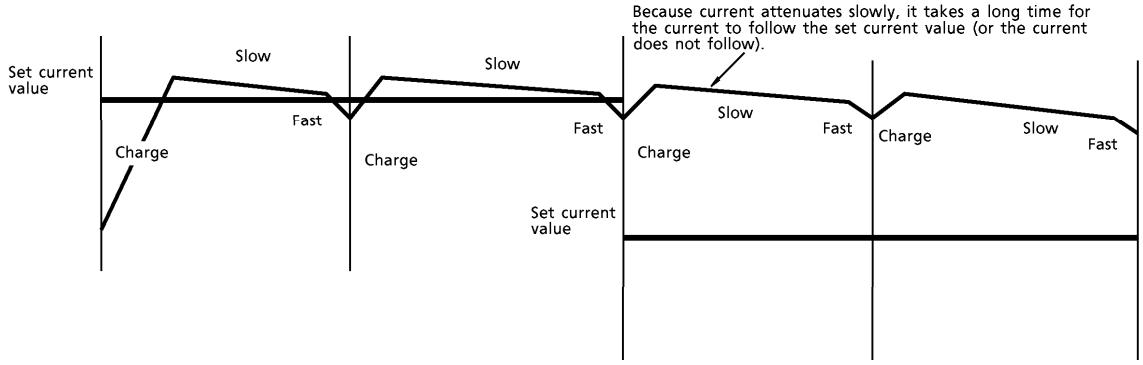
○ Sine wave in increasing (Slow Decay mode normally used)



○ Sine wave in decreasing (Mixed Decay mode normally used)

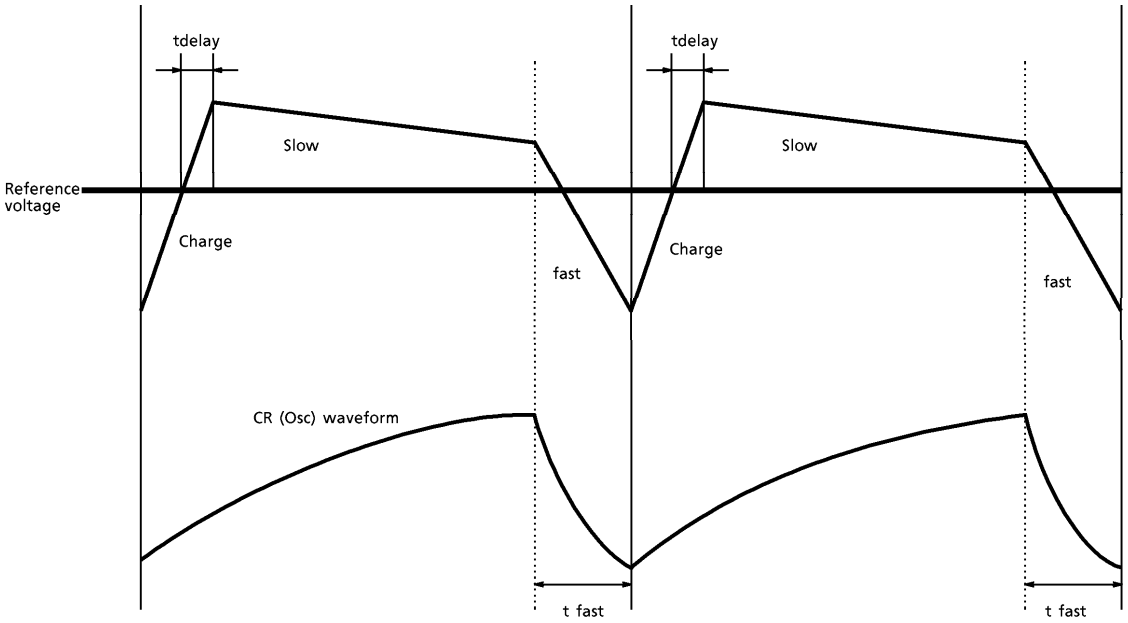


○ Sine wave in decreasing (Slow Decay mode normally used at attenuation)



(Note) The above charts are schematics. The actual current transient responses are curves.

Operation in Slow Decay mode

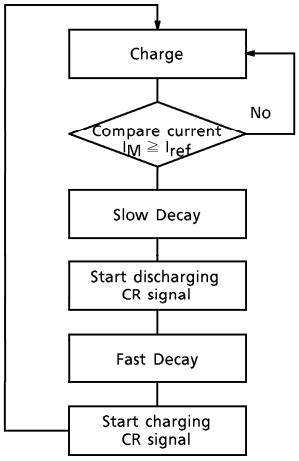


Using the oscillator waveform on the CR pin for chopping, Slow Decay mode is generated.

In Slow Decay mode, current chopping is performed in the flow chart shown on the right.

In Slow Decay mode, Fast mode continues as long as the feedback time delay (tdelay) for current comparison (from detection of motor current exceeding the reference current to output changed to Decay mode) and pulls up the current to the set current value.
Fast mode duration can be set by combining external capacitors on the CR pin.

Flow chart



IC power dissipation

IC power dissipation is classified into two : power consumed by transistors in the output block and power consumed by the logic block and the charge pump circuit.

- Power consumed by the output block (calculated with R_{on} = 0.6 Ω)

  In Charge mode, Fast Decay mode, or Slow Decay mode, power is consumed by the upper and lower transistors of the H bridges. The following expression expresses the power consumed by the transistors of a H bridge.

  $$P\ (out) = (upper\ T_r + lower\ T_r) \times I_{out}\ (A) \times V_{DS}\ (V) = 2 \times (I_{out})^2 \times R_{on} \quad \ldots\ldots\ (1)$$

  The average power dissipation for output under 4-bit micro step operation (phase difference between phases A and B is 90°) is determined by expression (1).
  Thus, power dissipation for output per unit is determined as follows (2) under the conditions below.

  R_{on} = 0.6 Ω (I_{out} = 0.9 A)
  $I_{out\ (Peak)}$ = 0.9 A
  V_M = 24 V
  V_{DD} = 5 V

  $$P\ (0.9\ A) = 0.97\ (W) \quad \ldots\ldots\ (2)$$

- Power consumed by the logic block and IM

  The following standard values are used as power dissipation of the logic block and IM at operation.

  I (LOGIC) = 4 mA (Typ.)
  I (IM3) = 15 mA (Typ.) (because of two units, 30 / 2 = 15 mA)

  The logic block is connected to V_{DD} (5 V). IM (total of current consumed by the circuits connected to V_M and current consumed by output switching) is connected to V_M (24 V). Power dissipation is calculated as follows :

  $$P\ (Logic\ \&\ IM) = 5\ (V) \times 0.004\ (A) + 24\ (V) \times 0.015\ (A) \quad \ldots\ldots\ (3)$$
  $$= 0.38\ (W)$$

  Thus, power dissipation for 1 unit (P) is determined as follows by (2) and (3) above.

  $$P = P\ (out) + P\ (Logic\ \&\ IM) = 1.35\ (W)$$

  Power dissipation when output current is 0.6 A is determined in the same way :

  $$P\ (0.6\ A) = P\ (out) + P\ (Logic\ \&\ IM)$$
  $$= 0.81\ (W)$$

  Power dissipation for 1 unit at standby is determined as follows :

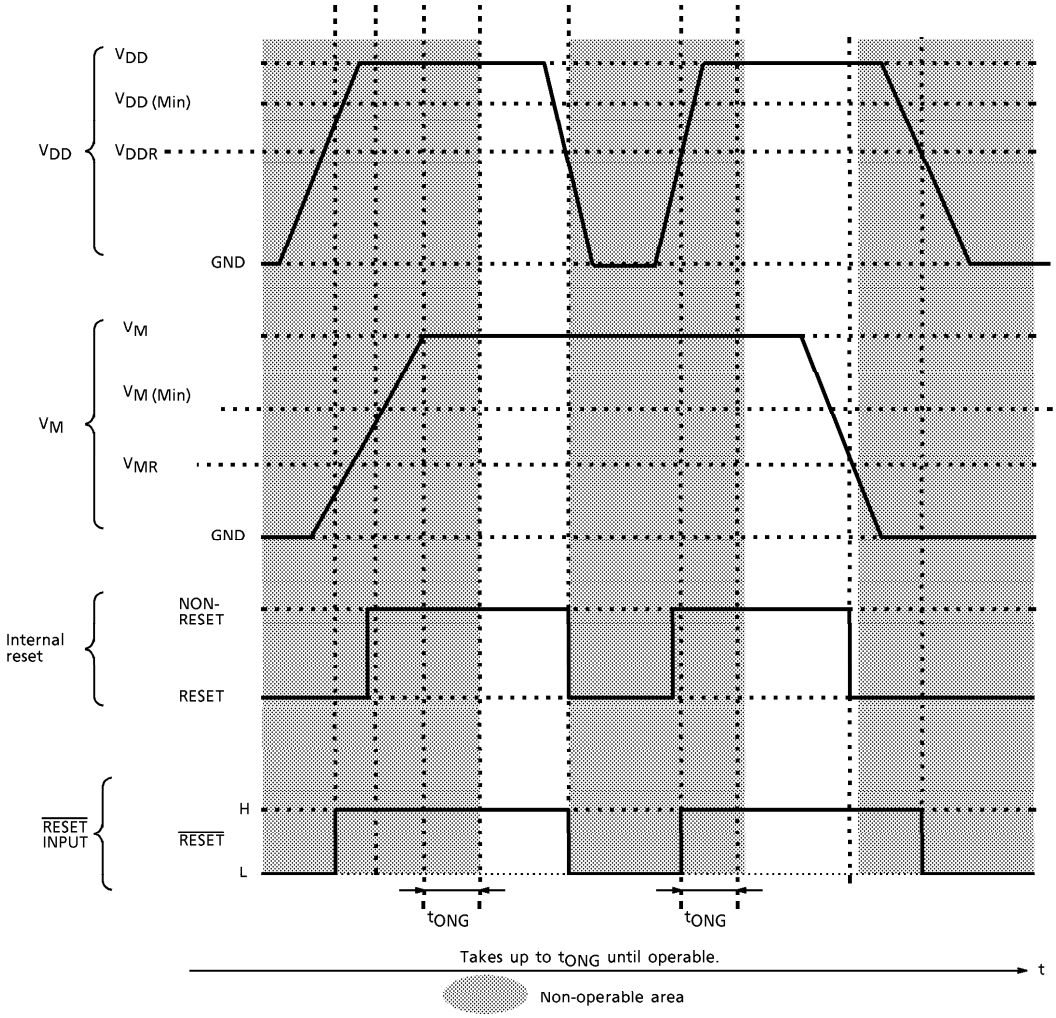
  $$P\ (standby) = 24\ (V) \times 0.015\ (A) + 5\ (V) \times 0.004\ (A)$$
  $$= 0.38\ (W)$$

  Power dissipation when Motor A = 100%, Motor B = 40%, P (TOTAL), is determined as follows :

  $$P\ (TOTAL) = P\ (Motor\ A\ OUT) \times 100\ (\%)\ Duty + P\ (Motor\ B\ OUT) \times 60\ (\%)\ Duty$$
  $$= 0.81\ (W) \times 100\ (\%) + 1.35\ (W) \times 40\ (\%) + 0.38\ (W) \times 60\ (\%)$$
  $$= 1.58\ (W)$$

  For thermal design on the board, evaluate by mounting the IC.

Power supply sequence (recommended)

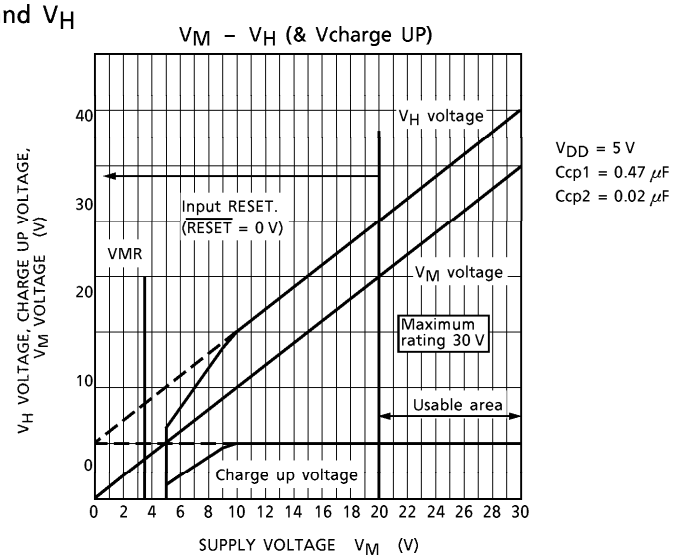


(Note 1) When the V_{DD} value drops to V_{DDR} or below, to avoid malfunction, the IC is internally reset. Likewise, when the V_M value drops to V_{MR} or below, the IC is internally reset. To avoid malfunction, when turning on V_M or V_{DD}, we recommend you input the $\overline{RESET}$ signal at the above timing.
It takes time for the output control charge pump circuit to stabilize. Wait up to t_{ONG} time after power on before driving the motors.

(Note 2) When the V_M value is between 3.3 to 5.5 V, the internal reset is released, thus output may be on. In such a case, the charge pump cannot drive stably because of insufficient voltage. We recommend the RESET state be maintained until V_M reaches 20 V or more.

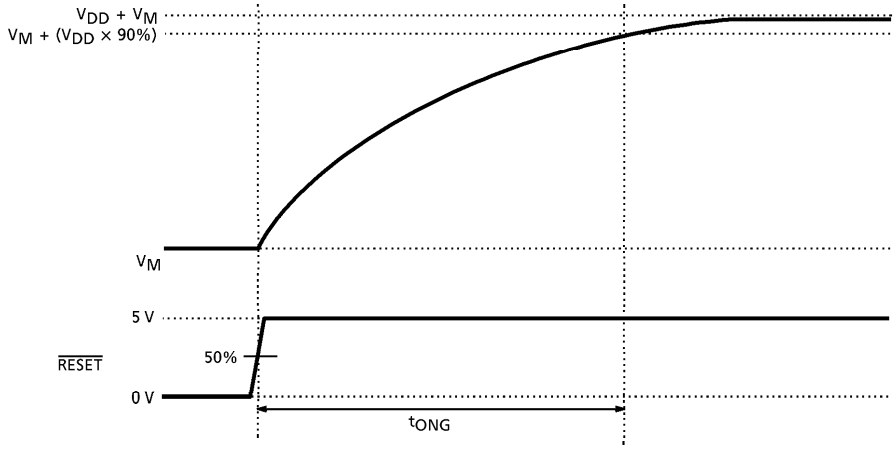
(Note 3) Since V_{DD} = 0 V and V_M = voltage within the rating are applied, output is turned off by internal reset. At that time, a current of several mA flows due to the bus between V_M and V_{DD}.

Relationship between V_M and V_H



(Note) To prevent faulty operation, stop the output circuit by inputting 0000 to the current data when V_M voltage is lower than the regulated voltage (20~30 V).
When output circuit is stropped, V_M can fluctuate between 0 V to the regulated voltage (20~30 V).

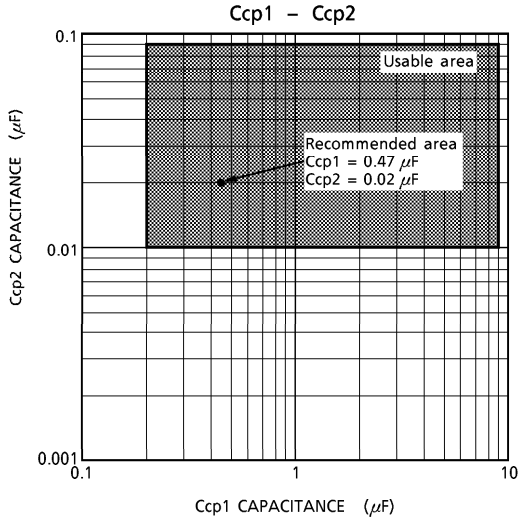
Charge up pump rise time



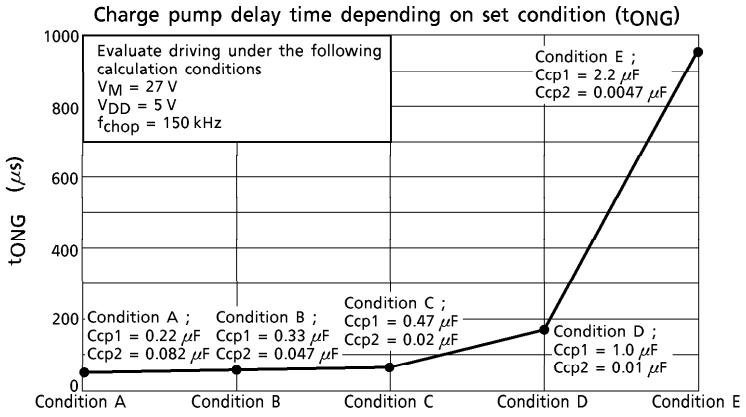
t_{ONG} : t_{ONG} is the time required after releasing reset until the Ccp2 capacitor (capacitor used to absorb charge) charges Ccp1 (capacitor used to save charge) to the $V_M + V_{DD}$ voltage. Until the Ccp1 voltage reaches the $V_M + V_{DD}$ voltage, the internal circuits cannot drive gates properly. Be sure to drive the motors at least t_{ONG}.
The Ccp1 capacitance can be increased. Reducing the Ccp1 capacitance shortens initial charge-up time but increases voltage fluctuation.
Depending on the combination of capacitors (especially if the Ccp2 capacitance is small), the voltage may not be sufficiently boosted. Toshiba recommends the following combination of capacitors :
Recommended capacitance : Ccp1 = 0.47 (μF), Ccp2 = 0.02 (μF)

External capacitors for charge pumps

When V_{DD} = 5 V, f_{chop} = 100 kHz, and L = 10 mH is driven with V_M = 24 V, I_{out} = 900 mA, the theoretical values for Ccp1 and Ccp2 are as shown below :

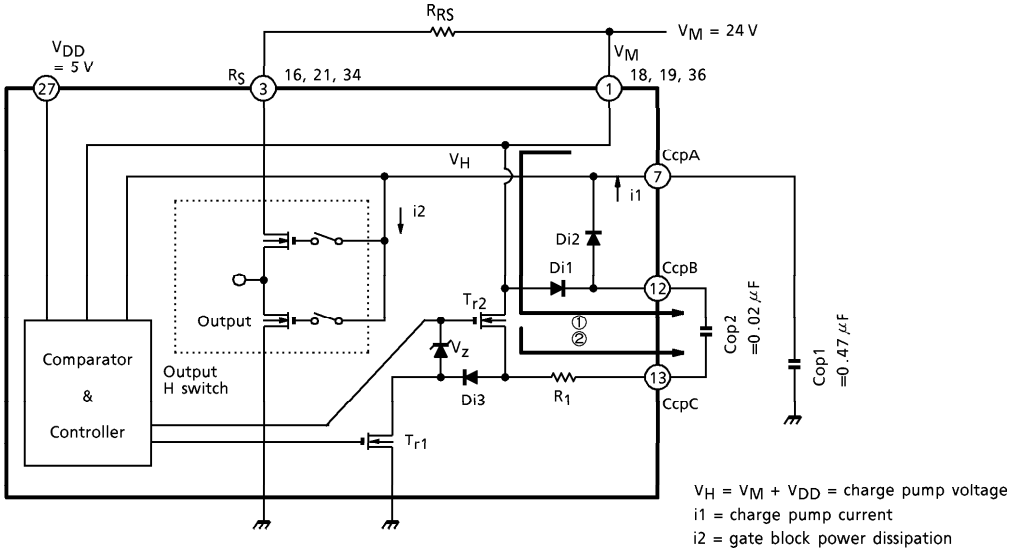


Charge pump delay time



(Note) Since the above values are theoretical, use our recommended conditions of Ccp1 = 0.47 μF, Ccp2 = 0.02 μF.

Operation of charge pump circuit



Initial charging

① When RESET is released, T_{r1} is turned on and T_{r2} turned off. Ccp2 is charged from Ccp2 via Di1.

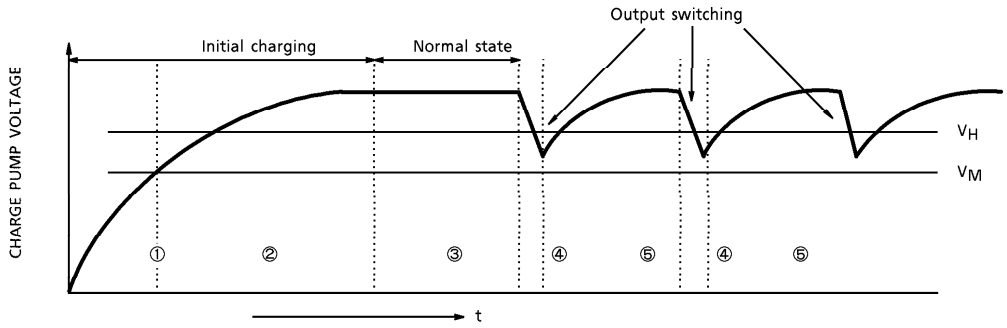
② T_{r1} is turned off, T_{r2} is turned on, and Ccp1 is charged from Ccp2 via Di2.

③ When the voltage difference between V_M and V_H (CcpA pin voltage = charge pump voltage) reaches V_{DD} or higher, operation halts (normal state).

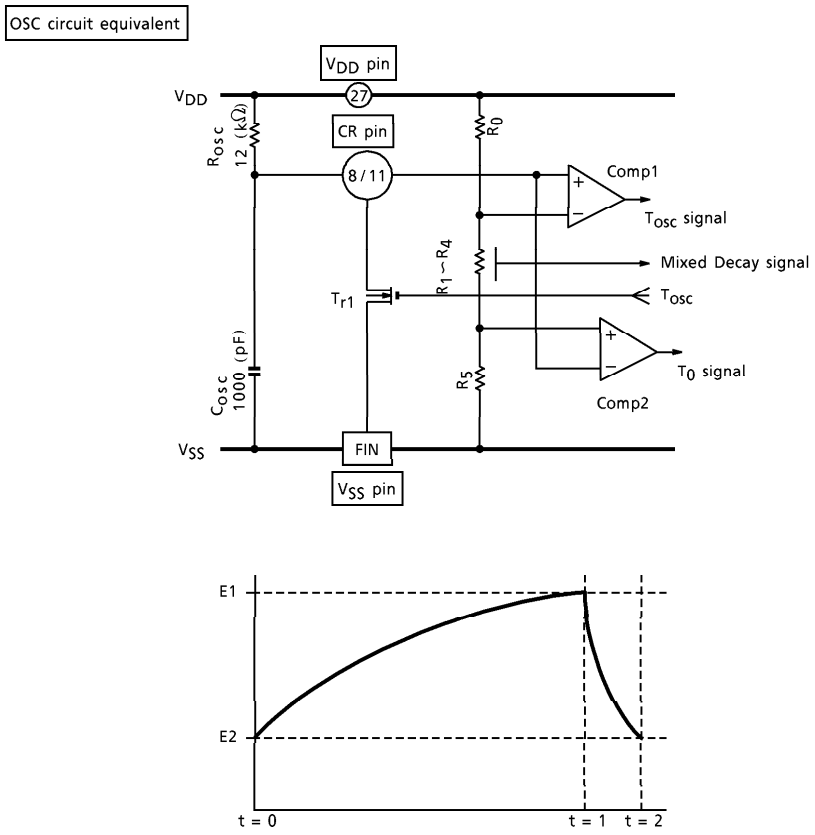
Actual operation

④ Ccp1 charge is used at f_{chop} switching and the V_H potential drops.

⑤ Charges up by ① and ② above.



OSC circuit frequency (chopping frequency)



The external capacitor for setting the chopping frequency (C_{osc}) is connected to the CR pin. It is charged by current flowing through the external resistor R_{osc} (t0~t1). When the voltage becomes $E_1 = V_{DD} \times (R_1 + R_2) / (R_0 + R_1 + R_2)$ (V), Comp2 output is turned on, triggering T_{r1} via the FF circuit. This attenuates the charged current from capacitor C_{osc} (t1~t2).

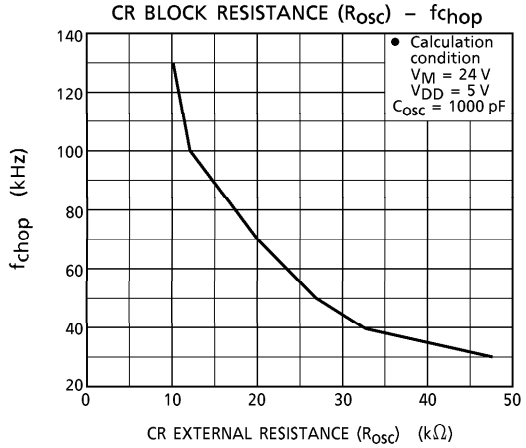
When the potential of the CR pin drops to $E_2 = V_{DD} \times R_2 / (R_0 + R_1 + R_2)$ (V), Comp1 is turned on, turning off the T_{r1} via the FF circuit (C_{osc} is charged). Repeating this generates a saw-tooth waveform.

The relationship between capacitance C_{osc} and resistance R_{osc} is expressed as follows :

$$T\ (s) = t_1 + t_2 = 0.7 \times C_{osc}\ (F) \times R_{ose}\ (\Omega) + 616 \times C_{osc}\ (F)$$

CR (OSC) frequency setting

- When the external capacitor (C_{OSC}) connected to the CR pin is fixed to 1000pF, the chopping frequency obtained by varying the R_{OSC} value is as shown below:



OSC frequency setting

Where the cycle is T (s), the following equation expresses the cycle.

$$T = t_1 + t_2 = 0.7 \times C_{OSC}\ (F) \times R_{OSC}\ (\Omega) + 616 \times C_{OSC}\ (F)$$

When R_{OSC} = 13 (kΩ), C_{OSC} = 1000 (pF), $T \fallingdotseq 9.7$ (μs). The chopping frequency f_{chop} is determined as follows :

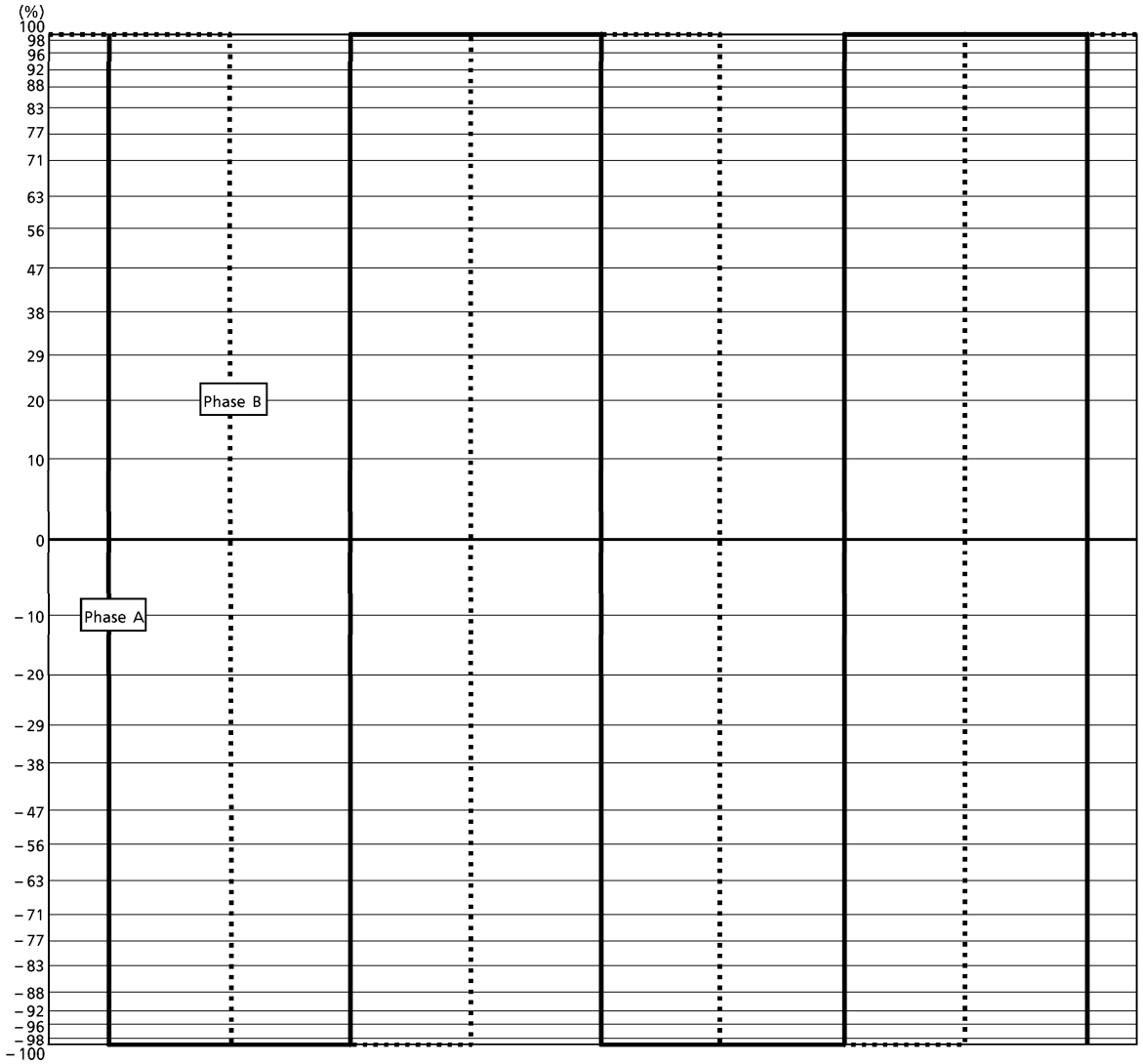
$$f_{chop} = 1/T = 1/9.7 \times 10^{-6} \fallingdotseq 103\ (kHz)$$

Application operation input data (example : 2-Phase Excitation mode)

	TORQUE 0	TORQUE 1	MDM B	DECAY B	B_0	B_1	B_2	B_3	PHASE B	MDM A	DECAY A	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1
2	1	1	0	0	1	1	1	1	0	0	0	1	1	1	1	1
3	1	1	0	0	1	1	1	1	0	0	0	1	1	1	1	0
4	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the STROBE signal.
For the input conditions, see page 9, Functions.
We recommend Mixed Decay mode (40%) as Decay mode. Set torque to 100%.

Output current waveform of 2-phase excitation sine wave



(Note) 2-phase excitation drive usable only in Mixed Decay mode.
2-phase excitation drive in Slow Decay mode is prohibited. Don't use it.

Application operation input data (example : 1-2 Phase Excitation mode)

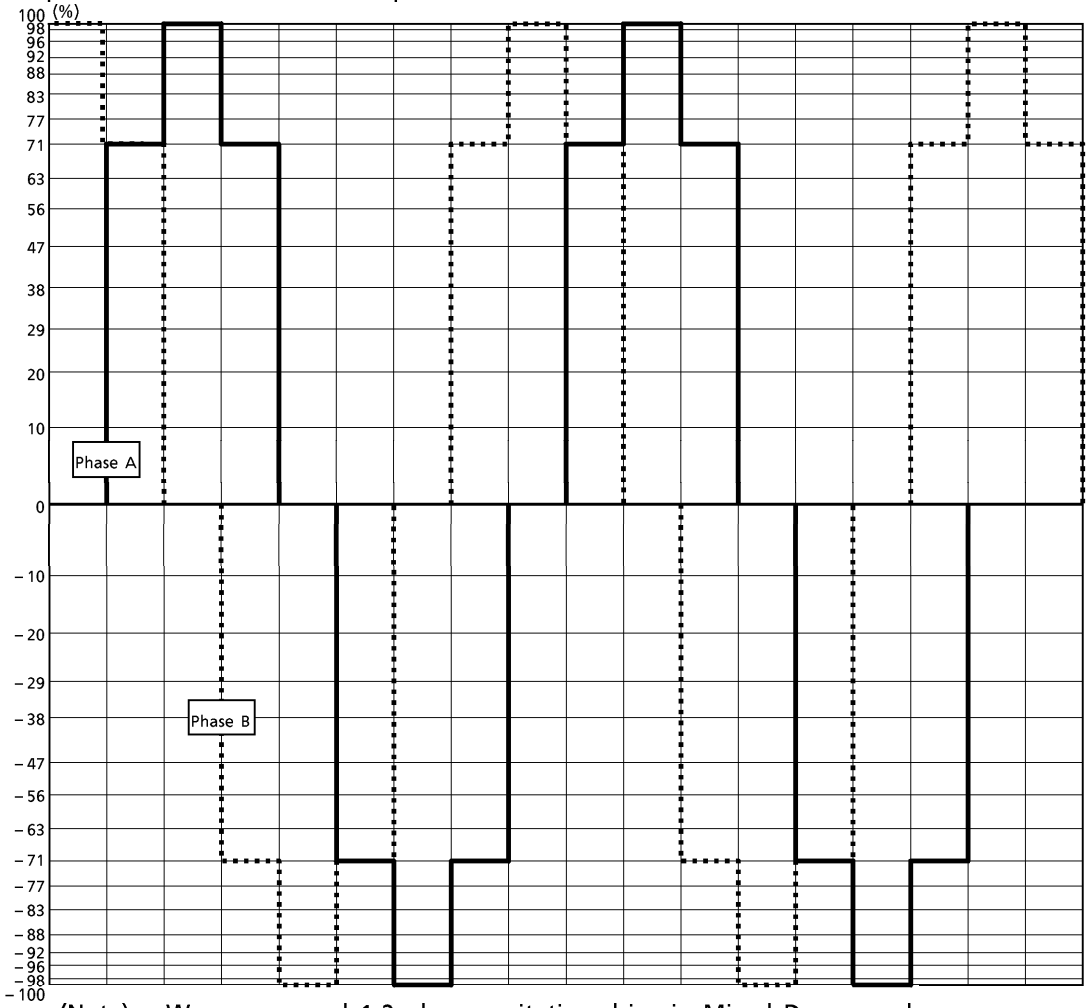
	TORQUE 0	TORQUE 1	MDM B	DECAY B	B_0	B_1	B_2	B_3	PHASE B	MDM A	DECAY A	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	1
2	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1
3	1	1	0	0	0	0	0	0	1	0	0	1	1	1	1	1
4	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1
5	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
6	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0
7	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0
8	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the STROBE signal.

For the input conditions, see page 9, Functions.

We recommend Mixed Decay mode (40%) as Decay mode. Set torque to 100%.

Output current waveform of 1-2 phase excitation sine wave



(Note) We recommend 1-2 phase excitation drive in Mixed Decay mode.

Application operation input data (example: 4-bit micro steps)

	TORQUE 0	TORQUE 1	MDM B	DECAY B	B_0	B_1	B_2	B_3	PHASE B	MDM A	DECAY A	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	1
2	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1
3	1	1	1	0	0	1	1	1	1	1	1	0	1	0	0	1
4	1	1	1	0	1	0	1	1	1	1	1	1	1	0	0	1
5	1	1	1	0	0	0	1	1	1	1	1	0	0	1	0	1
6	1	1	1	0	1	1	0	1	1	1	1	1	0	1	0	1
7	1	1	1	0	0	1	0	1	1	1	1	0	1	1	0	1
8	1	1	1	0	1	0	0	1	1	1	1	1	1	1	0	1
9	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1
10	1	1	1	0	1	1	1	0	1	1	1	1	0	0	1	1
11	1	1	1	0	0	1	1	0	1	1	1	0	1	0	1	1
12	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1
13	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1	1
14	1	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1
15	1	1	1	0	0	1	0	0	1	1	1	0	1	1	1	1
16	1	1	1	0	1	0	0	0	1	1	1	1	1	1	1	1
17	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1
18	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1	1
19	1	1	1	1	1	0	0	0	0	1	0	1	1	1	1	1
20	1	1	1	1	0	1	0	0	0	1	0	0	1	1	1	1
21	1	1	1	1	1	1	0	0	0	1	0	1	0	1	1	1
22	1	1	1	1	0	0	1	0	0	1	0	0	0	1	1	1
23	1	1	1	1	1	0	1	0	0	1	0	1	1	0	1	1
24	1	1	1	1	0	1	1	0	0	1	0	0	1	0	1	1
25	1	1	1	1	1	1	1	0	0	1	0	1	0	0	1	1
26	1	1	1	1	0	0	0	1	0	1	0	0	0	0	1	1
27	1	1	1	1	1	0	0	1	0	1	0	1	1	1	0	1
28	1	1	1	1	0	1	0	1	0	1	0	0	1	1	0	1
29	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1
30	1	1	1	1	0	0	1	1	0	1	0	0	0	1	0	1
31	1	1	1	1	1	0	1	1	0	1	0	1	1	0	0	1
32	1	1	1	1	0	1	1	1	0	1	0	0	1	0	0	1
33	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	1
34	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	1

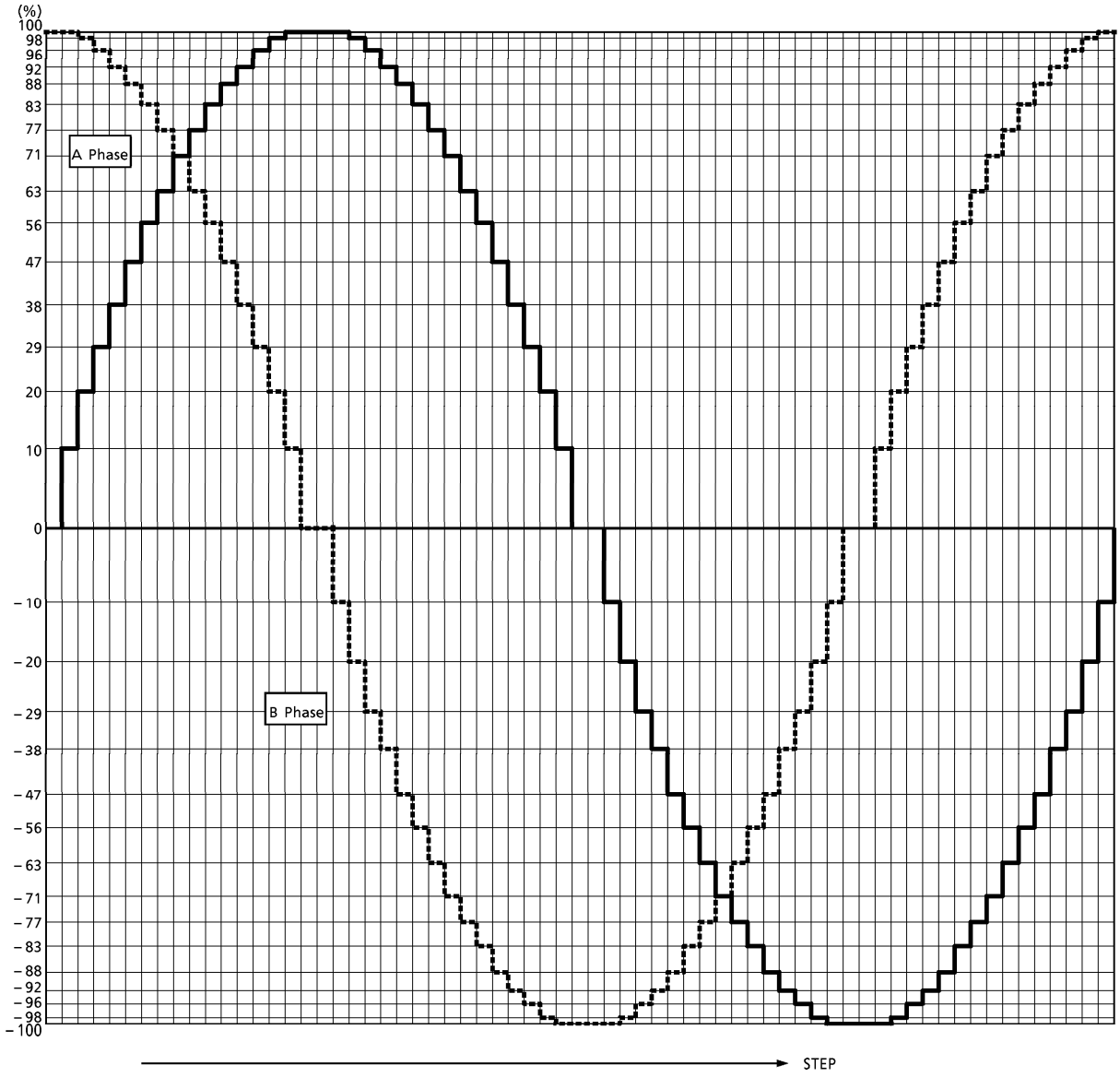
	TORQUE 0	TORQUE 1	MDM B	DECAY B	B_0	B_1	B_2	B_3	PHASE B	MDM A	DECAY A	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
35	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0
36	1	1	1	0	1	1	1	1	0	1	1	1	0	0	0	0
37	1	1	1	0	0	1	1	1	0	1	1	0	1	0	0	0
38	1	1	1	0	1	0	1	1	0	1	1	1	1	0	0	0
39	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	0
40	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	0
41	1	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
42	1	1	1	0	1	0	0	1	0	1	1	1	1	1	0	0
43	1	1	1	0	0	0	0	1	0	1	1	0	0	0	1	0
44	1	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0
45	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0
46	1	1	1	0	1	0	1	0	0	1	1	1	1	0	1	0
47	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0
48	1	1	1	0	1	1	0	0	0	1	1	1	0	1	1	0
49	1	1	1	0	0	1	0	0	0	1	1	0	1	1	1	0
50	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	0
51	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0
52	1	1	1	1	0	0	0	0	1	1	0	1	1	1	1	0
53	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	0
54	1	1	1	1	0	1	0	0	1	1	0	0	1	1	1	0
55	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	0
56	1	1	1	1	0	0	1	0	1	1	0	0	0	1	1	0
57	1	1	1	1	1	0	1	0	1	1	0	1	1	0	1	0
58	1	1	1	1	0	1	1	0	1	1	0	0	1	0	1	0
59	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	0
60	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1	0
61	1	1	1	1	1	0	0	1	1	1	0	1	1	1	0	0
62	1	1	1	1	0	1	0	1	1	1	0	0	1	1	0	0
63	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	0
64	1	1	1	1	0	0	1	1	1	1	0	0	0	1	0	0
65	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0
66	1	1	1	1	0	1	1	1	1	1	0	0	1	0	0	0
67	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0
68	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the STROBE signal.

For the input conditions, see page 9, Functions.

We recommend Slow Decay mode in the ascending direction of the sine wave ; Mixed Decay mode (40%) in the descending direction. Set torque to 100%.

Output current waveform of pseudo sine wave (4-bit micro steps)



17 micro-step from 0 to 90° drive is possible by combining current data (AB & CD) and phase data.

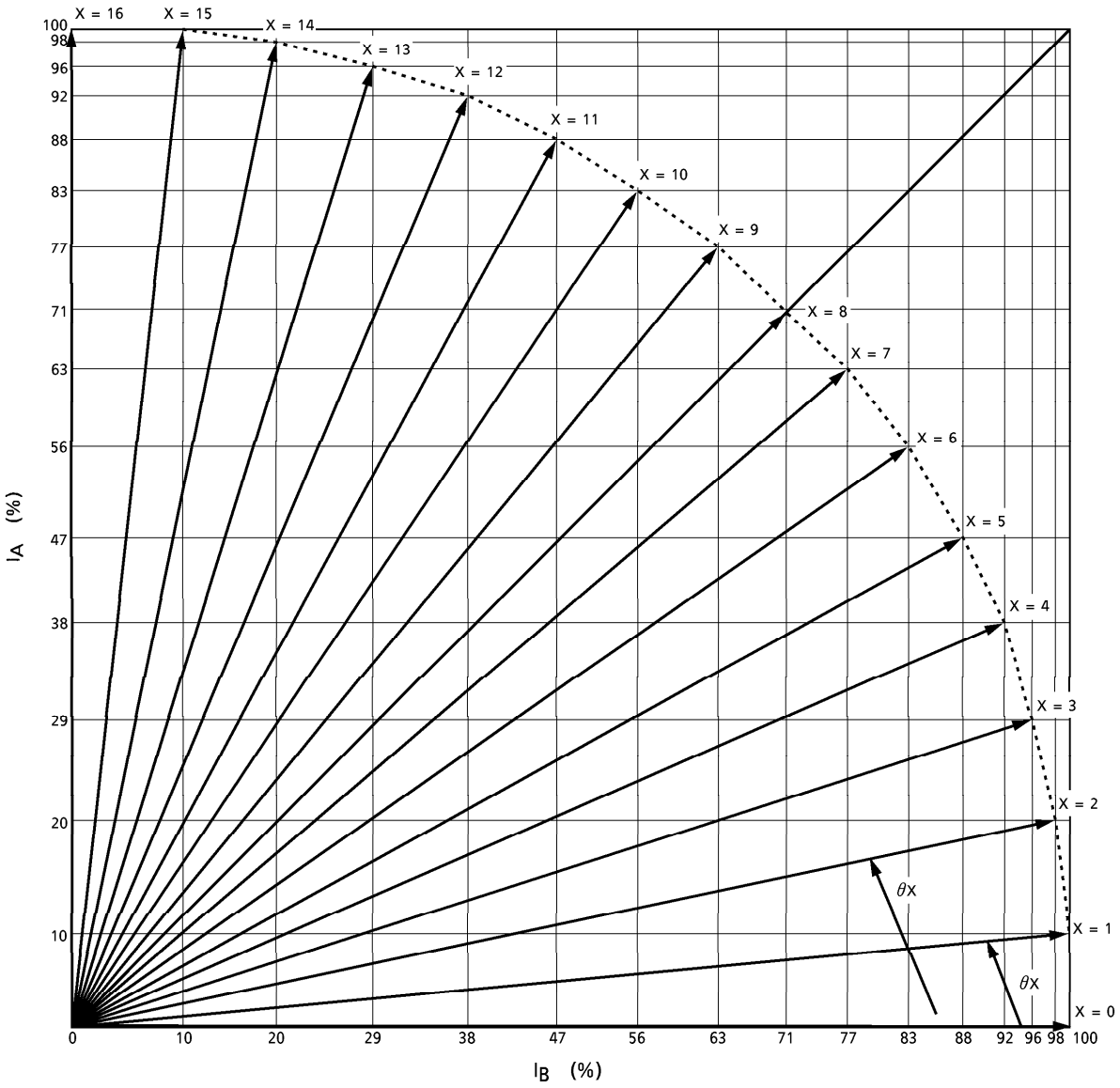
For input current data at that time, see section on Current X in the list of the Functions.

We recommend Slow Decay mode when the sine wave is rising (current increasing from 0); Mixed Decay mode (40%) when falling (current decreasing).

In Mixed Decay mode, select either 40% or 74% depending on the load.

4-bit micro steps

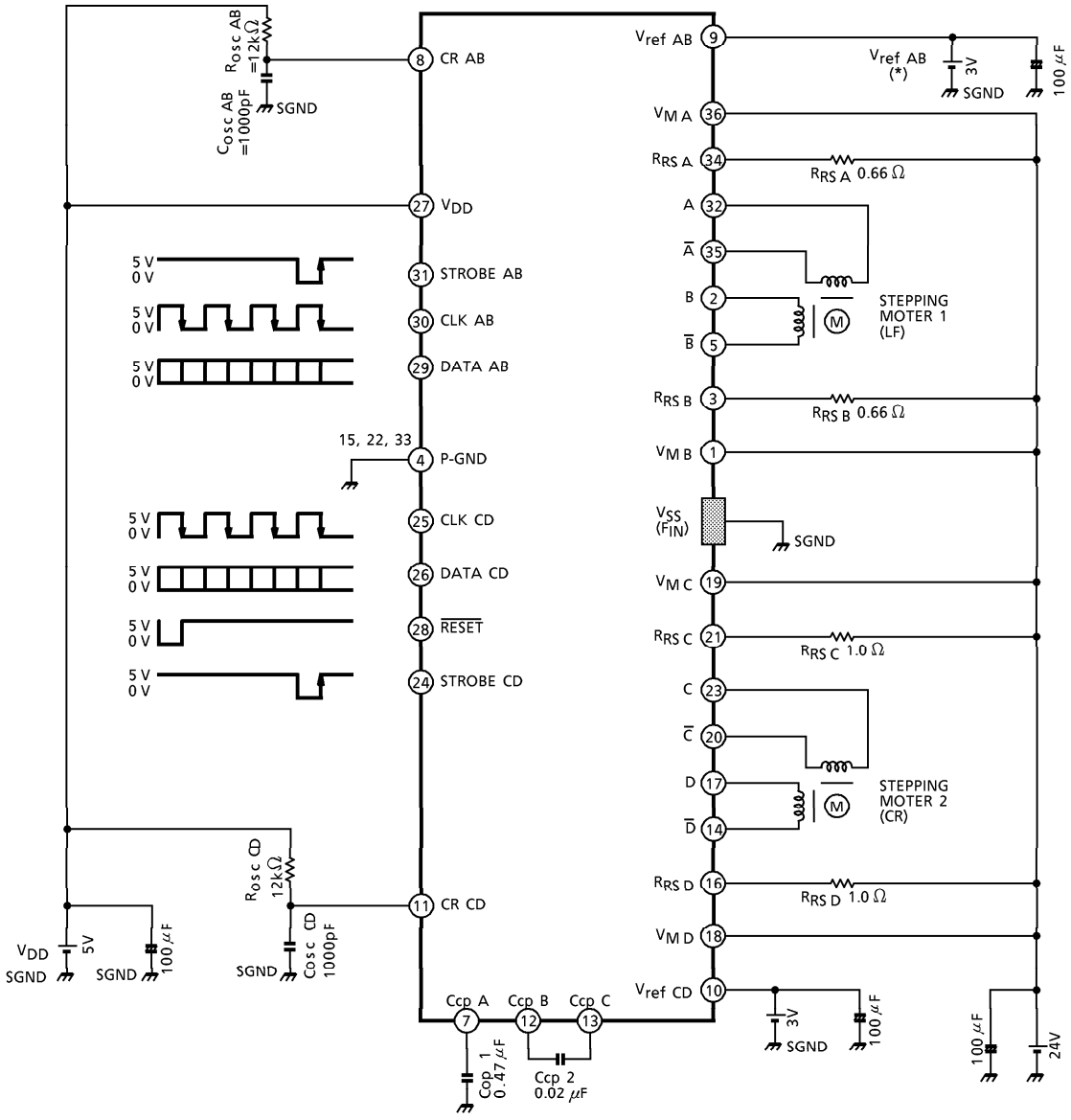
Output current vector line (Standardized 1 step as 90°)



For data to be input, see the function of Current AX (BX) in the list of Functions (10 page).

RECOMMENDED APPLICATION CIRCUIT

The values for the devices are all recommended values. For values under each input condition, see the above-mentioned recommended operating conditions.
(example : f_{chop} = 100 kHz, CR : I_{out} = 0.6 (A), LF : I_{out} = 0.9 (A))



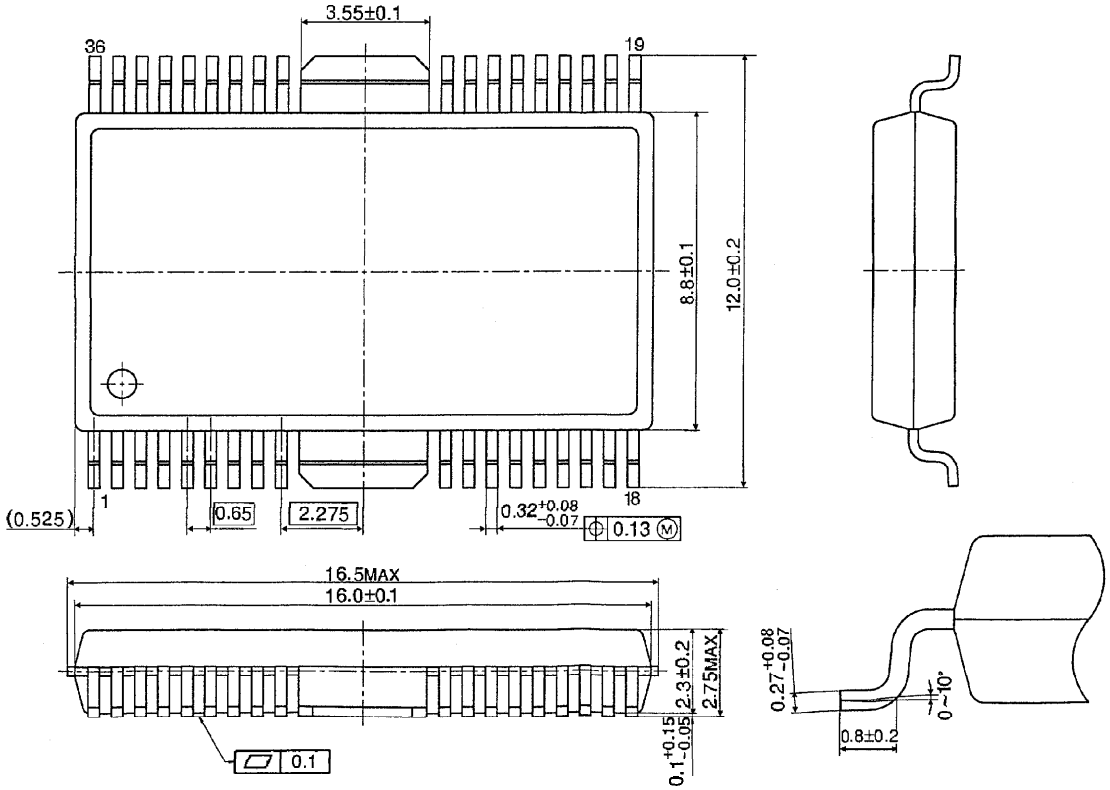
(*) We recommend the user add bypass capacitors as required.
Make sure as much as possible that GND wiring has only one contact point.
Also, make sure that the V_M pins are connected.

For the data to be input, see the section on the recommended input data.

Because there may be shorts between outputs, shorts to supply, or shorts to ground, be careful when designing output lines, V_{DD} (V_M) lines, and GND lines.

OUTLINE DRAWING

HSOP36-P-450-0.65 Unit : mm



Weight : 0.79 g (Typ.)