DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD98431

10/100 Mbps Ethernet™ CONTROLLER

DESCRIPTION

The μPD98431 is a 10/100 Mbps Ethernet controller having eight Media Access Control (MAC) ports conforming to IEEE 802.3 and IEEE 802.3u.

Each port can store 1 packet of receive data since each port has a 2 KB receive FIFO. This can reduce the generation of receive packet loss.

Both a 32-bit dual bus and 64-bit single bus FIFO bus interface are supported for interfacing with higher systems. Both provide a high-speed 66 MHz bus interface.

This controller is suitable for applications such as LAN switches and routers since a statistics counter is provided on each port to support RMON/SNMP.

Detailed function descriptions are provided in the following User's Manual. Be sure to read them before designing.

μPD98431 User's Manual: (S14054E)

FEATURES

- Eight 10/100 Mbps Ethernet MAC ports conforming to IEEE 802.3 and IEEE 802.3u
- Supports MII and 10 Mbps serial interface as interface with physical layer devices
- Each port has 2 KB of receive FIFO and 512 bytes of transmit FIFO.
- High-speed FIFO data bus interface of 32/64 bits × 66 MHz
- Full-duplex operation and IEEE 802.3x flow control
- Statistics counter supporting RMON/SNMP
- Filtering conditions can be set according to address type
- VLAN frame detection function
- Mirror port function
- JTAG support
- Supply voltage: 3.3 V

ORDERING INFORMATION

Part Number	Package
μPD98431S1-F6	352-pin plastic BGA (35 × 35)

Remark Active low pins/signals are indicated as ×××# (symbol # after pin/signal names) in this document.

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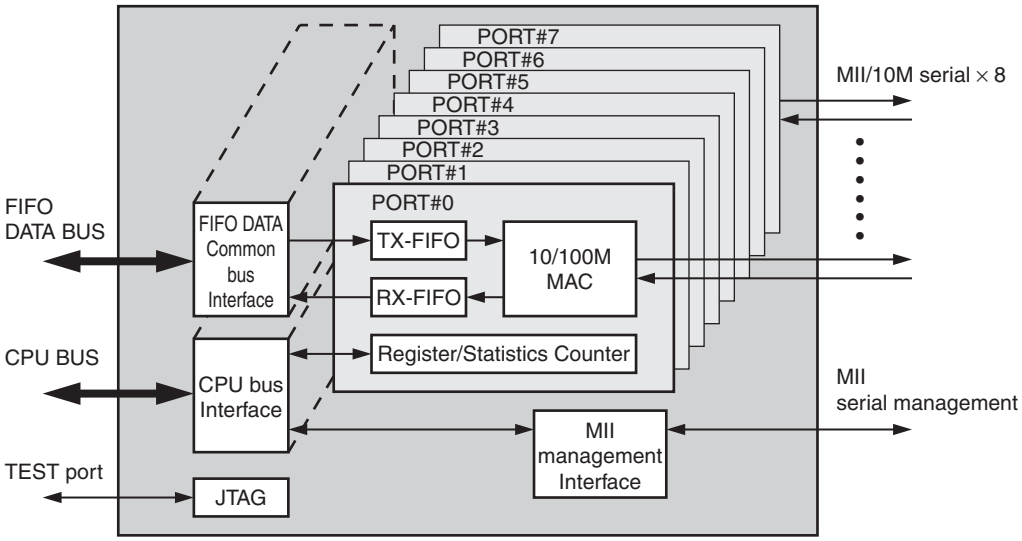
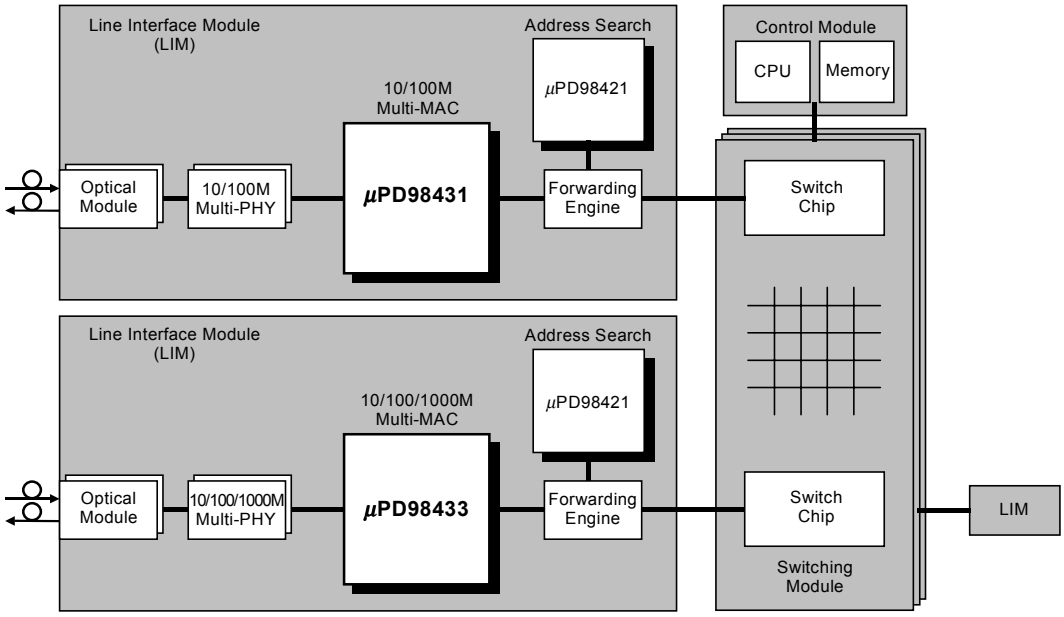
The mark ★ shows major revised points.

BLOCK DIAGRAM



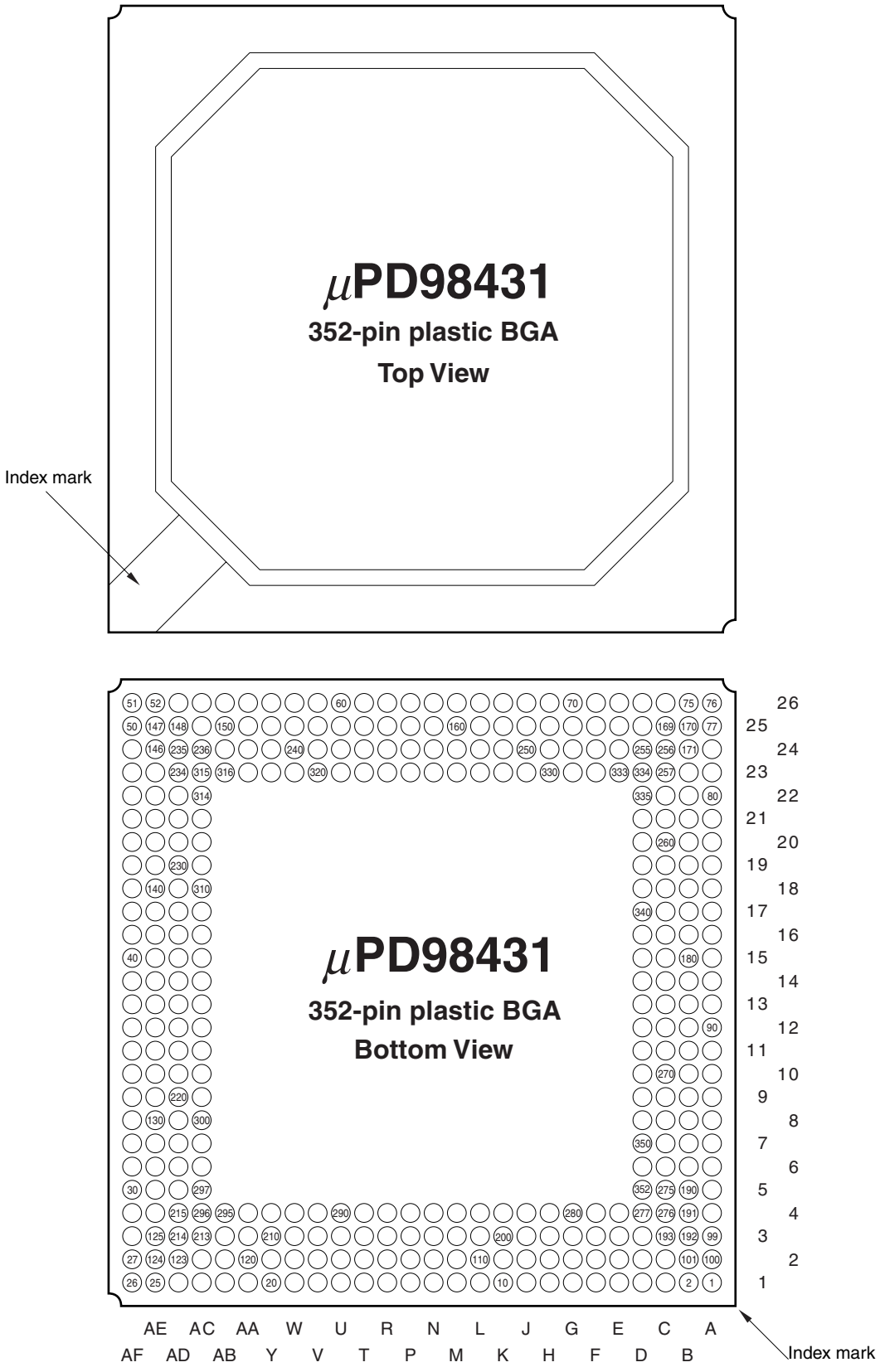
★ SYSTEM CONFIGURATION EXAMPLE of SWITCH/ROUTER



PIN CONFIGURATION

352-pin plastic BGA (35 × 35)

μPD98431S1-F6



PIN NAMES

(1/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1 (A1)	TXFD30/FD62	51 (AF26)	D28	101 (B2)	TXFD27/FD59	151 (AA25)	D16
2 (B1)	TXFD29/FD61	52 (AE26)	D27	102 (C2)	TXFD28/FD60	152 (Y25)	D13
3 (C1)	TXFD26/FD58	53 (AD26)	D24	103 (D2)	TXFD24/FD56	153 (W25)	D9
4 (D1)	TXFD23/FD55	54 (AC26)	D21	104 (E2)	TXFD21/FD53	154 (V25)	D6
5 (E1)	TXFD20/FD52	55 (AB26)	D18	105 (F2)	TXFD18/FD50	155 (U25)	D3
6 (F1)	TXFD17/FD49	56 (AA26)	D15	106 (G2)	TXFD15/FD47	156 (T25)	TXFBA7
7 (G1)	TXFD14/FD46	57 (Y26)	D12	107 (H2)	TXFD11/FD43	157 (R25)	TXFBA4
8 (H1)	TXFD10/FD42	58 (W26)	D8	108 (J2)	TXFD8/FD40	158 (P25)	TXFBA0
9 (J1)	TXFD7/FD39	59 (V26)	D5	109 (K2)	TXFD5/FD37	159 (N25)	TXFBA1
10 (K1)	TXFD4/FD36	60 (U26)	D2	110 (L2)	TXFD1/FD33	160 (M25)	TXFPT2
11 (L1)	TXFD0/FD32	61 (T26)	TXFBA6	111 (M2)	RXFDQ1/FDQ1	161 (L25)	TXFPT0
12 (M1)	RXFDQ2/FDQ2	62 (R26)	TXFBA3	112 (N2)	FCLK	162 (K25)	TXFDQ1
13 (N1)	RXFD31/FD31	63 (P26)	RXFPT2	113 (P2)	RXFA	163 (J25)	TXFEN#/FRW
14 (P1)	RXFD30/FD30	64 (N26)	RXFPT1	114 (R2)	RXFD28/FD28	164 (H25)	ACK#
15 (R1)	RXFD29/FD29	65 (M26)	RXFPT0	115 (T2)	RXFD26/FD26	165 (G25)	RW
16 (T1)	RXFD27/FD27	66 (L26)	TXFPT1	116 (U2)	RXFD23/FD23	166 (F25)	A8
17 (U1)	RXFD24/FD24	67 (K26)	TXFDQ2	117 (V2)	RXFD20/FD20	167 (E25)	A5
18 (V1)	RXFD21/FD21	68 (J26)	RXFEN#/FEN#	118 (W2)	RXFD17/FD17	168 (D25)	A3
19 (W1)	RXFD18/FD18	69 (H26)	SKIP	119 (Y2)	RXFD13/FD13	169 (C25)	TCK
20 (Y1)	RXFD14/FD14	70 (G26)	CS#	120 (AA2)	RXFD10/FD10	170 (B25)	TEST3
21 (AA1)	RXFD11/FD11	71 (F26)	A9	121 (AB2)	RXFD7/FD7	171 (B24)	MDIO
22 (AB1)	RXFD8/FD8	72 (E26)	A6	122 (AC2)	RXFD5/FD5	172 (B23)	TXER0
23 (AC1)	RXFD4/FD4	73 (D26)	A2	123 (AD2)	RXFD1/FD1	173 (B22)	TXD02
24 (AD1)	RXFD0/FD0	74 (C26)	TDO	124 (AE2)	TXD43	174 (B21)	TXCLK0
25 (AE1)	TEST0	75 (B26)	TRST#	125 (AE3)	TXEN4	175 (B20)	RXD03
26 (AF1)	CRS4	76 (A26)	TDI	126 (AE4)	TXD40	176 (B19)	RXD00
27 (AF2)	TXER4	77 (A25)	MDC	127 (AE5)	RXDV4	177 (B18)	CRS1
28 (AF3)	TXD42	78 (A24)	COL0	128 (AE6)	RXD41	178 (B17)	TXD12
29 (AF4)	TXCLK4	79 (A23)	TXEN0	129 (AE7)	COL5	179 (B16)	TXCLK1
30 (AF5)	RXD43	80 (A22)	TXD01	130 (AE8)	TXEN5	180 (B15)	RXD13
31 (AF6)	RXD40	81 (A21)	RXER0	131 (AE9)	TXD51	181 (B14)	RXCLK1
32 (AF7)	CRS5	82 (A20)	RXD02	132 (AE10)	RXDV5	182 (B13)	RXD10
33 (AF8)	TXD53	83 (A19)	RXCLK0	133 (AE11)	RXD51	183 (B12)	TXEN2
34 (AF9)	TXD50	84 (A18)	TXER1	134 (AE12)	COL6	184 (B11)	TXD22
35 (AF10)	RXD53	85 (A17)	TXD11	135 (AE13)	TXD63	185 (B10)	RXER2
36 (AF11)	RXD50	86 (A16)	RXER1	136 (AE14)	TXEN6	186 (B9)	RXD22
37 (AF12)	CRS6	87 (A15)	RXD12	137 (AE15)	TXCLK6	187 (B8)	RXCLK2
38 (AF13)	TXD62	88 (A14)	COL2	138 (AE16)	RXDV6	188 (B7)	TXER3
39 (AF14)	TXD61	89 (A13)	CRS2	139 (AE17)	RXD60	189 (B6)	TXD32
40 (AF15)	TXD60	90 (A12)	TXER2	140 (AE18)	CRS7	190 (B5)	TXCLK3
41 (AF16)	RXER6	91 (A11)	TXD23	141 (AE19)	TXD73	191 (B4)	RXDV3
42 (AF17)	RXD61	92 (A10)	TXCLK2	142 (AE20)	TXD70	192 (B3)	RXD30
43 (AF18)	COL7	93 (A9)	RXD23	143 (AE21)	RXDV7	193 (C3)	TXFD31/FD63
44 (AF19)	TXEN7	94 (A8)	RXD20	144 (AE22)	RXD71	194 (D3)	TXFD25/FD57
45 (AF20)	TXD71	95 (A7)	CRS3	145 (AE23)	RXCLK7	195 (E3)	TXFD22/FD54
46 (AF21)	RXER7	96 (A6)	TXD33	146 (AE24)	TEST2	196 (F3)	TXFD19/FD51
47 (AF22)	RXD72	97 (A5)	TXD30	147 (AE25)	D25	197 (G3)	TXFD16/FD48
48 (AF23)	RESET#	98 (A4)	RXD33	148 (AD25)	D26	198 (H3)	TXFD12/FD44
49 (AF24)	D31	99 (A3)	RXCLK3	149 (AC25)	D22	199 (J3)	TXFD9/FD41
50 (AF25)	D30	100 (A2)	TEST1	150 (AB25)	D19	200 (K3)	TXFD6/FD38

Remark Active low pins/signals are indicated as ×××# (symbol # after pin/signal names) in this document.

(2/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
201 (L3)	TXFD3/FD35	239 (Y24)	D14	277 (D4)	GND	315 (AC23)	GND
202 (M3)	TXFD2/FD34	240 (W24)	D10	278 (E4)	GND	316 (AB23)	GND
203 (N3)	RXFDQ0/FDQ0	241 (V24)	D7	279 (F4)	VDD	317 (AA23)	VDD
204 (P3)	RXFDQ3/FDQ3	242 (U24)	D4	280 (G4)	GND	318 (Y23)	GND
205 (R3)	RXFD25/FD25	243 (T24)	D1	281 (H4)	GND	319 (W23)	GND
206 (T3)	RXFD22/FD22	244 (R24)	D0	282 (J4)	TXFD13/FD45	320 (V23)	D11
207 (U3)	RXFD19/FD19	245 (P24)	TXFBA5	283 (K4)	VDD	321 (U23)	VDD
208 (V3)	RXFD16/FD16	246 (N24)	TXFBA2	284 (L4)	GND	322 (T23)	GND
209 (W3)	RXFD12/FD12	247 (M24)	TXFDQ3	285 (M4)	VDD	323 (R23)	VDD
210 (Y3)	RXFD9/FD9	248 (L24)	TXFDQ0	286 (N4)	GND	324 (P23)	GND
211 (AA3)	RXFD6/FD6	249 (K24)	PASS	287 (P4)	GND	325 (N23)	GND
212 (AB3)	RXFD3/FD3	250 (J24)	HCLK	288 (R4)	VDD	326 (M23)	VDD
213 (AC3)	RXFD2/FD2	251 (H24)	A10	289 (T4)	GND	327 (L23)	GND
214 (AD3)	COL4	252 (G24)	A7	290 (U4)	VDD	328 (K23)	VDD
215 (AD4)	TXD41	253 (F24)	A4	291 (V4)	RXFD15/FD15	329 (J23)	INT#
216 (AD5)	RXER4	254 (E24)	A1	292 (W4)	GND	330 (H23)	GND
217 (AD6)	RXD42	255 (D24)	A0	293 (Y4)	GND	331 (G23)	GND
218 (AD7)	RXCLK4	256 (C24)	TMS	294 (AA4)	VDD	332 (F23)	VDD
219 (AD8)	TXER5	257 (C23)	CRS0	295 (AB4)	GND	333 (E23)	GND
220 (AD9)	TXD52	258 (C22)	TXD03	296 (AC4)	GND	334 (D23)	GND
221 (AD10)	RXER5	259 (C21)	TXD00	297 (AC5)	VDD	335 (D22)	VDD
222 (AD11)	TXCLK5	260 (C20)	RXDV0	298 (AC6)	CLAMP	336 (D21)	CLAMP
223 (AD12)	RXD52	261 (C19)	RXD01	299 (AC7)	GND	337 (D20)	GND
224 (AD13)	RXCLK5	262 (C18)	COL1	300 (AC8)	VDD	338 (D19)	VDD
225 (AD14)	TXER6	263 (C17)	TXD13	301 (AC9)	CLAMP	339 (D18)	CLAMP
226 (AD15)	RXD63	264 (C16)	TXEN1	302 (AC10)	GND	340 (D17)	GND
227 (AD16)	RXCLK6	265 (C15)	TXD10	303 (AC11)	VDD	341 (D16)	VDD
228 (AD17)	TXER7	266 (C14)	RXDV1	304 (AC12)	CLAMP	342 (D15)	CLAMP
229 (AD18)	TXD72	267 (C13)	RXD11	305 (AC13)	GND	343 (D14)	GND
230 (AD19)	TXCLK7	268 (C12)	TXD21	306 (AC14)	RXD62	344 (D13)	TXD20
231 (AD20)	RXD73	269 (C11)	RXDV2	307 (AC15)	VDD	345 (D12)	VDD
232 (AD21)	RXD70	270 (C10)	RXD21	308 (AC16)	VDD	346 (D11)	VDD
233 (AD22)	TEST4	271 (C9)	COL3	309 (AC17)	GND	347 (D10)	GND
234 (AD23)	TEST5	272 (C8)	TXEN3	310 (AC18)	CLAMP	348 (D9)	CLAMP
235 (AD24)	D29	273 (C7)	TXD31	311 (AC19)	VDD	349 (D8)	VDD
236 (AC24)	D23	274 (C6)	RXER3	312 (AC20)	GND	350 (D7)	GND
237 (AB24)	D20	275 (C5)	RXD32	313 (AC21)	CLAMP	351 (D6)	CLAMP
238 (AA24)	D17	276 (C4)	RXD31	314 (AC22)	VDD	352 (D5)	VDD

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1. PIN FUNCTIONS

(1) Register interface

Pin Name	Pin No.	I/O	Function
CS#	70	Input	**Chip select.** When this signal is low, the internal registers of the chip can be accessed.
RW	165	Input	**Host read/write.** This pin is used by the host system to access the register bus. When a high level is input to this pin, the register bus is accessed for read. When a low level is input, the register bus is accessed for write.
A[10:0]	251, 71, 166, 252, 72, 167, 253, 168, 73, 254, 255	Input	**Register address.** The address necessary for selecting a port or register to be accessed when an internal register of the μPD98431 is to be accessed is given to A[10:0]. The μPD98431 has a 32-bit register for each port. A[10:8] specifies a port, and [A7:0] specifies a register address. The relationship between the setting of A[10:8] and a port number is as follows: Port 0 → A[10:8] = 000B Port 1 → A[10:8] = 001B Port 2 → A[10:8] = 010B Port 3 → A[10:8] = 011B Port 4 → A[10:8] = 100B Port 5 → A[10:8] = 101B Port 6 → A[10:8] = 110B Port 7 → A[10:8] = 111B
D[31:0]	49, 50, 235, 51, 52, 148, 147, 53, 236, 149, 54, 237, 150, 55, 238, 151, 56, 239, 152, 57, 320, 240, 153, 58, 241, 154, 59, 242, 155, 60, 243, 244	I/O, 3-state	**Register data.** These pins form a bidirectional data bus through which the internal registers of the μPD98431 are accessed.
INT#	329	Output, open drain	**Interrupt signal.** Interrupt request signal. This signal goes low if an interrupt source is generated. It is kept low until all the interrupt statuses are cleared if an interrupt occurs. This signal is an open-drain output signal.
RESET#	48	Input	**Hardware reset.** Active-low asynchronous reset signal. Immediately after hardware reset, all the registers are set to their default values, and all the FIFOs and counters are cleared.
ACK#	164	Output, 3-state	**Register data acknowledge.** This signal indicates that the data on D[31:0] is valid when a register is read. When this signal is low, the data read from the register exists on D[31:0]. When a register is written, this signal indicates completion of the writing.
HCLK	250	Input	**Register interface clock.** This pin inputs a synchronization clock used to access a register. The maximum frequency of the input clock is 66 MHz. **Caution Set HCLK so that its frequency always exceeds the frequency of RXCLK and TXCLK.**

(2) FIFO interface

(1/3)

Pin Name	Pin No.	I/O	Function
RXFEN#/ FEN#	68	Input	**FIFO bus reception enable/FIFO bus enable.** The function of this signal differs as follows depending on the FIFO bus mode: (1) 32-bit dual bus mode In this mode, this signal functions as RXFEN#. If this signal goes low, the receive FIFO bus interface is enabled, and data can be read from the receive FIFO. (2) 64-bit single bus mode In this mode, this signal functions as FEN#. If this signal goes low, the FIFO bus interface is enabled, and data can be read from the receive FIFO or written to the transmit FIFO.
TXFEN#/ FRW	163	Input	**FIFO bus transmission enable/FIFO bus direction.** The function of this signal differs as follows depending on the FIFO bus mode: (1) 32-bit dual bus mode In this mode, this signal functions as TXFEN#. If this signal goes low, the transmit FIFO bus interface is enabled, and data can be written to the transmit FIFO. (2) 64-bit single bus mode In this mode, this signal functions as FRW, and specifies the direction of FIFO bus access. While this signal is high, the FIFO bus is accessed by the receive FIFO for read. While it is low, the bus is accessed by the transmit FIFO for write.
FCLK	112	Input	**FIFO bus clock.** The FIFO bus is synchronized with FCLK. The maximum frequency of the input clock is 66 MHz. **Caution Set FCLK so that its frequency always exceeds the frequency of RXCLK and TXCLK.**
RXFPT[2:0]	63 to 65	Output, 3-state	**Receive port number.** These signals indicate a port number from which receive data is output when the receive FIFO is accessed for read. The relation between RXFPT[2:0] and a port number is as follows: Port 0 → RXFPT[2:0] = 000B Port 1 → RXFPT[2:0] = 001B Port 2 → RXFPT[2:0] = 010B Port 3 → RXFPT[2:0] = 011B Port 4 → RXFPT[2:0] = 100B Port 5 → RXFPT[2:0] = 101B Port 6 → RXFPT[2:0] = 110B Port 7 → RXFPT[2:0] = 111B

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Pin Name	Pin No.	I/O	Function
TXFPT[2:0]	160, 66, 161	Input	**Transmit port number.** These signals indicate the port number of the transmit FIFO to which transmit data is written when the transmit FIFO is accessed for write. The relation between TXFPT[2:0] and a port number is as follows: Port 0 → TXFPT[2:0] = 000B Port 1 → TXFPT[2:0] = 001B Port 2 → TXFPT[2:0] = 010B Port 3 → TXFPT[2:0] = 011B Port 4 → TXFPT[2:0] = 100B Port 5 → TXFPT[2:0] = 101B Port 6 → TXFPT[2:0] = 110B Port 7 → TXFPT[2:0] = 111B
TXFD[31:0], RXFD[31:0]/ FD[63:0]	193, 1, 2, 102, 101, 3, 194, 103, 4, 195, 104, 5, 196, 105, 6, 197, 106, 7, 282, 198, 107, 8, 199, 108, 9, 200, 109, 10, 201, 202, 110, 11, 13 to 15, 114, 16, 115, 205, 17, 116, 206, 18, 117, 207, 19, 118, 208, 291, 20, 119, 209, 21, 120, 210, 22, 121, 211, 122, 23, 212, 213, 123, 24	Input, Output, I/O, 3-state	**32-bit transmit FIFO data bus, 32-bit receive FIFO data bus/64-bit FIFO data bus.** These signals provide the data bus of the FIFO bus interface. The functions of these signals differ as follows depending on the FIFO bus mode. (1) 32-bit dual bus mode These signals function as TXFD[31:0] and RXFD[31:0]. This 64-bit data bus is divided into two unidirectional buses, TXFD[31:0] and RXFD[31:0], when the BUSWTH bit of the MISCR register is cleared to 0. (2) 64-bit single bus mode These signals function as FD[63:0]. This 64-bit data bus is used as a 64-bit bidirectional bus to access the FIFO when the BUSWTH bit of the MISCR register is set to 1.
TXFDQ[3:0]	247, 67, 162, 248	Input	**Transmit data attribute.** These signals indicate the attribute of the transmit data on the FIFO bus in the 32-bit dual bus mode. They indicate the attribute of the transmit data on FD[63:0] when the transmit FIFO is accessed for write. These signals are meaningless in the 64-bit single bus mode.
RXFDQ[3:0]/ FDQ[3:0]	204, 12, 111, 203	Output, I/O, 3-state	**Receive data attribute/FIFO bus attribute.** These signals indicate the attribute of data on the FIFO bus. The functions of these signals differ as follows depending on the bus mode: (1) 32-bit dual bus mode These signals function as RXFDQ[3:0] and output the attribute of the receive data output onto RXFD[31:0] when the FIFO bus is accessed by the receive FIFO for read. (2) 64-bit single bus mode These signals function as FDQ[3:0] and input the attribute of the transmit data on FD[63:0] when the transmit FIFO is accessed for write. When the receive FIFO is accessed for read, the attribute of the receive data output onto FD[63:0] is output.

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Pin Name	Pin No.	I/O	Function
TXFBA[7:0]	156, 61, 245, 157, 62, 246, 159, 158	Output, 3-state	**Transmit FIFO buffer available.** When these signals are high, the transmit FIFO has space to which transmit data can be written. If the quantity of the data in the transmit FIFO exceeds the value set to the TFDMH field of the TFIC register, these signals go low. A TXFBA signal is provided for each port, and TXFBA[n] is the TXFBA signal of port n.
RXFA	113	Output, 3-state	**Receive frame available.** When this signal is high, the port indicated by RXFPT has at least one packet from the receive data stream that is ready to be transferred to the host system.
PASS	249	Input	**Receive frame pass.** This signal is input to start transfer of the receive data currently on the FIFO bus when the bus is accessed by the receive FIFO for read.
SKIP	69	Input	**Receive frame skip.** This signal is input to skip the port currently on the FIFO bus and read data from the next port when the FIFO bus is accessed by the receive FIFO for read.

(3) MII (Media Independent Interface)

(1/3)

Pin Name	Pin No.	I/O	Function
TXCLK[7:0]	230, 137, 222, 29, 190, 92, 179, 174	Input	**MII transmit clock.** These pins input the transmit clock (duty: 50%) necessary for outputting data to the PHY device connected to each port. Transmit data from each port, TXD7[3:0] through TXD0[3:0], and TXEN[7:0] that indicates that the transmit data on TXD is valid are output to each port in synchronization with this clock. In the MII mode, a 2.5 MHz clock is input for 10 Mbps operation, and a 25 MHz clock is input for 100 Mbps operation. In this mode, TXD and TXEN are output in synchronization with the rising of TXCLK. In the 10 Mbps serial mode, a 10 MHz clock is input. In this mode, TXD and TXEN are output in synchronization with the rising of TXCLK. For the unused ports, fix TXCLK to high or low level.
TXD0[3:0]	258, 173, 80, 259	Output	**MII transmit data (port 0).** These pins output transmit data to the PHY device connected to port 0. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK0. In the 10 Mbps serial mode, only TXD0[0] is used to output serial transmit data at the rising edge of TXCLK0.
TXD1[3:0]	263, 178, 85, 265	Output	**MII transmit data (port 1).** These pins output transmit data to the PHY device connected to port 1. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK1. In the 10 Mbps serial mode, only TXD1[0] is used to output serial transmit data at the rising edge of TXCLK1.
TXD2[3:0]	91, 184, 268, 344	Output	**MII transmit data (port 2).** These pins output transmit data to the PHY device connected to port 2. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK2. In the 10 Mbps serial mode, only TXD2[0] is used to output serial transmit data at the rising edge of TXCLK2.
TXD3[3:0]	96, 189, 273, 97	Output	**MII transmit data (port 3).** These pins output transmit data to the PHY device connected to port 3. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK3. In the 10 Mbps serial mode, only TXD3[0] is used to output serial transmit data at the rising edge of TXCLK3.
TXD4[3:0]	124, 28, 215, 126	Output	**MII transmit data (port 4).** These pins output transmit data to the PHY device connected to port 4. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK4. In the 10 Mbps serial mode, only TXD4[0] is used to output serial transmit data at the rising edge of TXCLK4.
TXD5[3:0]	33, 220, 131, 34	Output	**MII transmit data (port 5).** These pins output transmit data to the PHY device connected to port 5. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK5. In the 10 Mbps serial mode, only TXD5[0] is used to output serial transmit data at the rising edge of TXCLK5.

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Pin Name	Pin No.	I/O	Function
TXD6[3:0]	135, 38 to 40	Output	**MII transmit data (port 6).** These pins output transmit data to the PHY device connected to port 6. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK6. In the 10 Mbps serial mode, only TXD6[0] is used to output serial transmit data at the rising edge of TXCLK6.
TXD7[3:0]	141, 229, 45, 142	Output	**MII transmit data (port 7).** These pins output transmit data to the PHY device connected to port 7. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK7. In the 10 Mbps serial mode, only TXD7[0] is used to output serial transmit data at the rising edge of TXCLK7.
TXEN[7:0]	44, 136, 130, 125, 272, 183, 264, 79	Output	**MII transmission enable.** These signals indicate whether the transmit data (TXD) of each port is valid. In the 10 Mbps serial mode, they remain high starting from the fist bit of a preamble, until the last bit of the transmit frame is output. In the MII mode, they remain high starting from the first nibble data indicating a preamble, until the last nibble data of the transmit frame is output.
RXCLK[7:0]	145, 227, 224, 218, 99, 187, 181, 83,	Input	**MII receive clock.** These pins input the clock (duty: 50%) received from the PHY device. RXD7[3:0] through RXD0[3:0] that are the data received from each port, and TXEN[7:0] that indicates the existence of transmit data on TXD are output in synchronization with this clock. In the MII mode, a 2.5 MHz clock is input for 10 Mbps operation, and a 25 MHz clock is input for 100 Mbps operation. In this mode, RXD and RXDV are input at the rising edge of RXCLK. In the 10 Mbps serial mode, a 10 MHz clock is input. In this mode, RXD is input at the rising edge of RXCLK. Fix RXCLK of an unused port to the high or low level.
RXD0[3:0]	175, 82, 261, 176	Input	**MII receive data (port 0).** These pins input data received from the PHY device connected to port 0. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK0. In the 10 Mbps serial mode, only RXD0[0] is used and serial receive data is input at the rising edge of RXCLK0.
RXD1[3:0]	180, 87, 267, 182	Input	**MII receive data (port 1).** These pins input data received from the PHY device connected to port 1. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK1. In the 10 Mbps serial mode, only RXD1[0] is used and serial receive data is input at the rising edge of RXCLK1.
RXD2[3:0]	93, 186, 270, 94	Input	**MII receive data (port 2).** These pins input data received from the PHY device connected to port 2. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK2. In the 10 Mbps serial mode, only RXD2[0] is used and serial receive data is input at the rising edge of RXCLK2.
RXD3[3:0]	98, 275, 276, 192	Input	**MII receive data (port 3).** These pins input data received from the PHY device connected to port 3. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK3. In the 10 Mbps serial mode, only RXD3[0] is used and serial receive data is input at the rising edge of RXCLK3.

(3/3)

Pin Name	Pin No.	I/O	Function
RXD4[3:0]	30, 217, 128, 31	Input	**MII receive data (port 4).** These pins input data received from the PHY device connected to port 4. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK4. In the 10 Mbps serial mode, only RXD4[0] is used and serial receive data is input at the rising edge of RXCLK4.
RXD5[3:0]	35, 223, 133, 36	Input	**MII receive data (port 5).** These pins input data received from the PHY device connected to port 5. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK5. In the 10 Mbps serial mode, only RXD5[0] is used and serial receive data is input at the rising edge of RXCLK5.
RXD6[3:0]	226, 306, 42, 139	Input	**MII receive data (port 6).** These pins input data received from the PHY device connected to port 6. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK6. In the 10 Mbps serial mode, only RXD6[0] is used and serial receive data is input at the rising edge of RXCLK6.
RXD7[3:0]	231, 47, 144, 232	Input	**MII receive data (port 7).** These pins input data received from the PHY device connected to port 7. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK7. In the 10 Mbps serial mode, only RXD7[0] is used and serial receive data is input at the rising edge of RXCLK7.
CRS[7:0]	140, 37, 32, 26, 95, 89, 177, 257	Input	**Carrier sense.** These are carrier sense signals input from the PHY device connected to each port. Fix CRS of an unused port to the low level.
RXDV[7:0]	143, 138, 132, 127, 191, 269, 266, 260	Input	**MII receive data valid.** These signals indicate, in the MII mode, that the data on RXD is valid for each port. When these signals are high, the data on RXD is valid. Fix RXDV of an unused port to the high or low level.
COL[7:0]	43, 134, 129, 214, 271, 88, 262, 78	Input	**Collision.** These pins input the collision signals detected by the PHY device connected to each port. Fix COL of an unused port to the low level.
TXER[7:0]	228, 225, 219, 27, 188, 90, 84, 172	Output	**MII transmission error.** These signals indicate that an error occurs at each port of the μPD98431 during transmission.
RXER[7:0]	46, 41, 221, 216, 274, 185, 86, 81	Input	**MII reception error.** These are input signals to detect errors occurring at each port of the PHY device during reception. Fix RXER of an unused port to the low level.
MDC	77	Output	**MII management clock.** This is a transfer clock for MII serial management data.
MDIO	171	I/O	**MII management data.** This is a bidirectional MII serial management data signal.

(4) JTAG pins (These functions can be supported upon request.)

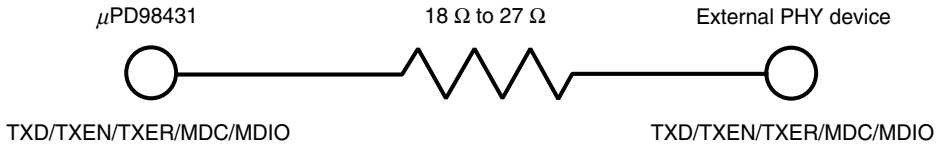
Pin Name	Pin No.	I/O	Function
TMS	256	Input	**JTAG test mode select.** This signal controls the boundary scan state machine. This pin is internally pulled up. (pull-up resistor: 50 kΩ)
TDI	76	Input	**JTAG test data input.** This signal is serial data input for boundary scan. This pin is internally pulled up. (pull-up resistor: 50 kΩ)
TDO	74	Output 3-state	**JTAG test data output.** This signal is serial data output for boundary scan.
TCK	169	Input	**JTAG test clock.** This is clock input used to synchronize test data input and output. This pin is internally pulled up (pull-up resistor: 50 kΩ)
TRST#	75	Input	**JTAG reset.** When this signal is deasserted low, the boundary scan operation is reset. This signal must be kept high during boundary scan operation. When not using the JTAG function, fix pins to low. This pin is internally pulled up. (pull-up resistor: 50 kΩ)

(5) Test pins and power pins

Pin Name	Pin No.	I/O	Function
TEST	234, 233, 170, 146, 100, 25	Input	**Test pins.** These pins are used to test the device. Always fix these pins to low.
VDD	279, 283, 285, 288, 290, 294, 297, 300, 303, 307, 308, 311, 314, 317, 321, 323, 326, 328, 332, 335, 338, 341, 345, 346, 349, 352	–	**Power supply (+3.3 V)**
GND	277, 278, 280, 281, 284, 286, 287, 289, 292, 293, 295, 296, 299, 302, 305, 309, 312, 315, 316, 318, 319, 322, 324, 325, 327, 330, 331, 333, 334, 337, 340, 343, 347, 350	–	**Ground (0 V)**
CLAMP	298, 301, 304, 310, 313, 336, 339, 342, 348, 351	–	**Clamp power supply.** This pin supplies a clamp voltage to the MII buffer circuit. Supply +5 V to this pin when an external 5 V PHY device is used. Supply +3.3 V when an external 3.3 V PHY device is used.

(6) μPD98431 MII output signal pin connection

When connecting the PHY device to the MII output signals (TXD, TTEN, TXER, MDC, MDIO), connect a serial resistor of 18 Ω to 27 Ω to each MII output signal as follows so that the drivability of the MII output buffer accords with the IEEE802.3u standard.



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
Clamp supply voltage	V_{CLAMP}		–0.5 to +6.6	V
Input/output voltage	V_{IO}	Except MII signal	–0.5 to +4.6	V
		MII signal	–0.5 to +7.3	V
Maximum power consumption	P_{MAX}		2.60	W
Operating temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.135	3.3	3.465	V
Clamp supply voltage	V_{CLAMP}		3.135	V_{DD}/5.0	5.5	V
Operating temperature	T_A		0		70	°C

DC Characteristics (T_A = 0 to +70°C, V_{DD} = +3.3 V ±5%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_I = 0.0 to 3.3 V			10	μA
Output leakage current	I_{LO}	V_O = 0.0 to 3.3 V			10	μA
Operating current	I_{DD}				750	mA
Clock input voltage, low	V_{CL}	HCLK, FCLK			0.8	V
Clock input voltage, high	V_{CH}	HCLK, FCLK	2.0			V
Input voltage, low	V_{IL}		0		+0.8	V
Input voltage, high	V_{IH}	Except MII interface	2.0		4.6	V
		MII interface	2.0		5.5	V
Output voltage, low	V_{OL}	I_{OL} = 6 mA, FD[63:0], FDQ[3:0], TXFBA[7:0], RXFPT[2:0], RXFA			0.4	V
		I_{OL} = 4 mA, TXDn [0:3], TXEN[7:0], TXER[7:0]			0.4	V
		I_{OL} = 3 mA, signals other than the above			0.4	V
Output voltage, high	V_{OH}	I_{OH} = –6 mA, FD[63:0], FDQ[3:0], TXFBA[7:0], RXFPT[2:0], RXFA	2.4			V
		I_{OH} = –4 mA, TXDn [0:3], TXEN[7:0], TXER[7:0]	2.4			V
		I_{OH} = –3 mA, signals other than the above	2.4			V

Capacitance (T_A = 25°C, f_C = 1 MHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	V_I = 0 V			15	pF
I/O capacitance	C_{IO}	V_{IO} = 0 V			15	pF

AC Characteristics (T_A = 0 to +70°C, V_{DD} = +3.3 V ±5%)

All AC characteristics values are based on the following conditions.

AC test conditions

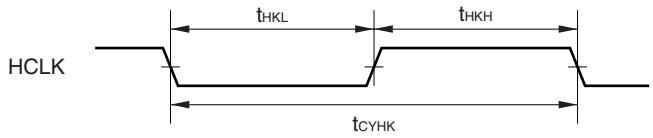
- Load condition: 30 pF (1 Schottky TTL gate + C_L)
- Input pulse level: 0.4 V to 2.4 V
- Test reference level: 1.5 V

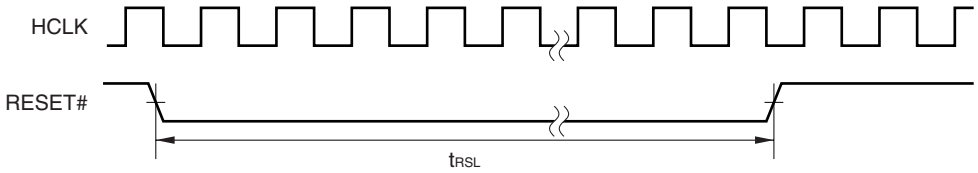
Register Bus Interface Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
HCLK clock width[Note]	t_{CYHK}		15		40	ns
HCLK low-level width	t_{HKL}		7		22	ns
HCLK high-level width	t_{HKH}		7		22	ns
RESET# pulse width	t_{RSL}		16 t_{CYHK}			ns
A[10:0] setup time	t_{SHKA}		5			ns
A[10:0] hold time	t_{HHKA}		0			ns
RW setup time	t_{SHKRW}		5			ns
RW hold time	t_{HHKRW}		0			ns
CS# setup time	t_{SHKCS}		5			ns
CS# hold time	t_{HHKCS}		0		t_{CYHK}	ns
ACK# output delay time	t_{DHKAC}				10	ns
ACK# float time	t_{FHKAC}				10	ns
D[31:0] output delay time	t_{DHKD}				10	ns
D[31:0] setup time	t_{SHKD}		5			ns
D[31:0] hold time	t_{HHKD}		0			ns
D[31:0] float time	t_{FHKD}				10	ns

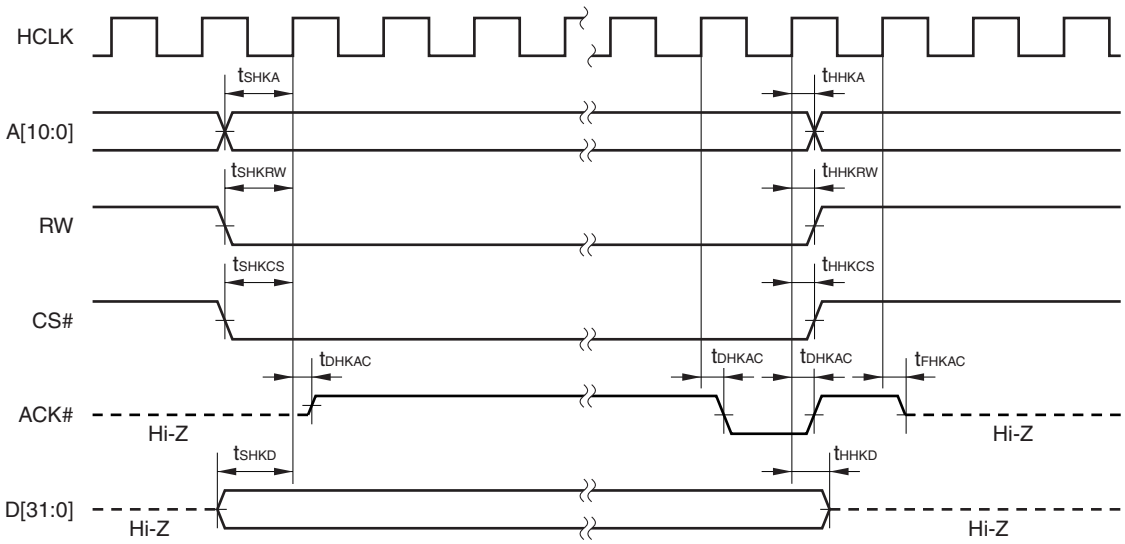
Note The HCLK clock width must always be shorter than both the RXCLK clock width and TXCLK clock width.

(1) HCLK timing

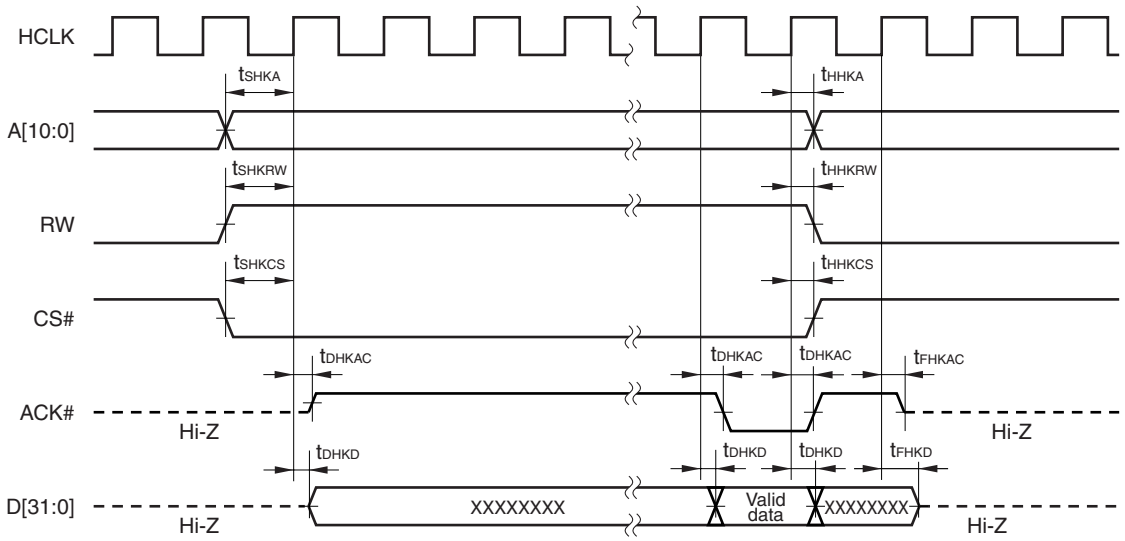




(2) Register bus interface write timing



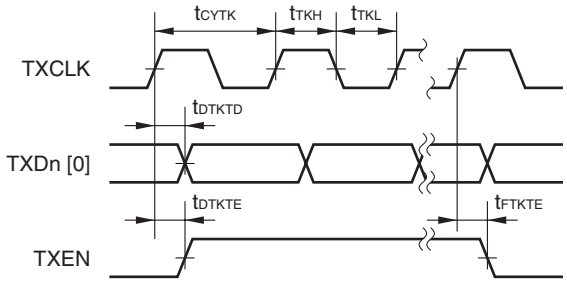
★ (3) Register bus interface read timing



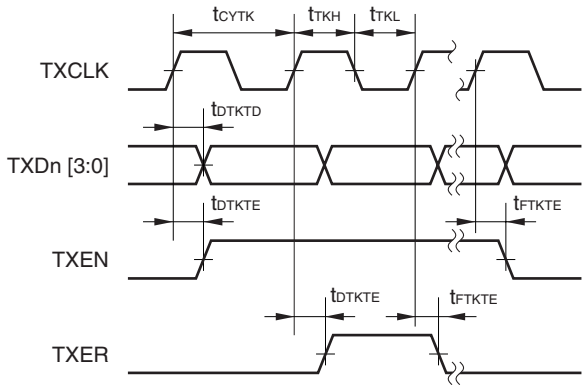
Ethernet Transmit Interface Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TXDn[3:0] delay time	t_{DTKTD}	C_L = 20 pF			20	ns
Transmit signal assert delay time	t_{DTKTE}	C_L = 20 pF			20	ns
Transmit signal deassert delay time	t_{FTKTE}	C_L = 20 pF			20	ns
TXCLK clock width	t_{CYTK}	MII mode		40/400		ns
		10 Mbps serial mode		100		ns
TXCLK high-level width	t_{TKH}	MII mode		20/200		ns
		10 Mbps serial mode		50		ns
TXCLK low-level width	t_{TKL}	MII mode		20/200		ns
		10 Mbps serial mode		50		ns

(a) 10 Mbps serial mode



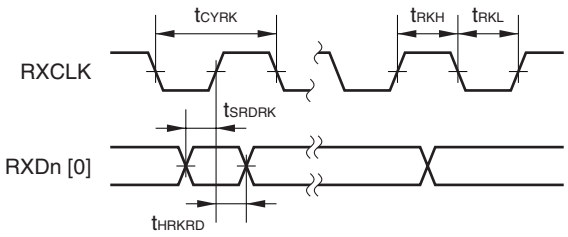
(b) MII mode



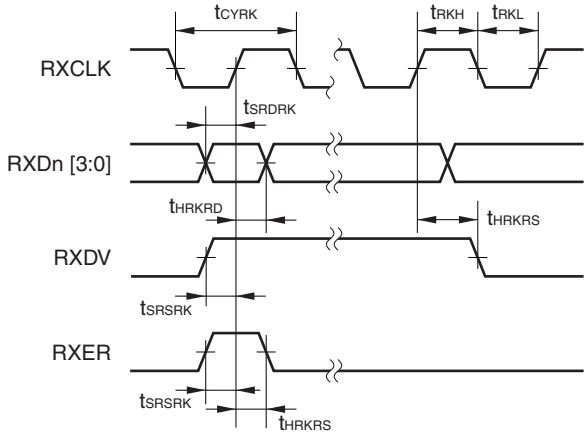
Ethernet Receive Interface Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RXDn[3:0] setup time	t_{SRDRK}		5			ns
RXDn[3:0] hold time	t_{HRKRD}		5			ns
Receive signal setup time	t_{SRSRK}		5			ns
Receive signal hold time	t_{HRKRS}		5			ns
RXCLK clock width	t_{CYRK}	MII mode		40/400		ns
		10 Mbps serial mode		100		ns
RXCLK high-level width	t_{RKH}	MII mode		20/200		ns
		10 Mbps serial mode		50		ns
RXCLK low-level width	t_{RKL}	MII mode		20/200		ns
		10 Mbps serial mode		50		ns

(a) 10 Mbps serial mode

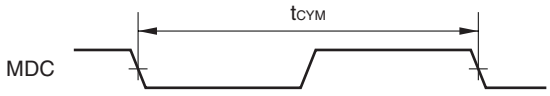


(b) MII mode

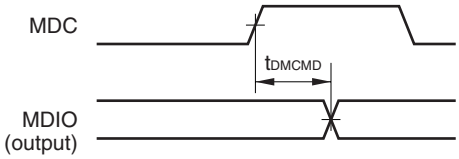


MII Management Interface Timing

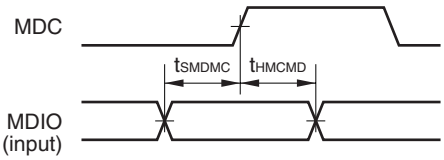
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MDC cycle	t_{CYM}		400		1080	ns
MDIO delay time	t_{DMCMD}		t_{CYHK}–5		t_{CYHK}+10	ns
MDIO setup time	t_{SMDMC}		t_{CYHK}+20			ns
MDIO hold time	t_{HMCMD}		0			ns



(a) Output



(b) Input



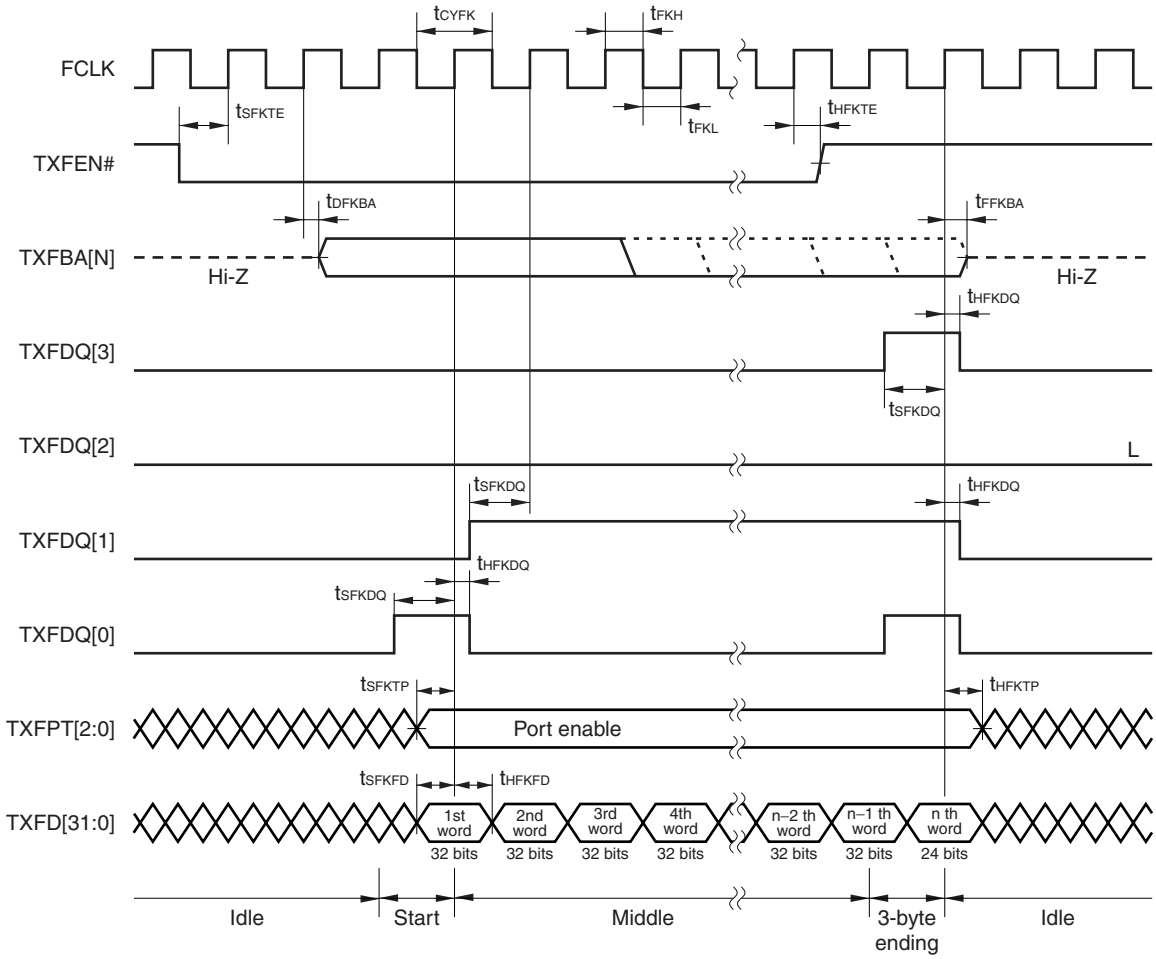
FIFO Bus Interface Write Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FCLK clock width[Note]	t_{CYFK}		15		40	ns
FCLK high-level width	t_{FKH}		7		22	ns
FCLK low-level width	t_{FKL}		7		22	ns
TXFEN#/FRW setup time	t_{SFKTE}		6			ns
TXFEN#/FRW hold time	t_{HFKTE}		0			ns
TXFBA[N] output delay time	t_{DFKBA}				10	ns
TXFBA[N] float time	t_{FFKBA}				10	ns
TXFDQ[3:0]/FDQ[3:0] setup time	t_{SFKDQ}		5			ns
TXFDQ[3:0]/FDQ[3:0] hold time	t_{HFKDQ}		0			ns
TXFPT[2:0] setup time	t_{SFKTP}		5			ns
TXFPT[2:0] hold time	t_{HFKTP}		0			ns
TXFD[31:0]/FD[63:0] setup time	t_{SFKFD}		6			ns
TXFD[31:0]/FD[63:0] hold time	t_{HFKFD}		0			ns
RXFEN#/FEN# setup time	t_{SFKRE}		5			ns
RXFEN#/FEN# hold time	t_{HFKRE}		0			ns

Note The FCLK clock width must always be shorter than both the RXCLK clock width and TXCLK clock width.

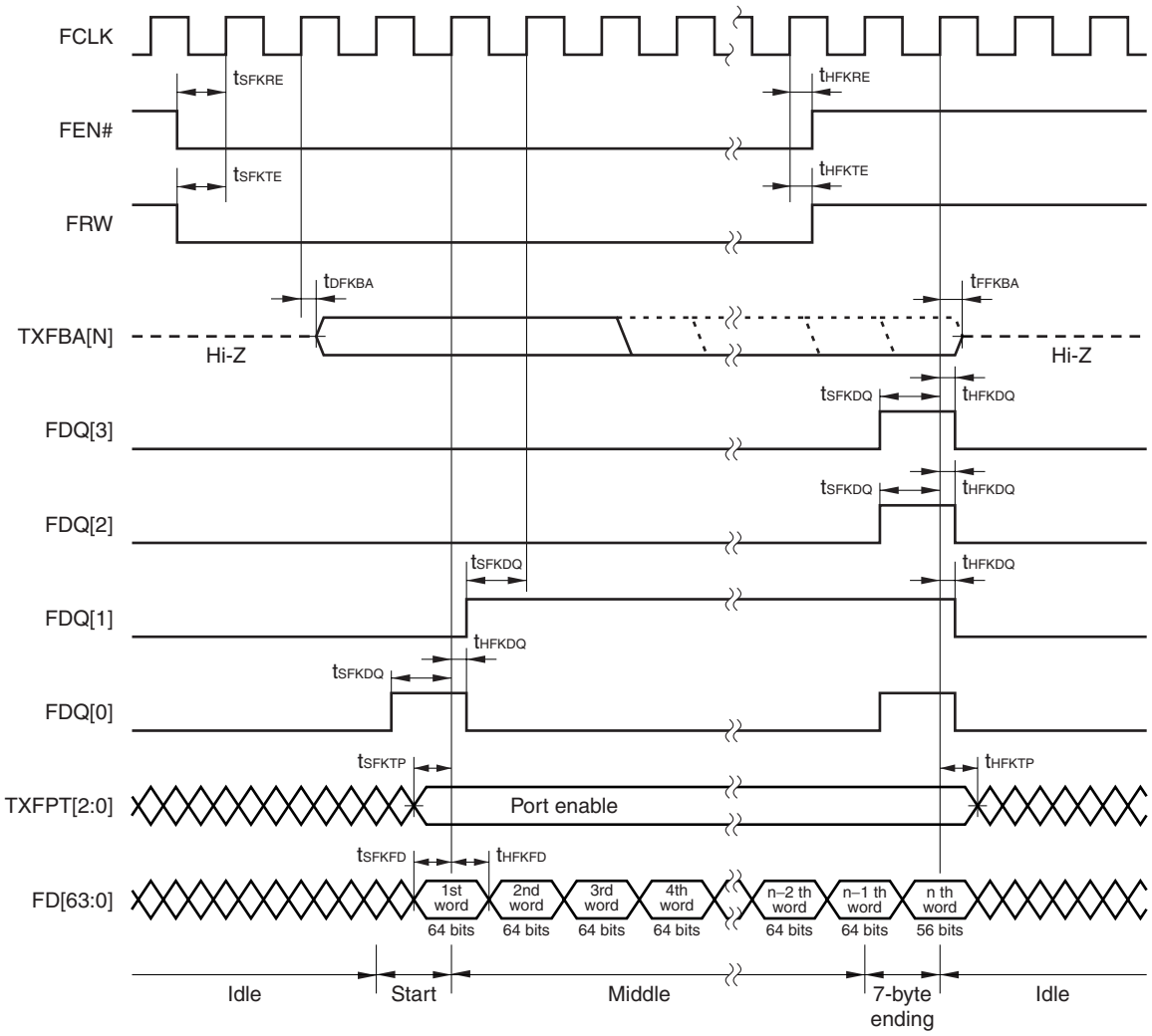
Remark TXFBA[N]: N = 0 to 7

(1) FIFO bus interface write timing (32-bit dual bus mode)



Remark TXFBA[N]: N = 0 to 7

(2) FIFO bus interface write timing (64-bit single bus mode)

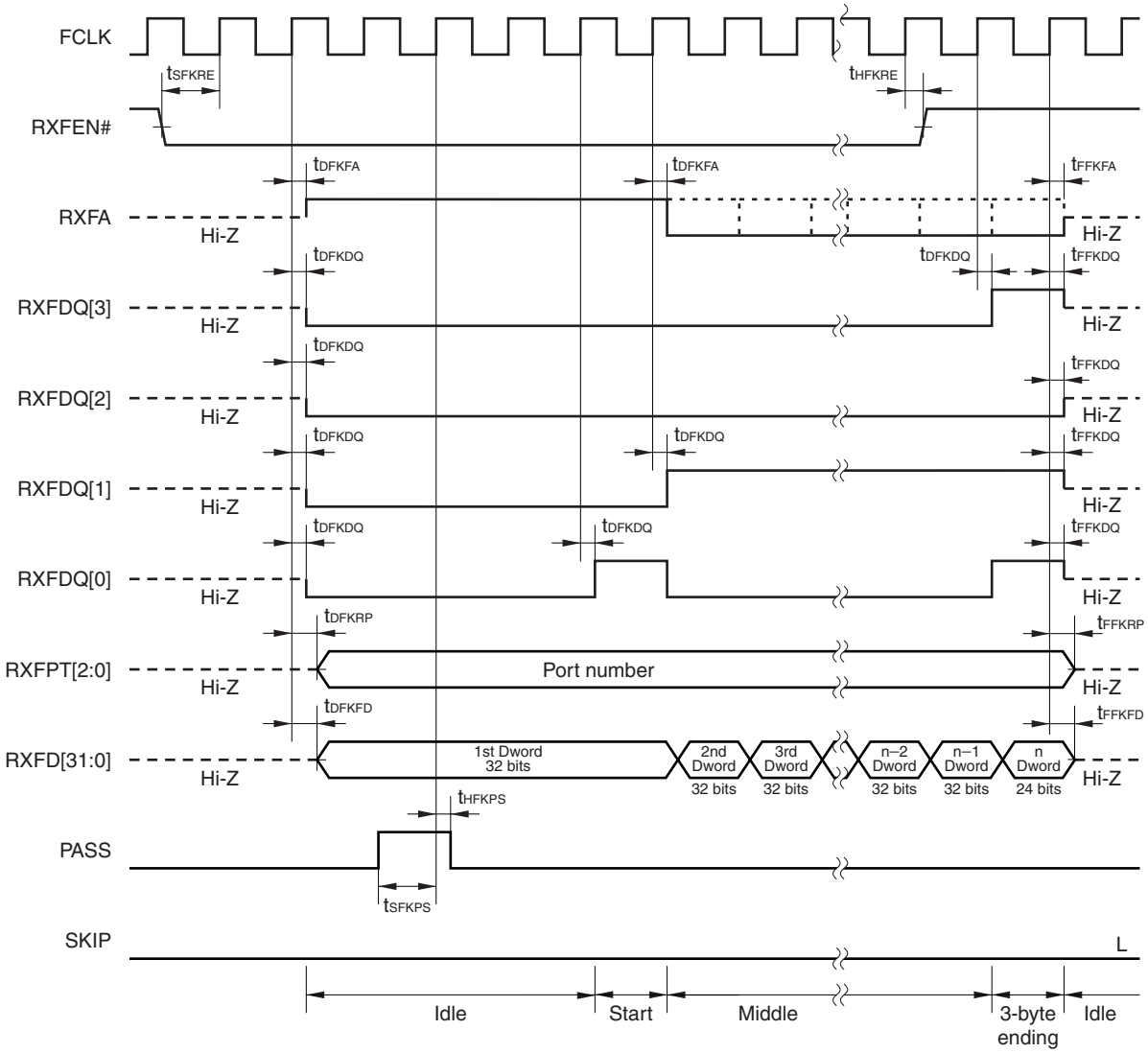


Remark TXFBA[N]: N = 0 to 7

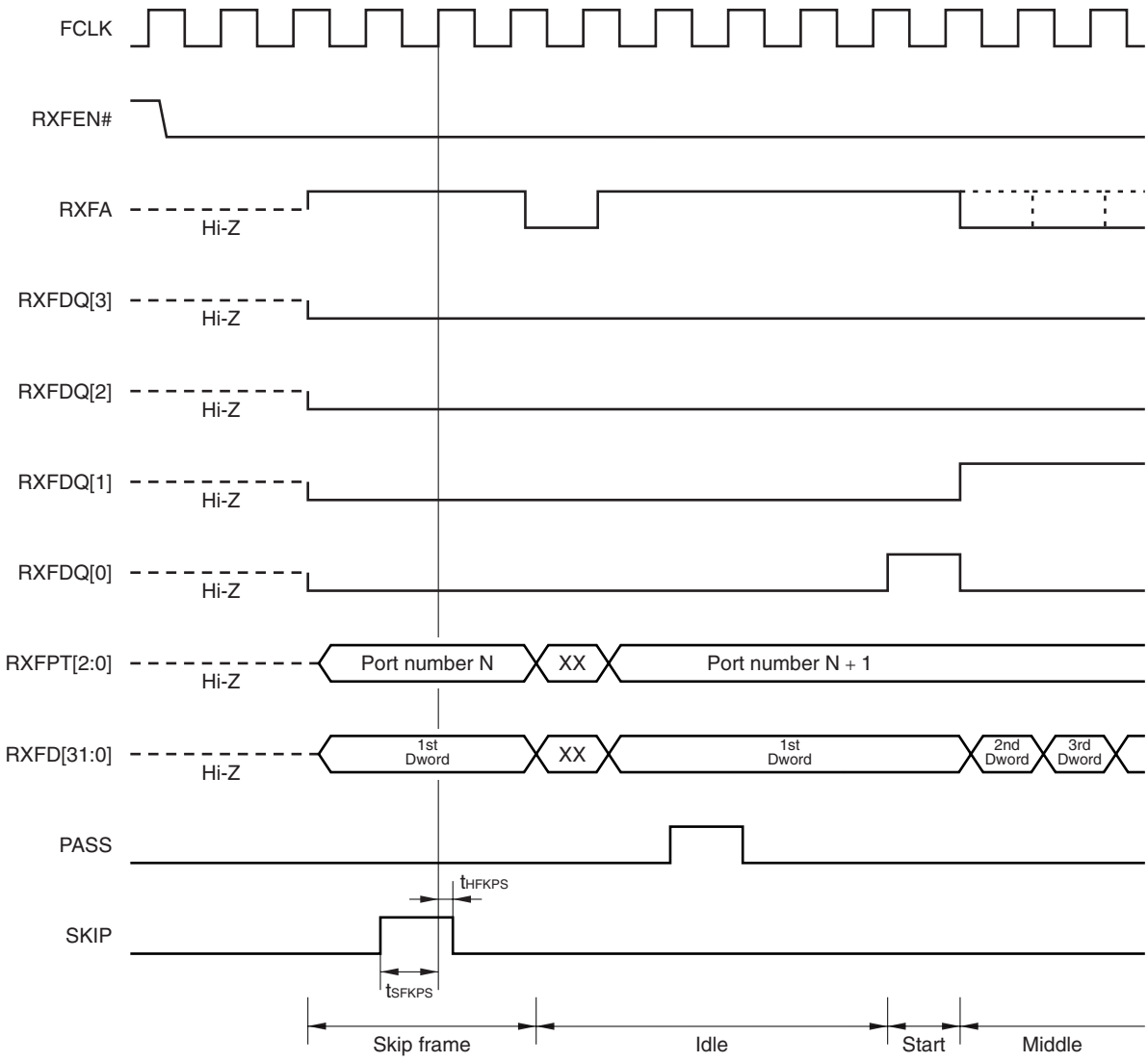
FIFO Bus Interface Read Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RXFA output delay time	t_{DFKFA}				10	ns
RXFA float time	t_{FFKFA}				10	ns
RXFDQ[3:0]/FDQ[3:0] output delay time	t_{DFKDQ}				10	ns
RXFDQ[3:0]/FDQ[3:0] float time	t_{FFKDQ}				10	ns
RXFPT[2:0] output delay time	t_{DFKRP}				10	ns
RXFPT[2:0] float time	t_{FFKRP}				10	ns
RXFD[31:0]/FD[63:0] output delay time	t_{DFKFD}				10	ns
RXFD[31:0]/FD[63:0] float time	t_{FFKFD}				10	ns
PASS setup time	t_{SFKPS}		5			ns
PASS hold time	t_{HFKPS}		0			ns
SKIP setup time	t_{SFKSP}		6			ns
SKIP hold time	t_{HFKSP}		0			ns

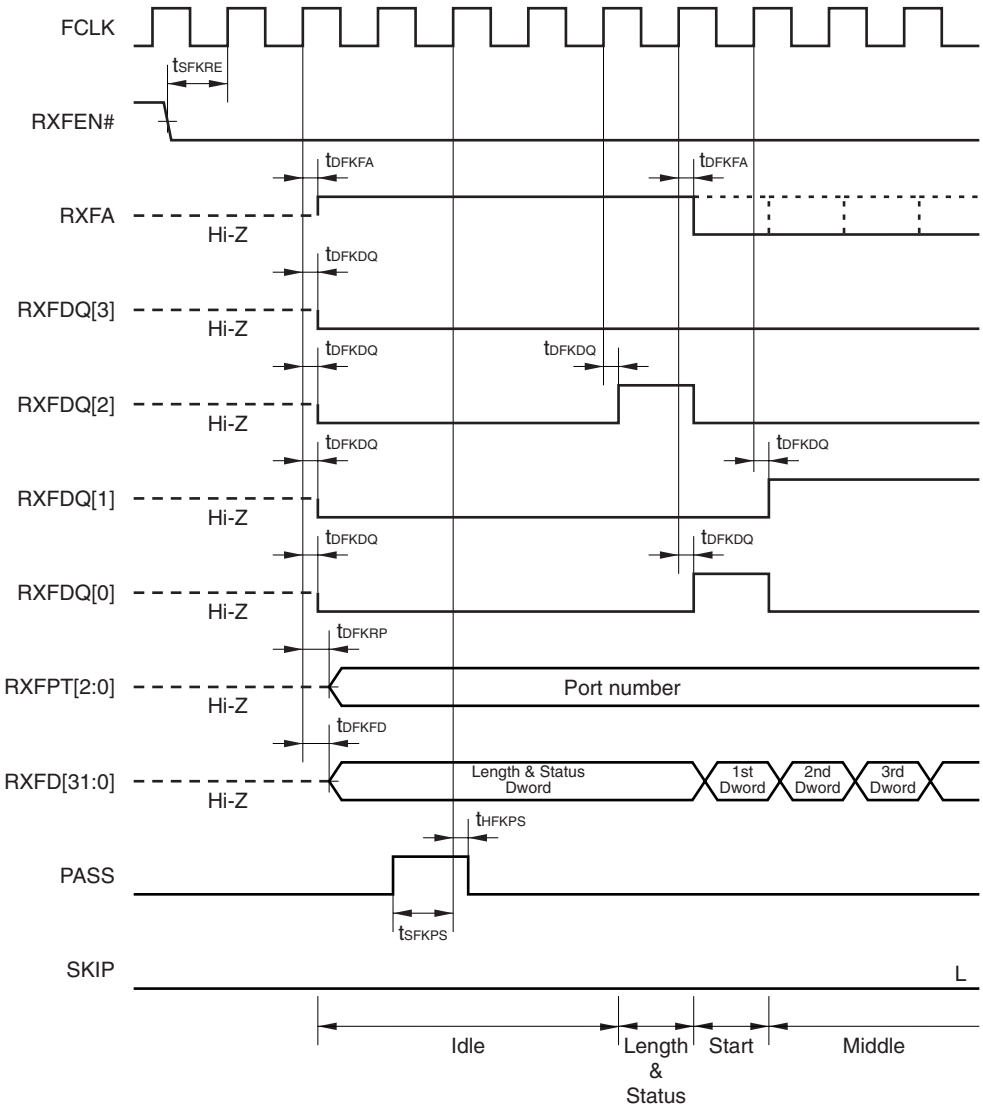
(1) FIFO bus interface read timing (32-bit dual bus mode) 1



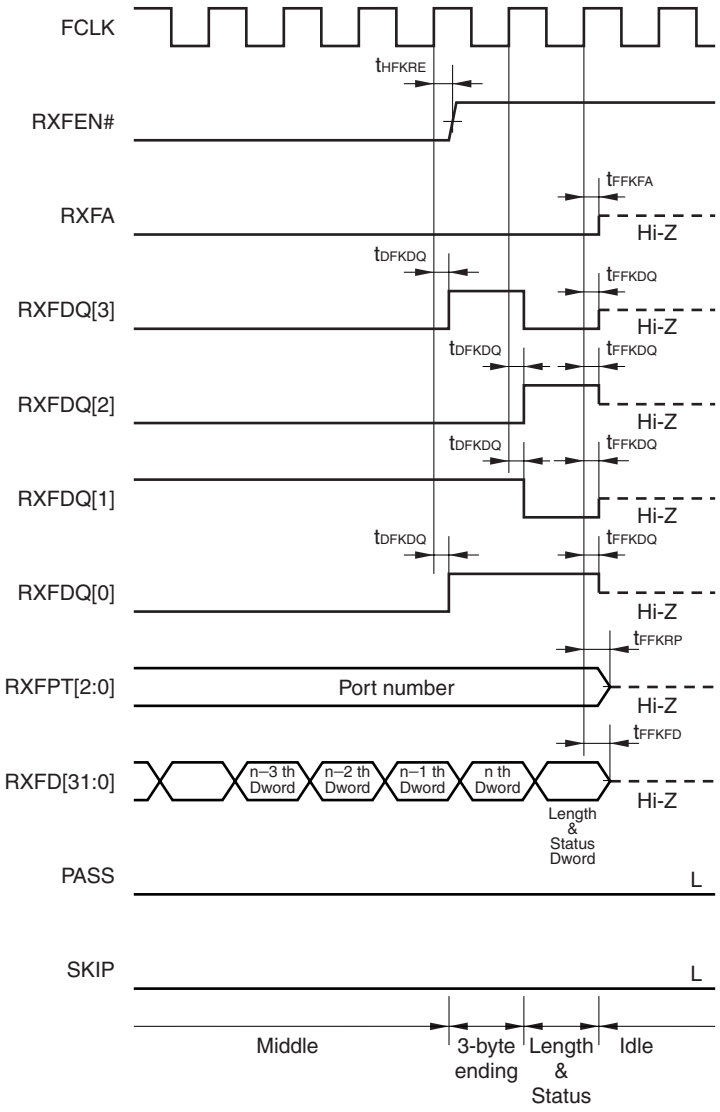
(2) FIFO bus interface read timing (32-bit dual bus mode) 2



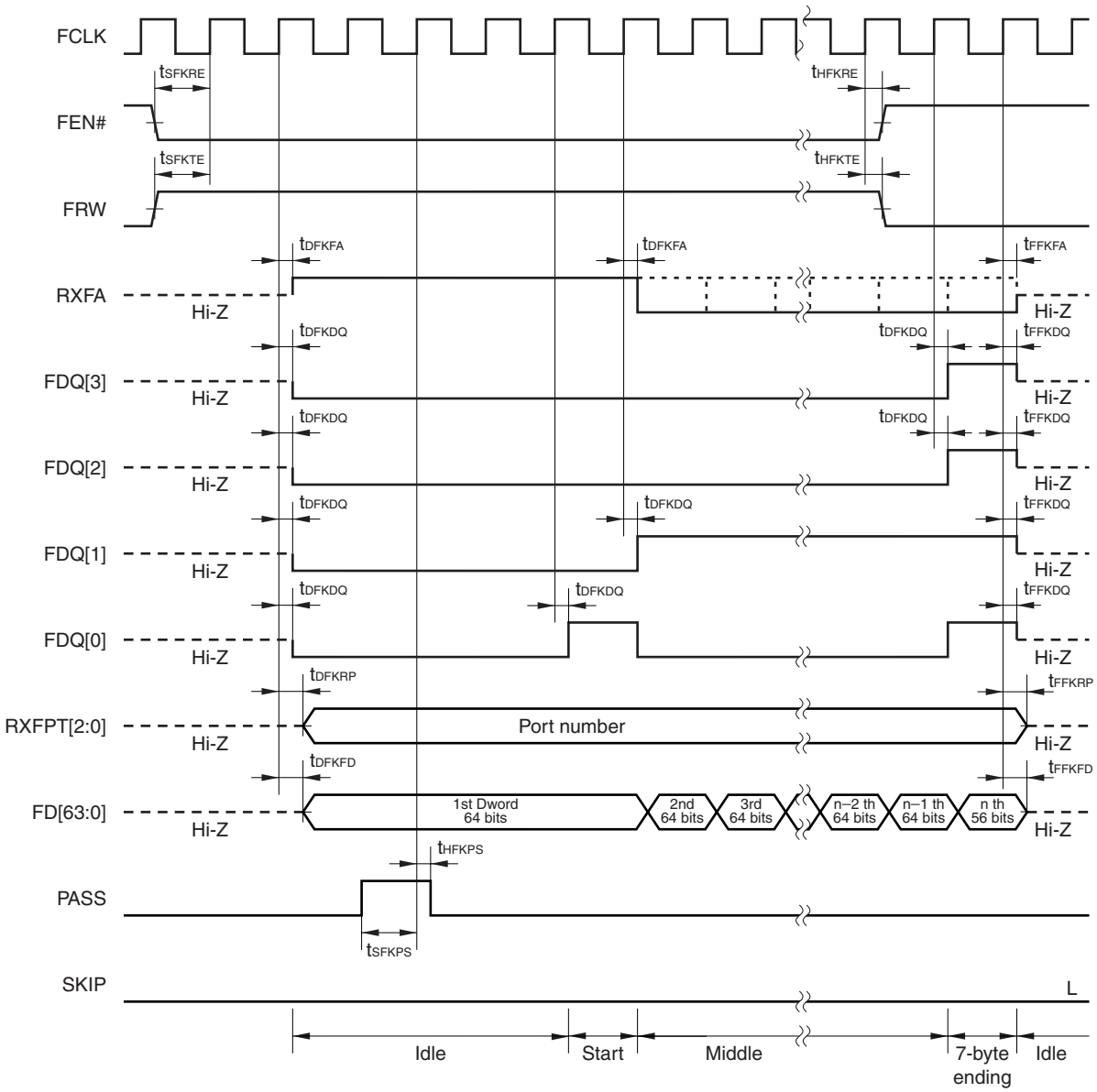
(3) FIFO bus interface read timing (32-bit dual bus mode) 3



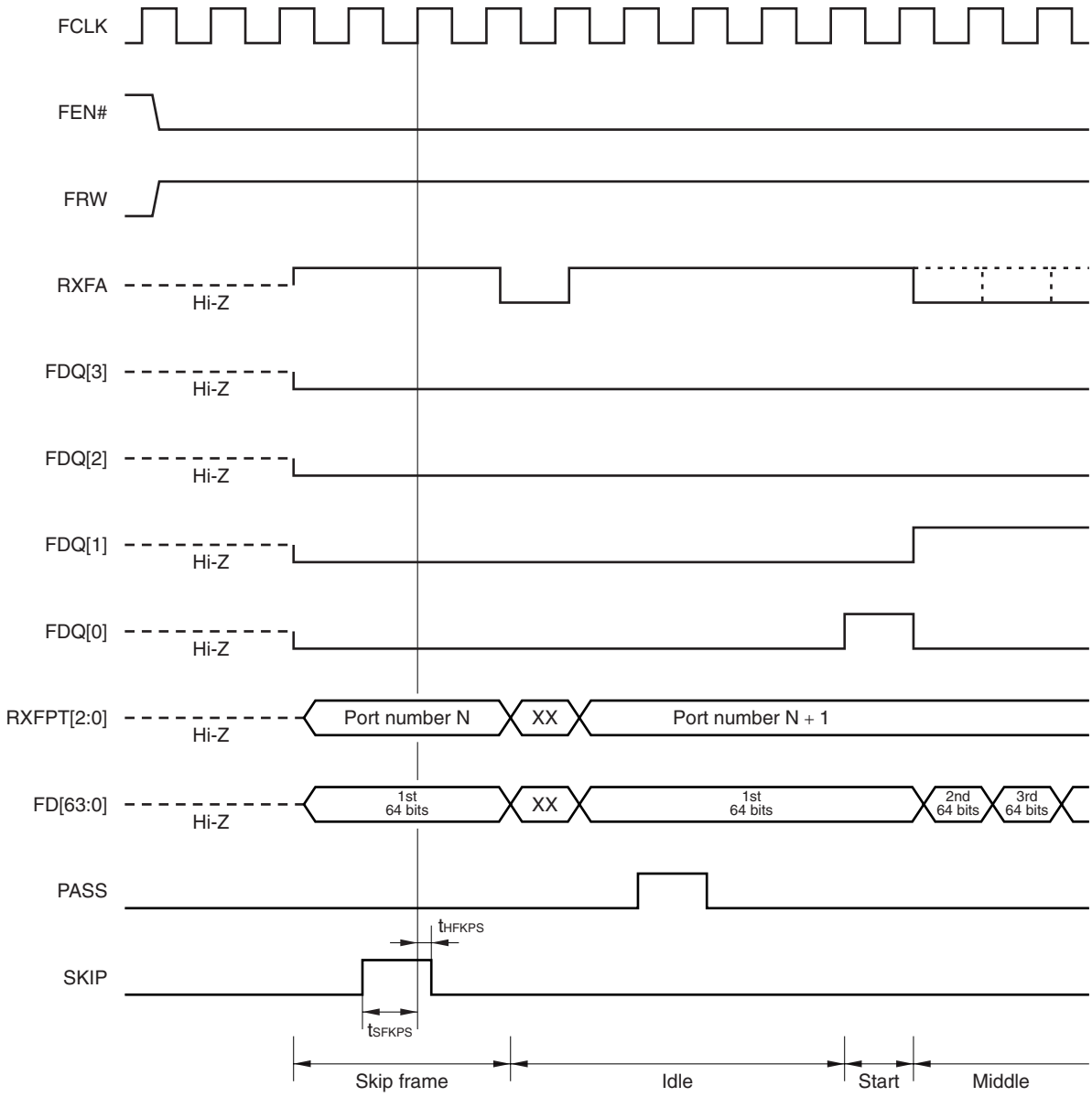
(4) FIFO bus interface read timing (32-bit dual bus mode) 4



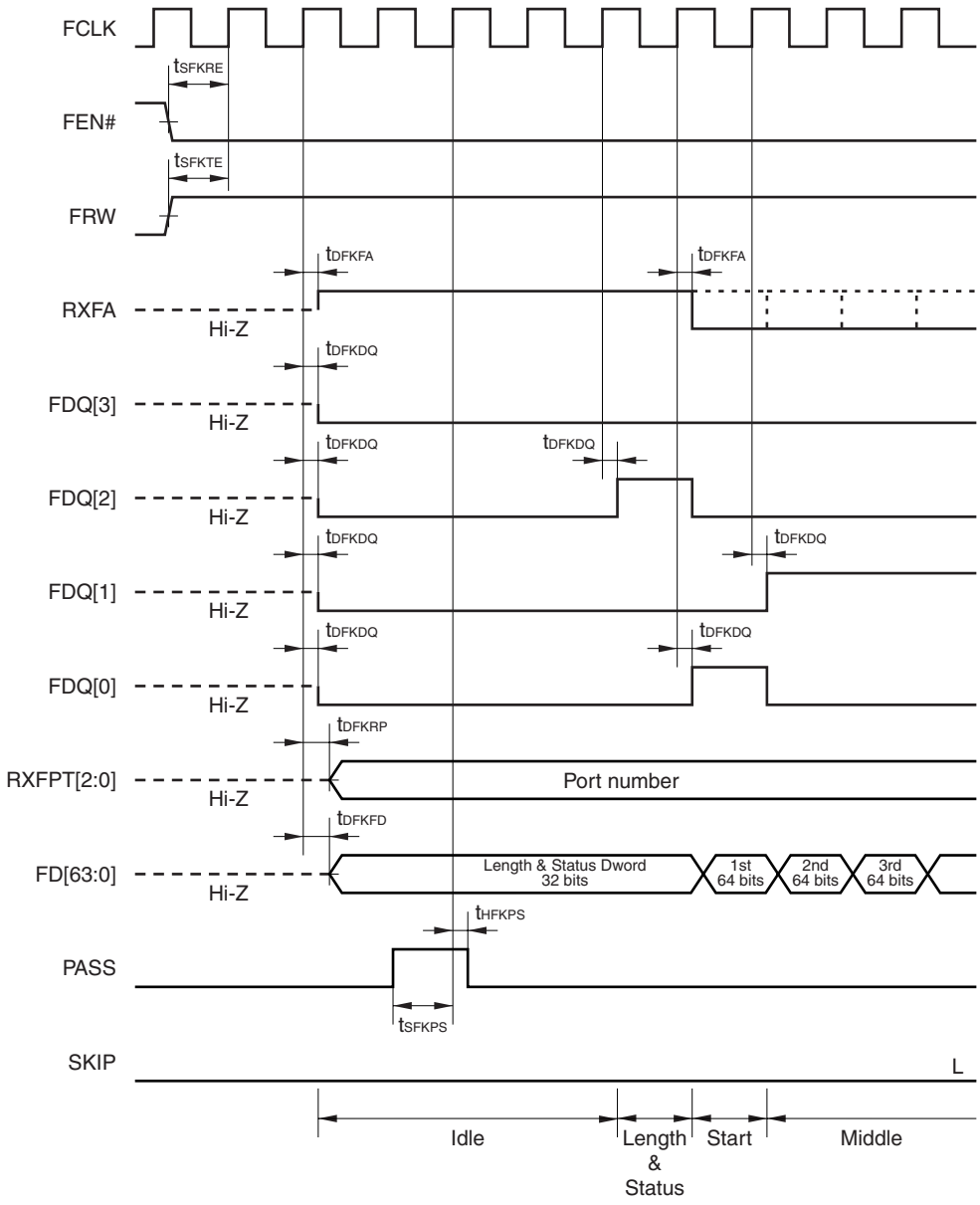
(5) FIFO bus interface read timing (64-bit single bus mode) 1



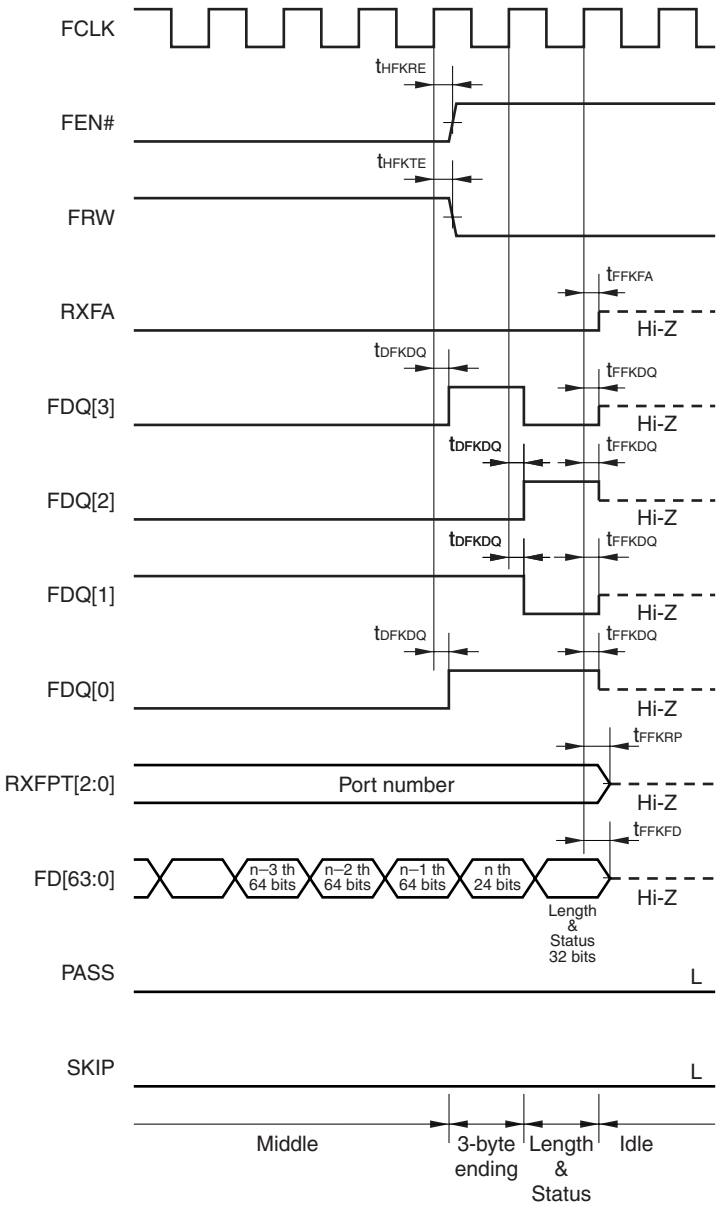
(6) FIFO bus interface read timing (64-bit single bus mode) 2



(7) FIFO bus interface read timing (64-bit single bus mode) 3

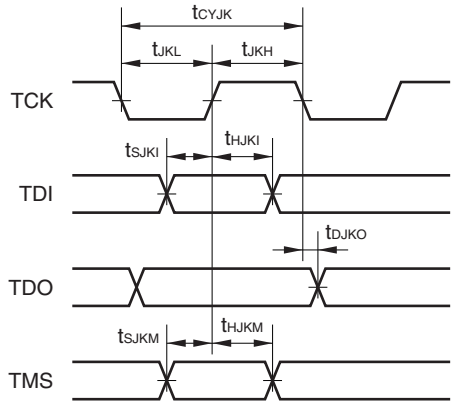


(8) FIFO bus interface read timing (64-bit single bus mode) 4



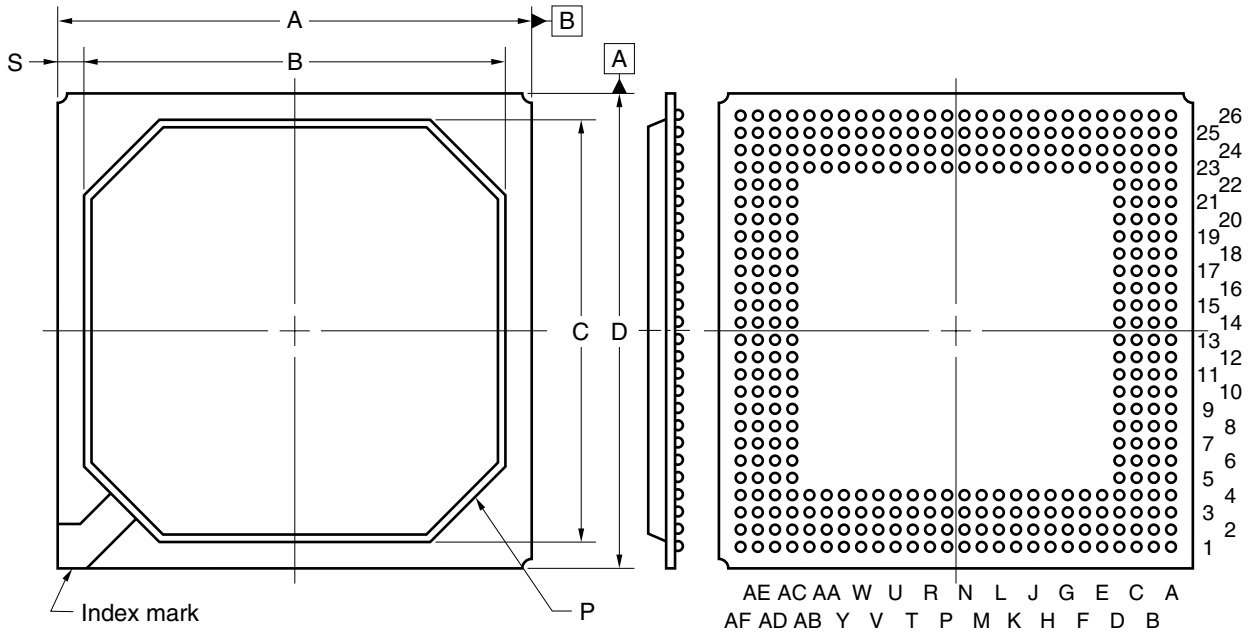
Boundary Scan (JTAG) Timing

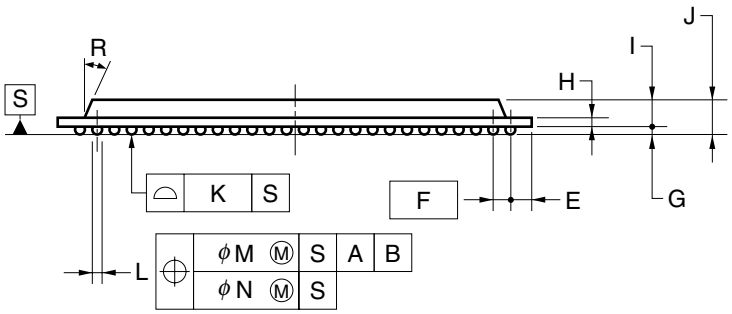
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCK clock width	t_{CYJK}		100			ns
TCK low-level width	t_{JKL}		50			ns
TCK high-level width	t_{JKH}		50			ns
TDI setup time	t_{SJKI}		5			ns
TDI hold time	t_{HJKI}		10			ns
TDO output delay time	t_{DJKO}				15	ns
TMS setup time	t_{SJKM}		5			ns
TMS hold time	t_{HJKM}		5			ns



3. PACKAGE DRAWING

352-PIN PLASTIC BGA (35x35)





ITEM	MILLIMETERS
A	35.00±0.20
B	32.0
C	32.0
D	35.00±0.20
E	1.62
F	1.27 (T.P.)
G	0.6±0.1
H	0.56
I	1.73±0.15
J	2.33±0.25
K	0.15
L	φ0.75±0.15
M	0.30
N	0.10
P	C4.0
R	25°
S	1.5

Y352S1-127-F6-4

4. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, contact your NEC sales representative.

Surface mounting type

μPD98431S1-F6: 352-pin plastic BGA (35 × 35)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR30-203-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Ethernet is a trademark of Xerox Corporation.

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