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FUJITSU

DATA SHEET

MB88510 SERIES

CMOS SINGLE CHIP 4-BIT MICROCOMPUTER WITH A/D CONVERTER

DESCRIPTION

The Fujitsu MB88510 series is a CMOS single–chip 4–bit microcomputer family is a CMOS version of the conventional NMOS MB88410 series. Its architecture and instruction set are upward the MB88500 series.

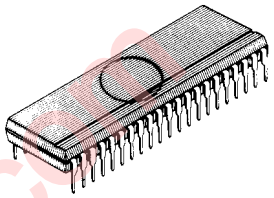
The MB88510 series consists of MB88511, MB88512, and MB88513. MB88511 contains a 4K by 8–bit mask ROM (program memory) and 256 by 4–bit static RAM (data memory) whereas, the MB88513 contains a 2K by 8–bit ROM and a 192 x 4–bit RAM. Besides the on–chip memory, each device has 34 I/O lines (including a serial port with a 4/8–bit buffer), an 8–bit timer/counter, a clock generator, and an 8–bit 4 channel programmable approximation type A/D converter. Otherwise, MB88512 contains 2K by 8–bit mask ROM and 128 by 4–bit static RAM. And 12 I/O lines, an 8–bit timer/counter, a clockgenerator, and an 8–bit 8–channel programmable approximation type A/D converter.

They are fabricated in silicon–gate CMOS process. MB88511 and MB88513 are housed in a 42–pin plastic standard/shrink DIP or 48–pin plastic flat package. Whereas MB88512 is housed in a 28–pin plastic standard DIP. They require +5V power supply and maximum 3MHz clock (6MHz clock with the prescaler), they operate 2.0µs minimum over a temperature range of –40°C to +85°C.

CMOS technology allows the device to operate with low power dissipation (6 mA max. using fc=1 MHz) and further the standby function (if implemented) enables data retention with lower current (15 µA max. using fc = 0MHz.)

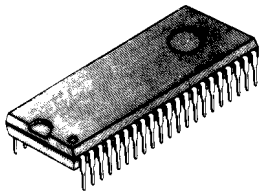
For user's development of the MB88510 series based system, Fujitsu provides the MB88400/500 cross assembler and host emulator which run on the PC–DOS machine, the MB2115 series evaluation tool system, and the MB88PG511/MB88PG512 piggyback devices which have an external 8K x 8–bit EPROM (MBM27C64). These development tools enables users to minimize their development time and cost.

MB88511–P/MB88513–P



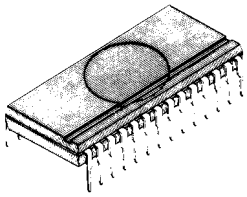
42–PIN PLASTIC STANDARD DIP
(DIP–42P–M01)

MB88511–PSH/MB88513–PSH



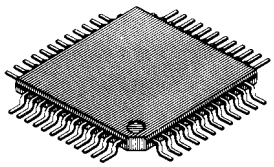
42–PIN PLASTIC SHRINK DIP
(DIP–42P–M02)

MB88512–P



28–PIN PLASTIC STANDARD DIP
(DIP–28P–M02)

MB88511–PF/MB88513–PF



48–PIN PLASTIC FLAT PACKAGE
(FPT–48P–M02)

MB88PG511–C **MB88PG512–C**

(See page 41, 42)

42–PIN CERAMI MODULE (MDP–42C–P04) **28–PIN CERAMIC MODULE (MDP–28C–P01)**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

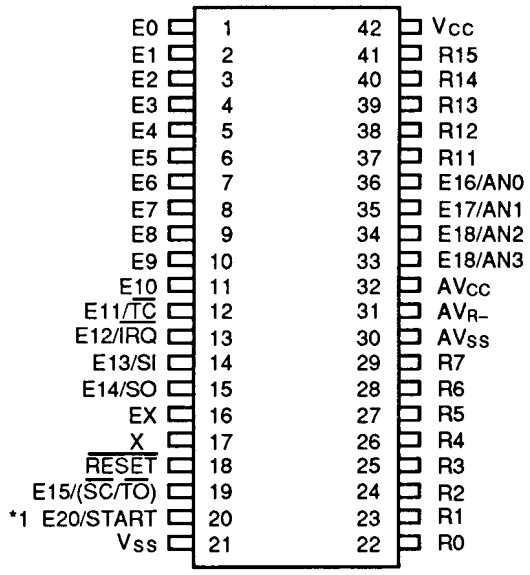
FEATURES

- CMOS Single–chip 4–bit Microcomputer
- Program Memory:
  - o MB88511 :4K x 8–bit mask ROM
  - o MB88512 and MB88513 :2K x 8–bit mask ROM
- Data Memory:
  - o MB88511 :256 x 4–bit static RAM
  - o MB88512 :128 x 4–bit static RAM
  - o MB88513 :192 x 4–bit static RAM
- I/O Lines:
  - o MB88511 and MB88513: 34 I/O lines
    - – R–Port: Three 4–bit/One 1–bit parallel input/output or 13 individual input/output
    - – E–Port: Five 4–bit/One 1–bit parallel input/output or 21 individual output
      Following ports have an other features.
      E16–E19 :Serial I/O, interrupt input, timer/counter input, and timing output
      E11–E15 :8–bit 4–channel A/D converter input
      E20 :Standby release input
  - o MB88512: 12 I/O lines
    - – R–Port: Three 4–bit parallel input/output or 12 individual input/output
      Following ports have an other features.
      R8, R9 :Interrupt input and timing output
- 8–bit Programmable Successive Approximation Type A/D Converter with Sample–hold Circuit:
  - o MB88511 and MB88513 :4 channel
  - o MB88512 :8 channel
- Five (Two) Selectable Output Port Types for E–, and R–Ports with Mask Option:
  - o Standard open–drain
  - o Standard pull-up
  - o 12V interface open–drain (Only applied to MB88511 and MB88513)
  - o High–current interface open–drain (Only applied to MB88511 and MB88513)
  - o High–current pull–up (Only applied to MB88511 and MB88513)
- 8–bit Programmable Timer/Counter with Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)
- Software Selectable 4–/8–bit Serial Buffer with Three Software Selectable Shift Clock Modes (Only applied to MB88511 and MB88513):
  - o Internal clock
  - o External clock
  - o Software clock
- On–chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC–network or external clock drive
- Divide–by–two Clock Prescaler for Expanding Clock Range with Mask Option
- Single Level Four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty
- 8–nesting Levels for Subroutine Calls
- Instruction Set: Upward compatible with the MB88500 series instruction set
  - o Number of instructions : – MB88511 and MB88513: 79
    – MB88512 : 69
  - o Instruction length/cycle : – 1 byte/1 cycle, 2 byte/2 cycle, and 2 byte/3 cycle

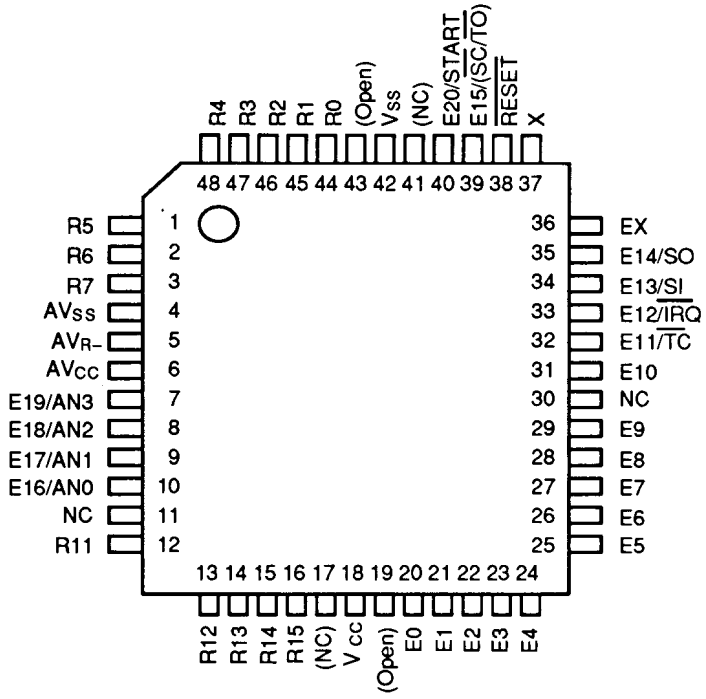
- o Execution time : 2.0 µs min. using 6.0 MHz clock with prescaler
- On–chip Power–on Reset Circuit
- Low Power Standby Function with Mask Option:
  - o No standby function
  - o Software–initiation standby function
- Two Output States During Standby with Mask Option:
  - o Hold
  - o High Impedance
- Two Software Selectable Oscillator States During Standby:
  - o Idle
  - o Stop
- Standby Off Reset with Mask Option:
- Watch Dog Timer Function with Mask Option
- Low Power Dissipation:
  - o 6 mA at Vcc = 5.5 V at fc = 1 MHz max. (Active mode)
  - o 15 µA at Vcc = 6.0 V at fc = 0 MHz max. (Standby mode)
- +5V Power Supply:
  - o 4.5 V to 5.5 V (Active mode)
  - o 3.5 V to 6.0 V (Standby mode)
- Wide Operation Temperating Range: T_A=–40°C to +85°C
- Silicon Gate CMOS Technology
- Package Options:
  - o MB88511 and MB88513
    - – 42–pin plastic standard DIP :suffix –P
    - – 42–pin plastic shrink DIP :suffix –PSH
    - – 48–pin plastic flat package :suffix –PF
  - o MB88512
    - – 28–pin plastic standard DIP :suffix –P
- Powerful Development Support:
  - o PC–DOS cross–assembler (SM07615–AXXX)
  - o PC–DOS host emulator software for monitoring evaluation tool and symbolic debugging (SM07615–GXXX)
  - o MB2115 series evaluation tool for software debugging
    - – MB88511 and MB88513 : MB2115–01, –02, –04 (–100), and –38
    - – MB88512 : MB2115–01, –02, –04 (–100), and –44
  - o CMOS piggyback EPROM evaluation devices:
    - – MB88511 and MB88513 :MB88PG511
    - – MB88512 :MB88PG512

Figure 1 MB88511, MB88513, and MB88PG511 Pin Assignment

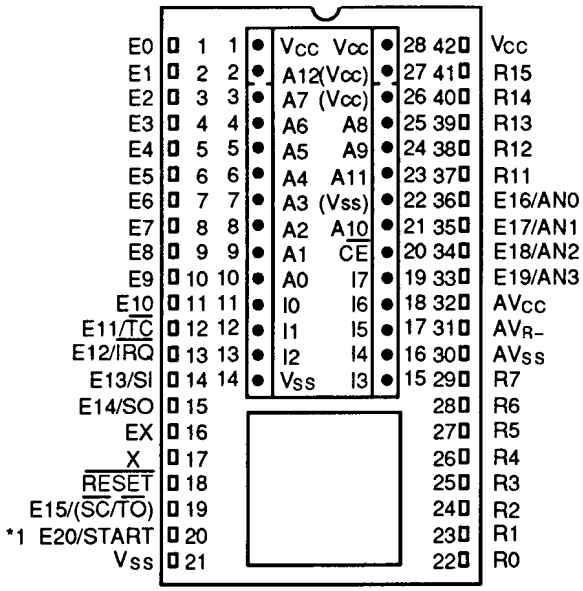
MB88511–P/–PSH and MB88513–P/PSH
(Top view)



MB88511–PF and MB88513–PF
(Top view)



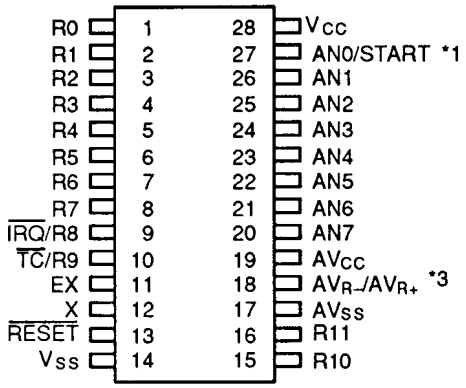
MB88PG511–C
(Top view)



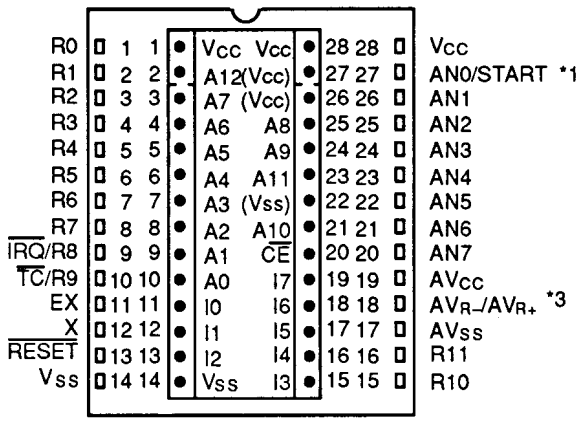
Notes: *1 Either E20 or START pin is selected using mask option.

Figure 2 MB88512 and MB88PG512 Pin Assignment

MB88512–P
(Top view)

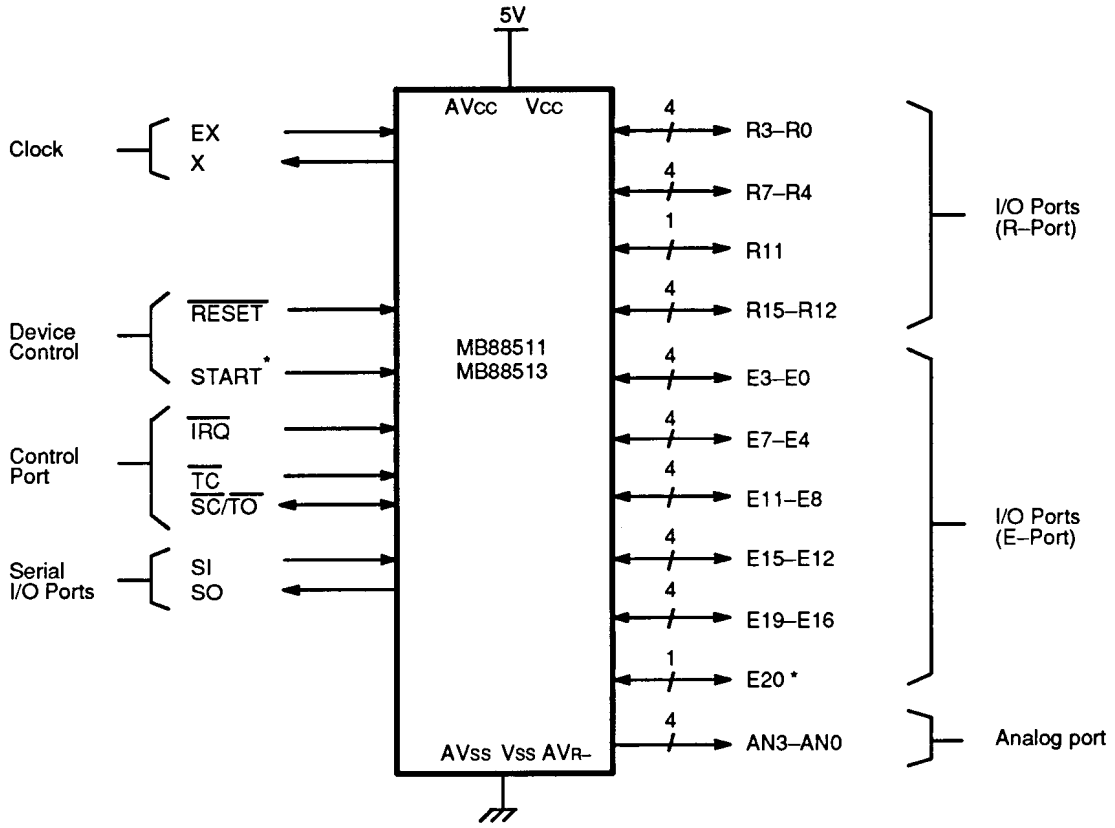


MB88PG512–C
(Top view)



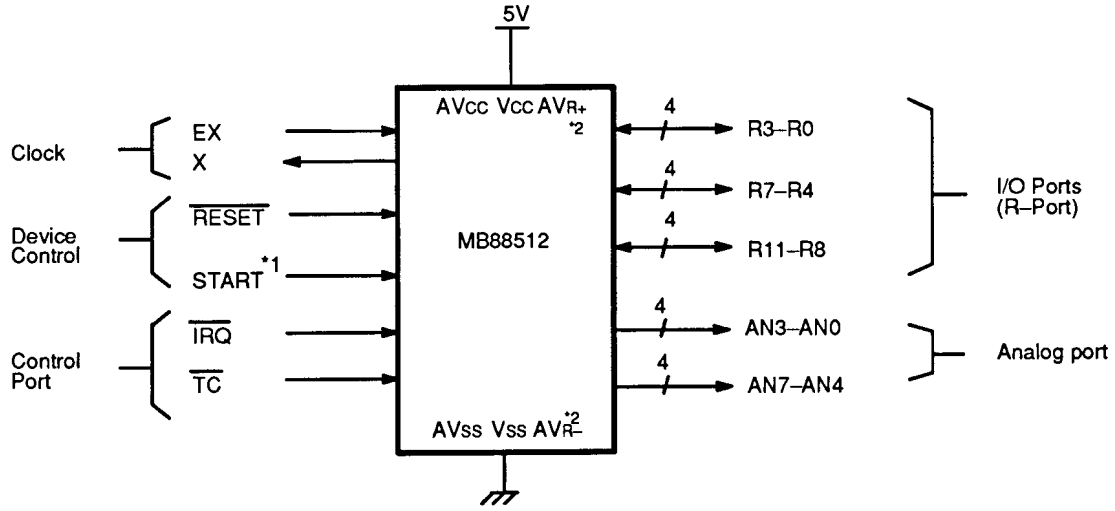
Notes: *1 Either AN0 or START pin is selected using mask option.
*2 Either AV_{R-} or AV_{R+} pin is selected using mask option.

Figure 3 MB88511 and MB88513 Logic Symbol



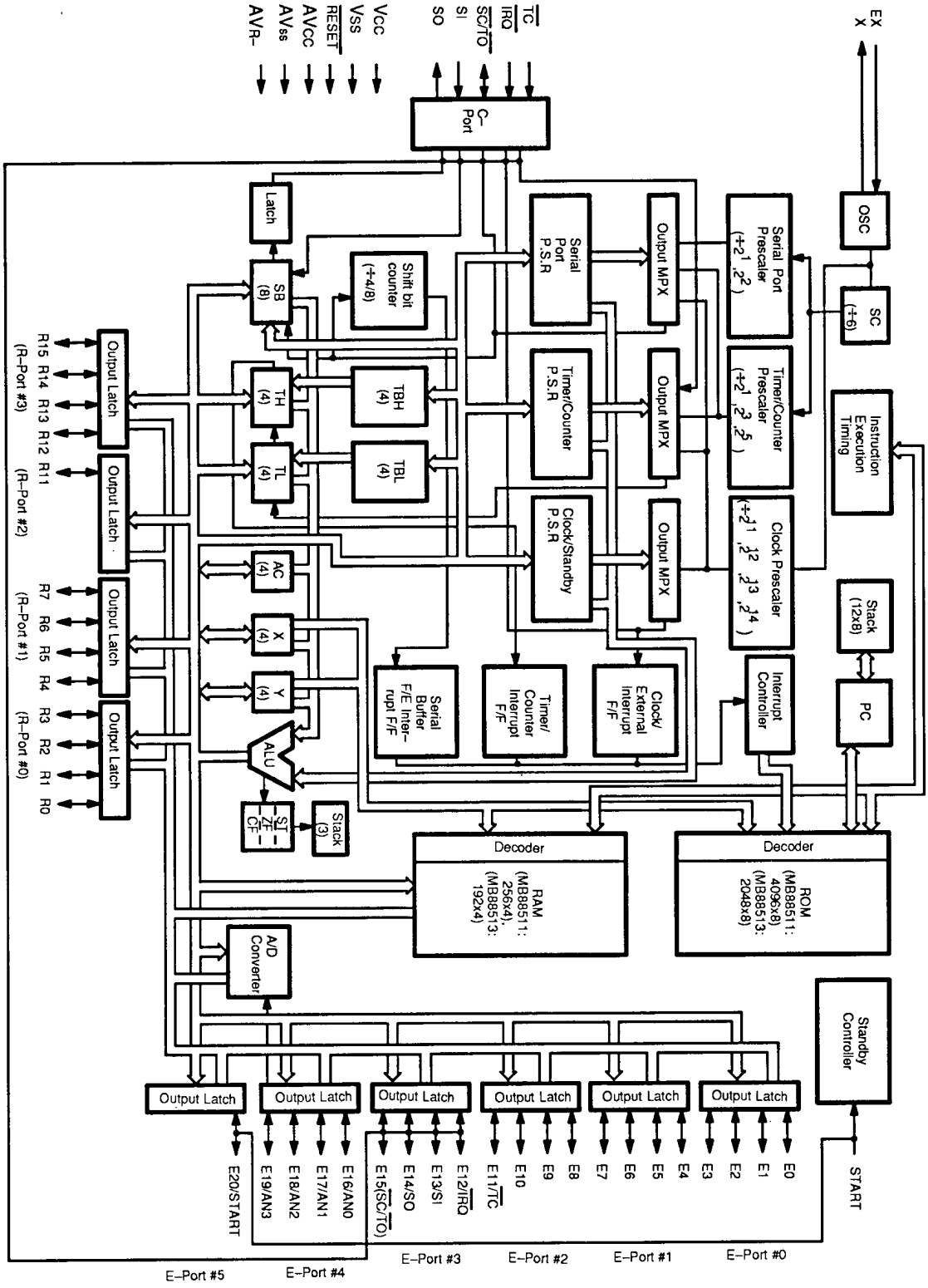
Note: * Either E20 or START pin is selected using mask option.

Figure 4 MB88512 Logic Symbol



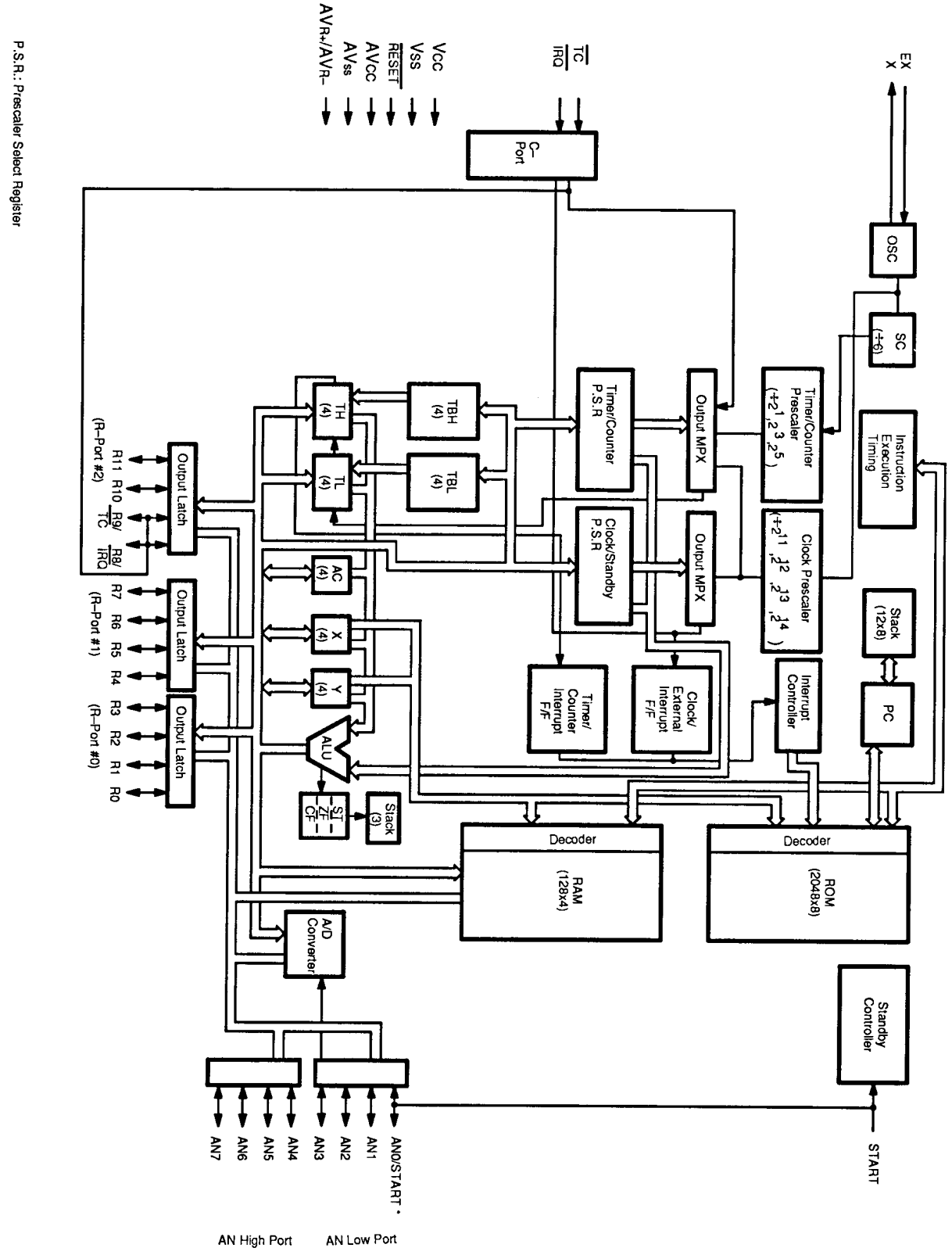
Notes: *1 Either E20 or START pin is selected using mask option.
*2 Either AV_{R+} or AV_{R-} pin is selected using mask option.

Figure 5 MB88511 and MB88513 Block Diagram



P.S.R.: Prescaler Select Register

Figure 6 MB88512 Block Diagram



PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB88510 series.

Table 1 Pin Description

Symbol	Pin No.		Type	Name & Function
	MB88511 MB88513	MB88512		
Power Supply				
Vcc	42(18)	28	—	+5V DC power supply pin.
Vss	21(42)	14	—	Ground pin.
Clock				
EX	16(36)	11	I	**Oscillator Input:** Input to the inverting amplifier that forms the on–chip oscillator. An external crystal/ceramic resonator or RC–network is connected between the EX and X pins. Either of these two oscillation types can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non–hysteresis input when the crystal/ceramic oscillator is selected, and a hysteresis input when the RC–network oscillator is selected.
X	17(37)	12	O	**Oscillator Output**: Output of the inverting amplifier that forms the on–chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC–network is connected between the EX and X pins. Either of these two oscillator types can be selected using mask option. When an external oscillator is used, the X pin should be left open.
Device Control				
$\overline{\text{RESET}}$	18(38)	13	I	**Reset:** This pin functions as an external reset input or power–on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{\text{RESET}}$ pin forcedly stops the MCU's operations, and initializes its internal state. After the $\overline{\text{RESET}}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{\text{RESET}}$ pulse must be low for at least two instruction cycleswhile the oscillator is stably running after power on. This pin is a hysteresis input with an internal pullup resistor. An external capacitor from the $\overline{\text{RESET}}$ pin to the Vss pin (and the internal pull–up resistor), whose time constant should be greater than the reset time required (12 clock periods) composes the external reset circuit. Power on reset output: A reset output from the on–chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the Vcc voltage after power on outputs a low level on the $\overline{\text{RESET}}$ pin, and them automatically returns high 2^8clock periods (62ms), after the oscillator starts by power on. This pin is a hysteresis input with an internal pull–up resistor.
START	20(40)	27	I	**Start**: A standby release input to the internal standby control and statusregisters that control and monitor the on–chip standby control circuit. A high level on the START pin during the standby mode sets the standby release flag (STF) in the standby status register, resets the standby enable flag (STBE) in the standby control register, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the Vcc voltage must return to the active operation range when the battery back up is used. Also, the START pin must be low before the standby mode is initiated.

Table 1 Pin Discription (Continued)

Symbol	Pin No. MB88511 MB88513	Pin No. MB88512	Type	Name & Function
Device Control (Continued)				
START	20(40)	27	I	The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the standby status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8). This pin is a hysteresis input with an internal pull–down resistor. This pin a common to the E20 or AN0 pins, case of the MB88511/513 or MB88512.
C–Port				
$\overline{IRQ}$	13(33)	9	I	**Interrupt Request:** A maskable external interrupt input to the on–chip interrupt control circuit. The falling edge of the $\overline{IRQ}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{IRQ}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{IRQ}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pull–up resistor. This pin a common to the E12 or R8 pins, case of the MB88511/513 or MB88512.
$\overline{TC}$	12(32)	10	I	**Timer/Counter**: An external count clock input to the on–chip 8–bit timer/counter. The falling edge of the $\overline{TC}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming, the timer/counter prescaler select register using OUT instruction (with Y=B). Also the $\overline{TC}$ pin state (logical level), which is reflected in the timer/counter input flag (TCIF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter mode, is testable by reading the prescaler select register using IN instruction (with Y = B). (When $\overline{TC}$ = L, TCIF = 1; otherwise TCIF = 0.) This pin is inactive as a count clock input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pull–up resistor. This pin is a common to the E11 pin.
$\overline{SC}/\overline{TO}$	19(39)	–	i/O I O	**Shift Clock/Timing Output:** One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction. $\overline{SC}$: 1) Shift clock input to the on–chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selected or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2) Shift clock output from the on–chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization. $\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on–chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output.

Table 1 Pin Description (Continued)

Symbol	Pin No. MB88511 MB88513	Pin No. MB88512	Type	Name & Function
C-Port (Continued)				
$\overline{SC}/\overline{TO}$	19(39)	–	I/O	This pin is a hysteresis input with an internal pullup resistor. This pin is a common to the E15 pin.
SI	14(34)	–	I	**Serial Data Input**: Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instruction (with Y=A). This pin is a common to the E13 pin.
SO	15(35)	–	O	**Serial Data Output**: Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appears on the SO pin. This pin is a CMOS pull-up output, and is set high by reset. This pin is a common to the E14 pin.
I/O Ports				
R3–R0, R7–R4, R10–R8, R11, R15–R12	25–22(47–44), 29–26(3–1,48), – 37(12), 41–38(16–13)	4–1, 8–5 15,10,9, 16 –	I/O	**R-Port:** This port functions as 4-bit parallel input (non-latched)/output (latched) ports, or individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit (1-bit) port is named R-Port #0 (R3–R0), R-Port #1 (R7–R4), R-Port #2 (R11–R8), and R-Port #3 (R15–R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode.) Individual I/O: Each line from R15 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3–R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11–R8) is directly testable in particular by TSTD instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) Refer to Table 3 User mask options for available making option.
E3–E0, E7–E4, E11–E8, E15–E12, E19–E16, E20	4–1(23–20), 8–5(27–24), 12–9(32,31, 29,28), 19,15–13(39, 35–33), 33–36(7–10), 20(40)	–	I/O	**E-Port:** This port functions as five 4-bit parallel input (non-latched)/output (latched) ports, or 21 individual input (non-latched)/output (latched) lines, depending on instructions. Each 4-bit is named E-Port #0 (E3–E0), E-Port #1 (E7–E4), E-Port #2 (E11–E8), E-Port #3 (E15–E12), E-Port #4 (E19–E16), and E-Port #5 (E20) and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of E-Ports #0 to #5 by OUTX instruction. 4-bit data on the addressed port is input into the accumulator by INX instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode.) Individual output: A data of the accumulator is output to the each line by ANDX, ORX, and OUTX instruction. Refer to Table 3 User mask options for available making option.

Table 1 Pin Description (Continued)

Symbol	Pin No.		Type	Name & Function
	MB88511 MB88513	MB88512		
I/O Ports (Continued)				
NC	(11,17,30,41)	–	–	Non connection pin.
OPEN	(19,43)	–	–	**Open**: This pin should not to be connect.
A/D Converter Voltage				
AVcc	32(6)	19	–	A/D converter supply voltage.
AVss	30(4)	17	–	A/D converter ground pin.
AVR–	31(5)	–	–	A/D converter reference voltage.
AVR–/AVR+	–	18	–	A/D reference voltage. AVR– and AVR+ is selected by mask option.
AN3–AN0, AN7–AN4	33–36(7–10) –	24–27, 20–23	I	**8–bit Resolution A/D Converter Input**: Analog input pin are selectable from among the AN7 to AN0 by OUT (Y=D) instruction. Analog data is inputted from selected AN pin, it is Analog–to Digital converted by OUT (Y=9) instruction. And digital data stored into internal memory as 8 bits digital data. Low of 4 bits digital data transfer into the accumulator by IN (Y=E) instruction, and high of 4 bits digital data transfer into the accumulator by IN (Y=F) instruction. In the MB88511/513, analog input pins are common to the E19–E16. In the MB88512, AN0 is common to the START pin, AN0 should be select by the mask option. During standby mode, this function doesn't worked, and A/D converted data is not hold.

Note: Parenthesis number is applied to MB88511–PF and MB88513–PF.

INPUT/OUTPUT CIRCUITS

All input–only pins are internally pulled up, and all output–only and input/output pins except E–,P–, and R–Ports have push–pull output buffer (standard pull–up). E– and R–Ports can have push–pull (standard or high–current pull–up) or open–drain (standard or high–current, or 12 V interface)buffer using mask option.

Table 2 Input/Output Circuit

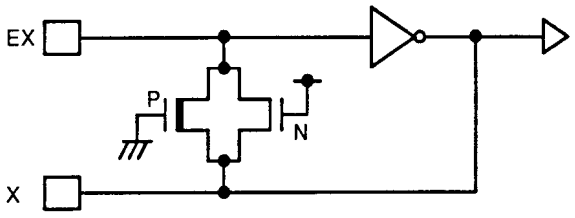
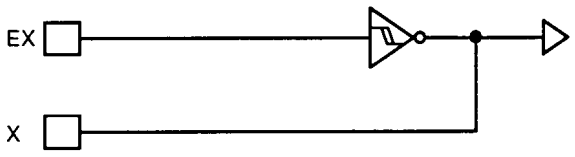
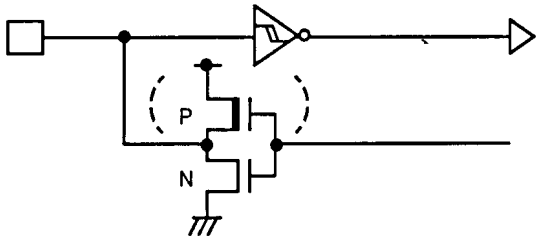
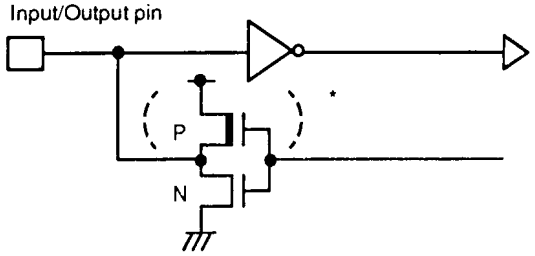
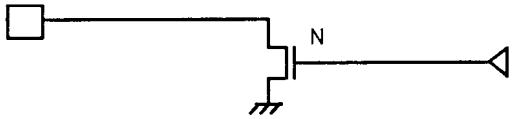
Pin	Circuit	Remarks
EX, X	• Crystal/Ceramic oscillation or external clock* 	1. Non–hysteresis inverter 2. Feedback resistor: Approx. 2 MΩ typ. (at Vcc=5V) * When only external clock drive is used, we recommend RC–network oscillation.
	• RC–Network oscillation or external clock* 	1. Hysteresis inverter 2. Without feedback resistor * When only external clock drive is used, we recommend RC–network oscillation.
$\overline{\text{RESET}}$	• Input/Output pin 	• Output pull–up resistor (P–ch. Tr.): Approx. 300kΩ typ. (at Vcc=5V)
MB88511/513: R15–R11, R7–R0, E10–E0 (Except 12V interface open–drain) MB88512: R11–R0	• Input/Output pin 	• Output port options for P–, and R–Ports 1: Standard/high–current pull–up: Pull–up resistor (P–ch. Tr.). Approx. 10kΩ typ. (at Vcc=5V) *2: Standard/high–current open–drain: Without P–ch. pull–up resistor ** High–current pull–up/open–drain outputs are only applied to MB88511 and MB88513.
MB88511/513: E10–E0 (Except 12V interface open–drain)	• Output only pin 	• 12V interface open–drain

Table 2 Input/Output Circuits (Continued)

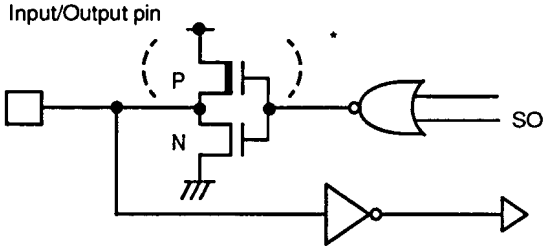
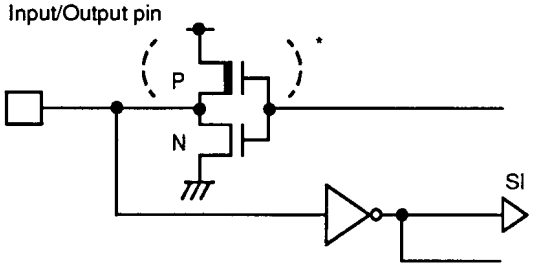
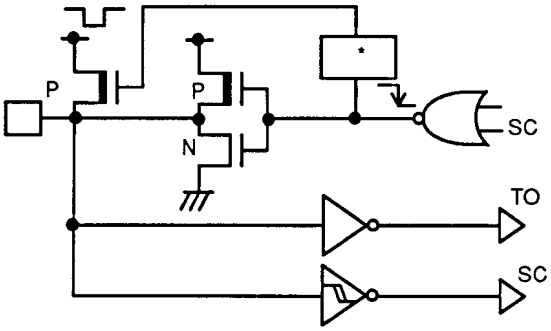
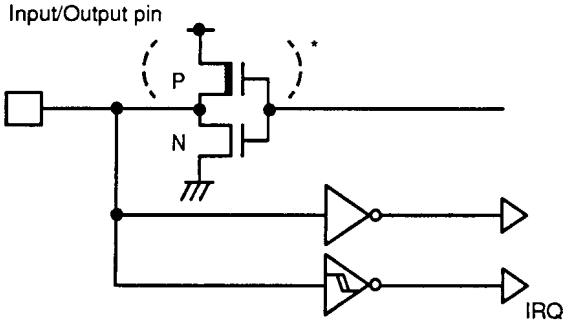
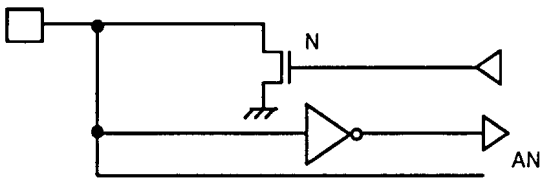
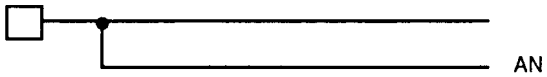
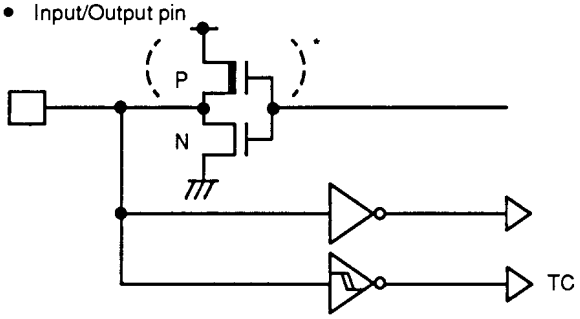
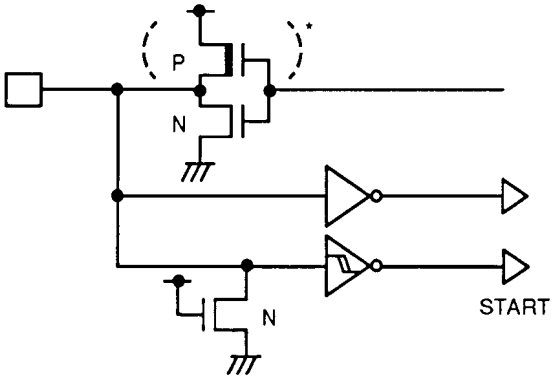
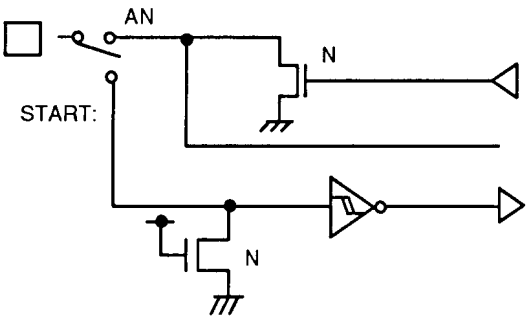
Pin	Circuit	Remarks
MB88511/513: E14/SO	• Input/Output pin 	• Output port options: 1: Standard/high–current pull–up: Pull–up resistor (P–ch. Tr.). Approx. 10kΩ typ. (at Vcc=5V) *2: Standard/high–current open–drain: Without P–ch. pull–up resistor ** High–current pull–up/open–drain outputs are only applied to MB88511 and MB88513.
MB88511/513: E13/SI	• Input/Output pin 	
MB88511/513: E15/SO	• Input/Output pin 	• With pull–up resistor P–ch. Tr. approx. 10kΩ: * This additional circuit makes the load MOS FET turn, at the timing when high level is output on the TO line, so that the TO line can goes high immediately.
MB88511/513: E12/$\overline{IRQ}$ MB88512: R8/$\overline{IRQ}$	• Input/Output pin 	• Output port options: 1: Standard/high–current pull–up: Pull–up resistor (P–ch. Tr.). Approx. 10kΩ typ. (at Vcc=5V) *2: Standard/high–current open–drain: Without P–ch. pull–up resistor ** High–current pull–up/open–drain outputs are only applied to MB88511 and MB88513.

Table 2 Input/Output Circuits (Continued)

Pin	Circuit	Remarks
MB88511/513: E16/AN0–E19/AN3	• Input/Output pin 	• Open–drain output
MB88512: AN0–AN7	• Input/Output pin 	• Open–drain output
MB88511/513: E11/$\overline{TC}$ MB88512: R9/$\overline{TC}$	• Input/Output pin 	• Output port options: 1: Standard/high–current pull–up: Pull–up resistor (P–ch. Tr.). Approx. 10kΩ typ. (at Vcc=5V) *2: Standard/high–current open–drain: Without P–ch. pull–up resistor ** High–current pull–up/open–drain outputs are only applied to MB88511 and MB88513.
MB88511/513: E20/START	• Input/Output pin 	E20: • Output port options: 1: Standard/high–current pull–up: Pull–up resistor (P–ch. Tr.). Approx. 10kΩ typ. (at Vcc=5V) *2: Standard/high–current open–drain: Without P–ch. pull–up resistor START: With N–ch. pull–down resistor approx. 300kΩ
MB88512: AN0/START	• Input/Output pin 	AN0: START: With N–ch. pull–down resistor (N–ch. Tr.): Approx. 300kΩ typ. (at Vcc=5.0V)

USER MASK OPTIONS

The MB88510 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 3 User Mask Options

Optional Feature	Symbol	Option	Option No.	Note	
Clock Prescaler	CLK	No	0	fc=1 MHz to 3 MHz	
		Yes	1	fc=2 MHz to 6 MHz	
Oscillation Type	OSC	Crystal/ceramic oscillation or External clock*	0	* When only external clock drive is used, we recommend RC–network oscillation.	
		Crystal/ceramic oscillation or External clock	1	We recommended no clock prescaler.	
Output Port Type (R–, E–Ports)	PORT	Standard open–drain	L	Except E15.	In the MB88511/513, mixed option is available.
		Standard pull–up	M	Except E19–E16.	
		High–current open–drain	K	Except E15. Only, MB88511/513.	
		High–current pull–up	T	Except E19–E15. Only, MB88511/513.	
		12V interface open–drain	G	Only E10–E0. Only, MB88511/513.	
Standby Function	STBY	No	0	MB88511/513 : Pin 20(40) is applied to E20. MB88512 : Pin 27 is applied to AN0.	
		Yes Software initiation	1	MB88511/513 : Pin 20(40) is applied to START. MB88512 : Pin 27 is applied to START.	
Output Port State During Standby	STATE	Hold	0	Output port state option selected should be the same for all of R–, and E–Ports.	
		High–Z	1		
Standby Off Reset Function	SOR	No	0		
		Yes	1		
Watch–Dog Timer	WDR	No	0		
		Yes	1	Only MB88511/513.	

NOTES ON OPERATION

• Latch–up Prevention

Latch–up may occur in CMOS devices when a voltage higher than Vcc or lower than Vss is applied to input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between Vcc and Vss pins. If latch–up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

• Treatment of Unused Pins

Unused input pins should be externally pulled up or down with resistors because such unused input pins may cause some malfunction if they are left open. (However, the X pin should be open when an external clock oscillator is used.)

• A/D Converter Supply

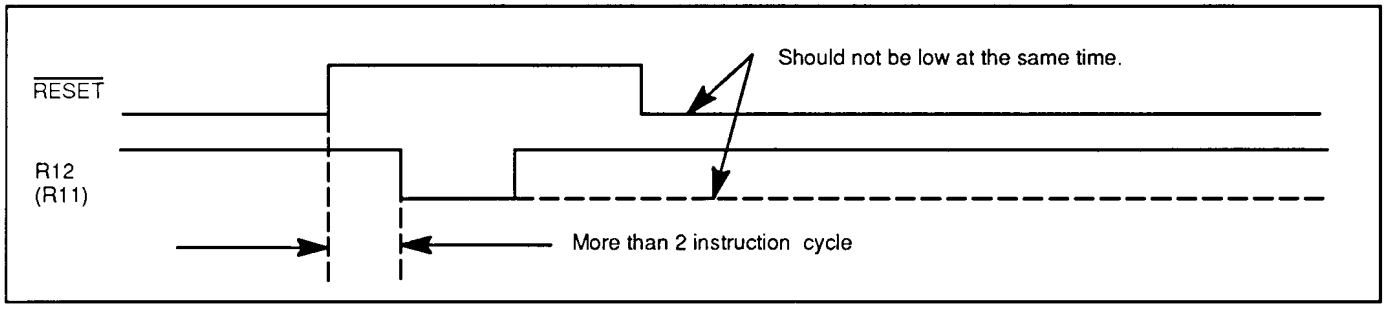
Even if the A/D converter function doesn't used, AVcc and AVss A/D converter supply should be connect the supply and ground.

• Special Function of R12 of MB88511/513 and R11 of MB88512 Pins

The R12 of MB88511/513 and R11 of MB88512 pin has another function as a test terminal, in addition to its normal function R–Port. If the R12 (R11) pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the R12 (R11) pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

Especially when the open–drain is selected for the output port option, the R12 (R11) pin should be externally pulled up because such open–drain outputs are subject to noise disturbance if left floating.

At least 2 instruction cycles are required to change R12 (R11) from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



• External Capacitors for Crystal Oscillation

Figures 9 gives an aim of an area where the on–chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use cystal with a freuency higher than required oscillation frequency, togetherwith the on–chip divided–by–two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

• Supply Voltage

Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:

(1) Vcc ripple (peak–to–peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical Vcc value.

(2) Vcc transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88510 series instructions set includes 79 of MB88511/513, 69 of MB88512 instructions, 78% (83%) of whichare single–byte and 20% (15%) two–byte two cycle, and 1% of two byte three cycle. The MB88510 series instruction set is theupward–compatible with the MB88500 series, and is divided into nine functional groups:

- Register–to–register transfer
- Register–to–memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/output
- Branch
- Flag manipulation

Table 4 and 5 summarizes the MB88510 series instruction set.

Table 4 Instruction Set Summary

	Mnemonic +Operand	Code (Hex.)	Flag/Status			Byte/ Cycle	Operation
			ZF	CF	ST		
Register–to–Register Transfer	TATH	05	•	•	•	1/1	TH ← (AC)
	TATL	06	•	•	•	1/1	TL ← (AC)
	TAS *4	07	•	•	•	1/1	SB ← (AC)
	TAY	04	•	•	•	1/1	Y ← (AC)
	TSA *4	17	•	•	•	1/1	4–bit mode: AC ← (SB_L) 8–bit mode: AC ← (SB_L), X ← (SB_H)
	TTHA	15	↕	•	•	1/1	AC ← (TH)
	TTLA	16	↕	•	•	1/1	AC ← (TL)
	TYA	14	↕	•	•	1/1	AC ← (Y)
	XX	1B	↕*1	•	•	1/1	(AC)⇆(X)
Register–to–Memory Transfer	L	0D	↕	•	•	1/1	AC ← {M(X,Y)}
	LS *4	2B	↕	•	•	1/1	SB ← {M(X,Y)}
	ST	1D	•	•	•	1/1	M(X,Y) ← (AC)
	STDC	1A	•	•	↓C	1/1	M(X,Y) ← (AC), Y ← (Y)–1
	STIC	0A	•	•	↓C	1/1	M(X,Y) ← (AC), Y ← (Y)+1
	STS *4	2A	↕	•	•	1/1	M(X,Y) ← (SB_L)
	X	0B	↓*1	•	•	1/1	(AC)⇆{M(X,Y)}
	XD D	50–53*	↓*1	•	•	1/1	(AC)⇆{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54–57*	↓*2	•	•	1/1	(Y) ⇆{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	•	•	1/1	AC ← 0 (Included in LI instruction)
	LI imm	90–9F*	↕	•	•	1/1	AC ← imm; imm=0 to 15
	LXI imm	58–5F*	↕	•	•	1/1	X3 ← 0, X2 to X0 ← imm; imm=0 to 7
	LXID	3D90–3D9F*	↕	•	•	2/2	X ← imm; imm=0 to 15
	LRXA imm	3D20–3D3F*	•	•	•	2/3	X ← { ROM (imm | X | Y) } d, d=7–4 AC ← { ROM (imm | X | Y) } d, d=3–0 imm=0 to 31
	LYI imm	80–8F*	↕	•	•	1/1	Y ← imm; imm=0 to 15

Table 4 Instruction Set Summary (Continued)

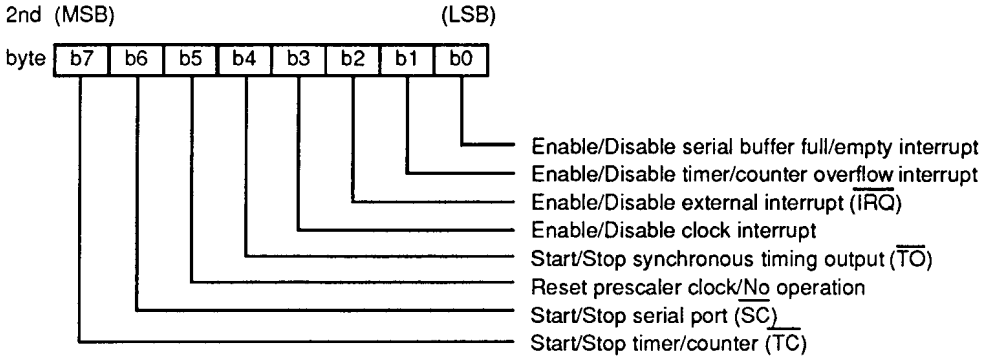
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	Flag/Status CF	Flag/Status ST	Byte/ Cycle	Operation
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC ← (AC)+{M(X,Y)}+(CF)
	AI imm	3D80–3D8F	↕	↕	↓C	2/2	AC ← (AC)+imm; imm=0 to 15
	AND	0F	↕	•	↓Z	1/1	AC ← (AC) ∩ {M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}–(AC)
	CI imm	B0–BF*	↕	↕	↓Z	1/1	imm–(AC); imm=0 to 15
	CYI imm	A0–AF*	•	•	↓Z	1/1	imm–(Y) ; imm=0 to 15
	DAA	10	•	↕	↓C	1/1	AC ← (AC)+6 if (AC) > 9 or (CF)=1
	DAS	11	•	↕	↓C	1/1	AC ← (AC)+10 if (AC) > 9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	2/2	AC ← (AC)+15(Included in AI instruction)
	DCM	19	↕	•	↓C	1/1	M(X,Y) ← {M(X,Y)} –1
	DCY	18	•	•	↓C	1/1	Y ← (Y)–1
	EOR	2F	↕	•	↓Z	1/1	AC ← {M(X,Y)} ⊕ (AC)
	ICA	3D81	↕	↕	↓C	2/2	AC ← (AC)+1(Included in AI instruction)
	ICM	09	↕	•	↓C	1/1	M(X,Y) ← {M(X,Y)}+1
	ICX	3DAC	•	•	↓C	2/2	X ← (X)+1
	ICY	08	↕	•	↓C	1/1	Y ← (Y)+1
	NEG	2D	•	•	↓Z	1/1	AC ← $\overline{(AC)}$+1
	OR	1F	↕	•	↓Z	1/1	AC ← {M(X,Y)} ∪ (AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC ← {M(X,Y)}–(AC)–(CF)
Bit Manipulation	RBIT bp	34–37*	•	•	•	1/1	{M(X,Y)}bp ← 0; bp=0 to 3
	SBIT bp	30–33*	•	•	•	1/1	{M(X,Y)}bp ← 1; bp=0 to 3
	RBA bp	3DA4–3DA7 *	•	•	•	2/2	(AC)bp ← 0 ; bp=0 to 3
	SBA bp	3DA0–3DA3 *	•	•	•	2/2	(AC)bp ← 1 ; bp=0 to 3
	TBA bp	4C–4F*	•	•	↓Z	1/1	(AC)bp–1 ; bp=0 to 3
	TBIT bp	38–3B*	•	•	↓Z	1/1	{M(X,Y)}bp–1 ; bp=0 to 3
Control	EN imm	3E00–3EFF*	•	•	•	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00–3FFF*	•	•	•	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	•	•	•	2/2	System initialization
Input/ Output	IN	13	↕	•	•	1/1	AC ← (R)Y ; Y=0 to 3 (Port #) AC ← (REG)Y ; Y=9 to 15
	INK *4	12	↕	•	•	1/1	AC ← (R15–R12)
	INX *4	3DAA	•	•	•	2/2	AC ← (E)Y ; Y=0 to 5 (Port #) *4
	OUT	03	•	•	•	1/1	(R)Y ← (AC); Y=0 to 3 (Port #) (REG)Y ← (R); Y=9 to 15
	OUTP *4	02	•	•	•	1/1	E3–E0 ← (AC)
	OUTX *4	3DAB	•	•	•	2/2	(E)Y ← (AC); Y=0 to 5 (Port #) *4
	ANDX *4	3DA8	•	•	•	2/2	(E)Y ← (AC) ∩ E(Y); Y=0 to 5 (Port #) *4
	ORX *4	3DA9	•	•	•	2/2	(E)Y ← (AC) ∪ E(Y); Y=0 to 5 (Port #) *4

Table 4 Instruction Set Summary (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Input/ Output	RSTD d	44–47*	•	•	•	1/1	(R)d ← 0; d=0 to 3 (Bit # of Port #)
	RSTR	22	•	•	•	1/1	MB88511/513:(R)Y ← 0;Y=0–7, 11–15 (Bit #) MB88512 :(R)Y ← 0;Y=0 to 11 (Bit #)
	SETD d	40–43*	•	•	•	1/1	(R)d ← 1; d=0 to 3 (Bit # of Port #0)
	SETR	20	•	•	•	1/1	MB88511/513:(R)Y ← 1; Y=0–7, 11–15 (Bit #) MB88512 :(R)Y ← 1; Y=0 to 11 (Bit #)
	TSTD d	48–4B*	•	•	↓C	1/1	MB88511/513:(R)d–1; d=11 (Bit #) MB88512 :(R)d–1; d=8 to 11 (Bit #)
	TSTR	24	•	•	↓C	1/1	MB88511/513:(R)Y–1; d=0–7, 8–15 (Bit #) MB88512 :(R)Y–1; d=0 to 11 (Bit #)
Branch	CALL addr	6000–6FFF*	•	•	•	2/2	If ST=1, Subroutine call for addr; addr=0 to 4095. ST=0, Not subroutine call.
	JMP addr	C0–FF*	•	•	•	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No branch.
	JPL addr	7000–7FFF*	•	•	•	2/2	If ST=1, Branch to addr; addr =0 to 4095. ST=0, No branch.
	JPXY addr	3D00–3D1F*	•	•	•	2/2	Branch always to addr on page #n;
	NOP	00	•	•	•	1/1	No operation
	RTI	3C	•	•	•	1/1	Return from interrupt routine
	RTS	2C	•	•	•	1/1	Return from subroutine
Flag Manipulation	RSTC	23	•	↓	•	1/1	CF ← 0
	SETC	21	•	↑	•	1/1	CF ← 1
	TSTC	28	•	•	↓CF	1/1	(CF)–1
	TSTI	25	•	•	↓IF	1/1	(IF)–1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	•	•	↓SF	1/1	(SF)–1, SF ← 0
	TSTV	26	•	•	↓VF	1/1	(VF)–1, VF ← 0
	TSTZ	29	•	•	↓ZF	1/1	(ZF)–1

Notes:

* : Code is variable depending on the operand.
*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows



*4: Available only for MB88511 and MB88513.

Symbols and Abbreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
•	Not affected

Abbreviations	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
E	E–Port (#0: E3–E0, #1: E7–E4, #2: E11–E8, E3: E15–E12, E4:E19–E16, and #5: E20) E–Port #n specified by Y–register (Y=0 to 5)
IF	Interrupt flag
imm	Immediate data
$\overline{IRQ}$	Interrupt request
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly adressed by data pointer (X– and Y–registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
R	R–Port (#0: R3–R0, #1: R7–R4, #2: R11–R8, #3: R15–R12)
(R)Y; Y=n	1) R–Port #n specified by Y–register (Y=0 to 3) 2) R–Port bit n specified by Y–register (Y=0 to 15)
(R)d; d=n	R–Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X–register (that indicates page # in data memory RAM)
Xn	The n–th bit of X–register
Y	Y–register
Z	Zero
ZF	Zero flag

Table 5 Instruction Code Summary

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	Unused	*1 OUTP	OUT	TAY	TATH	TATL	*1 TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	*1 INK	IN	TYA	TTHA	TTLA	*1 TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	*1 STS	*1 LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD d				XYD d				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

Notes: : 1–byte/1–cycle instruction : 2–byte/2–cycle instruction : See the next page.

Table 5 Instruction Code Summary Extended Instruction (Continued)

3DH \ 3DL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3																
4	Unused															
5																
6																
7																
8		(ICA)	AI imm													(DCA)
9	LXID imm															
A	SBA bp				RBA bp				*1 ANDX	*1 ORX	*1 INX	*1 OUTX	ICX	RST	Unused	
B	Unused															
C																
D																
E																
F																

Notes: ☐ : 2 byte/2 cycle instruction or 2 byte/3 cycle instruction

*1 : Available only for MB88511 and MB88513.

DIFFERENCES BETWEEN MB88500 SERIES AND MB88510 SERIES

Table 6 Difference Between MB88501 and MB88510 Series

Item \ Device	MB88501	MB88510 Series
ROM Size	• 4K x 8 bits	• MB88511 :4K x 8 bits • MB88512/513 :2K x 8 bits
RAM Size	• 192 x 4 bits	• MB88511 :256 x 4 bits • MB88512 :128 x 4 bits • MB88513 :192 x 4 bits
Minimum Instruction Execution Time	• 2.86µS	• 2.0 µs
I/O Port: –K–Port –P–Port –O–Port –R–Port –E–Port	• 36 – 4 bits x 1 – 4 bits x 1 – 8 bits x 1 – 4 bits x 4 – No	• MB88511/513:33 – No – No – No – 4 bits x 3 and 1 bit x 1 – 4 bits x 5 and 1 bit x 1 • MB88512:12 – No – No – No – 4 bits x 3 – No
Output PLA	• Yes	• No
Serial Buffer	• 4 bits	• MB88511/513 :4/8 bits software selectable • MB88512 :No
A/D Converter	• No	• MB88511/513 :8 bits resolution x 4 channel • MB88512 :8 bits resolution x 8 channel
Low–Voltage Reset Function	• Mask option	• No
Package	• 42 pin plastic standard DIP • 42 pin plastic shrink DIP • 48 pin plastic flat package	• 42 pin plastic standard DIP (MB88511/513) • 42 pin plastic shrink DIP (MB88511/513) • 48 pin plastic flat package (MB88511/513) • 28 pin plastic standard DIP (MB88512)
Instruction Number	• 75	• MB88511/513 :79 • MB88512 :69
Members	• MB88501–P/–P–SH/–PF A– and L–versions are available for each part above.	• MB88511–P/–PSH/–PF • MB88512–P • MB88513–P/–PSH/–PF

PRODUCT LINE–UP AND DEVELOPMENT TOOLS

The MB88510 series consists of the MB88511, MB88512, and MB88513. The MB88PG511 are available as piggyback EPROM evaluation devices of the MB88511/513 and MB88PG512 is MB88512. Refer to Table 7.

Table 7 MB88510 Series Product Line–up & Development Tools

	MB88511–P/–PSH/–PF (MB88513–P/–PSH/–PF)	MB88PG511–C–101/–102/–201/–202	MB88512–P	MB88PG512–C–101/–102/–103
ROM Size	4K x 8 bits (2K x 8 bits) on–chip mask ROM	8K x 8 bits External EPROM	2K x 8 bits on–chip mask ROM	4K x 8 bits External EPROM
RAM Size (Directly addressed locations)	256 x 4 bits (192 x 8 bits) (0–7)	256 x 4 bits (0–7)	128 x 4 bits (0–7)	128 x 4 bits (0–7)
I/O Port:	34	34	12	12
–Input only port	0	0	0	0
–Output only port	0	0	0	0
–I/O port	34	34	12	12
–Control port	5 (Including serial I/O)		2 (Except serial I/O)	
Output Port Type	• Standard pull–up • Standard open–drain • High–current open–drain • High–current pull–up • 12V interface open–drain (Mask option)	• High–current open–drain (MB88PG511–C–101/–201) • High–current pull–up (MB88PG511–C–102/–202)	• Standard pull–up • Standard open–drain	• Standard pull–up (MB88PG512–C–102/–103) • Standard open–drain (MB88PG512–C–101)
A/D Converter: –Resolution –Channel	8 bits 4 channel		8 bits 8 channel	
Stack Depth (Nesting level)	8 levels			
Timer/Counter: –Buffer size –Clock source	Yes 8 bits Internal/External			
Serial I/O: –Buffer size –Clock source –Output latch	Yes 4/8 bits Internal/External Yes		No – – –	
Clock Generator: –Oscillator type: –Clock Frequency (With prescaler)	Yes • Crystal/External • RC–network/External (Mask option) 1 MHz – 3 MHz (2 MHz – 6 MHz)	Yes • Crystal/External (Fixed) – (2 MHz – 6 MHz)	Yes • Crystal/External • RC–network/External (Mask option) 1 MHz – 3 MHz (2 MHz – 6 MHz)	Yes • Crystal/External (Fixed) – (2 MHz – 6 MHz)
Clock Prescaler (Divided by two)	Yes/No (Mask option)	Yes (Fixed)	Yes/No (Mask option)	Yes (Fixed)
Interrupt Function: –Nesting level –Interrupt sources	Yes Single level 4 sources			

Table 7 MB88510 Series Product Line-up & Development Tools (Continued)

	MB88511–P/–PSH/–PF (MB88513–P/–PSH/–PF)	MB88PG511–C–101/–102/–201/–202	MB88512–P	MB88PG512–C–101/–102/–103
Standby Function:	Yes/No (Mask option)	• Yes(MB88PG511–201/–202) • No(MB88PG511–101/–102)	Yes/No (Mask option)	• Yes(MB88PG512–101/–102) • No(MB88PG512–103)
–Initiation method	Software	Software	Software	Software
–Oscillator state during standby	Idle/Stop (Software selectable)	Idle/Stop (Software selectable)	Idle/Stop (Software selectable)	Idle/Stop (Software selectable)
–Output state during standby	Hold/High–Z (Mask option)	• Hold(MB88G511–202) • High–Z(MB88PG511–201)	Hold/High–Z (Mask option)	• Hold(MB88G512–101) • High–Z(MB88PG512–102)
–Standby off reset function	Yes/No (Mask option)	• No(MB88PG511–201/–202)	Yes/No (Mask option)	• Yes(MB88PG512–101) • No(MB88PG512–102)
Watch Dog Timer Function	Yes/No (Mask option)	No (Fixed)	No (Fixed)	No (Fixed)
Number of Instructions	79	81	69	71
Instruction Length/Cycle	1/1, 2/2, or 2/3			
Min. Instruction Execution Time	2.0 µs at 6 MHz (With prescaler)			
Power Supply: –Active –Standby	+5V 4.5V to 5.5V 3.5V to 6.0V	+5V 4.5V to 5.5V –	+5V 4.5V to 5.5V 3.5V to 6.0V	+5V 4.5V to 5.5V –
A/D Converter Power Supply: – Reference voltage	+5V –	+5V –	+5V AV_{R+}/AV_{R-} (Mask option)	+5V AV_{R+} (Fixed)
Operating Temperature Range	–40°C to +85°C			
Process	CMOS			
Package	• DIP–42P • SH–DIP–42P • QFP–48P	• MDIP–42C	• DIP–28P	• MDIP–28C
Development Tools: –Hardware	MB2115–01 : CRT unit (Common) MB2115–02 : Monitor board with keyboard (Common) MB2115–04 or MB2115–100: EPROM writer (Common) MB2115–38 : DUE board for MB88511 and MB88513 MB2115–44 : DUE board for MB88512			
–Software	SM07615–AXXX : PC–DOS cross–assembler SM07615–GXXX : PC–DOS host emulator			

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS †

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Supply Voltage	Vcc	Vss–0.3		Vss+7.0	V	
	Vss		0		V	
Supply Voltage	AVcc	Vss–0.3		Vss+7.0	V	Should not exceed Vcc.
	AVR– AVR+		0		V	AVR– is only applied to select by the mask option in the MB88512.
Input Voltage	VIN	Vss–0.3		Vss+7.0	V	Should not exceed Vcc+0.3V.
Output Voltage	VOUT	Vss–0.3		Vss+7.0	V	Should not exceed Vcc.
		Vss–0.3		Vss+15.0	V	12 V interface open–drain.
Output Low Current	IOL			15	mA	
Total Output Low Current	∑IOL			80	mA	
Power Dissipation	PD			380	mW	
Operating Ambient Temperature	TA	–40		+85	°C	
Storage Temperature	TSTG	–55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUMRATINGS are exceeded, Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
Analog Supply Voltage	AVcc	4.5		5.5	V	
	AV_{R-}			0.2•AVcc	V	MB88511 and MB88513
	AV_{R+}	0		AV_{R+}	V	AVR+ is selected by the mask option in the MB88512
	AV_{R-}	AV_{R-}		AVcc	V	AVR– is selected by the mask option in the MB88512
Input High Voltage	V_{IH}	0.7•Vcc		Vcc+0.3	V	EX (Crystal/ceramic resonator), R–, E–Ports, SI
	V_{IHS}	0.8•Vcc		Vcc+0.3	V	EX (RC–network), $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, SC/$\overline{\text{TO}}$
Input Low Voltage	V_{IL}	Vss–0.3		0.3•Vcc	V	EX (Crystal/ceramic resonator), R–, E–Ports, SI
	V_{ILS}	Vss–0.3		0.2•Vcc	V	EX (RC–network), $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, SC/$\overline{\text{TO}}$
Operating Ambient Temperature	T_A	–40		+85	°C	

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Pin/Port	Conditions	Value			Unit
				Min	Typ	Max	
Output High Voltage	V_{OH}	R–Port(High–current/standard pull–up), E–Port (MB8851/513, high–current/standard pull–up), $\overline{SC}/\overline{TO}$* (MB88511/513), SO (MB88511/513)	V_{CC} = 4.5V I_{OH} = –200µA	2.4			V
			V_{CC} = 4.5V I_{OH} = –10µA	4.0			V
Output Low Voltage	V_{OL}	R–Ports (All option), $\overline{RESET}$, SO (MB88511/513), $\overline{SC}/\overline{TO}$ (MB88511/513), E–Port(88512, all option)	V_{CC} = 4.5V I_{OL} = 1.8mA			0.4	V
			V_{CC} = 4.5V I_{OL} = 3.6mA			0.6	V
		R–Port(High–current open–drain/ pull–up), E–port (MB88511/513, high–current/ open–drain/pull–up)	V_{CC} = 4.5V I_{OL} = 10mA			2.0	V
Input Leakage Current	I_{IL}	R–Port(High–current/standard pull–up), E–port (MB88512, high–current/ standard pull–up), SI, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$ (MB88511/513)	V_{CC} = 5.5V V_{IH} = 5.5V			–1.8	mA
		EX, $\overline{RESET}$	V_{CC} = 5.5V V_{IL} = 0.4V			–60	µA
	I_{IH}	EX, START	V_{CC} = 5.5V V_{IL} = 0.4V			60	µA
Open–Drain Output Leakage Current	I_{LEAK}	R–Port(High–current/standard open–drain), E–Port (MB88511/513, high–current/standard open–drain)	V_{CC} = 5.5V V_{OH} = 5.5V		0.1	10	µA
		E10–E0 (MB88511/513, 12V interface open–drain)	V_{CC} = 5.5V V_{OH} = 13.2V			40	µA
Total I/O High Impedance Leakage Current	ΣI_{IZ}	R–Port(all options), $\overline{IRQ}$, $\overline{TC}$, SI $\overline{SC}/\overline{TO}$ (MB88511/513), SO (MB88511/513), E–Port(MB88511/513)	V_{CC} = 6.0V V_{IN} = 0V to 6.0V (Standby mode)			±25	µA
Supply Current	I_{CC}	V_{CC}	V_{CC} = 5.0V (Typ), 5.5V(Max), fc=1MHz(Operation) All outputs open		3	6	mA
	I_{CCH}	V_{CC} (standby mode)	V_{CC} = 6.0V, fc=0MHz, (Standby) All outputs open		3	15	µA
Input Capacitance	C_{IN}	All pins except Vcc and Vss	fc=1MHz		10	20	pF

*: When use serial port at internal clock mode, $\overline{SC}/\overline{TO}$ output voltage should be over the V_{OH}=0.8•Vcc.

AC CHARACTERISTICS

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Frequency	f_c	EX, X	Crystal/ceramic or RC–network OSC or external clock drive Figures 7 and 8	1	3	MHz	Without prescaler
				2	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figures 7 and 8	0.33	2	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figures 7 and 8)	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figures 7 and 8	5	200	ns	

Figure 7 Clock Timing

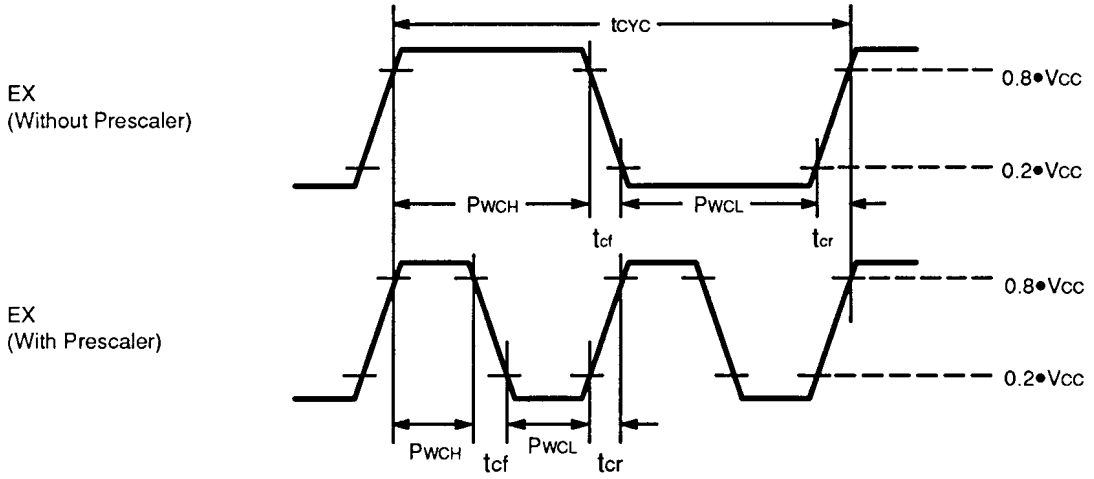
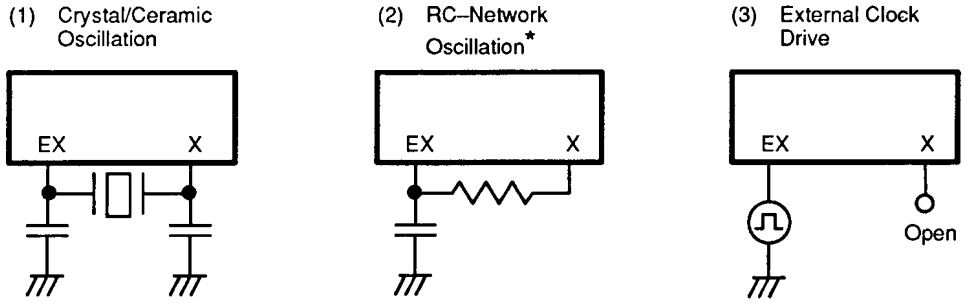


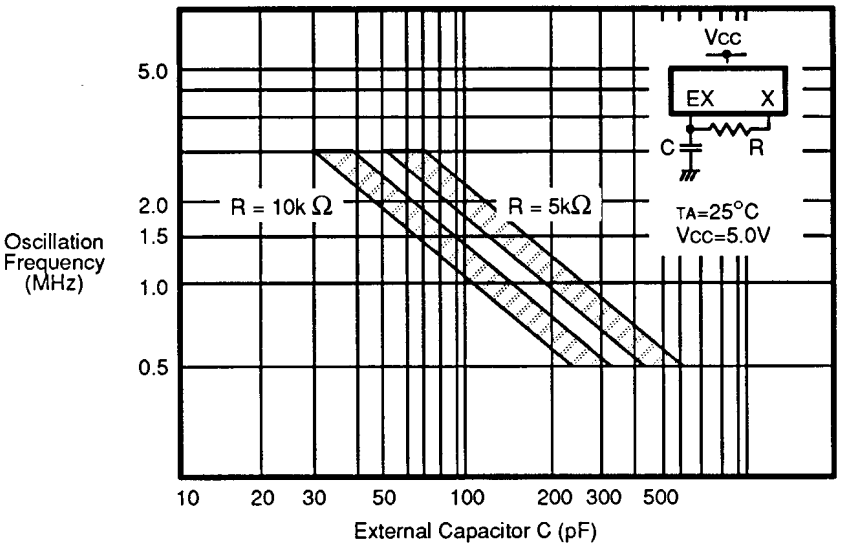
Figure 8 Clock Circuit Configuration



*When the RC–network oscillation is used, the following conditions must be met:

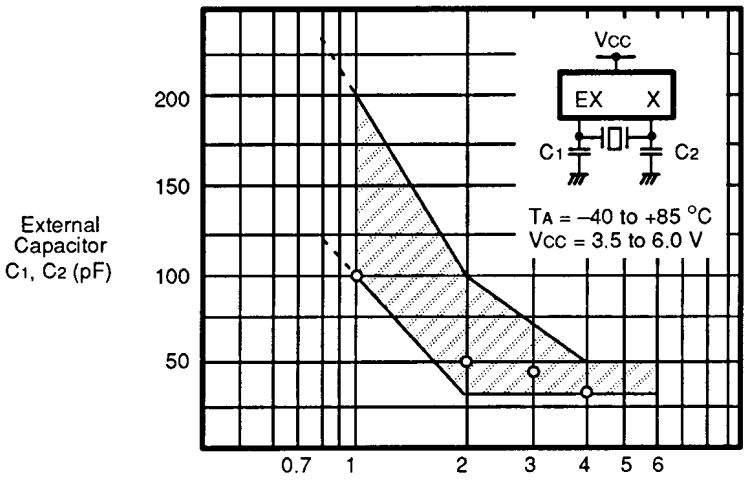
1) The prescaler is not used.
2) V_{CC}=5 V ± 10%
3) T_A=–40°C to + 85°C
4) f_c does not exceed 3 MHz

Figure 9 RC–Network Oscillation Characteristics (Example)



Note:
When the RC–network oscillations is used, the following conditions must be met:
1) The prescaler is not used.
2) Vcc=5V±10%
3) TA=–40°C to +85°C

Figure 10 Crystal Oscillation Characteristics (Example)



Note:

1) The cross–hatched portion shows an area where the on–chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of theexternal capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed,a capacitor value should be determined, adjusting to individual crystal resonator characteristics.
2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on–chip oscillator characteristics. So, we recommendto use high–frequency crystal resonator with on–chip 1/2 prescaler.

OUTPUT TIMING (MB88511/MB88513) (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min	Max	
E–, R–Ports Delay Time	t_{PDH}	R–Port, E–Port	Figure 11		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Figure 11		1000	ns
	t_{SDL}				350	

Notes:
1. A 10kΩ pull–up is required when open–drain output is used.
2. All the output loading values are 50pF + 1TTL. See figure below.

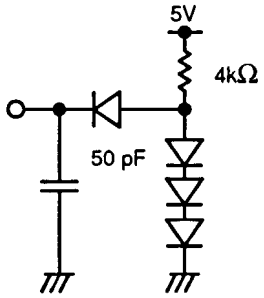
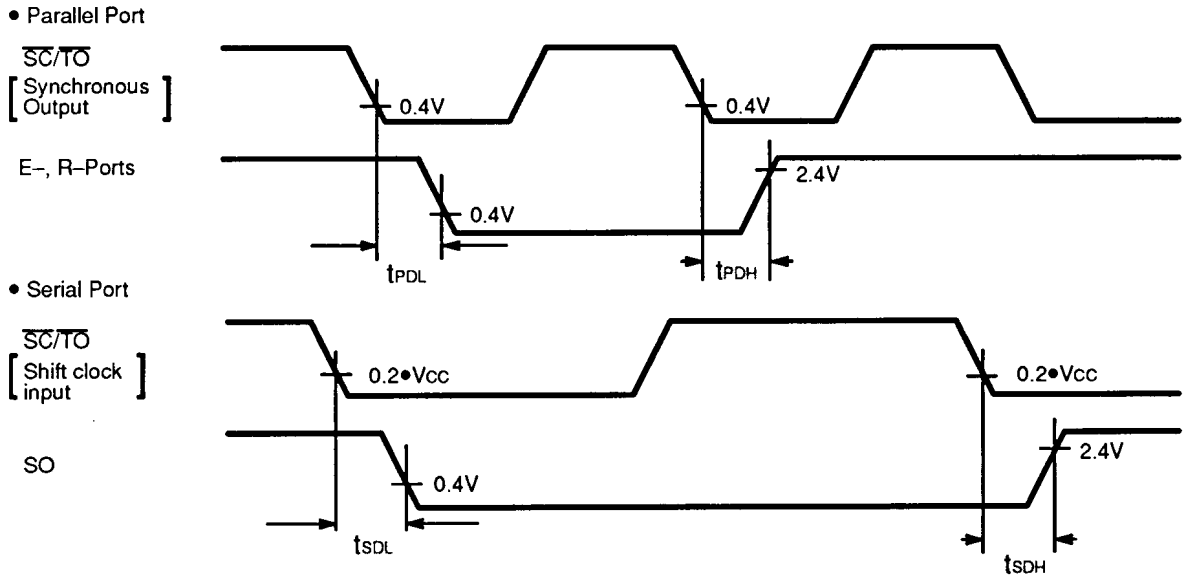


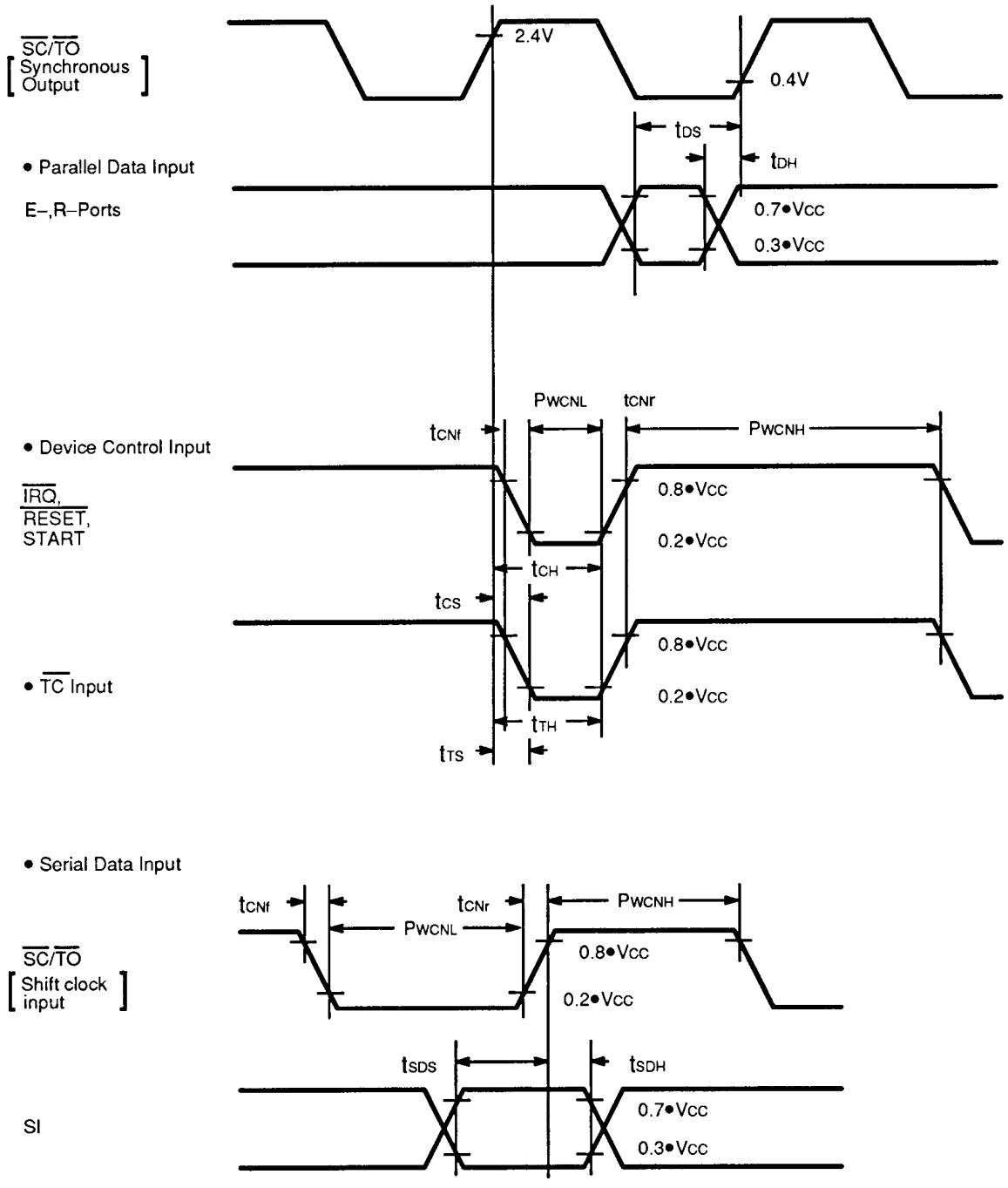
Figure 11 Output Timing



INPUT TIMING (MB88511/513) (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min	Max	
Input Data Setup Time	t_{DS}	E20–E0, R15–R11, R7–R0	Figure 12	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}–50	
SI Input Setup Time	t_{SDS}	SI	Figure 12	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{\text{RESET}}$	Figure 12		2t_{cyc}–200	ns
		$\overline{\text{IRQ}}$			2t_{cyc}–200	
Device Control Hold Time (synchronous mode)	t_{CH}	$\overline{\text{RESET}}$	Figure 12	8t_{cyc}+50		ns
		$\overline{\text{IRQ}}$		2t_{cyc}+50		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{\text{TC}}$	Figure 12		2t_{cyc}–200	ns
Timing Input Hold Time (synchronous mode)	t_{TH}	$\overline{\text{TC}}$	Figure 12	2t_{cyc}+50		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{\text{SC}}$/$\overline{\text{TO}}$	Figure 12	6t_{cyc}+250		ns
		$\overline{\text{IRQ}}$, $\overline{\text{TC}}$		6t_{cyc}+250		
		$\overline{\text{RESET}}$		12t_{cyc}+250		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{\text{SC}}$/$\overline{\text{TO}}$	Figure 12	12t_{cyc}+250		ns
		$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$		6t_{cyc}+250		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{\text{SC}}$/$\overline{\text{TO}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, $\overline{\text{TC}}$	Figure 12	Should be less than 200ns		

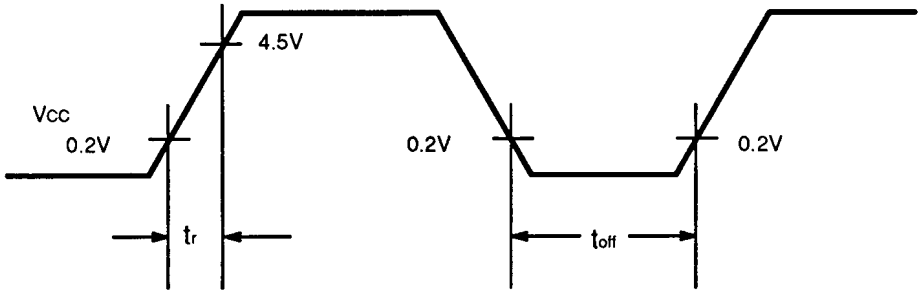
Figure 12 Input Timing



POWER-ON RESET (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power Supply Rise Time	t_r	Figure 13	0.05	50	ms	Required for operation of the power–oh reset circuit
Power Supply Shut–off Time	t_{off}	Figure 13	1		ms	Required for accurate circuit operation repeatability

Figure 13 Power–on Reset Timing



Note:
Power supply should be raised smoothly.

A/D CONVERTER CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Resolution						8	Bit
Linearity Error			Only applied to select AV_{R-} (MB88512) [T_A=25°C, AV_{CC}=5.0V, AV_{R+}=5.0V]			±1.0	LSB
Differential Linearity Error						±0.9	LSB
Zero Transition Voltage	V_{OT}		MB88511/513 and select AV_{R+} (MB88512) [T_A=25°C, AV_{CC}=5.0V, AV_{R-}=0V]	–20	+10	+40	mV
Full Scale Transition Voltage	V_{FST}			+4910	+4970	+5030	mV
Conversion Time			144 x t_{CYC}	48 *1		144 *2	µS
Analog Port Input Current	I_{AIN}	AN3–AN0, AN7–AN4				5	µA
Analog Input Voltage		AN3–AN0, AN7–AN4	MB88511/513 and select AV_{R-} (MB88512)	AV_{R-}		AV_{CC}	V
		AN3–AN0* AN7–AN4	Select AV_{R+} (MB88512).	0		AV_{R+}	V
Reference Voltage		AV_{R-}	MB88511/513	0	0	0.2•AV_{CC}	V
		AV_{R+}	Select AV_{R+} (MB88512)	0		AV_{R+}	V
		AV_{R-}	Select AV_{R-} (MB88512).	AV_{R-}		AV_{CC}	V
Reference Voltage Supply Current	I_R		Only applied to the MB88512, AV_{R+} :Between AV_{R+} and AV_{SS}, AV_{R-} :Between AV_{R-} and AV_{CC}		170		µA
Supply Current	I_A	AV_{CC}	AV_{CC}=5.0V, AV_{R-}=0V or AV_{R+}=5V A/D converting		1.7		mA
	I_{AH1}		AV_{CC}=6.0V, AV_{R-}=6V or AV_{R+}=0V Standby			5	µA
	I_{AH2}		Only applit to the MB88511/513, AV_{CC}=6.0V, AV_{R-}=0V Standby and stop A/D converting		250		µA

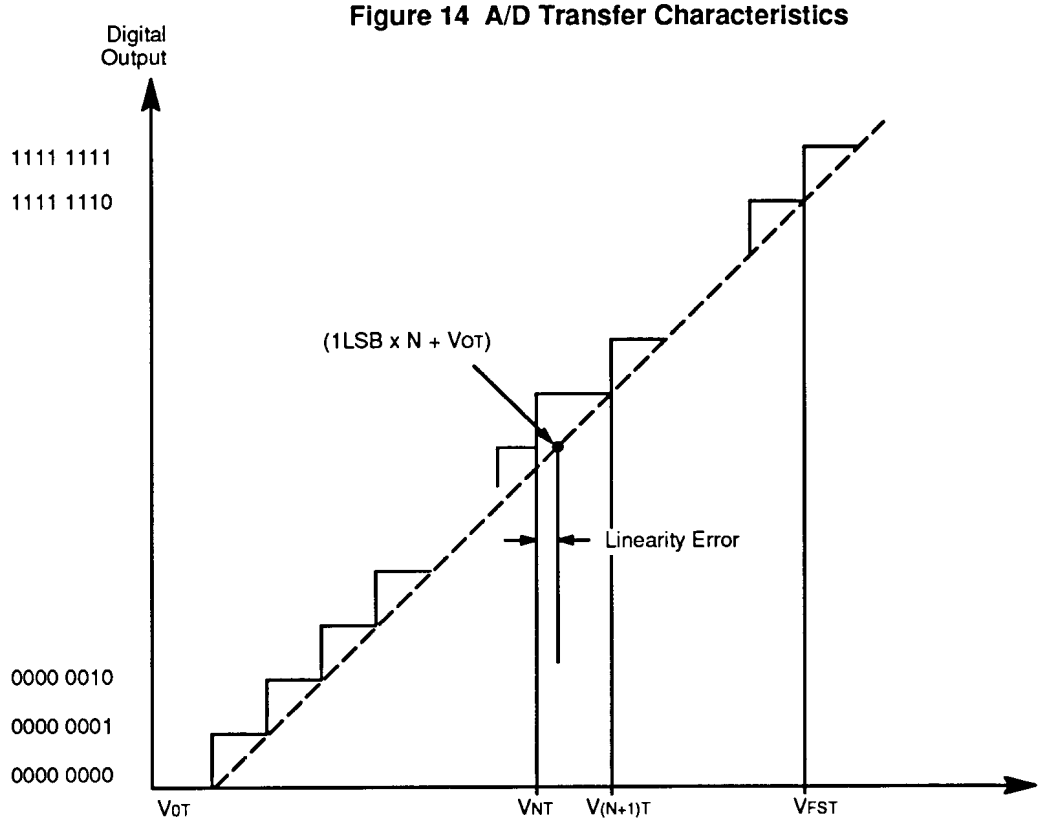
Notes:

* AN7–AN4 is applied to only MB88512.
1. Error between analog inputs is within 1/2 LSB when AV_{CC} – AV_{R-}=5.0V
2. Full–scale and offset can be adjust by an appropriate setting of AV_{CC} and AV_{R-}.
3. Error becomes relatively larger as |AV_{CC} – AV_{R-}| becomes smaller.

*1 fc = 6.0 MHz (with prescaler)
*2 fc = 1.0 MHz (without prescaler)

- Resolution
  The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into $2^8 = 256$ parts.)
- Linearity Error
  The difference between the line connecting the device zero transition point ("0000 0000" ↔ "0000 00001") with the full scale transition point ("0000 0000" ↔ "0000 00001"), the actual conversion characteristics.
- Differential Linearity Error
  The difference from ideal input voltage required to change the output voltage code by 1 LSB.

Figure 14 A/D Transfer Characteristics



$$1LSB = \frac{V_{FST} - V_{OT}}{254}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1\ LSB \times N + V_{OT})}{1\ LSB} \quad (LSB)$$

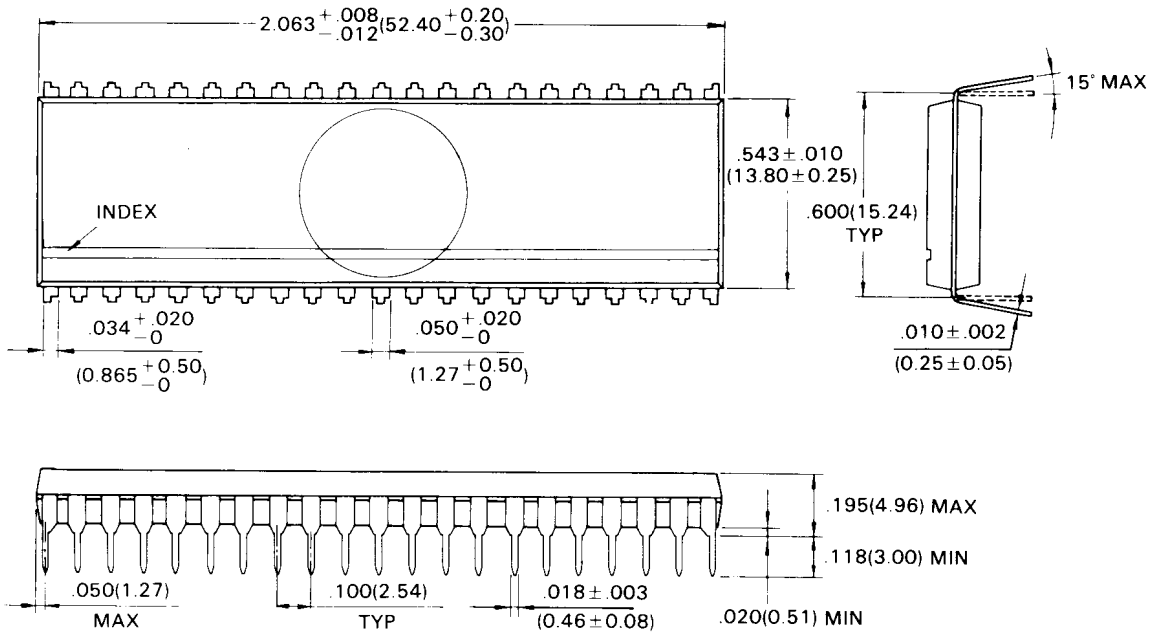
$$\text{Differential Linearity Error} = \frac{V_{(N+1)} - V_{NT}}{1\ LSB} - 1 \quad (LSB)$$

PACKAGE DIMENSIONS

MB88511–P and MB88513–P

42-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-42P-M01)

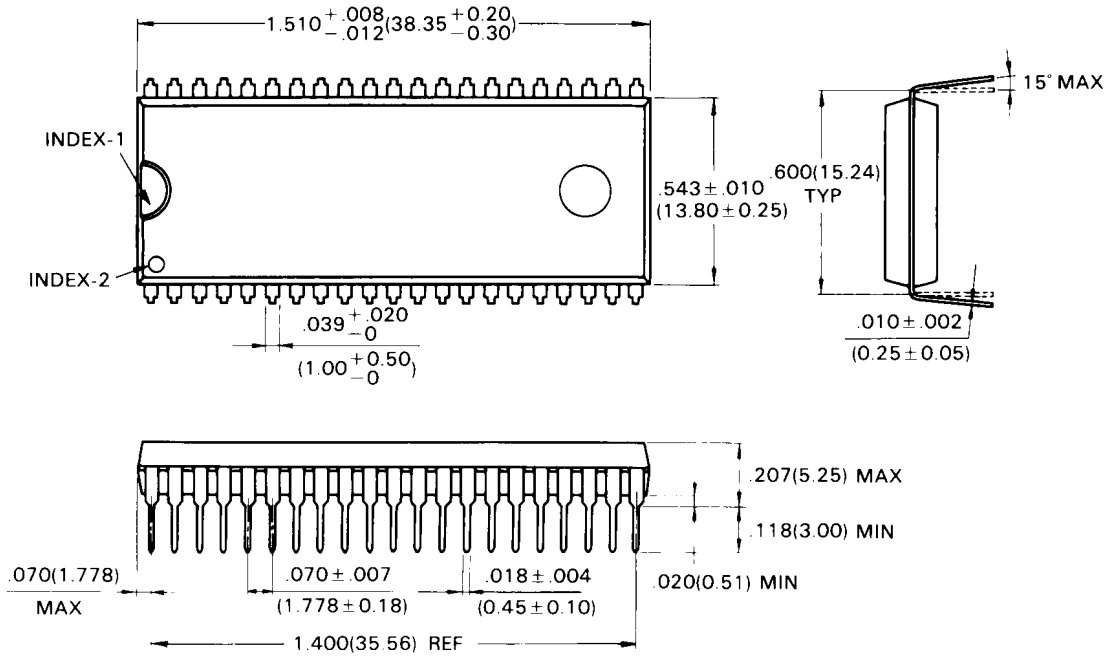


Dimensions in
inches (millimeters)

MB88511–PSH and MB88513–PSH

42-LEAD PLASTIC DUAL IN-LINE PACKAGE

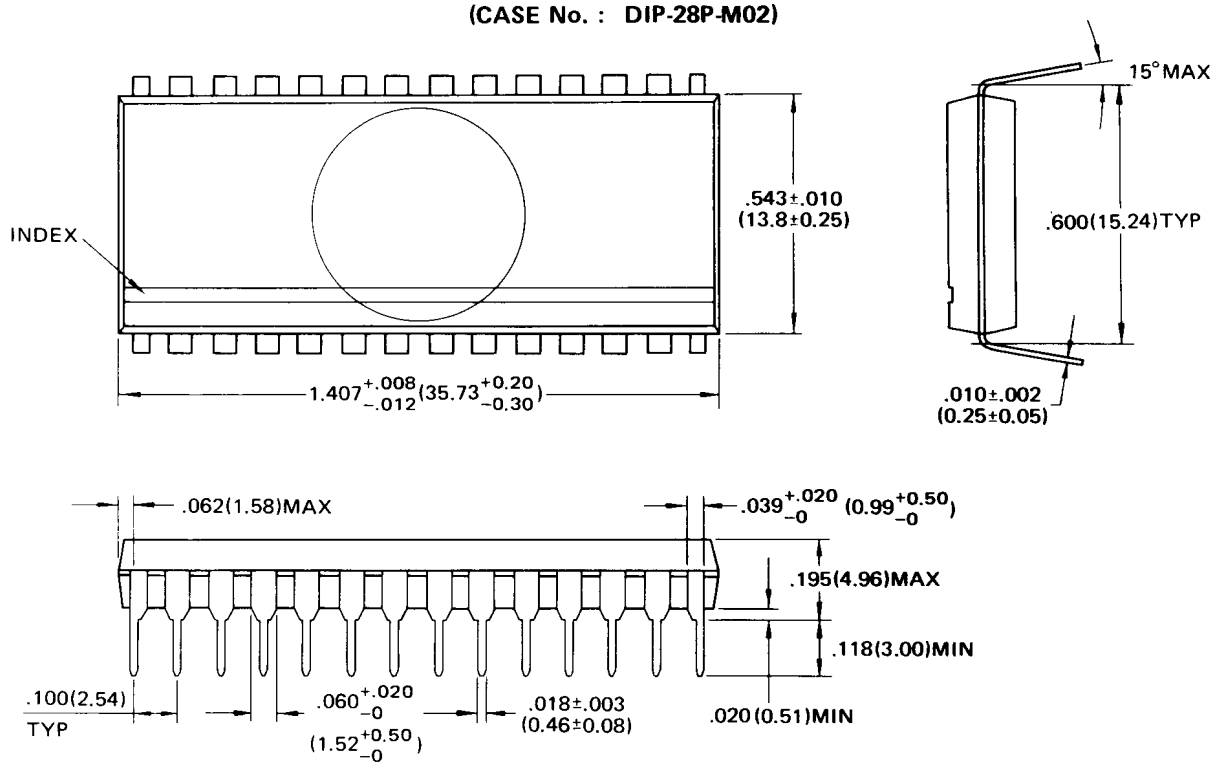
(Case No. : DIP-42P-M02)



Dimensions in
inches (millimeters)

MB88512–P

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)

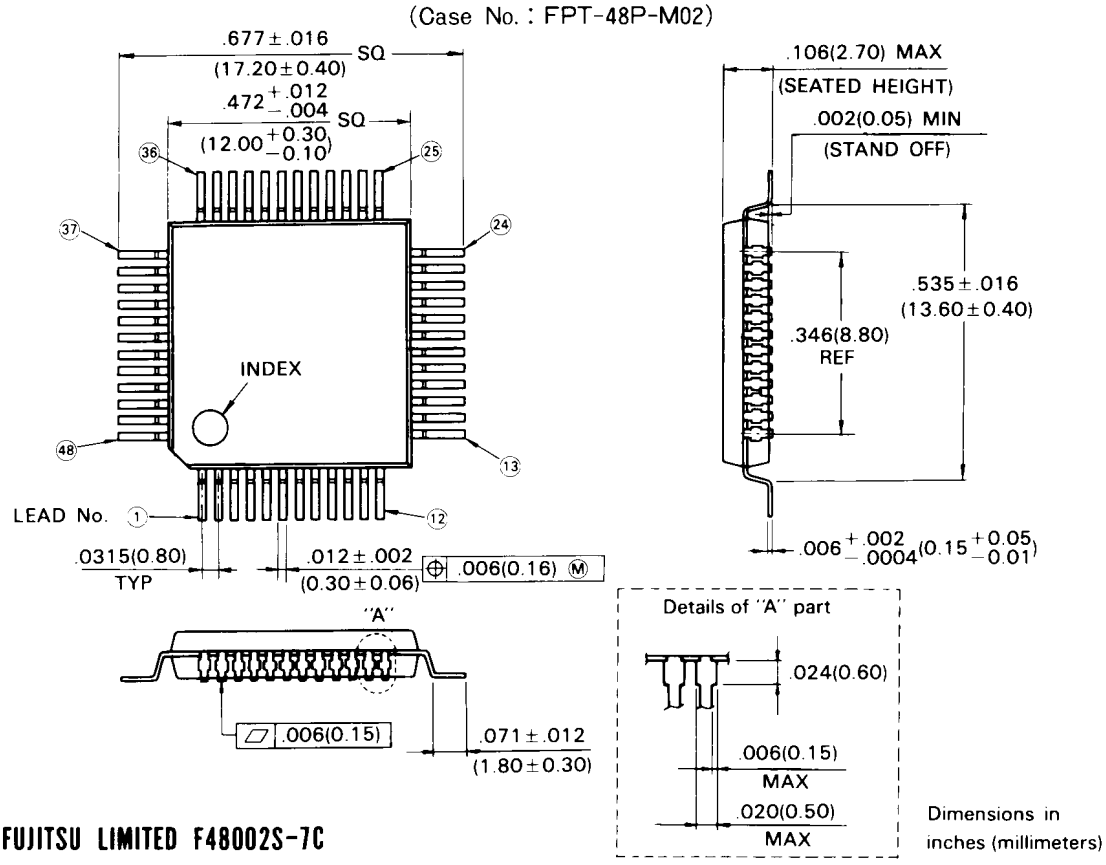


Dimensions in
inches (millimeters)

MB88511–PF and MB88513–PF

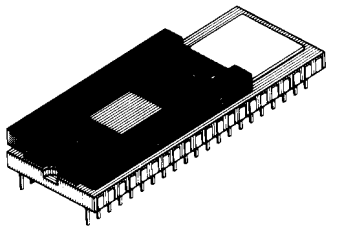
48-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-48P-M02)



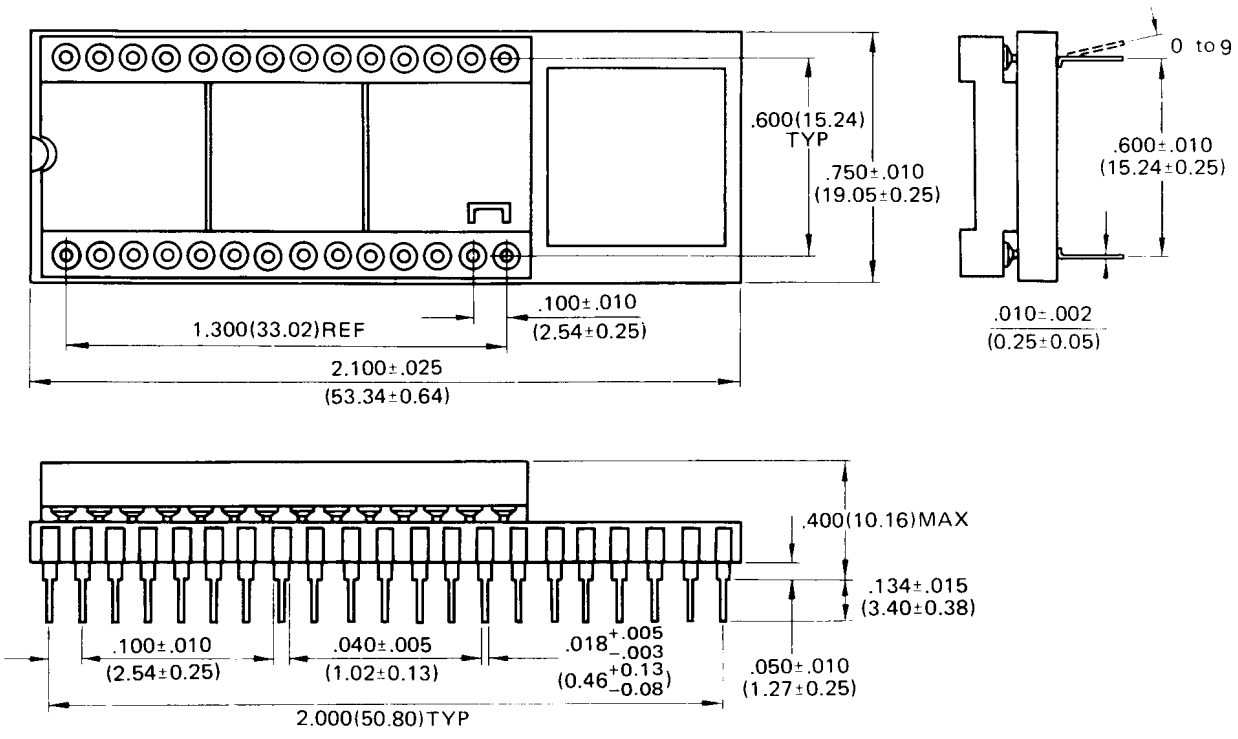
Dimensions in inches (millimeters)

MB88PG511–C



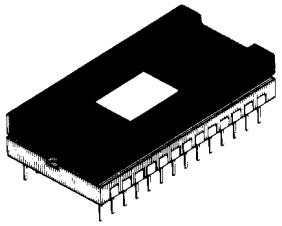
MDP–42C–P04

42-LEAD DUAL IN-LINE PACKAGE MODULE
(CASE No.: MDP-42C-P04)



Dimension in inches
and (millimeters)

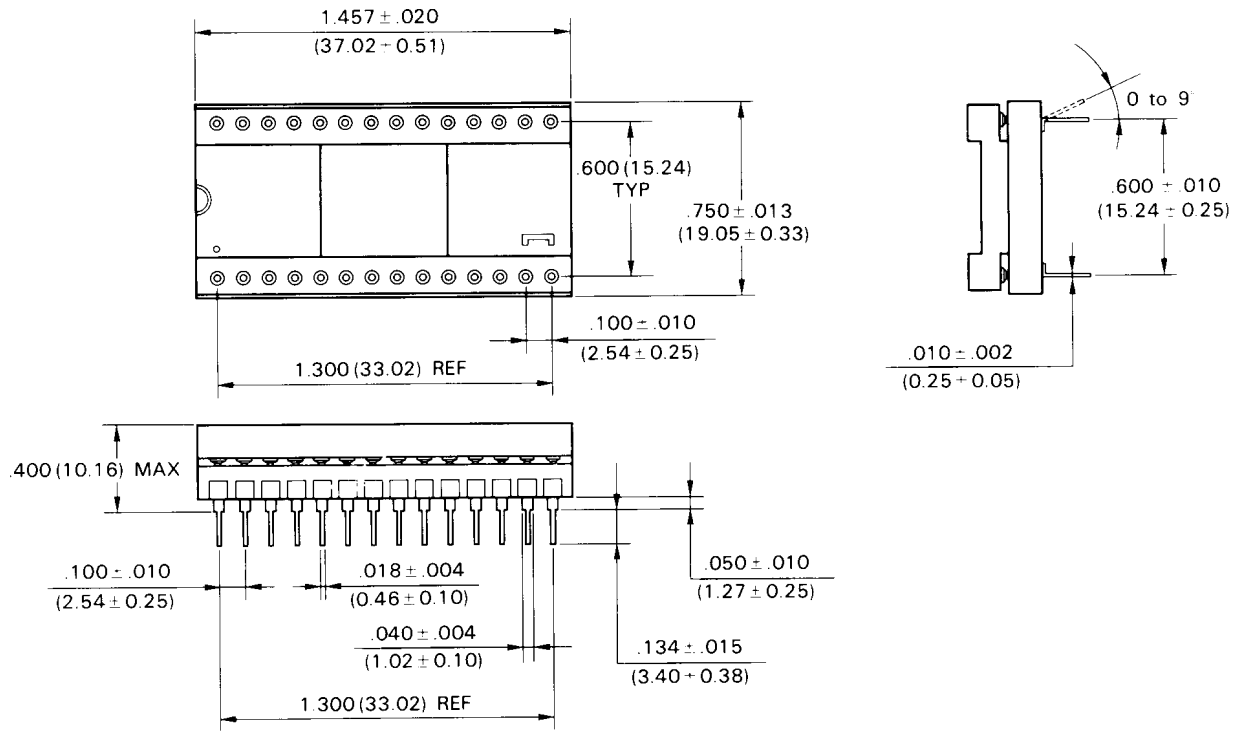
MB88PG512–C



MDP–28C–P01

28-LEAD CERAMIC DUAL IN-LINE TYPE MODULE

(Case No. : MDP-28C-P01)



Dimensions in
inches (millimeters)

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