DATA SHEET

PCK857

50-150MHz differential 1:10 SDRAM clock driver

Product data
Supersedes data of 2000 Jun 15

2003 Jul 31

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50-150 MHz differential 1:10 SDRAM clock driver PCK857

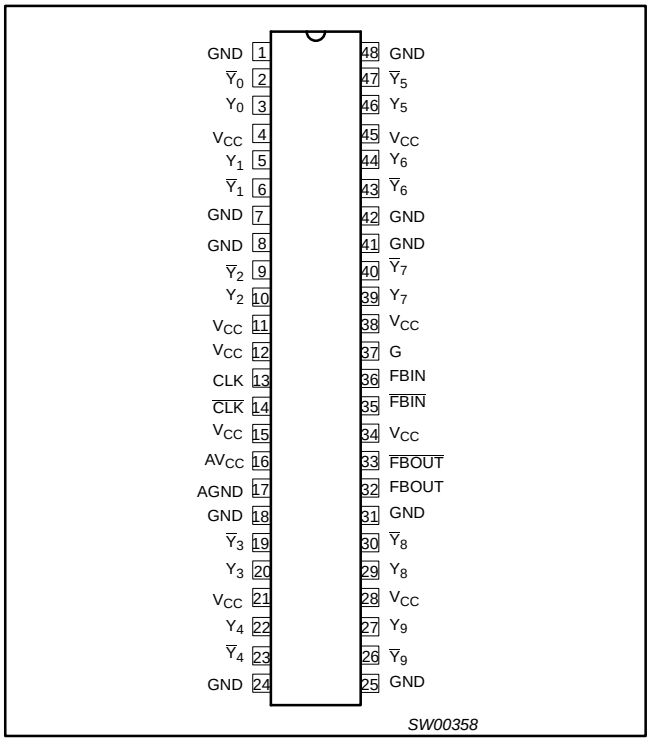
FEATURES

- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications
- 1-to-10 differential clock distribution
- Very low skew (< 100 ps) and jitter (< 100 ps)
- 3 V AV_{CC} and 2.5 V V_{CC}
- SSTL_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTL16857 and CBT3857

DESCRIPTION

Zero delay buffer to distribute an SSTL differential clock input pair to 10 SSTL_2 differential output pairs. Outputs are slope controlled. External feedback pin for synchronization of the outputs to the input. A CMOS style Enable/Disable pin is provided for low power disable.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +85 °C	PCK857DGG	SOT362-1

PIN DESCRIPTION

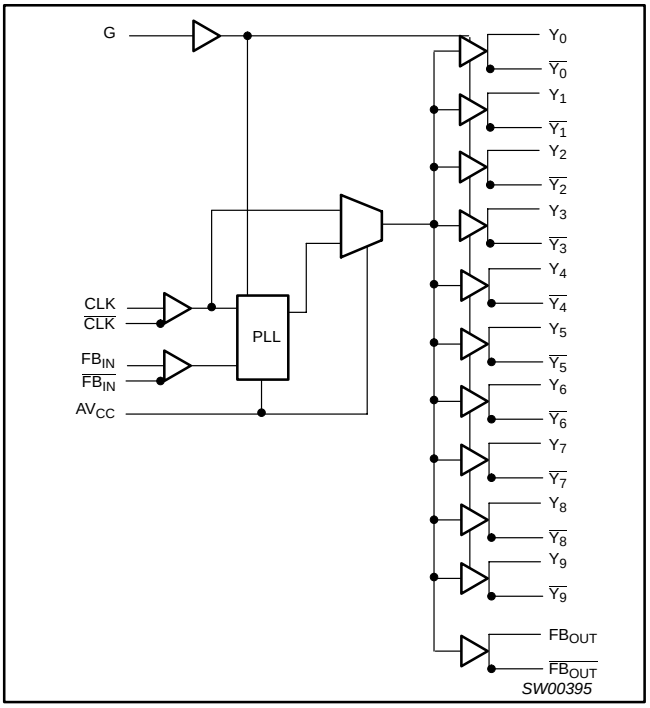
PINS	SYMBOL	I/O	DESCRIPTION
17	AGND	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
16	AV_{CC}	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (G = 0), the PLL is powered down.
13, 14	CLK, $\overline{CLK}$	I	Clock input. CLK provides the clock signal to be distributed by the PCK857 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
36, 35	FB_{IN}, $\overline{FB_{IN}}$	I	Feedback input. FB_{IN} provides the feedback signal to the internal PLL. FB_{IN} must be hard-wired to FB_{OUT} to complete the PLL. The integrated PLL synchronizes CLK and FB_{IN} so that there is nominally zero phase error between CLK and FB_{IN}.
32, 33	FB_{OUT}, $\overline{FB_{OUT}}$	O	Feedback output. FB_{OUT} is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FB_{IN}, FB_{OUT} completes the feedback loop of the PLL.
37	G	I	Output bank enable. G is the output enable for outputs Y and $\overline{Y}$. When G is low outputs Y are disabled to a high-impedance state. When G is high, all outputs Y are enabled and switch at the same frequency as CLK.
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	Ground	Ground
4, 11, 12, 15, 21, 28, 34, 38, 45	V_{CC}	Power	Power supply
3, 5, 10, 20, 22, 46, 44, 39, 29, 27	Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9	O	Clock outputs. These outputs provide low-skew copies of CLK.
2, 6, 9, 19, 23, 47, 43, 40, 30, 26	$\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$, $\overline{Y3}$, $\overline{Y4}$, $\overline{Y5}$, $\overline{Y6}$, $\overline{Y7}$, $\overline{Y8}$, $\overline{Y9}$	O	Clock outputs. These outputs provide low-skew copies of $\overline{CLK}$.

FUNCTION TABLE

INPUTS			OUTPUTS				PLL ON/OFF
G	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	FBOUT	
L	L	H	Z	Z	Z[1]	Z[1]	OFF
L	H	L	Z	Z	Z[1]	Z[1]	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X[2]	< 20 MHz	< 20 MHz	Z	Z	Z[1]	Z[1]	OFF

NOTES:
H = HIGH voltage level
L = LOW voltage level
Z = HIGH impedance OFF-state
X = don't care
1. Subject to change. May cause conflict with FBIN pins.
2. Additional feature that senses when the clock input is less than 20 MHz and places the part in sleep mode.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
V_{IK}	Input voltage	All input pins	V_{CC} = 2.3 V; I_I = -18 mA			-1.2	V
V_{OH}	HIGH-level output voltage		V_{CC} = min to max; I_{OH} = -1 mA	V_{CC} -0.1			V
			V_{CC} = 2.3 V; I_{OH} = -12 mA	1.7			
V_{OL}	LOW-level output voltage		V_{CC} = min to max; I_{OL} = 1 mA			0.1	V
			V_{CC} = 2.3 V; I_{OL} = 12 mA			0.6	
I_{OH}	HIGH-level output current		V_{CC} = 2.3 V; V_O = 1 V	-18	-32		mA
I_{OL}	LOW-level output current		V_{CC} = 2.3 V; V_O = 1.2 V	26	35		mA
I_I	Input current	G	V_{CC} = 2.7 V; V_I = 0 V to 2.7 V			±10	µA
		CLK, FB_{IN}	V_{CC} = 2.7 V; V_I = 0 V to 2.7 V			±10	
I_{OZ}	HIGH-impedance output current		V_{CC} = 2.7 V; V_O = V_{CC} or GND			±10	µA
V_{OC}	Output crossing point voltage			(V_{CC}/2)-0.1	V_{CC}/2	(V_{CC}/2)+0.1	V
I_{CCZ}	Supply current, disabled		AV_{CC} and V_{CC} = max, G = L or no input CLK signal		500	800	µA
I_{CC}	Supply current on AV_{CC}		V_{CC} = 2.7 V, All outputs switching environment; f_O = 167 MHz, 16 pF in 60 Ω See Figure 3		235	330	mA
AI_{CC}	Supply current on AV_{CC}		AV_{CC} = 3.6 V; f_O = 167 MHz		9	12	mA
C_I	Input capacitance		V_{CC} = 2.5 V;V_I = V_{CC} or GND		2		pF
C_O	Output capacitance		V_{CC} = 2.5 V; V_O = V_{CC} or GND		3		pF

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{CC}/AV_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage	Note 2	-0.5	V_{DDQ} + 0.5	V
V_O	Output voltage	Note 2	-0.5	V_{DDQ} + 0.5	V
I_{IK}	Input diode current	V_I < O or V_I > V_{CC}		± 50	mA
I_{OK}	Output diode current	V_O < O or V_O > V_{CC}		± 50	mA
I_O	Output source or sink current	V_O = O to V_{CC}		± 50	mA
T_{stg}	Storage temperature range		-65	+150	°C
θJA	Package thermal impedance	Note 3		89	°C/W

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD51.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.3	2.5	2.7	V
AV_{CC}	Analog supply voltage		3.0	3.3	3.6	V
V_{IL}	G input				0.3 XV_{CC}	V
V_{IH}	G input		0.7 XV_{CC}			V
V_I	CLK, FB_{IN}		-0.3		V_{CC} + 0.3	V
I_{OH}	HIGH-level output current				-12	mA
I_{OL}	LOW-level output current				12	mA

timing requirements over recommended ranges or supply voltage and operating free-air temperature

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_C	Clock frequency		66	167	MHz
	Input clock duty cycle		40%	60%	
	Stabilization time[1]			100	µS

NOTE:
1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics are not applicable. This parameter does not apply for input modulation under SSC application.

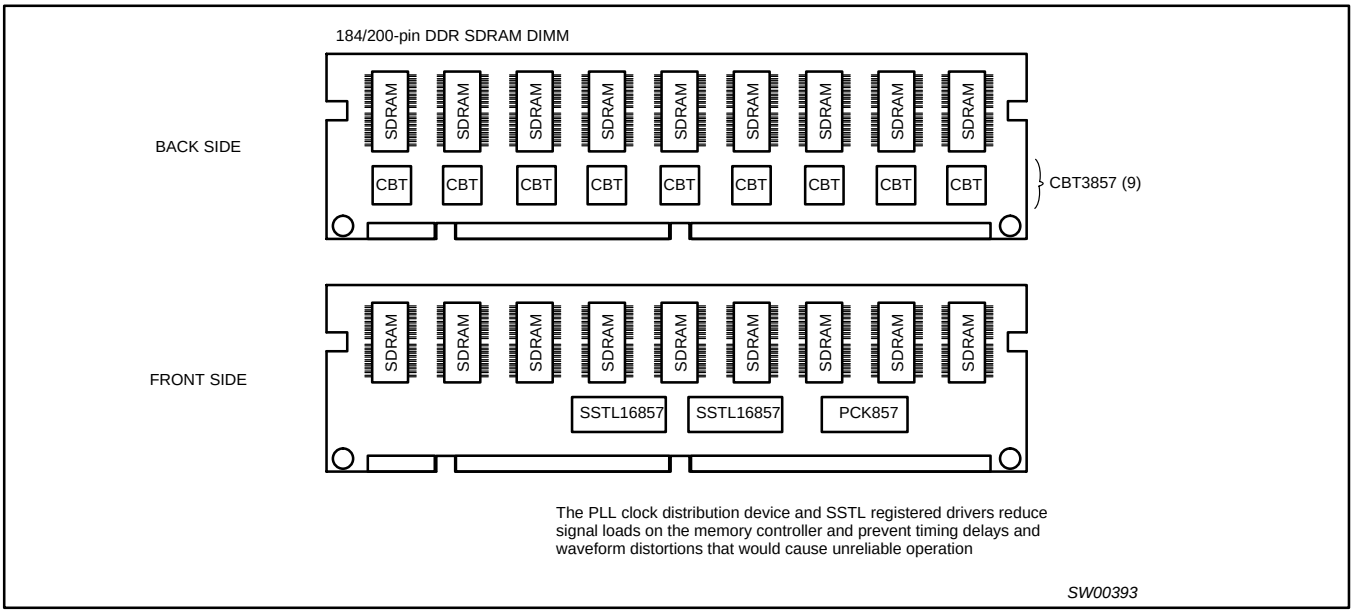
AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH}[1]	Low to high propagation	Figure 4	CLK to any output	1.5	3.5	6	ns
t_{PHL}[1]	High to low propagation	Figure 4	CLK to any output	1.5	3.5	6	ns
$f_{PHASERROR}$	Phase error			-150	0	150	ps
f_{SK}	Output clock skew	Figure 1				100	ps
$fdif_{SK}$	Differential clock skew					100	ps
f_{SL}	Output clock skew rate			1	1.5		V/ns
$Jitter_{pp}$	Peak-to-Peak jitter (long term)			-100		100	ps
$Jitter_{cc}$	Cycle-to-cycle jitter (short term)	Figure 3		> -100		< 100	ps
f_{DC}	Duty cycle	Figure 2		45		55	%
C_{in}	Input capacitance			2.5		4	pF
t_r, t_f	Output rise and fall times		20%-80%	650	800	950	ps

NOTE:

1. Refers to transition of reinverting output.



AC WAVEFORMS

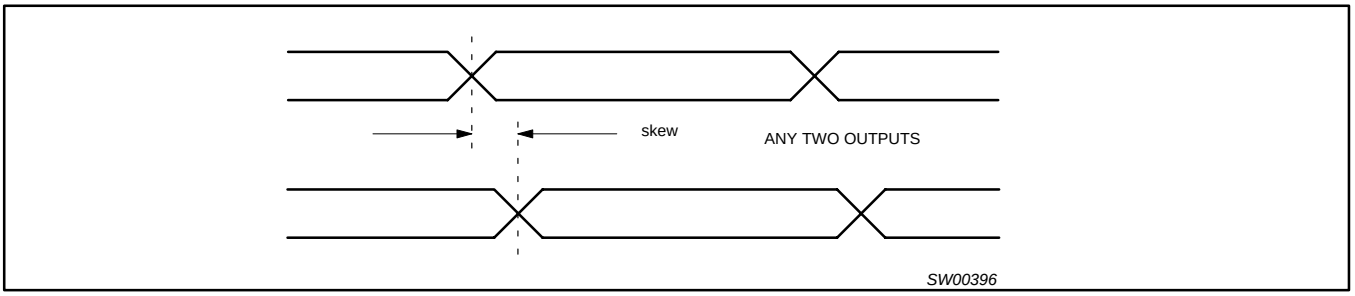


Figure 1. Skew between any two outputs.

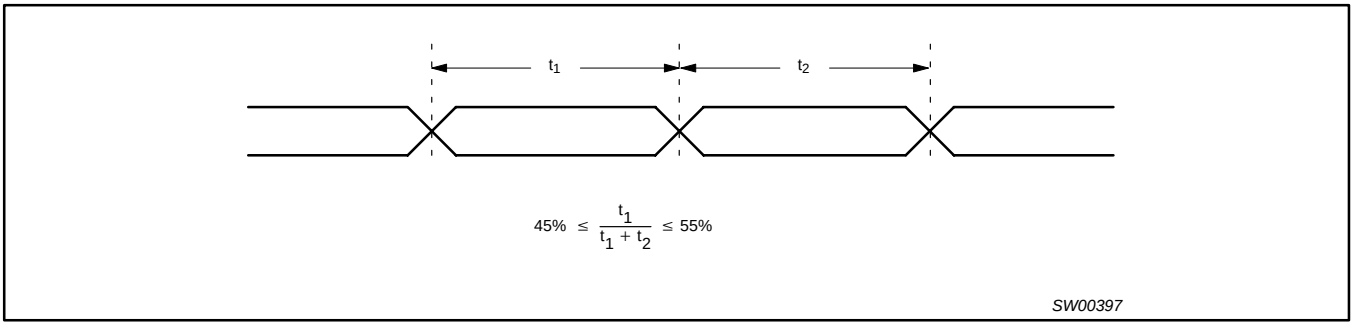


Figure 2. Duty cycle limits and measurement

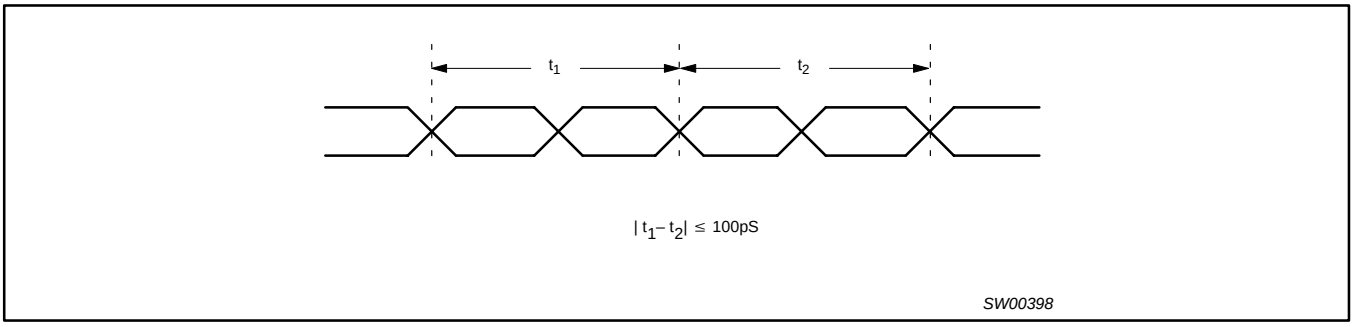


Figure 3. Jitter limit and measurement

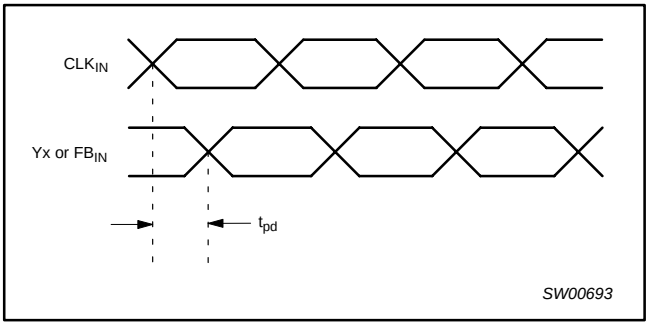
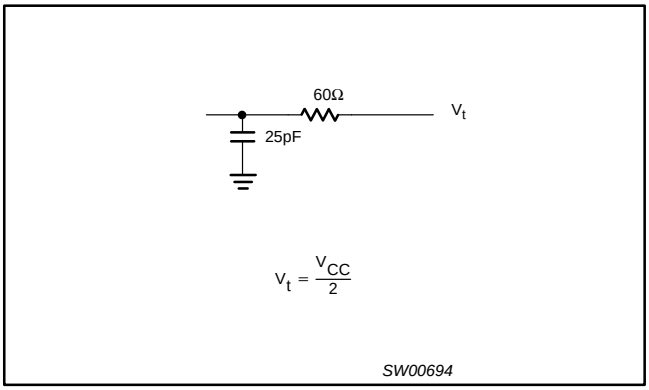
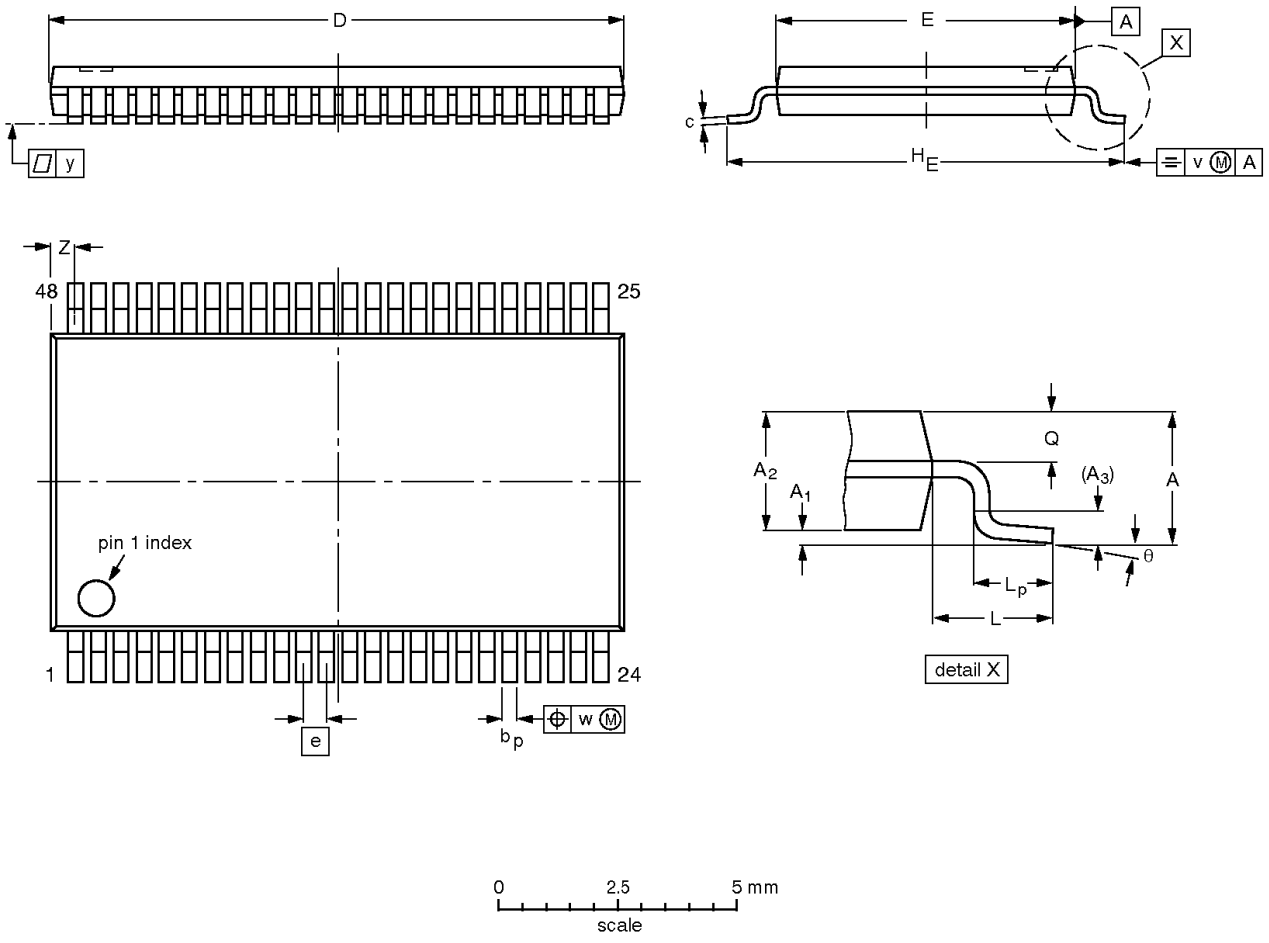


Figure 4. Propagation delay time; t_{PLH}, t_{PHL}

TEST CIRCUIT



TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030731	**Product data (9397 750 11764); ECN 853-2199 30051 of 18 June 2003; supersedes data of 2000 June 15 (9397 750 07193).** Modifications: • Corrections and minor changes to existing product specifications.
_2	20000715	Product data (9397 750 07193); ECN 853-2199 23880 of 2000 June 15.

50-150 MHz differential 1:10 SDRAM clock driver PCK857

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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