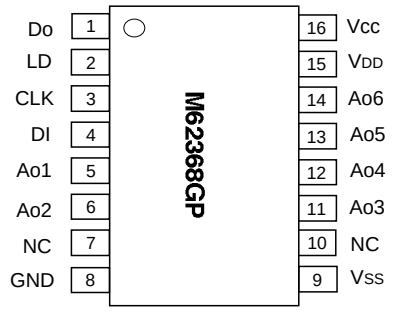
M62368GP

3V TYPE 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62368GP is a CMOS semiconductor IC, containing 6 channels of 8-bit D-A converters. It is operable with a low supply voltage between 2.7~3.6V,and is easy to use due to serial data input,and 3-pin(DI,CLK,LD)connection with microcomputer.
The IC also contains Do pin terminal,enabling cascade connection,and therefore is suitable for automatic control in combination with a microcomputer.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2E-A

NC:NO CONNECTION

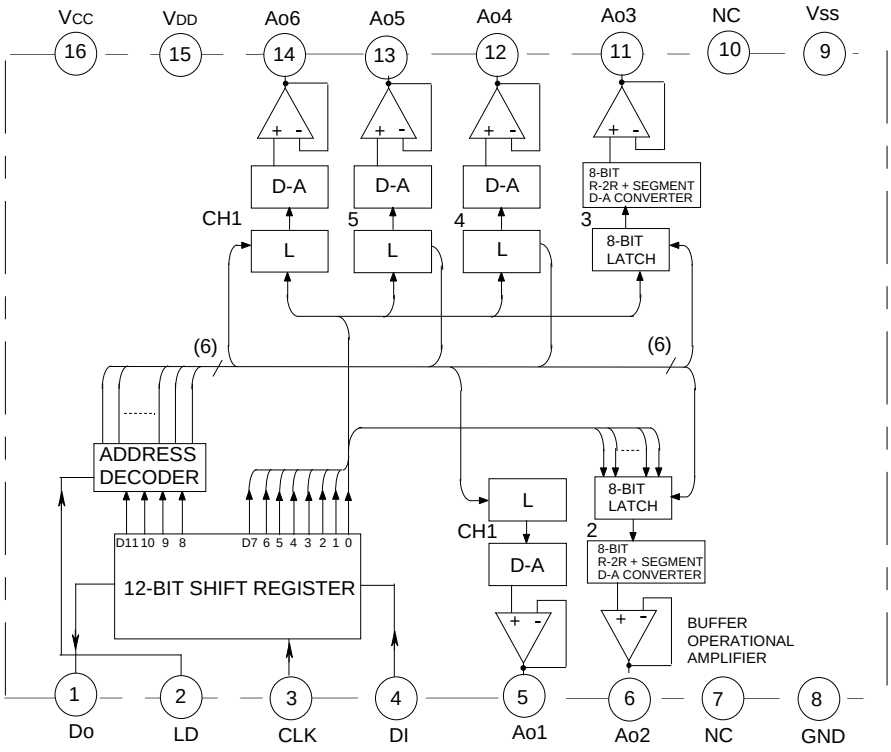
FEATURES

- Operable with a low voltage between 2.7~3.6V
- 12-bit serial data input(connected via 3 pins:DI,CLK,LD)
- 6 channels of R-2R and segment type high-performance 8-bit D-A converters
- 6 buffer operational amplifiers with full swing of output voltage between Vcc and GND.
- High oscillation stability against the capacitive load of buffer operational amplifiers.

APPLICATION

Digtal-analog conversion in industrial or home-use electronic equipment.
Automatic control in combination with EEPROM and microcomputer(Substitute for conventional semi-fixed resistor)

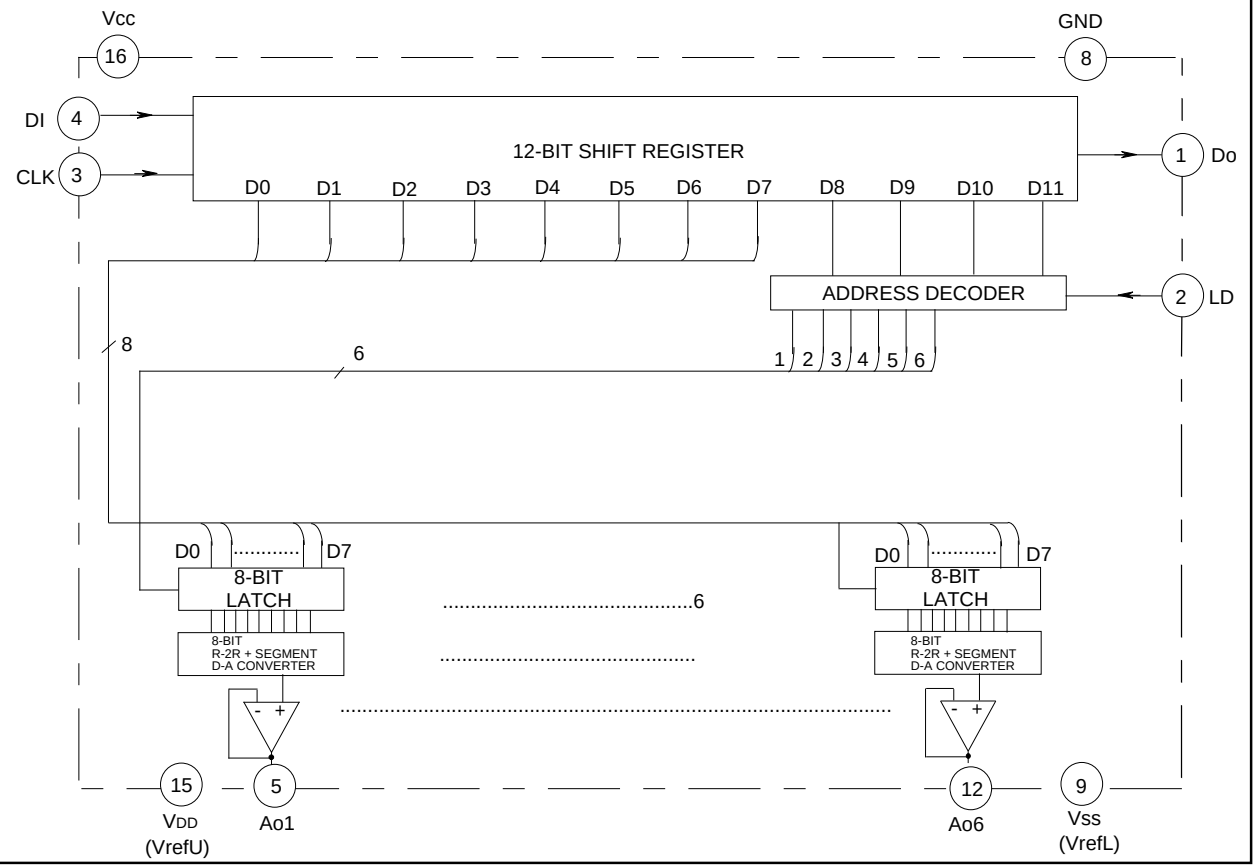
BLOCK DIAGRAM



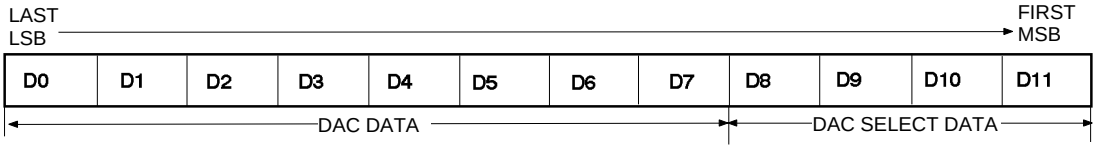
EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
④	DI	Serial data input terminal to input 12-bit long serial data
①	Do	Terminal to output MSB data of 12-bit shift register
③	CLK	Shift clock input terminal.Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
②	LD	When H-level signal is input to this terminal,the value stored in 12-bit shift register is loaded in decoder and D-A converter output register
⑤	Ao1	8-bit D-A converter output terminal
⑥	Ao2	
⑪	Ao3	
⑫	Ao4	
⑬	Ao5	
⑭	Ao6	
⑯	V_{CC}	Power supply terminal
⑧	GND	GND terminal
⑮	V_{DD}	D-A converter upper reference voltage input terminal
⑨	V_{SS}	D-A converter lower reference voltage input terminal

BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



DIGITAL DATA FORMAT

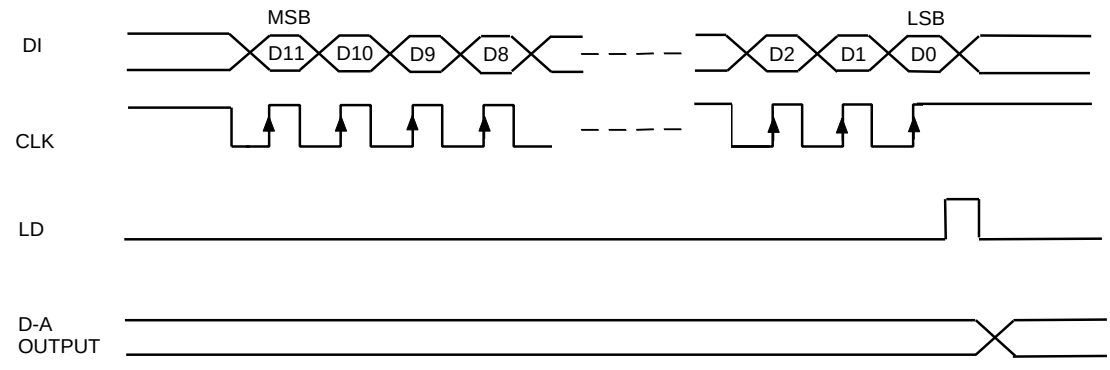


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 1 +VrefL
1	0	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 2 +VrefL
0	1	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 3 +VrefL
1	1	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 4 +VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(VrefU-VrefL) / 256 X 255 +VrefL
1	1	1	1	1	1	1	1	VrefU

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Don't care
1	0	0	0	Don't care
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

* VrefU=V_{DD}
VrefL=Vss

TIMING CHART (MODEL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~+7.0	V
V_{DD}	Upper reference voltage of D-A converter		-0.3~+7.0	V
V_{IN}	Input voltage		-0.3~V_{CC}+0.3	V
Vo	Output voltage		-0.3~V_{CC}+0.3	V
Pd	Power dissipation		150	mW
Topr	Operating temperature		-20~+85	℃
Tstg	Storage temperature		-40~+125	℃

ELECTRICAL CHARACTERISTICS

Digital part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},GND,VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		2.7	3.0	3.6	V
Icc	Circuit current	CLK=1MHz operation,Vcc=3V,I_{AO}=0μA			3.5	mA
I_{ILK}	Input leak current	V_{IN}=0~V_{CC}	-10		10	μA
V_{IL}	Input low voltage				0.2V_{CC}	V
V_{IH}	Input high voltage		0.8V_{CC}			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400μA	V_{CC}-0.4			V

Analog part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
IrefU	Current dissipation	VrefU=3V,VrefL=0V Data condition:maximum current		1.4	2.5	mA
VrefU	D-A converter upper reference voltage range	Reference voltage can not always be set to any value in this range,because it is restricted to the buffer amplifier output voltage range	0.7Vcc		Vcc	V
VrefL	D-A converter lower reference voltage range		GND		0.3Vcc	V
V_{AO}	Buffer amplifier output voltage range	I_{AO}=±500μA	0.1		Vcc-0.1	V
		I_{AO}=+500μA -200μA	0.2		Vcc-0.2	
I_{AO}	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-0.3		1	mA
S_{DL}	Differential nonlinearity error	Vcc=2.760V VrefU=2.610V VrefL=0.050V(10mV/LSB) Without load(I_{AO}=±0)	-1.0		1.0	LSB
S_L	Nonlinearity error		-1.5		1.5	LSB
S_{ZERO}	Zero code error		-2		2	LSB
S_{FULL}	Full scale error		-2		2	LSB
Co	Output capacitative load				0.1	μF
Ro	Buffer amplifier output impedance			5		Ω

AC CHARACTERISTICS(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},GND,VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		30			ns
t_{CHD}	Data hold time		60			ns
t_{CHL}	LD set up time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse duration		100			ns
t_{Do}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	D-A output setting time	CL≥100pF,V_{AO}:0.1⇄ 2.6V The time until the output becomes the final value of 1/2 LSB			300	µs

TIMING CHART