# SAA7893HL

Super audio media player

**Rev. 02 — 26 February 2003** **Product data**

## 1. General description

Thanks to the superior sound quality and multichannel capability of Super Audio CD (SACD) technology, multimedia devices such as DVD players and home cinema systems are incorporating SACD functionality. Philips' Super Audio Media Player (SA-MP) provides a flexible, state-of-the-art solution for SACD playback on DVD architectures.

Built around the SAA7893HL SACD processor, SA-MP system solution delivers complete SACD functionality, avoiding the need for continual redesign and re-integration of SACD into various applications. The system is completed with a single 64 Mbit SDRAM and has extensive software processing options, resulting in low total system cost (see Figure 1).

With integrated support for multiple loaders, the SAA7893 supports a variety of DVD platforms. High level and standard software interfaces – optimized for easy design-in – further enhance adaptability, enabling designers to build SACD players on many different hardware and software platforms. This ensures that the SA-MP can be left unchanged even if the SACD playback hardware is altered, again minimizing development effort.

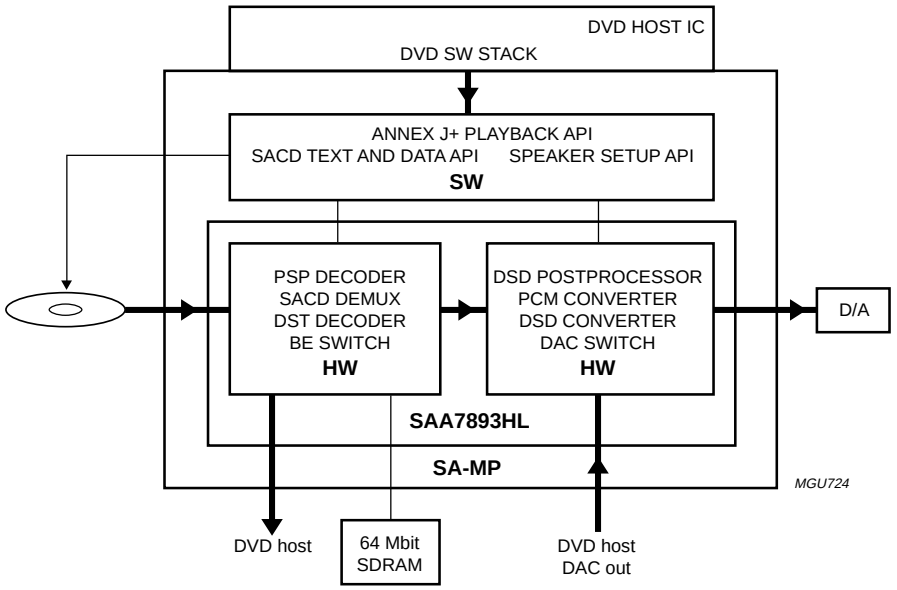



**Fig 1. General block diagram.**

## 1.1 Hardware

The SA-MP hardware consists of the SAA7893HL device. A typical HW block diagram of a DVD system incorporating the SAA7893HL is shown in Figure 2.

The SAA7893HL takes sector data from the front-end. The front-end is controlled by the DVD host via the SA-MP software stack. The SAA7893HL uses one 64 Mbit SDRAM for audio data buffering and storage of SACD TOCs. The front-end timing can be fully asynchronous from all clocks.

The 6-channel DAC outputs of the DVD host are routed via the SAA7893HL which provides a DAC switch function between SACD mode and DVD mode. The audio outputs of the SAA7893HL operate on the system audio clock.

The DVD back-end communicates with the SAA7893HL via a host bus. The system clock and the system audio clock are allowed to be asynchronous.

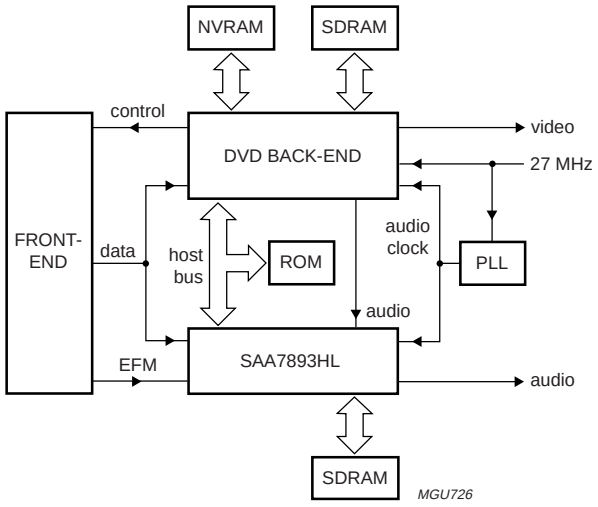



**Fig 2. Hardware block diagram.**

## 1.2 Software

The SA-MP software is delivered in the form of a library in the development environment of the DVD host. The SA-MP software has been developed in ANSI-C using conventional software technology to allow easy integration into any development environment. A typical software block diagram of a DVD system incorporating SA-MP is shown in Figure 3.

At the device driver and HW-level, SA-MP interfaces with the SAA7893HL and a front-end driver. At the infrastructure level, SA-MP interfaces with an Operating System Abstraction layer (OSA). At the application level, SA-MP provides a high-level playback and post-processing interface which is easy to integrate into typical applications.

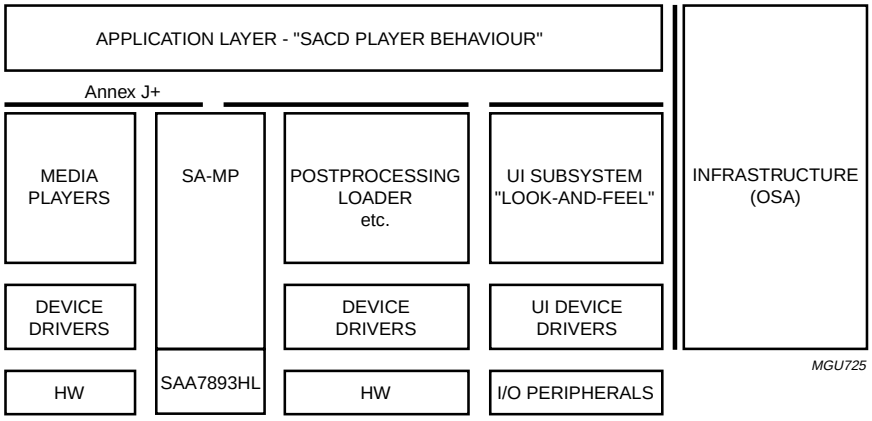



**Fig 3. Software block diagram.**

# 2. Features

## 2.1 Components

- SAA7893HL second generation SACD processor IC
- SA-MP Annex J+ level software stack.

## 2.2 HW interfaces

- Front-end, supports 3 types:
  - UDE
  - FEC
  - $I^2S$-bus
- Flexible PSP detection from EFM signal with AGC, without EFM clock (digital PLL)
- (DVD-)host bus, supports 3 types:
  - Separate address/data bus (SAD16) with 16-bit data bus (3 different modes)
  - Multiplexed address/data bus (MAD16) with 16-bit data bus (2 different modes)
  - Separate address/data bus (SAD08) with 8-bit data bus (1 mode)
- 16-bit 100 MHz SDRAM interface supports one 64 Mbit device
- 6-channel $I^2S$-PCM audio input 44.1, 48, 88.2, 96, 176.4 or 192 kHz at 16-bit or 24-bit
- 6-channel DSD or $I^2S$-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- 2-channel DSD or $I^2S$-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- Audio clock reference $256f_s$, $384f_s$, $512f_s$ or $768f_s$
- System clock 27 to 35 MHz.

## 2.3 SW interfaces

- Annex J+ level playback interface

- High-level audio post-processing control
- SACD data interface
- System configuration

## 2.4 System

- Full SACD Menu TOC and Area TOC storage in VBR
- Front-end clock asynchronous to other clocks

## 2.5 System configuration

- D/A converters:
  - DSD and PCM selectable pin sharing configuration
  - DSD clock polarity
- Audio and system clock asynchronous
- Front-end type

## 2.6 SACD playback

- SACD playback:
  - Multi-channel
  - 2-channel
- PSP processing
- Decrypting and demultiplexing
- VBR management
- DST decoding
- Fade processing
- Annex J+ level software interface:
  - Stop
  - Pause
  - Play
  - Fast forward
  - Fast reverse
  - Next/previous track
  - Program and play playlist
  - Repeat (Track, All or AB)
  - Shuffle
  - Introscan
  - Time search

## 2.7 Audio postprocessing

- DSD Bass Management with support of:
  - Dolby® configuration 0 (LLL1)
  - Dolby® configuration 1 (SSS1)
  - Dolby® configuration 2 (LSS0)
- Programmable bass filter frequency and slope:

- 60, 80, 100, 120 Hz
- 12, 18, 24 dB/Oct

(other frequencies or slopes are possible on customer request)

- DSD down mixing:
  - 2/2
  - 3/0
  - 2/0
  - separate 2/0
- DSD attenuation function 0 to −90 dB, programmable per channel
- DSD delay function total 65 ms (approximately 20 meters), programmable per channel
- 6-channel PCM input:
  - 44.1, 88.2, 176.4, 48, 96 or 192 kHz at 16-bit or 24-bit
  - PCM to DSD upsampling with 3 programmable Sigma-Delta and anti-aliasing filter modes
  - Attenuation and delay as with DSD
- DSD to PCM conversion 88.2, 176.4 kHz at 24-bit.

### 2.8 SACD data and text

- Album info
- Disc info
- Album or disc text
- Area text
- Track data
- Track text.

### 2.9 General

- E-JTAG for board test and debug
- 3.3 V pad supply voltage
- 1.8 V core supply voltage
- 1.8 V analog supply voltage
- LQFP128 package
- 0.18 µm CMOS process.

## 3. Applications

- Consumer DVD players
- Home cinema
- Car audio systems.

# 4. Ordering information

**Table 1: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| SAA7893HL | LQFP128 | plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm$^2$ | SOT425-1 |

# 5. Block diagram

Figure 4 shows the block diagram of the SAA7893HL with all defined functions.

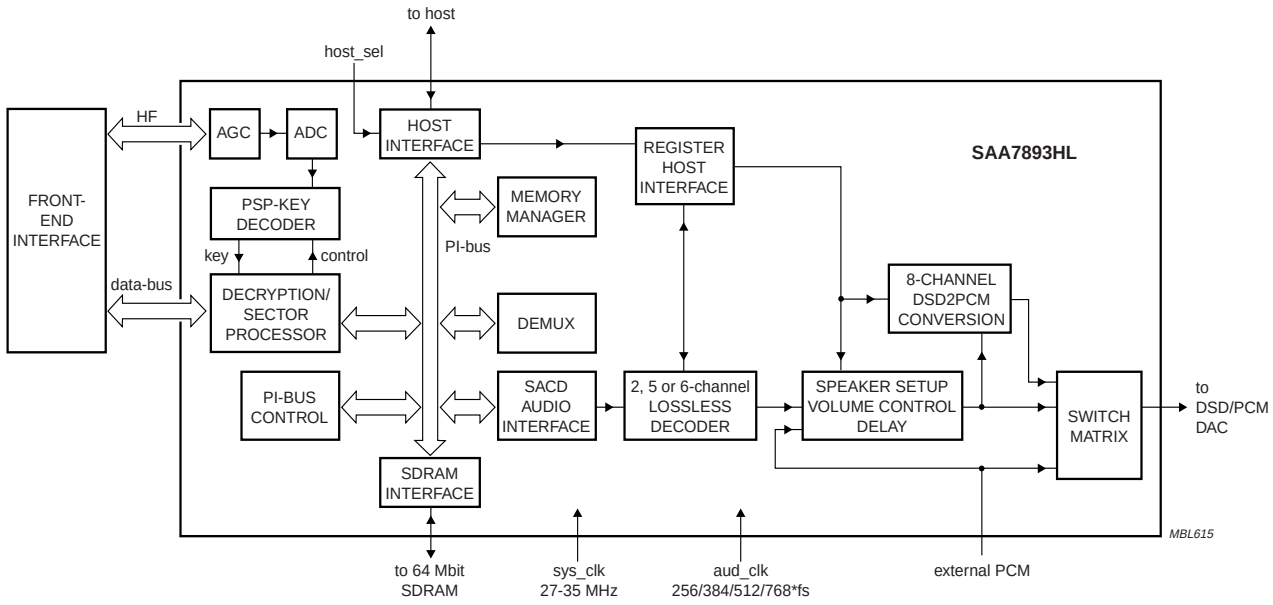



**Fig 4. Block diagram.**

# 6. Pinning information

## 6.1 Pinning

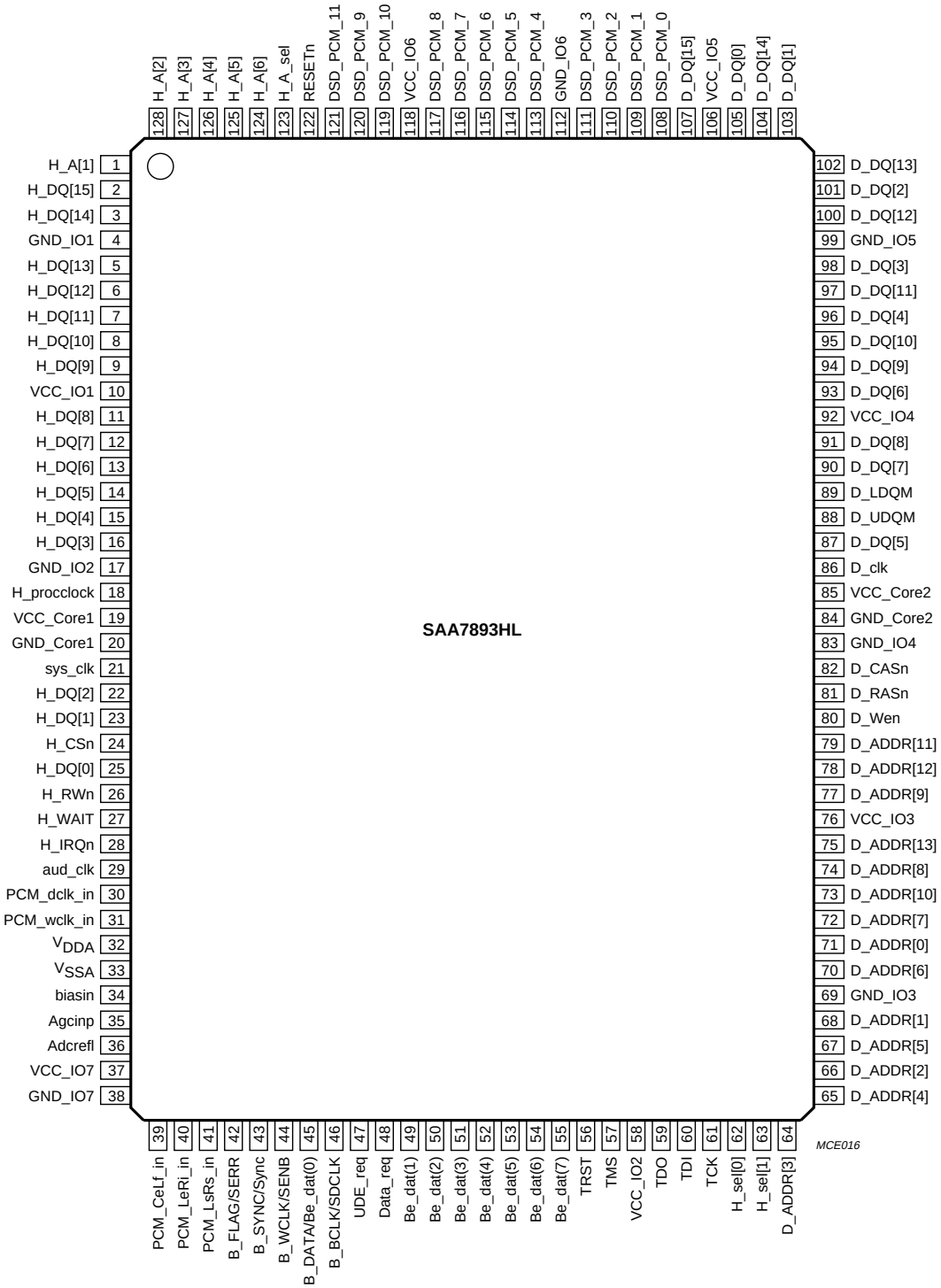



**Fig 5. Pin configuration.**

## 6.2 Pin description

**Table 2: Pin description**

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| H_A[1] | 1 | IN | address bus |
| H_DQ[15] | 2 | I/O10 | data bus |
| H_DQ[14] | 3 | I/O10 | data bus |
| GND_IO1 | 4 | GND_IO | GND I/O pads |
| H_DQ[13] | 5 | I/O10 | data bus |
| H_DQ[12] | 6 | I/O10 | data bus |
| H_DQ[11] | 7 | I/O10 | data bus |
| H_DQ[10] | 8 | I/O10 | data bus |
| H_DQ[9] | 9 | I/O10 | data bus |
| VCC_IO1 | 10 | VCC_IO | $V_{CC}$ I/O pads |
| H_DQ[8] | 11 | I/O10 | data bus |
| H_DQ[7] | 12 | I/O10 | data bus |
| H_DQ[6] | 13 | I/O10 | data bus |
| H_DQ[5] | 14 | I/O10 | data bus |
| H_DQ[4] | 15 | I/O10 | data bus |
| H_DQ[3] | 16 | I/O10 | data bus |
| GND_IO2 | 17 | GND_IO | GND I/O pads |
| H_procclock | 18 | IN | host processor EMI interface clock |
| VCC_Core1 | 19 | VCC_core | core supply voltage |
| GND_Core1 | 20 | GND_core | core ground |
| sys_clk | 21 | IN | system clock |
| H_DQ[2] | 22 | I/O10 | data bus |
| H_DQ[1] | 23 | I/O10 | data bus |
| H_CSn | 24 | IN | host chip select; active LOW |
| H_DQ[0] | 25 | I/O10 | data bus |
| H_RWn | 26 | IN | read = 1; write = 0 |
| H_WAIT | 27 | O10 | wait signal |
| H_IRQn | 28 | O10 | interrupt request; active LOW |
| aud_clk | 29 | IN | DSD audio clock |
| PCM_dclk_in | 30 | IN | PCM data clock |
| PCM_wclk_in | 31 | IN | PCM word clock |
| $V_{DDA}$ | 32 | VDDCO | $V_{DD}$ of ADC |
| $V_{SSA}$ | 33 | VSSCO | $V_{SS}$ of AGC and ADC; connected to substrate |
| biasin | 34 | APIO | bias current input |
| Agcinp | 35 | APIO | AGC positive input signal; HF in |
| Adcrefl | 36 | APIO | ADC decoupling |
| VCC_IO7 | 37 | VCC_IO | $V_{CC}$ I/O pads |
| GND_IO7 | 38 | GND_IO | GND I/O pads |
| PCM_CeLf_in | 39 | IN | PCM data center or LFE |

**Table 2: Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| PCM_LeRi_in | 40 | IN | PCM data left or right |
| PCM_LsRs_in | 41 | IN | PCM data left or right surround |
| B_FLAG/SERR | 42 | IN | $I^2S$-bus flag (EDC flag) |
| B_SYNC/Sync | 43 | IN | sector sync or absolute time sync |
| B_WCLK/SENB | 44 | IN | $I^2S$-bus word clock or UDE data sense from host |
| B_DATA/Be_dat(0) | 45 | IN | $I^2S$-bus data or LSB data of parallel interface |
| B_BCLK/SDCLK | 46 | IN | $I^2S$-bus bit clock |
| UDE_req | 47 | IN | host request data from front-end; routed via the SAA7893HL |
| Data_req | 48 | O10 | data request for UDE |
| Be_dat(1) | 49 | IN | front-end parallel data interface |
| Be_dat(2) | 50 | IN | front-end parallel data interface |
| Be_dat(3) | 51 | IN | front-end parallel data interface |
| Be_dat(4) | 52 | IN | front-end parallel data interface |
| Be_dat(5) | 53 | IN | front-end parallel data interface |
| Be_dat(6) | 54 | IN | front-end parallel data interface |
| Be_dat(7) | 55 | IN | front-end parallel data interface |
| TRST | 56 | IN1 | boundary scan reset |
| TMS | 57 | IN1 | boundary scan mode select |
| VCC_IO2 | 58 | VCC_IO | $V_{CC}$ I/O pads |
| TDO | 59 | O10 | output |
| TDI | 60 | IN1 | boundary scan data input |
| TCK | 61 | IN | boundary scan clock |
| H_sel[0] | 62 | IN | host select signals: SAD16, MAD16 and SAD08 |
| H_sel[1] | 63 | IN | host select signals: SAD16, MAD16 and SAD08 |
| D_ADDR[3] | 64 | O10 | SDRAM address bus |
| D_ADDR[4] | 65 | O10 | SDRAM address bus |
| D_ADDR[2] | 66 | O10 | SDRAM address bus |
| D_ADDR[5] | 67 | O10 | SDRAM address bus |
| D_ADDR[1] | 68 | O10 | SDRAM address bus |
| GND_IO3 | 69 | GND_IO | GND I/O pads |
| D_ADDR[6] | 70 | O10 | SDRAM address bus |
| D_ADDR[0] | 71 | O10 | SDRAM address bus |
| D_ADDR[7] | 72 | O10 | SDRAM address bus |
| D_ADDR[10] | 73 | O10 | SDRAM address bus |
| D_ADDR[8] | 74 | O10 | SDRAM address bus |
| D_ADDR[13] | 75 | O10 | SDRAM address bus |
| VCC_IO3 | 76 | VCC_IO | $V_{CC}$ I/O pads |
| D_ADDR[9] | 77 | O10 | SDRAM address bus |

**Table 2: Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| D_ADDR[12] | 78 | O10 | SDRAM address bus |
| D_ADDR[11] | 79 | O10 | SDRAM address bus |
| D_Wen | 80 | O10 | read or write |
| D_RASn | 81 | O10 | row address select; active LOW |
| D_CASn | 82 | O10 | column address select; active LOW |
| GND_IO4 | 83 | GND_IO | GND I/O pads |
| GND_Core2 | 84 | GND_core | core ground |
| VCC_Core2 | 85 | VCC_core | core supply voltage |
| D_clk | 86 | O10 | clock signal needed for SDRAM |
| D_DQ[5] | 87 | I/O10 | data bus |
| D_UDQM | 88 | O10 | DQ mask enable (upper) |
| D_LDQM | 89 | O10 | DQ mask enable (lower) |
| D_DQ[7] | 90 | I/O10 | data bus |
| D_DQ[8] | 91 | I/O10 | data bus |
| VCC_IO4 | 92 | VCC_IO | $V_{CC}$ I/O pads |
| D_DQ[6] | 93 | I/O10 | data bus |
| D_DQ[9] | 94 | I/O10 | data bus |
| D_DQ[10] | 95 | I/O10 | data bus |
| D_DQ[4] | 96 | I/O10 | data bus |
| D_DQ[11] | 97 | I/O10 | data bus |
| D_DQ[3] | 98 | I/O10 | data bus |
| GND_IO5 | 99 | GND_IO | GND I/O pads |
| D_DQ[12] | 100 | I/O10 | data bus |
| D_DQ[2] | 101 | I/O10 | data bus |
| D_DQ[13] | 102 | I/O10 | data bus |
| D_DQ[1] | 103 | I/O10 | data bus |
| D_DQ[14] | 104 | I/O10 | data bus |
| D_DQ[0] | 105 | I/O10 | data bus |
| VCC_IO5 | 106 | VCC_IO | $V_{CC}$ I/O pads |
| D_DQ[15] | 107 | I/O10 | data bus |
| DSD_PCM_0 | 108 | O10 | 6-channel data output |
| DSD_PCM_1 | 109 | O10 | 6-channel data output |
| DSD_PCM_2 | 110 | O10 | 6-channel data output |
| DSD_PCM_3 | 111 | O10 | 6-channel data output |
| GND_IO6 | 112 | GND_IO | GND I/O pads |
| DSD_PCM_4 | 113 | O10 | 6-channel data output |
| DSD_PCM_5 | 114 | O10 | 6-channel data output |
| DSD_PCM_6 | 115 | O10 | 6-channel clock/control |
| DSD_PCM_7 | 116 | O10 | 6-channel clock/control |
| DSD_PCM_8 | 117 | O10 | 2-channel clock/control |
| VCC_IO6 | 118 | VCC_IO | $V_{CC}$ I/O pads |

**Table 2: Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| DSD_PCM_10 | 119 | O10 | 2-channel data output |
| DSD_PCM_9 | 120 | O10 | 2-channel clock or control |
| DSD_PCM_11 | 121 | O10 | 2-channel data output |
| RESETn | 122 | IN | asynchronous reset; active LOW |
| H_A_sel | 123 | IN | address select |
| H_A[6] | 124 | IN | address bus |
| H_A[5] | 125 | IN | address bus |
| H_A[4] | 126 | IN | address bus |
| H_A[3] | 127 | IN | address bus |
| H_A[2] | 128 | IN | address bus |

[1] Explanation of input and output ports:
IN: digital input port; all dedicated inputs are TTL tolerant.
IN1: digital input port with internal pull-up resistor.
I/O10: bidirectional port with 10 ns slew rate.
O10: 3-state (in test mode) output port with 10 ns slew rate.
APIO: analog input port.
VDDCO: analog $V_{DD}$ port (1.8 V).
VSSCO: analog $V_{SS}$ port.
GND_IO: ground for I/O pads.
VCC_IO: $V_{CC}$ for I/O pads (3.3 V).
GND_core: ground for core.
VCC_core: $V_{CC}$ for core (1.8 V).

# 7. Interfaces

## 7.1 Host interface

Different types of host busses are supported:

- Separate address/data bus with 16-bit data bus (3 different modes)
- Multiplexed address/data bus with 16-bit data bus (2 different modes)
- Separate address/data bus with 8-bit data bus (1 mode).

The host interface type is set via the dedicated pins H_sel and sys_clk. The SAA7893HL has a dedicated interrupt output pin.

## 7.2 Front-end interface

### 7.2.1 Data input interface

The SAA7893HL supports three different front-end interfaces which are selectable via the host interface:

- $I^2S$-bus interface: the front-end interface is in essence an $I^2S$-bus interface and therefore, it has to conform to the $I^2S$-bus specification.
- FEC interface

- Parallel interface (UDE data interface part): a parallel front-end interface with a handshake protocol.

### 7.2.2 Analog HF input

The analog HF input, coming from the optical pickup unit, is also fed to the SAA7893HL to extract the copy protection information PSP.

## 7.3 Audio interface

### 7.3.1 Audio input

The audio input is a 6-channel PCM-$I^2S$ input.

### 7.3.2 DAC interface

The audio output is a 6-channel output and a separate stereo output. Both outputs can be set in DSD and in PCM-$I^2S$ mode.

## 7.4 SDRAM interface

The SDRAM interface forms a glueless interface to one 64 Mbit SDRAM device.

Supported devices are only PC100 compliant or faster SDRAM devices:

- Organization: 64 Mbit (1M $\times$ 16 $\times$ 4 banks)
- Refresh period: 4096 cycles per 64 ms
- Clock frequency: $f_{clk} \geq 100$ MHz
- Refresh cycle: $t_{rcar} \leq 70$ ns
- Command period: $t_{rc} \leq 70$ ns.

## 7.5 Clock and reset input

Different processing clocks are needed in the SAA7893HL:

- sys_clk: system clock for data processing part; frequency can be between 27 and 35 MHz; see Figure 6 and Table 3
- aud_clk: audio clock reference; can be 256/384/512/768 $\times$ $f_s$ ($f_s$ = 44.1 to 48 kHz); see Figure 7 and Table 4
- proc_clk: host processor clock (only used in SAD16_01/02 mode)
- B_BCLK: front-end bit/byte clock.

It is not required that these clocks are locked.

RESETn is an asynchronous reset and should be kept LOW for at least 10 periods of sys_clk.

### 7.5.1 System clock (sys_clk) definitions

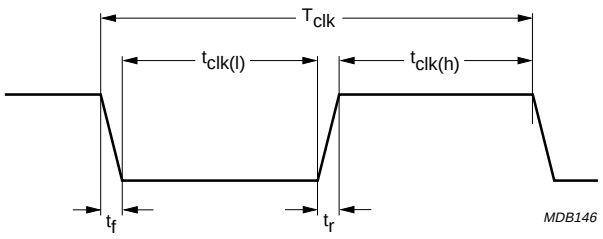



**Fig 6. Sys_clk characteristics**

**Table 3: Definitions of sys_clk**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | clock cycle time | clock frequency from 27 to 35 MHz | 28.5 | 37.4 | ns |
| $t_{clk(l)}$ | clock time low | | 11.4 | 22.4 | ns |
| $t_{clk(h)}$ | clock time high | | 11.4 | 22.4 | ns |
| $t_f$ | fall time | | - | 4 | ns |
| $t_r$ | rise time | | - | 4 | ns |
| $\delta_{clk}$ | clock duty cycle | | 40 | 60 | % |

### 7.5.2 Audio clock (aud_clk) definitions

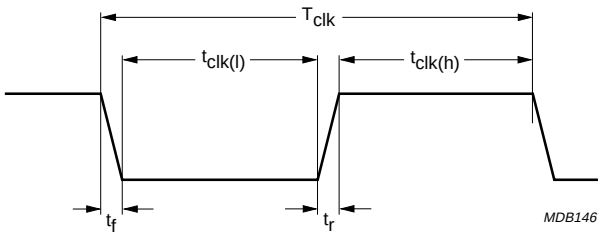



**Fig 7. Aud_clk characteristics**

**Table 4: Definitions of aud_clk**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | clock cycle time | clock frequency from 256 × 44.1 kHz to 768 × 48 kHz | 27 | 88.6 | ns |
| $t_{clk(l)}$ | clock time low | | 10.8 | 53.1 | ns |
| $t_{clk(h)}$ | clock time high | | 10.8 | 53.1 | ns |
| $t_f$ | fall time | | - | 4 | ns |
| $t_r$ | rise time | | - | 4 | ns |
| $\delta_{clk}$ | clock duty cycle | | 40 | 60 | % |

## 7.6 Test inputs

Standard BST functionality is provided. Device data:

Version: B0010

Manufacturer ID: B000 0001 0101

Part no: B0011 0101 0110 0100.

# 8. Host interface

## 8.1 General description

The SAA7893HL is capable to communicate with the hosts (families) via their own busses as given in Table 5.

**Table 5: Host communications**

| Name | Description |
|---|---|
| SAD16_01 | Separate Address/Data on 16-bit data bus with wait signal, based on proc_clk |
| SAD16_02 | Separate Address/Data on 16-bit data bus with wait signal, based on sys_clk and proc_clk |
| SAD16_03 | Separate Address/Data on 16-bit data bus without wait signal |
| MAD16_01 | Multiplexed Address/Data on 16-bit data bus mode 01 |
| MAD16_02 | Multiplexed Address/Data on 16-bit data bus mode 02 |
| SAD08 | Separate Address/Data on 8-bit data bus |

The type of host is selected via two input pins H_sel[1] and H_sel[0] and the proc_clk signal. In Table 6 the settings for the different host modes are given with the expected input clock(s).

**Table 6: Clock selection**

| H_sel[1:0] | Mode | External provided clocks | | Internal used system clock |
|---|---|---|---|---|
| | | sys_clk | proc_clk | |
| 00 | SAD16_01 | no | yes | proc_clk/2 |
| 10 | SAD16_02 | yes | yes | sys_clk |
| 01 | SAD16_03 | yes | logic 1 | sys_clk |
| 11 | MAD16_01 | yes | logic 0 | sys_clk |
| 11 | MAD16_02 | yes | logic 1 | sys_clk |
| 01 | SAD08 | yes | logic 0 | sys_clk |

In all modes the range of the required internal system clock is between 27 and 35 MHz.

The pin mapping in the different modes is shown in Table 7.

**Table 7: Host communication data mapping**

| SAA7893HL name | Type | SAD16_01; SAD16_02 | SAD08 | MAD16_01 | MAD16_02 | SAD16_03 |
|---|---|---|---|---|---|---|
| H_A_sel | IN | CPU_A(7) | A(11) | ALE | ALE | LA(7) |
| H_A[3:1] | IN | CPU_A(4:1) | A(3:1) | LA(2:0) | addr[3:1] | LA(3:1) |
| H_A[4] | IN | CPU_A(4:1) | A(4) | LA(3) | n.c. | LA(4) |
| H_A[6:5] | IN | CPU_A(6:5) | A(6:5) | AD(21:20) | n.c. | LA(6:5) |
| H_DQ[7:0] | I/O | CPU_D(7:0) | D(7:0) | AD(11:4) | data(7:0) | LD(7:0) |

**Table 7: Host communication data mapping** *...continued*

| SAA7893HL name | Type | SAD16_01; SAD16_02 | SAD08 | MAD16_01 | MAD16_02 | SAD16_03 |
|---|---|---|---|---|---|---|
| H_DQ[11:8] | I/O | CPU_D(11:8) | A(10:7) | AD(1512) | data(11:8) | LD(11:8) |
| H_DQ[12] | I/O | CPU_D(12) | n.c. | AD(16) | data(12) | LD(12) |
| H_DQ[13] | I/O | CPU_D(13) | ASn | AD(17) | data(13) | LD(13) |
| H_DQ[14] | I/O | CPU_D(14) | DSn | AD(18) | data(14) | LD(14) |
| H_DQ[15] | I/O | CPU_D(15) | A(0) | AD(19) | data(15) | LD(15) |
| H_IRQn | O | IRQN | IRQn | IRQN | IRQN | IRQN |
| H_procclock | IN | CPU_procclk | logic 0 | logic 0 | logic 1 | logic 1 |
| sys_clk | IN | n.c.; sysclk | PCI-clk | Sclk | sys_clk | sys_clk |
| H_RWn | IN | CPU_RWn | R/Wn | RD_ | RD_ | RD_ |
| H_WAITn | O | CPU_wait | DSACKn | ACK | HDTACKn | n.c. |
| H_CSn | IN | CPU_CSn | CS | XIO | CSn | CSn |
| H_sel[0] | IN | 0 | logic 1 | logic 1 | logic 1 | logic 1 |
| H_sel[1] | IN | logic 0: mode 1; logic 1: mode 2 | logic 0 | logic 1 | logic 1 | logic 0 |

The internal SAA7893HL address is differently composed in the different modes.

## 8.2 SAD16_01/02 mode

Reading and writing is always done on 16 bits (Hword) base. To save physical pins on the SAA7893HL, the data bus is used to write the 16 MSB address bits, hereafter called ‘the base address’ into the SAA7893HL. Therefore, to access an address inside the SAA7893HL first these 16 MSB bits of the address must be written as a base address for the SAA7893HL indicated by the H_A_sel line. Pin H_A_sel can be mapped to a physical address pin of the host device.

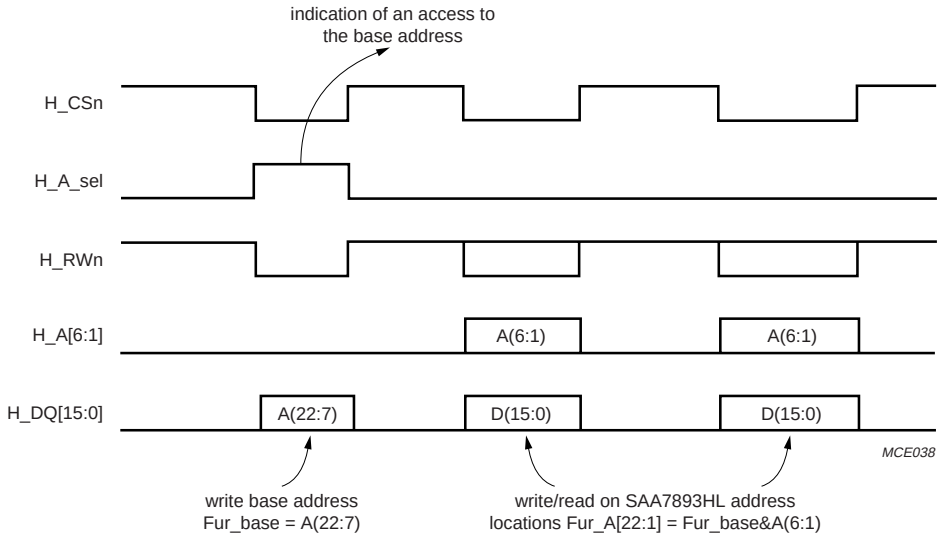



**Fig 8. Write to or read from the SAA7893HL.**

In Figure 8 the principle of first writing the base address indicated by H_A_sel is here visualized. Pin H_A_sel is mapped on address pin H_A[7] of the host. The timing is, of course, not to scale. When the base address is written, multiple accesses can be done whereby the different LSB addresses are mapped on pins H_A[6:1]. In this way a burst of 64 Hwords can be read or written to the same address. The 16 bits base address can be read when H_A_sel is logic 1 and the signal H_RWn indicates a read operation.

Remark: The H_waitn signal is synchronized to H_procclock (pin 18). So it depends on the host used which H_procclock is provided. When the host can accept an asynchronous H_waitn signal, the clock signal connected to the sys_clk input (pin 21) can also be used as the clock signal to the H_procclock input.

### 8.2.1 Write mode: minimum cycle

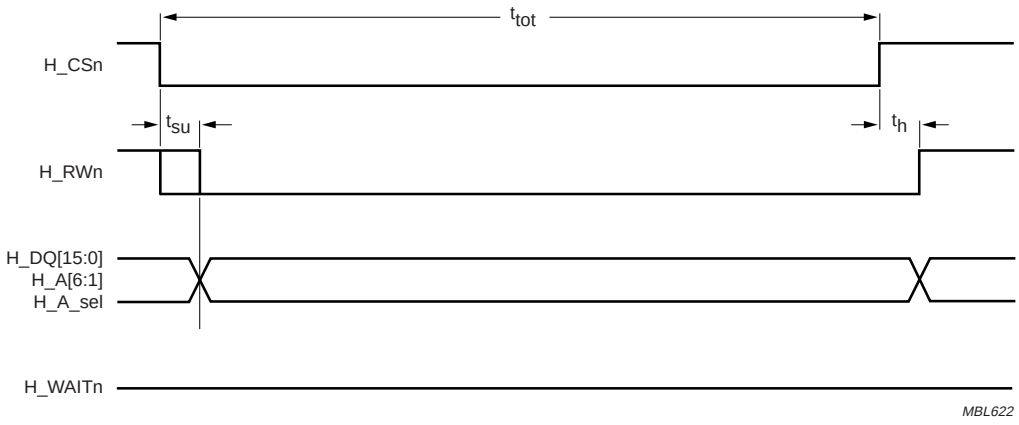



**Fig 9. Timing diagram of writing registers with no wait cycles.**

**Table 8: Timing numbers of writing registers with no wait cycles**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total CSn time | 14 | - | - | sys_clk |
| $t_{su}$ | set-up time from CS to host control/address lines | - | - | 30 | ns |
| $t_h$ | hold time from CS to host control/address lines | 0 | - | - | ns |

### 8.2.2 Read mode: minimum cycle

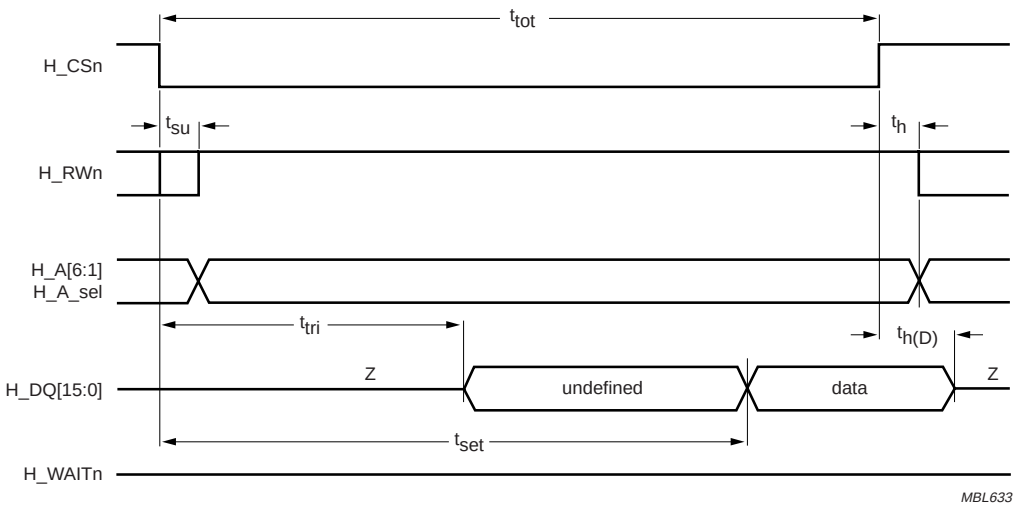



**Fig 10. Timing diagram of reading registers with no wait cycles.**

**Table 9: Timing numbers of reading registers with no wait cycles**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{tot}$ | total CSn time | | 14 | - | - | sys_clk |
| $t_{su}$ | set-up time from CS to host control/address lines | | 0 | - | 30 | ns |
| $t_h$ | hold time from CS to host control/address lines | maximum time is not needed; can be forever | 0 | - | - | ns |
| $t_{tri}$ | time that data bus is set from 3-state to output | | 1 | - | 3 | sys_clk |
| $t_{set}$ | time that data is valid before CS is set to logic 1 | | 60 | - | - | ns |
| $t_{h(D)}$ | hold time from CS to data bus | | 0 | - | - | ns |

### 8.2.3 Write mode: cycles extended using wait protocol

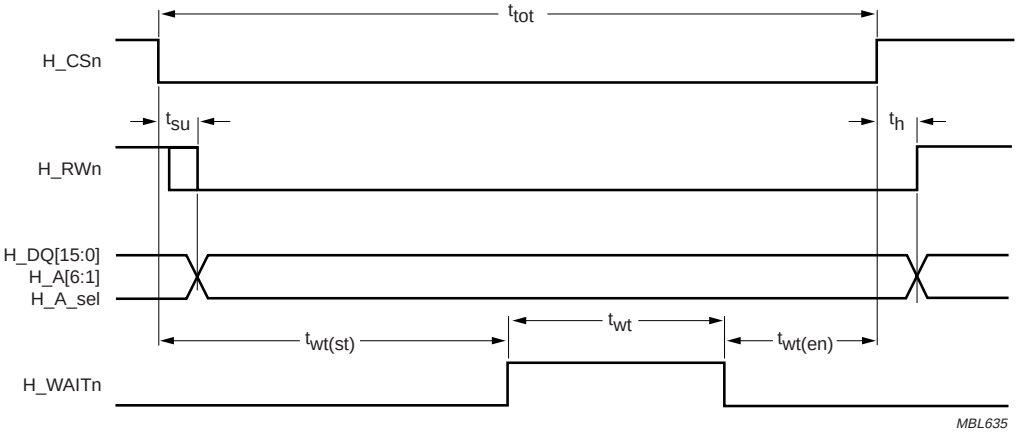



**Fig 11. Timing diagram of writing registers with wait cycles.**

**Table 10: Timing numbers of writing registers with wait cycles**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{tot}$ | total CSn time | | 14 | - | - | sys_clk |
| $t_{su}$ | set-up time from CS to host control/address lines | | 0 | - | 30 | ns |
| $t_h$ | hold time from CS to host control/address lines | | 0 | - | - | ns |
| $t_{wt}$ | active time of H_WAIT when Pi registers are accessed | speed is dependent on load on PI-bus | 3 | 8 | 11 | sys_clk |
| | active time of H_WAIT when external SDRAM is accessed | speed is dependent on load on PI-bus | 3 | 11 | 17 | sys_clk |
| $t_{wt(st)}$ | time from CS until wait becomes active | | 5[1] | - | 6[1] | sys_clk |
| $t_{wt(en)}$ | time H_WAIT inactive until CS becomes inactive | | 10 | - | - | ns |

[1] When the SAA7893HL SAD16 interface is programmed to generate always a H_WAIT signal, the minimum time will be 2 sys_clk cycles and the maximum time will be 3 sys_clk cycles.

### 8.2.4 Read mode: cycles extended using wait protocol

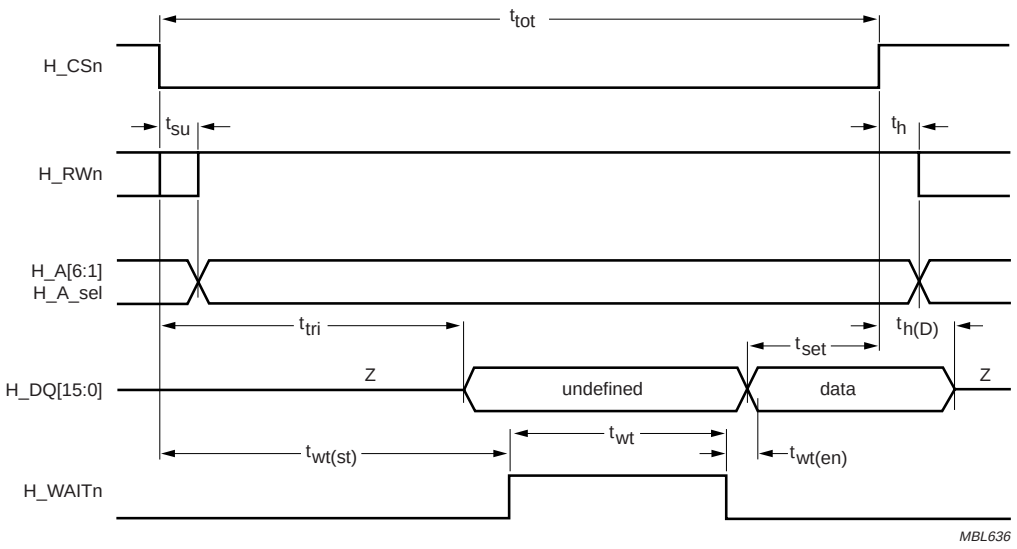



**Fig 12. Timing diagram of reading registers via PI-bus.**

**Table 11: Timing numbers of reading registers via PI-bus**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{tot}$ | total CSn time | | 14[1] | - | - | sys_clk |
| $t_{su}$ | set-up time from CS to host control/address lines | | 0 | - | 30 | ns |
| $t_h$ | hold time from CS to host control/address lines | | 0 | - | - | ns |
| $t_{wt}$ | active time of H_WAIT when Pi registers are accessed | speed is dependent on load on PI-bus | 3 | 8 | 11 | sys_clk |
| | active time of H_WAIT when external SDRAM is accessed | speed is dependent on load on PI-bus | 3 | 11 | 17 | sys_clk |
| $t_{wt(st)}$ | time from CS until wait becomes active | | 5[2] | - | 6[2] | sys_clk |

**Table 11: Timing numbers of reading registers via PI-bus** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{wt(en)}$ | time from H_WAIT negative slope to data set-up | | - | - | 0 | ns |
| $t_{tri}$ | time that data bus is set from 3-state to output | | 1 | - | 3 | sys_clk |
| $t_{set}$ | time that data is valid before CS is set to logic 1 | | 30 | - | - | ns |
| $t_{h(D)}$ | hold time from CS to H_data bus | | 0 | - | - | ns |

[1] When the SAA7893HL SAD16 interface is programmed to generate always a H_WAIT signal of at least 7 sys_clk cycles, then it is no longer required that the minimum time of $t_{tot}$ is 14 sys_clk cycles. The data at the H_DQ output is always available at the negative edge of the H_WAIT signal. The host can deactivate the H_CS signal after the negative edge of the H_WAIT signal and when it has read the data at the H_DQ lines. When a H_WAIT signal is always generated then the timing diagrams in Figure 9 and Figure 10 are no longer applicable.

[2] When the SAA7893HL SAD16 interface is programmed to generate always a H_WAIT signal, the minimum time will be 2 sys_clk cycles and the maximum time will be 3 sys_clk cycles.

### 8.2.5 Host interface connection

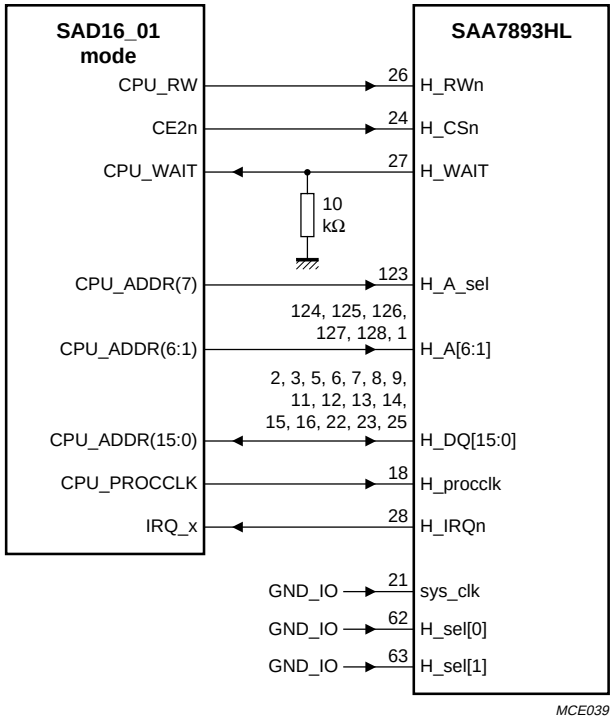



**Fig 13. Host interface connection.**

## 8.3 SAD16_03 mode

To save physical pins on the SAA7893HL, the data bus is used to write the 16 MSB address bits, hereafter called 'the base address', into the SAA7893HL. Therefore, to access an address inside the SAA7893HL first this 16 MSB bits of the address must be written as a base address for the SAA7893HL indicated by the H_A_sel line. Pin H_A_sel can be mapped to a physical address pin of the host device.

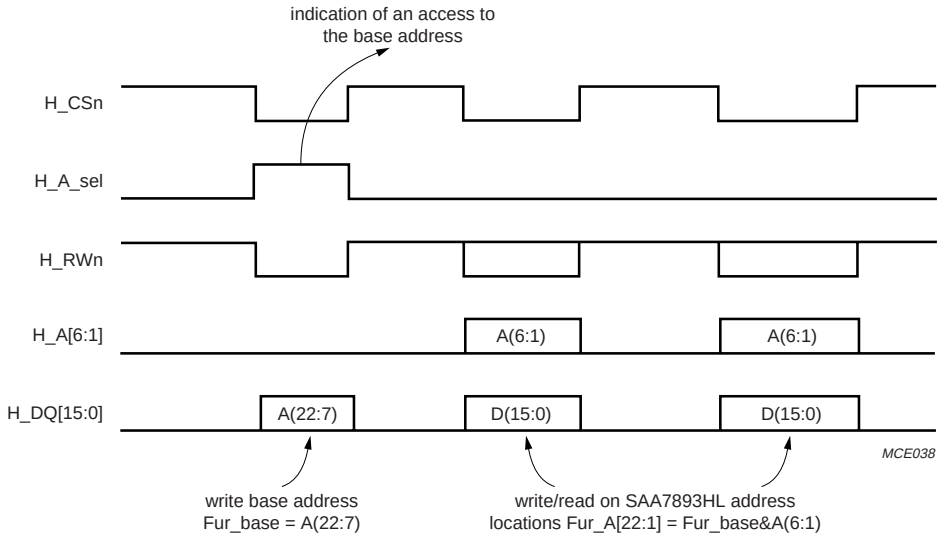



**Fig 14. Write to or read from the SAA7893HL.**

In Figure 14 the principle of first writing the base address indicated by H_A_sel is here visualized. Pin H_A_sel is mapped on address pin H_A[7] of the host. The timing is of course not to scale. When the base address is written, multiple accesses can be done whereby the different LSB addresses are mapped on pins H_A[6:1]. In this way a burst of 64 Hwords can be read or written to the same address. The 16 bits base address can be read when H_A_sel is logic 1 and the signal H_RWn indicates a read operation. In SAD16_03 mode there is in principle no handshake available. Therefore, to read data a double read must be done.

### 8.3.1 Read mode

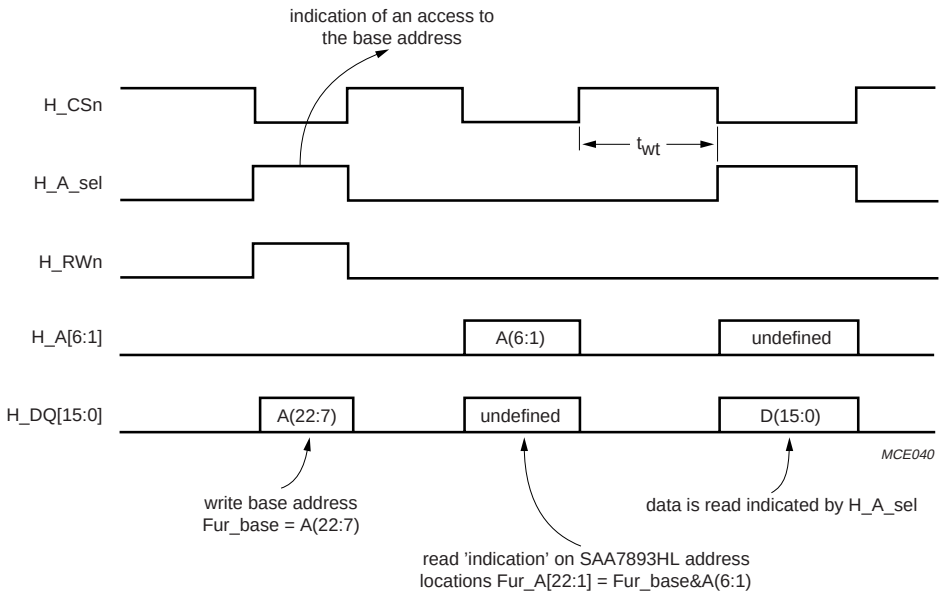



**Fig 15. Read from the SAA7893HL.**

First the 16 bits of the base address are set indicated by the H_A_sel line. Then a read access is started. In SAD16_03 mode there is no handshake line on which the SAA7893HL can indicate that internal read operation is ready. Therefore, to be sure that the requested data is read correctly, an extra read is needed indicated by the H_A_sel line. In this read the data is presented as read by the previous read access. The maximum time that the host must wait before this extra read is started is approximately 30 sys_clk cycles. If in this time a new access is activated this access can be lost.

### 8.3.2 Write mode

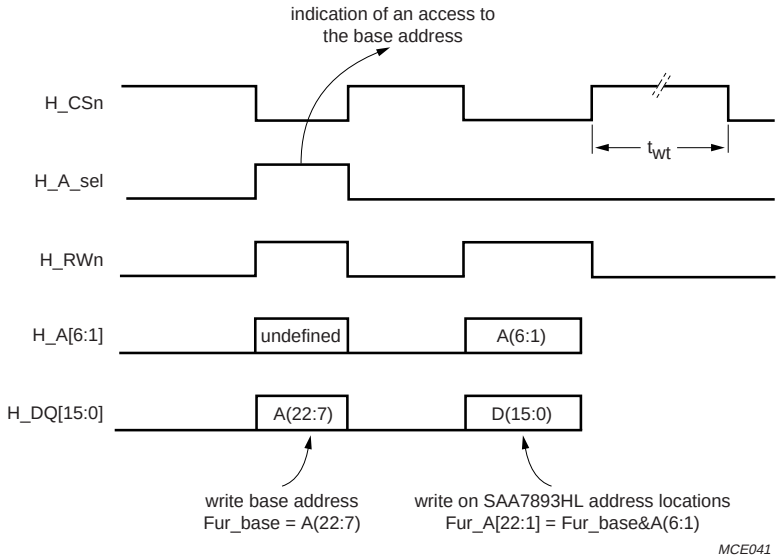



**Fig 16. Write to the SAA7893HL.**

When a write operation is issued the same wait time $t_{wt}$ must be taken into account before a next access may start, but here no double write has to be done.

### 8.3.3 Writing of base address

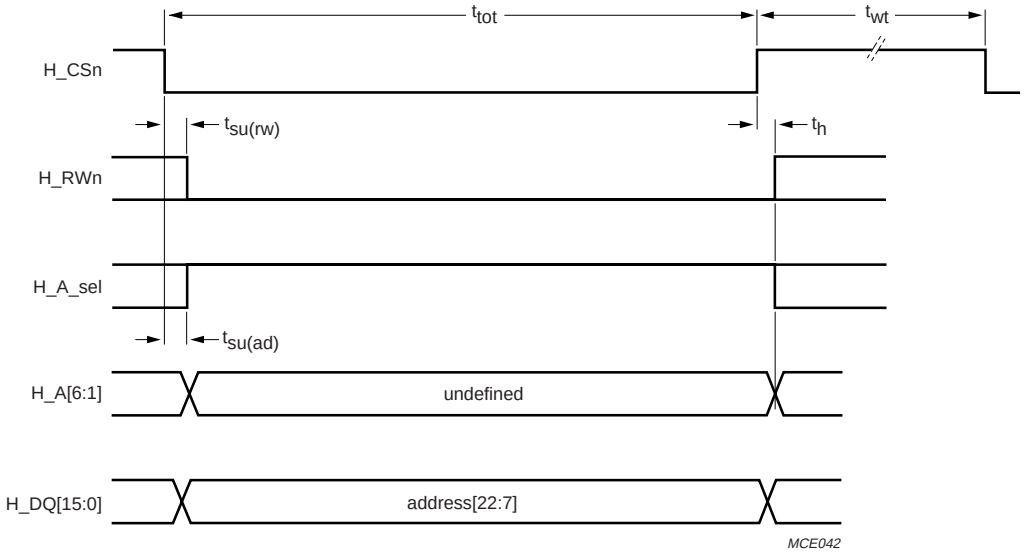



**Fig 17. Timing diagram of writing the base address.**

**Table 12: Timing numbers of base address writing**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total LOW time of H_CSn | | 270 | - | ns |
| $t_{wt}$ | wait time before next cycle may start | if in this time a new cycle is started, the new access cycle could be neglected | 100 | - | ns |
| $t_{su(rw)}$ | set-up time of H_RWn | | - | 0 | ns |
| $t_{su(ad)}$ | set-up time for address | | - | 10 | ns |

### 8.3.4 Writing data to the SAA7893HL

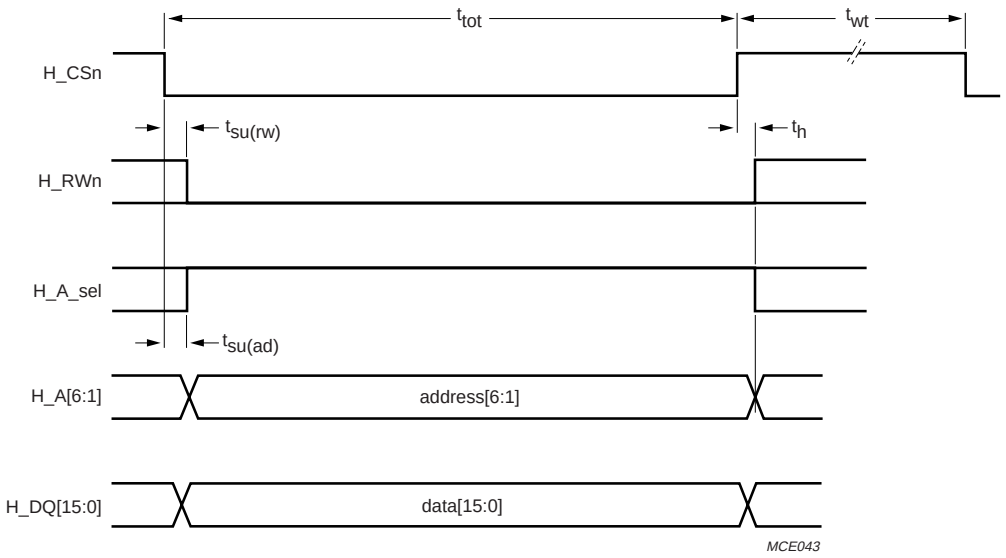



**Fig 18. Writing data to the SAA7893HL.**

**Table 13: Timing numbers of writing data**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total LOW time of H_CSn | | 270 | - | ns |
| $t_{wt}$ | wait time before next cycle may start | if in this time a new cycle is started, the new access cycle could be neglected | 700 | - | ns |
| $t_{su(rw)}$ | set-up time of H_RWn | | - | 0 | ns |
| $t_{su(ad)}$ | set-up time for address | | - | 10 | ns |
| $t_h$ | hold time of H_RWn/address/data with respect to H_CSn | | 0 | - | ns |

### 8.3.5 Reading data from the SAA7893HL

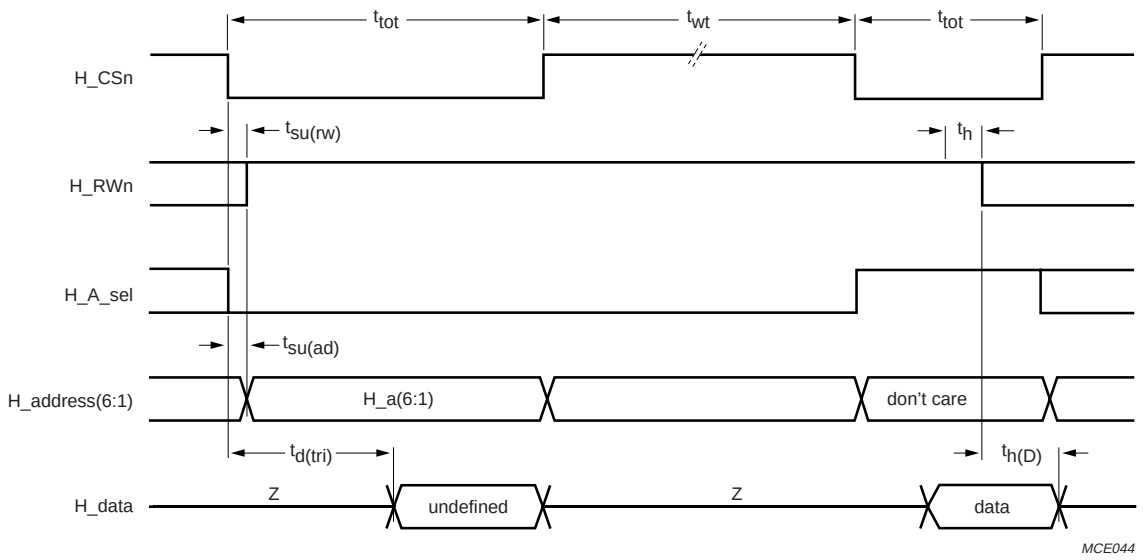



**Fig 19. Reading data from the SAA7893HL.**

**Table 14: Timing numbers of reading data**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total LOW time of H_CSn | | 270 | - | ns |
| $t_{wt}$ | wait time before next cycle may start | if in this time a new cycle is started, the new access cycle could be neglected | 700 | - | ns |
| $t_{su(rw)}$ | set-up time of H_RWn | | - | 0 | ns |
| $t_{su(ad)}$ | set-up time for address | | - | 10 | ns |
| $t_{tri}$ | time that data bus is enabled | time dependent on system clock | 1 | 3 | sys_clk |

### 8.3.6 Host interface connection

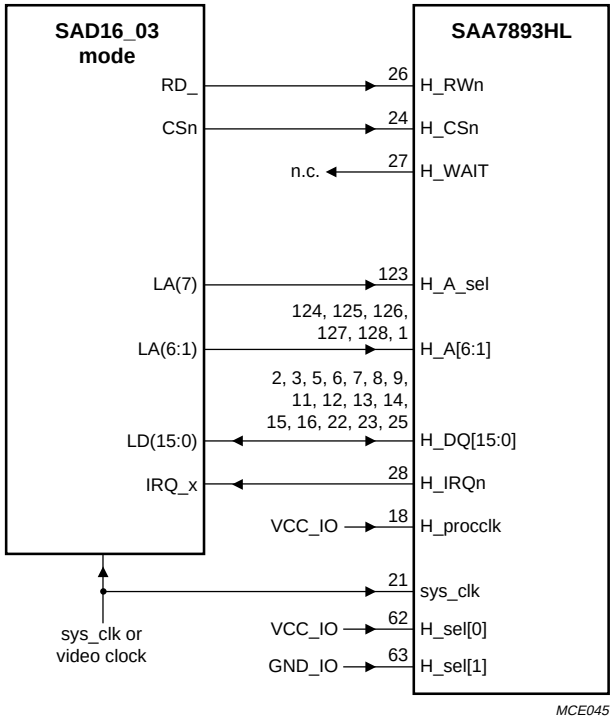



**Fig 20. Host interface connection.**

## 8.4 MAD16_01 mode

Data communication is here always done on a 16-bit data bus. The address is mapped on 6 separate address pins and 16 address/data pins of the SAA7893HL. Therefore, in this mode the complete address is transferred directly in each access cycle.

In Table 7 the internal SAA7893HL address is mapped as follows to the SAA7893HL pins: Fur_H_A[22:1] = H_A[6:5] & H_DQ[15:0] & H_A[4:1].

This address mapping is the default setting, the following address is also possible: Fur_H_A[22:1] = H_A[6:1] & H_DQ[15:0].

The system clock provided in the MAD16_01 mode must be synchronized to the host interface timing.

### 8.4.1 Write mode: minimum cycle

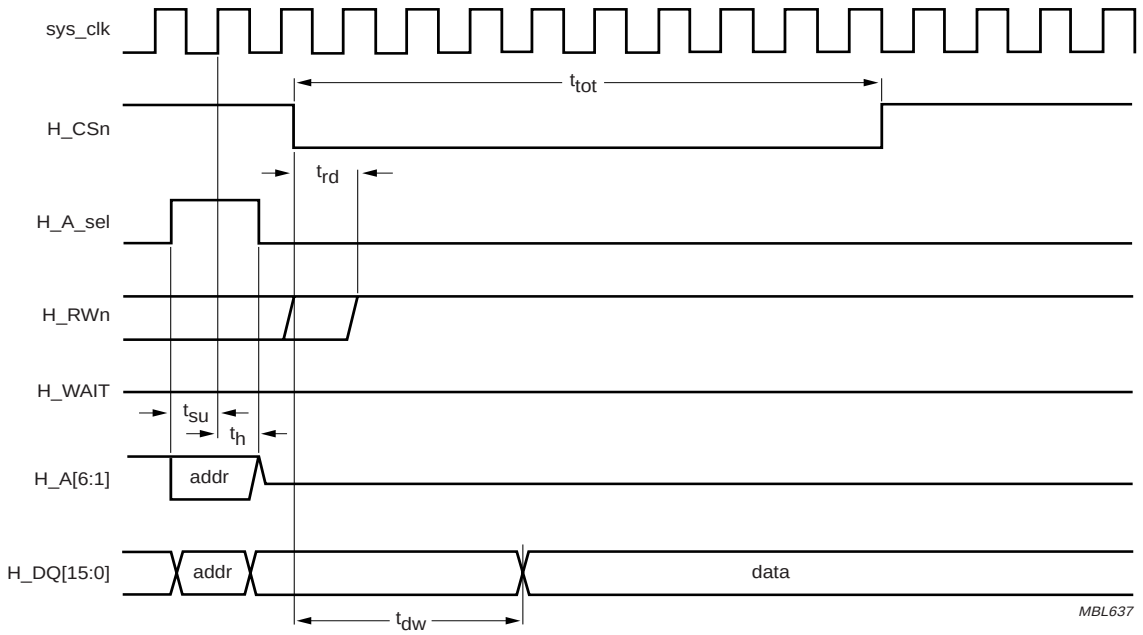



**Fig 21. Timing diagram writing to the SAA7893HL.**

**Table 15: Timing numbers of writing registers**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{tot}$ | total H_CSn time | 8 | - | sys_clk |
| $t_{su}$ | set-up time H_A_sel | 5 | - | ns |
| $t_h$ | hold time of H_A_sel with respect to sys_clk | 5 | - | ns |
| $t_{rd}$ | time H_RWn can change from H_CSn signal | - | 1 | sys_clk |
| $t_{su(D)}$ | data set-up time after H_CSn | 0 | 1 | sys_clk |

### 8.4.2 Read mode: minimum cycle

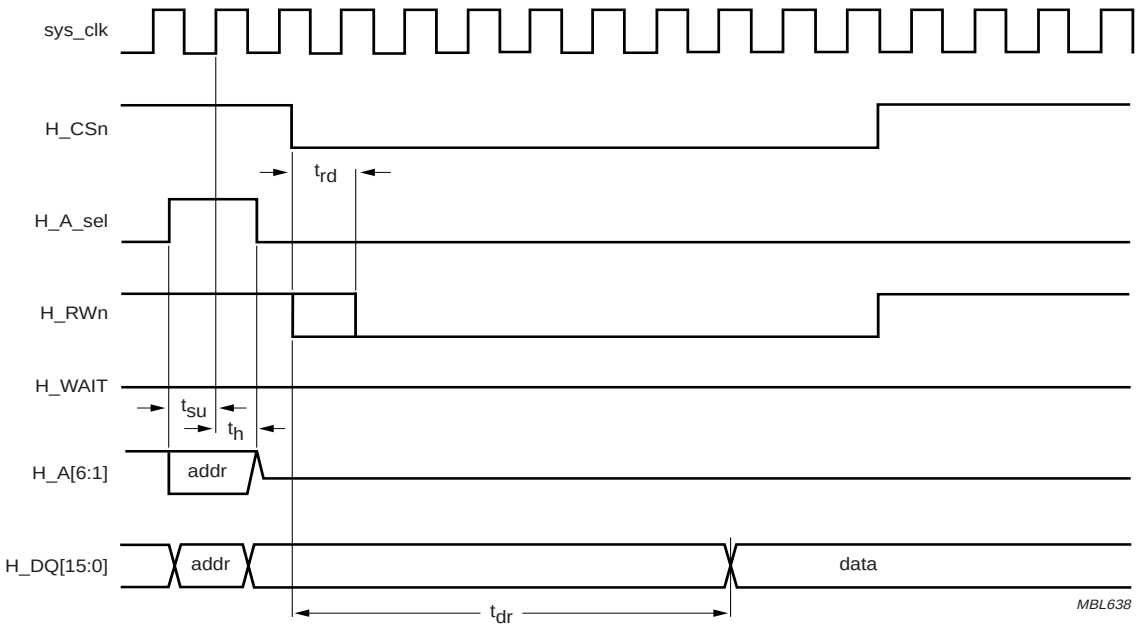



**Fig 22. Timing diagram reading from the SAA7893HL.**

**Table 16: Timing numbers of reading registers**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{su}$ | set-up time H_A_sel | | 5 | - | ns |
| $t_h$ | hold time of H_A_sel with respect to sys_clk | | 5 | - | ns |
| $t_{rd}$ | time H_RWn can change from H_CSn signal | | - | 1 | sys_clk |
| $t_{dr}$ | data set-up time after CSn | time dependent on system clock used | 6 | 8 | sys_clk |
| $t_{dc}$ | data hold time before CSn | not important data is sample after detecting H_CSn = logic 0 | - | - | ns |

### 8.4.3 Write mode: cycles extended using wait protocol

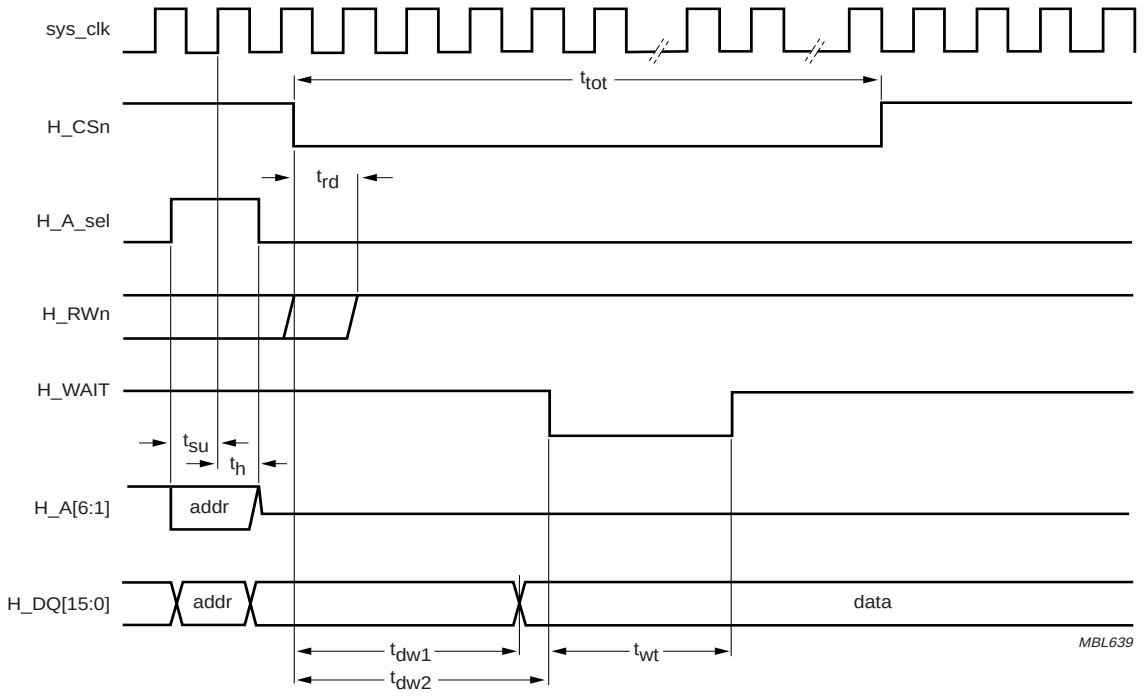



**Fig 23. Timing diagram writing to the SAA7893HL (with wait cycles).**

**Table 17: Timing numbers of writing registers (with wait cycles)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total H_CSn time | | 8 | - | sys_clk |
| $t_{su}$ | set-up time H_A_sel | | 5 | - | ns |
| $t_h$ | hold time of H_A_sel with respect to sys_clk | | 5 | - | ns |
| $t_{rd}$ | time H_RWn can change from H_CSn signal | | - | 1 | sys_clk |
| $t_{dw1}$ | data set-up time after H_CSn | time dependent on system clock used | 1 | 3 | sys_clk |
| $t_{dw2}$ | time H_WAIT is activated after H_CSn is activated | dependent on SAA7893HL settings | 2 | 6 | sys_clk |
| $t_{wt}$ | total time wait can be active | | 2 | 24 | sys_clk |

### 8.4.4 Read mode: cycles extended using wait protocol

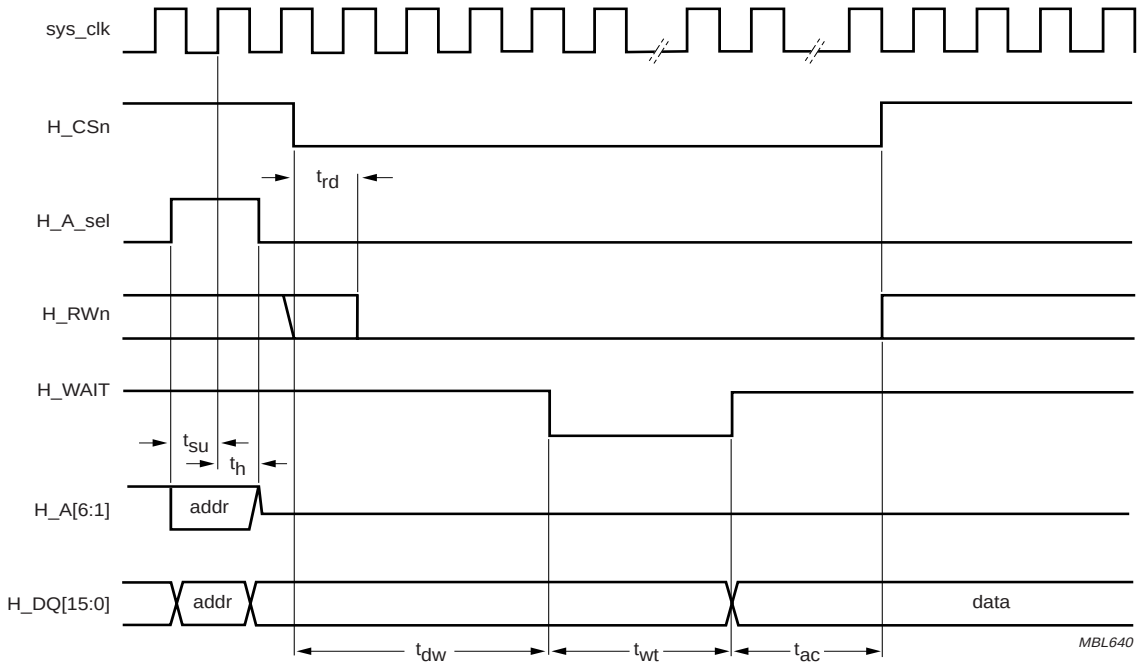



**Fig 24. Timing diagram reading from the SAA7893HL (with wait cycles).**

**Table 18: Timing numbers of reading registers (with wait cycles)**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total H_CSn time | | 8 | - | sys_clk |
| $t_{su}$ | set-up time H_A_sel | | 5 | - | ns |
| $t_h$ | hold time of H_A_sel with respect to sys_clk | | 5 | - | ns |
| $t_{rd}$ | time H_RWn can change from H_CSn signal | | - | 1 | sys_clk |
| $t_{dw}$ | time H_WAIT is activated after H_CSn is activated | dependent on SAA7893HL settings | 2 | 5 | sys_clk |
| $t_{wt}$ | total time wait can be active | | 2 | 24 | sys_clk |
| $t_{ac}$ | data active until H_CSn is deactivated | | 1 | - | sys_clk |

### 8.4.5 Host interface connection

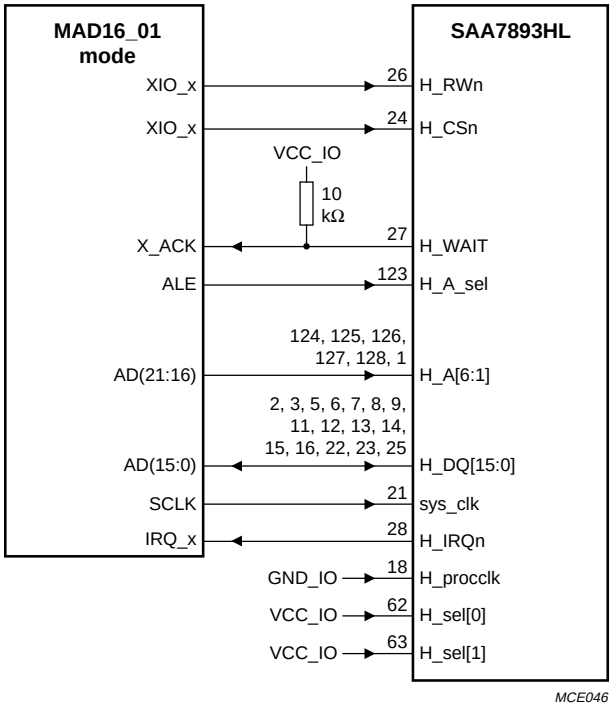



**Fig 25. Host interface connection.**

## 8.5 MAD16_02 mode

In the MAD16_02 mode there is a 16-bit combined address/data bus and a dedicated 3-bit address bus.

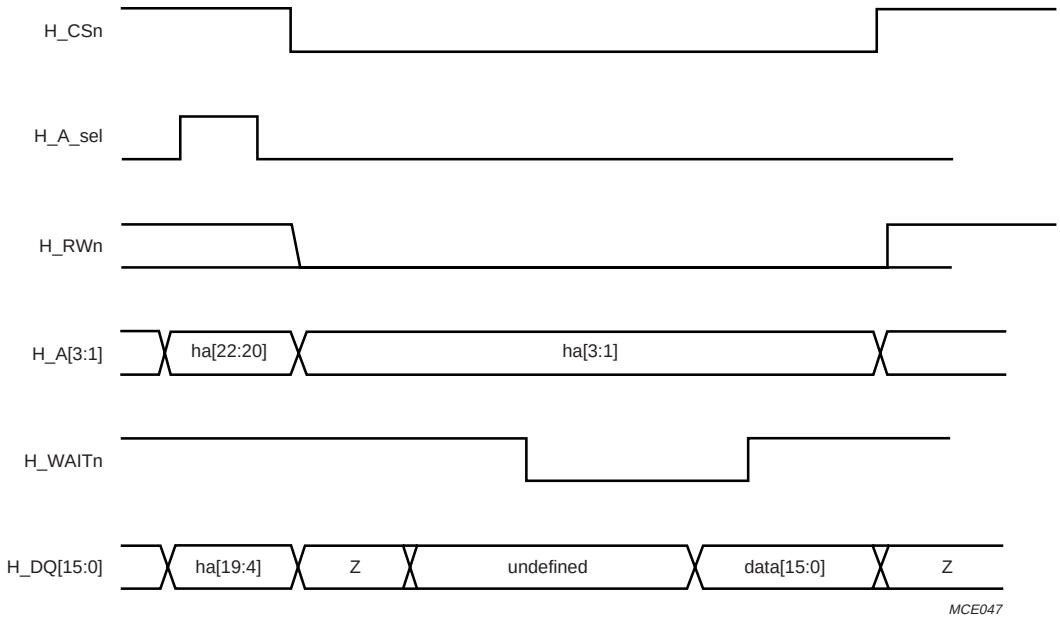



**Fig 26. Principle read.**

The multiplexing of the address/data pins is done as a regular host communication, meaning that during a read or write the host must automatically generate the timing according to Figure 26. It is not needed that the provided system clock is a synchronous clock with respect to the H_A_sel line.

### 8.5.1 Write mode

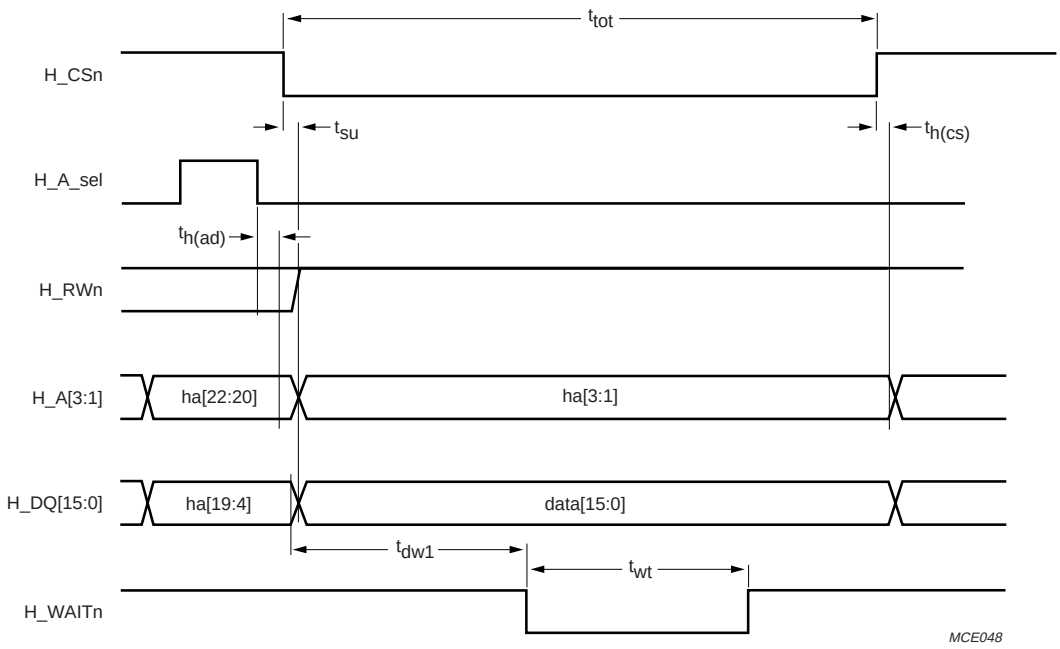



**Fig 27. Timing diagram writing to the SAA7893HL.**

**Table 19: Timing numbers of MAD16_02 write**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{tot}$ | total LOW time of H_CSn | 300 + $t_{wt}$ | - | ns |
| $t_h$ | hold time of address/data with respect to H_A_sel | 10 | - | ns |
| $t_{dw1}$ | wait time until H_WAIT is activated | 2 | 5 | sys_clk |
| $t_{wt}$ | time of H_WAIT signal | 2 | 24 | sys_clk |
| $t_{su}$ | set-up time of H_RWn/address with respect to H_CSn | - | 10 | ns |

### 8.5.2 Read mode

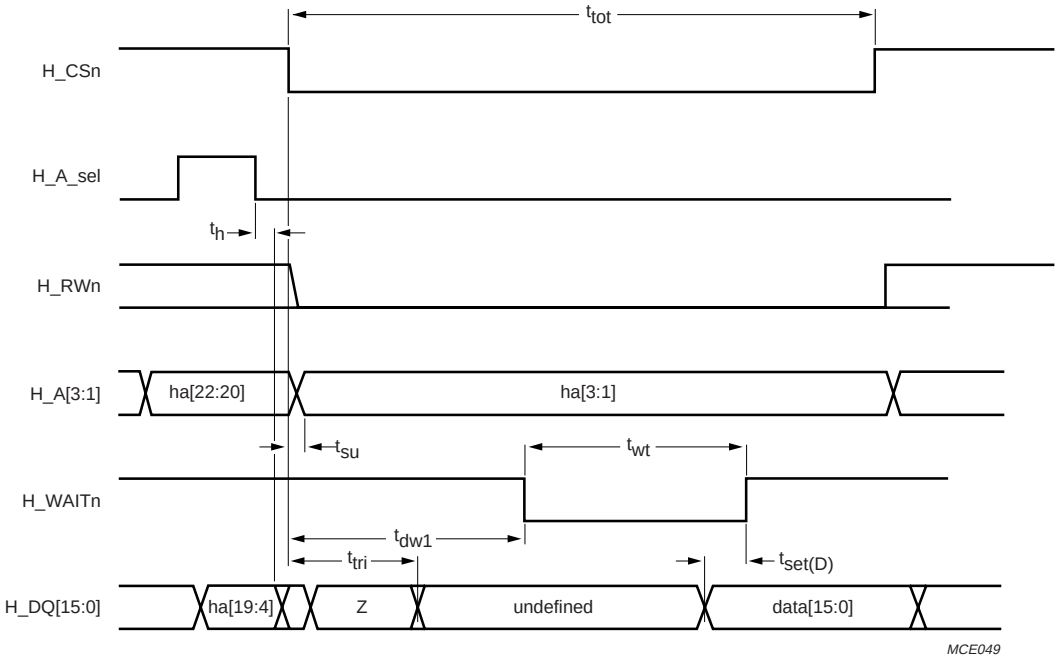



**Fig 28. Timing diagram reading from the SAA7893HL.**

**Table 20: Timing numbers of MAD16_02 read**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{tot}$ | total H_CSn time | 8 + $t_{wt}$ | - | - | ns |
| $t_{su}$ | set-up time of address/data/H_RWn with respect to H_CSn | - | - | 0 | ns |
| $t_h$ | hold time of address with respect to H_A_sel falling edge | 10 | - | - | ns |
| $t_{dw1}$ | time H_WAIT is activated after H_CSn is activated | - | - | 4 | sys_clk |

Table 20: Timing numbers of MAD16_02 read...*continued*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{tri}$ | time data bus becomes active after H_CSn | - | 2 | - | sys_clk |
| $t_{set(D)}$ | time data available with respect to H_WAIT signal | 15 | - | - | ns |
| $t_{wt}$ | time H_WAIT can be active | 2 | - | 24 | sys_clk |

### 8.5.3 Host interface connection

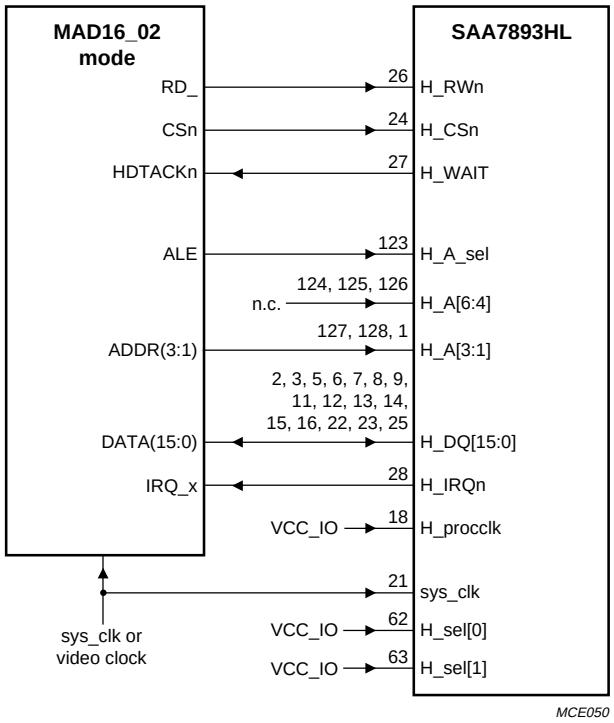



Fig 29. Host interface connection.

## 8.6 SAD08 mode

Here the reading and writing is always done on 8-bit. From pin mapping it can be seen that the byte indication is done via bit A(0) which is mapped on H_DQ(15) of the SAA7893HL. The internal SAA7893HL communication stays on 16-bit. Therefore, the host interface block 'translates' the 8 bits external communication to the 16 bits internal. To save physical pins on the SAA7893HL device, the data bus and 4 address bits are used to write the 12 MSB address bits, hereafter called 'the base address', into the SAA7893HL device. Therefore, to access an address inside the SAA7893HL first this 12 MSB bits of the address must be written as a base address for the SAA7893HL indicated by the H_A_sel line. Pin H_A_sel can be mapped to a physical address pin of the host.

### 8.6.1 Writing base address

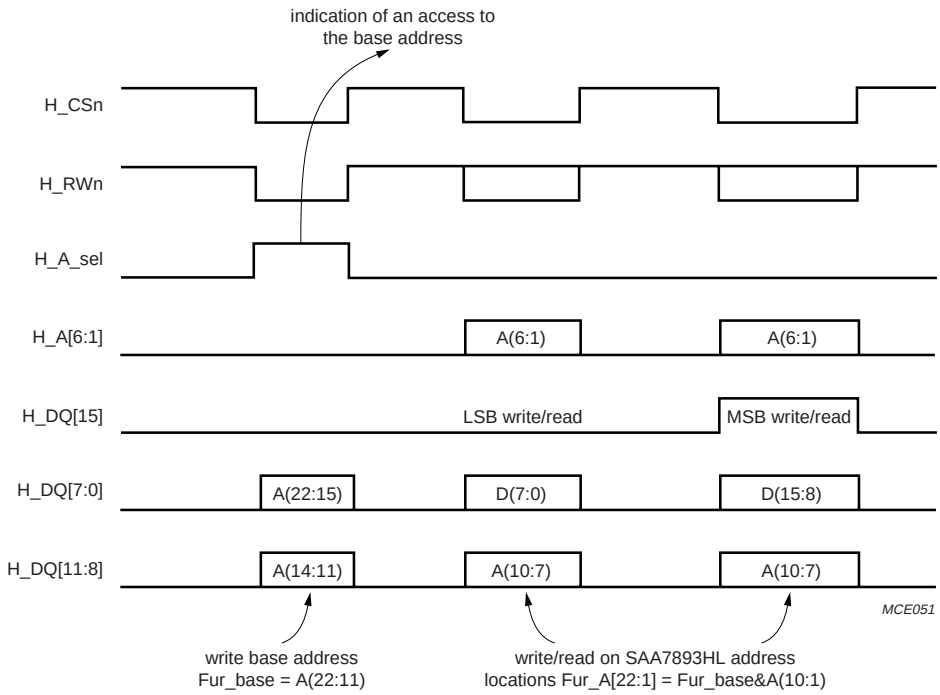



**Fig 30. Base address writing.**

In Figure 30 the writing of the base address and a Hword to the host is given in SAD08 mode. First, the 12 bits base address is written indicated by H_A_sel line. The SAA7893HL samples the base address on H_DQ(7:0) and H_DQ(11:8). After that the normal write operation is performed as explained in Section 8.6.2.

### 8.6.2 Writing to the SAA7893HL

A write to address N of 16 bits to the SAA7893HL will be translated to two byte accesses. First the LSB byte is written to address N [so A(0) = logic 0] and stored in cache. Then the MSB byte is written to address N+1 [so A(0) = logic 1]. When the SAA7893HL receives a write command at an odd address [A(0) = logic 1] always 16 bits are internally written whereby the Hword is composed of LSB byte in cache and the MSB byte received at present write command. The SAA7893HL can be set to big and little endian, whereby the described situation is the power-on state. Byte read or write operations are not supported in SAD08 mode.

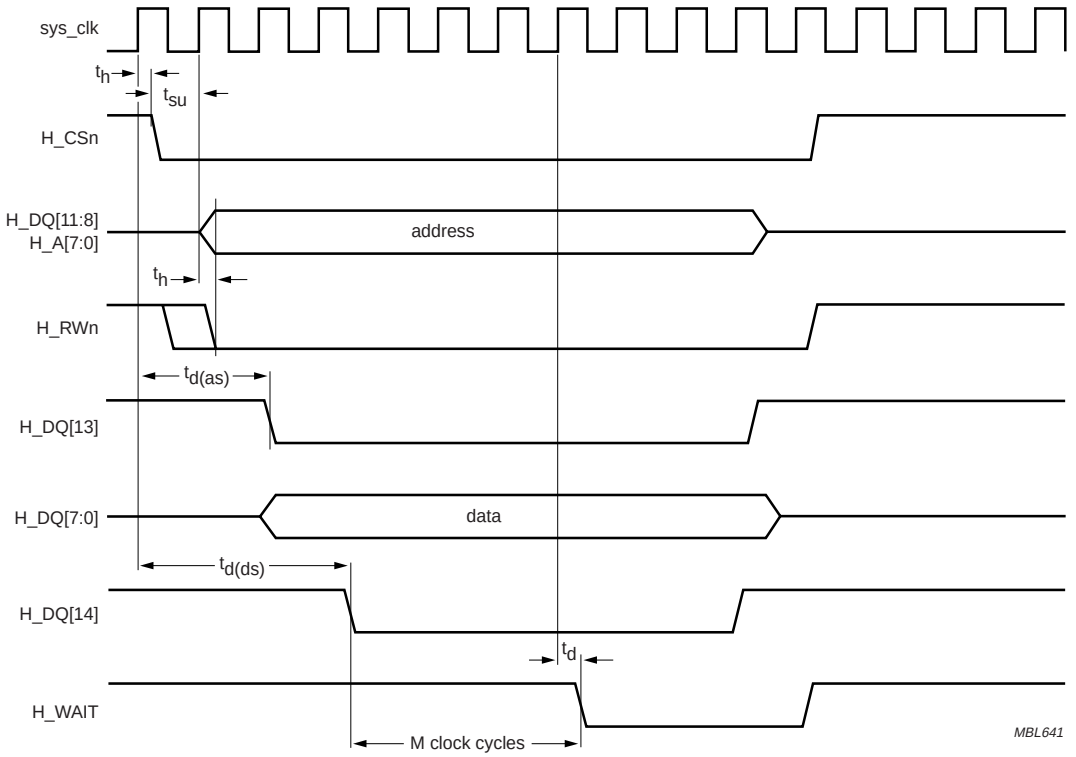



**Fig 31. Timing diagram SAD08 write to SAA7893HL.**

**Table 21: Timing numbers of SAD08 write**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{su}$ | set-up time from H_CSn, H_RWn and H_DQ(13) to sys_clk | | 5 | - | ns |
| $t_h$ | hold time from clk to H_CSn, H_RWn and H_DQ(13) | | 5 | - | ns |
| $t_{d(as)}$ | delay from H_CSn to negative slope of H_DQ(13) | | - | 1 | sys_clk |
| $t_{d(ds)}$ | delay from H_CSn to negative slope of H_DQ(14) and data | | - | 2 | sys_clk |
| M | number of clock cycles | dependent on access type and traffic on PI-bus | 4 | 15 | sys_clk |
| $t_d$ | delay from clk to DSACKn | | 2 | 12 | ns |

### 8.6.3 Reading from the SAA7893HL

When the LSB is read [A(0) = logic 0], the host interface will read an Hword on the address location A(22:1). The LSB byte is set on the output bus and the read MSB byte is stored internally. When a read action is now started whereby the MSB byte is selected to read [A(0) = logic 1] the stored byte is available on the output independent on the other address bits A(22:1).

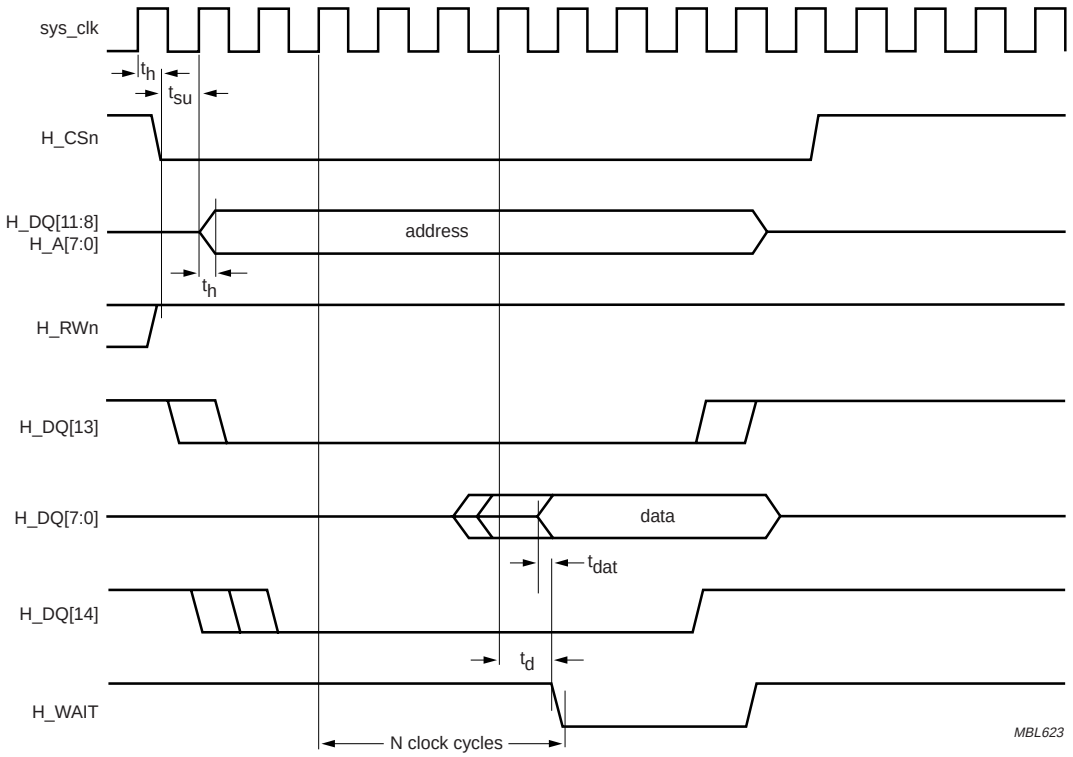



**Fig 32. Timing diagram SAD08 read from the SAA7893HL.**

**Table 22: Timing numbers of SAD08 read**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{su}$ | set-up time from H_CSn, H_RWn and H_DQ[13] to sys_clk | | 5 | | ns |
| $t_h$ | hold time from clk to H_CSn, H_RWn and H_DQ[13] | | 5 | | ns |
| N | number of clock cycles | dependent on access type and traffic on PI-bus. | 5 | 20 | sys_clk |
| $t_d$ | delay from clk to H_WAIT | | 2 | 12 | ns |
| $t_{dat}$ | data available before H_WAIT is asserted | | - | 0 | ns |

### 8.6.4 Host interface connection

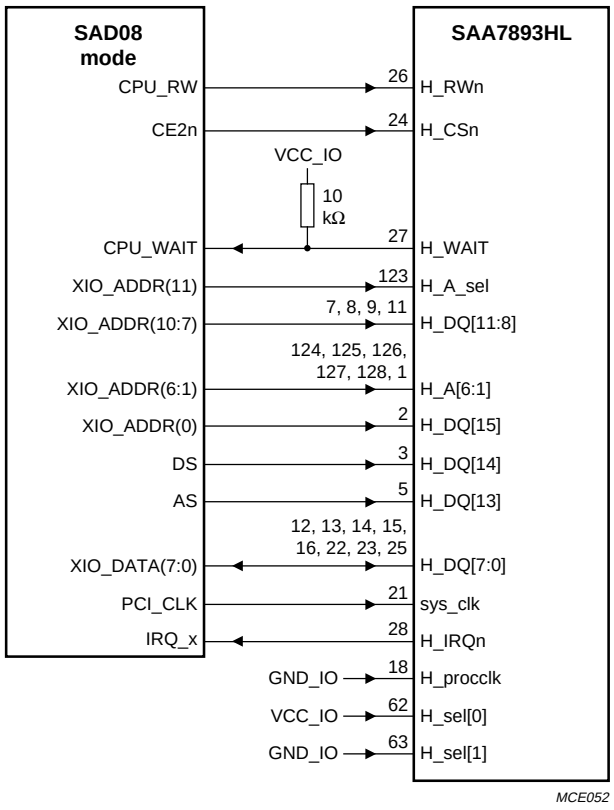



**Fig 33. Host interface connection.**

## 8.7 Interrupt

The interrupt output is a LOW level interrupt which must be connected to the interrupt input of the DVD host.

# 9. Front-end interface

First the SACD sector structure is explained and how to connect the SAA7893HL in the different modes. For these different modes the interface timing figures will be given.

The supported sector format interface is sketched in Figure 34.

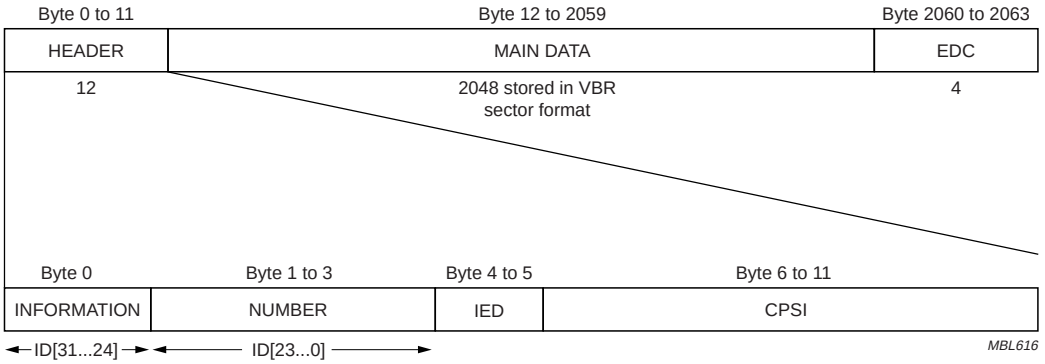



**Fig 34. SACD sector format.**

The SAA7893HL supports a data input bit rate of maximal 40 Mbits/s.

The connections to the SAA7893HL in the different front-end modes are given in Table 23.

**Table 23: Connection of different front-end interfaces**

| SAA7893HL name | Type | I2S_mode | FEC | Parallel mode |
|---|---|---|---|---|
| B_FLAG | IN | I2S_err | n.c.[1] | SERR |
| B_SYNC | IN | I2S_sync | OUT_SYNC | SYNC |
| B_WCLK | IN | I2S_wclk | OUT_DVALID | SENB |
| B_BCLK | IN | I2S_bclk | OUT_CLK | SDCLK |
| B_DATA | IN | I2S_data | OUT_DATA0 | MPEG(0) |
| Be_dat(7:1) | IN | n.c.[1] | n.c.[1] | MPEG(7:1) |
| UDE_req | IN | n.c.[1] | n.c.[1] | UDE_req |
| Data_req | O | n.c. | n.c. | REQ |

[1] The n.c. input pins must be connected to $V_{CC}$ or GND.

## 9.1 I²S-bus interface

### 9.1.1 Input timing

In Figure 35 the functional input timing is given. Note that B_SYNC, B_FLAG are sampled simultaneously with D11. Since B_FLAG indicates the error in a byte, it is also sampled simultaneously with D3. The sampling moment during D11 for the high byte (D15 to D8), sampling moment D3 for the low byte (D7 to D0).

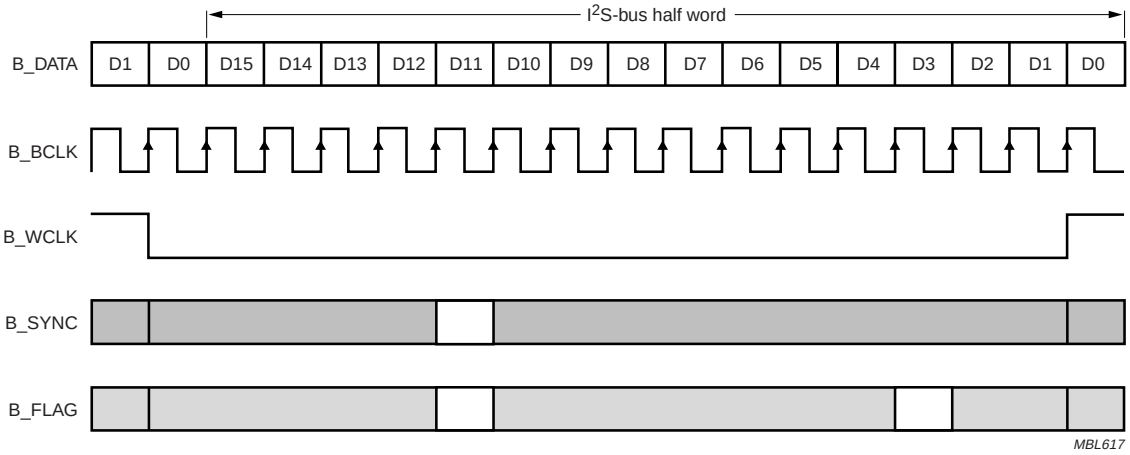



**Fig 35. Front-end input timing.**

When the B_SYNC signal is set to logic 1 between bit position D15 and D11 the SAA7893HL accepts this word as the start of a sector. The SAA7893HL does not perform EDC checking on the main data, but is dependent on the B_FLAG. A sector is set to erroneous if B_FLAG is set to logic 1.

### 9.1.2 Interface timing

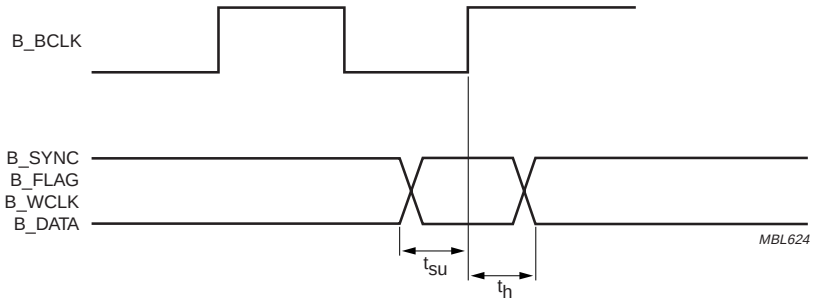
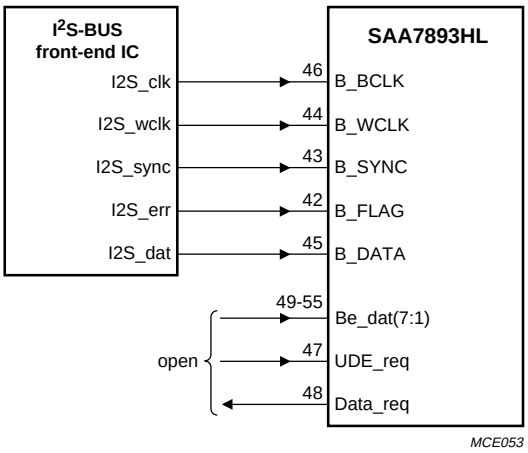



**Fig 36. Timing in I²S-bus interface.**

**Table 24: Timing in I²S-bus interface**

| Symbol | Parameter | Min | Unit |
|---|---|---|---|
| $t_{su}$ | set-up time to rising edge of the clock | 5 | ns |
| $t_h$ | hold time after rising edge of the clock | 5 | ns |

### 9.1.3 Interface connection




Not used input pins must be connected to $V_{CC}$ or GND.

**Fig 37. Front-end interface connection.**

## 9.2 UDE data interface

In the SA-MP the synchronous parallel mode is supported. There are three types of parallel data transfer modes supported:

- Synchronous mode (see Section 9.2.1)
- Asynchronous mode:
  - Handshake to enable data transfer
  - Handshake for every byte transfer.

### 9.2.1 Parallel mode

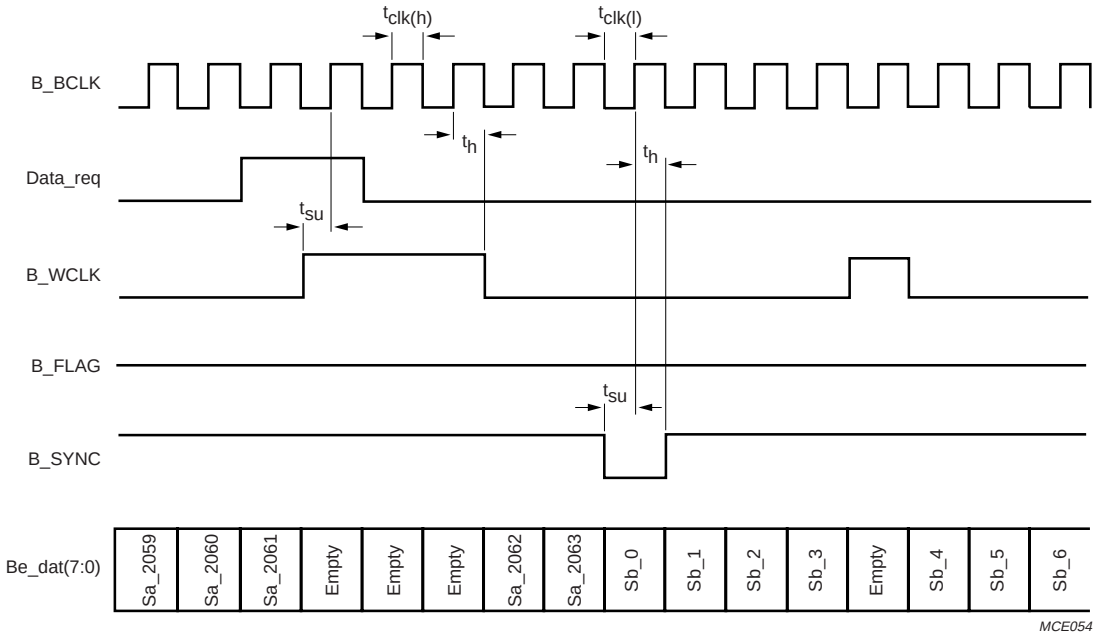



**Fig 38. Timing diagram for UDE interface with level sync mode.**

Polarity of Data_req, B_WCLK, B_FLAG and B_SYNC is programmable.

The UDE transmitter must react on the Data_req signal within 5 B_BCLK cycles. The SAA7893HL samples the data on the positive slope of B_BCLK when the B_WCLK signal is active.

When B_FLAG signal is active for one byte of the sector, the total sector will be treated as erroneous.

The maximum clock frequency of B_BCLK is 20 MHz.

The Data_req line generated by the SAA7893HL is synchronized to the internal sys_clk signal. Therefore, the Data_req line is asynchronous with respect to BCLK line.

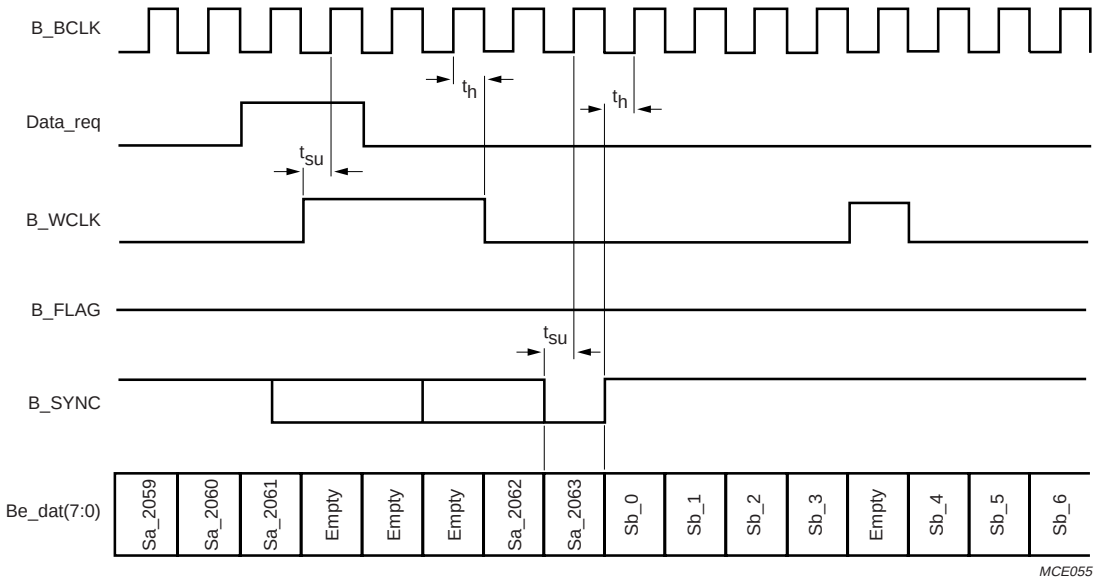



**Fig 39. Timing diagram for UDE interface with sync edged triggered mode.**

Polarity of Data_req, B_WCLK, B_FLAG and B_SYNC is programmable.

**Table 25: Timing in synchronous parallel mode**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{clk(h)(l)}$ | HIGH/LOW time of the B_BCLK signal | maximum clock frequency of B_BCLK is 20 MHz | 20 | - | ns |
| $t_{su}$ | set-up time to rising edge of the clock | data/control must be stable during $t_{su}$ before positive slope of B_BCLK | 10 | - | ns |
| $t_h$ | hold time after rising edge of the clock | data/control must be kept at least during $t_h$ after positive slope of B_BCLK | 5 | - | ns |
| $t_o$ | output delay from the clock | | 2 | 15 | ns |

### 9.2.2 Interface connection

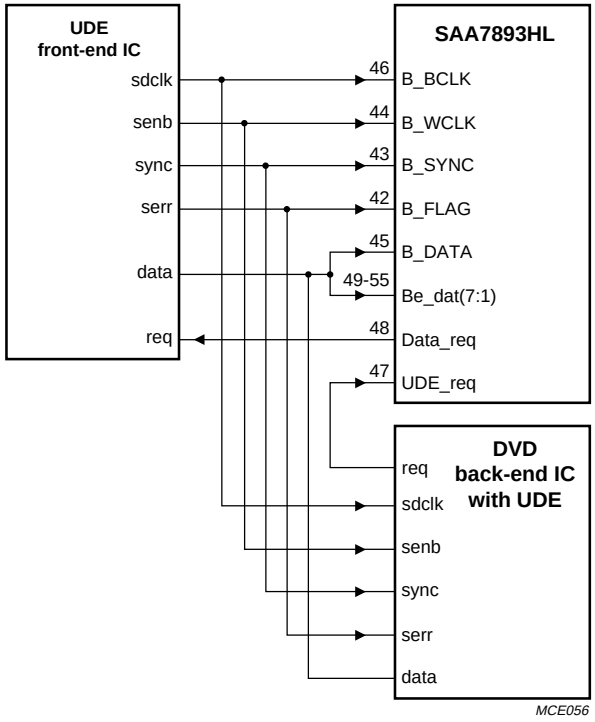



**Fig 40. Front-end interface connection.**

## 9.3 FEC interface

This is a serial interface for communication to a special front-end IC.

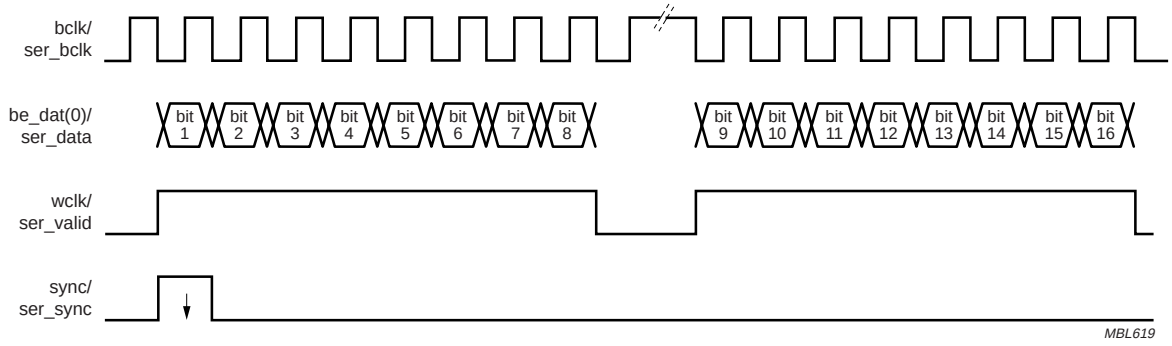



**Fig 41. FEC interface.**

The timing diagram of the FEC interface is given in Figure 41. The first bit of a sector is indicated by the sync signal; this is the MSB bit of the first byte of the header. The sector error indication is in FEC mode indicated by two extra bytes at the end of the sector. This means that the sector length is increased to 2066 bytes. The indication of errors is as follows:

FF = error; 00 = no error.

### 9.3.1 Timing

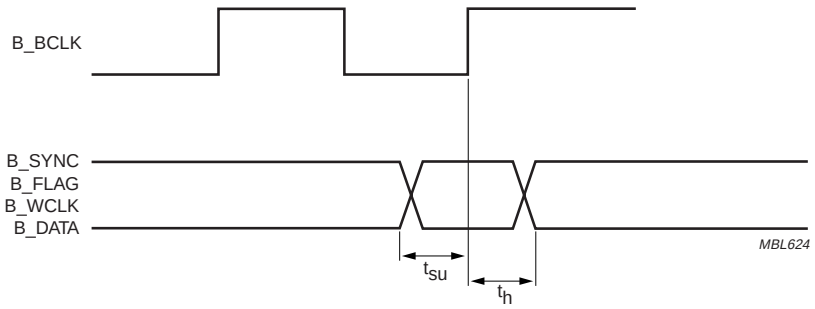



Fig 42. Timing in FEC interface.

Table 26: Timing in FEC interface

| Symbol | Parameter | Min | Unit |
|---|---|---|---|
| $t_{su}$ | set-up time to rising edge of the clock | 10 | ns |
| $t_h$ | hold time after rising edge of the clock | 5 | ns |

### 9.3.2 Interface connection

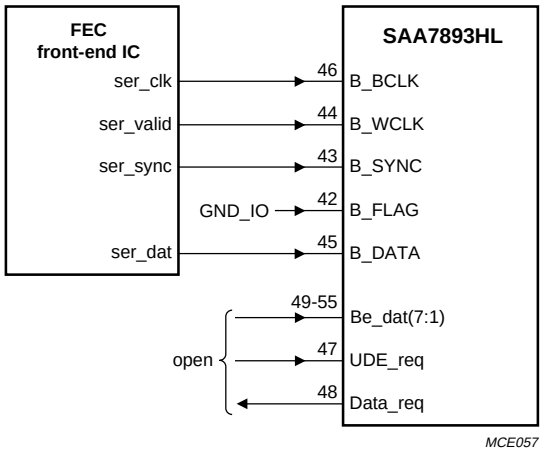



Fig 43. Front-end interface connection.

## 10. HF input

### 10.1 General

On every SACD disc a PSP signal must be recorded. The player is only allowed to play a disc if a valid PSP signal is detected. This PSP key is recorded via a special mechanism in the EFM signal on disc. The EFM+ signal must be fed to the SAA7893HL as shown in Figure 44.

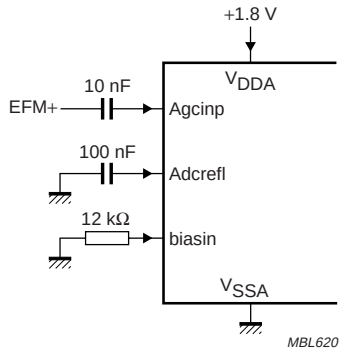



**Fig 44. Connection of EFM+ input.**

The detection of the PSP key is dependent of the polarity of the EFM+ signal. The SA-MP settings are that a pit on the disc must have a higher output voltage than the land. The EFM+ input signal has no timing requirements with respect to the digital input of the front-end interface of the SAA7893HL.

The SAA7893HL supports also an inversion of the EFM+ signal.

## 10.2 HF input specification

The AGC circuit must be able to handle the following signal characteristics of the HF input signal.

**Table 27: HF signal characteristics**

| HF | Value | Remark |
|---|---|---|
| Input range | 0.2 to 0.8 V (p-p) | HF input voltage |
| Bandwidth | 9 MHz | front-end running on maximum speed needed for SACD |

The HF is AC-coupled via a capacitor of 10 nF to pin Agcinp. The internal resistance of pin Agcinp is 1 MΩ.

**Table 28: Signal connections**

| Pin name | Description |
|---|---|
| Agcinp | HF output from pickup unit connected via a 10 nF couple capacitor |
| biasin | bias current; connect a 12 kΩ resistor to $V_{SS}$ (ground) |
| Adcrefl | reference voltage for internal resistor trap; decouple with 100 nF to $V_{SS}$ (ground) |
| $V_{SSA}$ | analog ground |
| $V_{DDA}$ | 1.8 V analog power supply |

### 10.3 HF-input application diagram

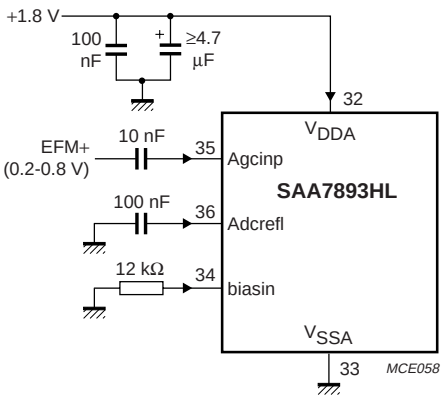



**Fig 45. EFM input interface connection.**

## 11. Audio interfaces

### 11.1 Audio input interface

The PCM-I²S audio input signals can be either directly couple, without any processing to the DSD_PCM output lines, or further processed inside the SAA7893HL. When directly coupled, only a combinatorial delay must be taken into account; no dependency on any clock signal (see Section 11.1.1). The input signal characteristics, when audio processing must be performed, are given in Section 11.1.2.

#### 11.1.1 Audio input directly coupled

When no processing is done inside the SAA7893HL with respect to the I²S-PCM input stream, this input stream is sent via a multiplexer to the I²S-bus output paths. So no clocking is done on this signal, meaning that also no locked audio clock needs to be present.

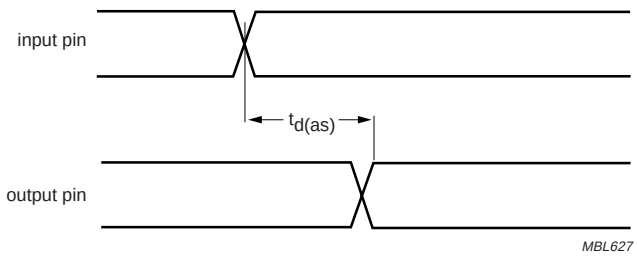



**Fig 46. Delay from input to output pin.**

**Table 29: Timing numbers in PCM audio**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{d(as)}$ | asynchronous delay | 8 | 13 | 18 | ns |

### 11.1.2 Audio input ‘with processing’

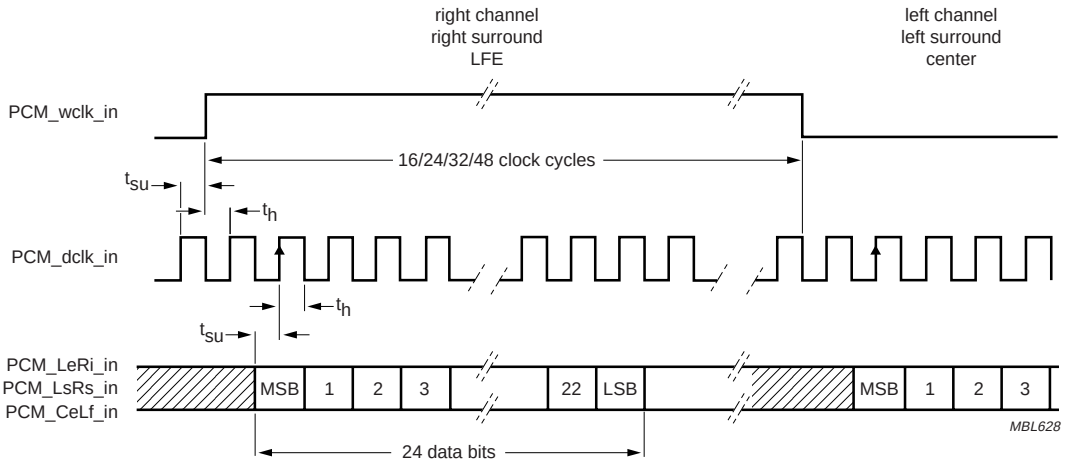



**Fig 47. Audio I²S-bus input timing.**

**Table 30: Timing numbers in PCM audio**

| Symbol | Parameter | Conditions | Min | Unit |
|---|---|---|---|---|
| $t_{su}$ | set-up time to rising edge to the pcm_dclk_in signal | in PCM-I²S mode, the data is always outputted on the negative edge of the bit clock; so here data is sampled on positive edge of the clock | 8 | ns |
| $t_h$ | hold time after rising edge of the pcm_dclk_in signal | in PCM-I²S mode, the data is always outputted on the negative edge of the bit clock; so here data is sampled on positive edge of the clock | 5 | ns |

### 11.1.3 Interface connection

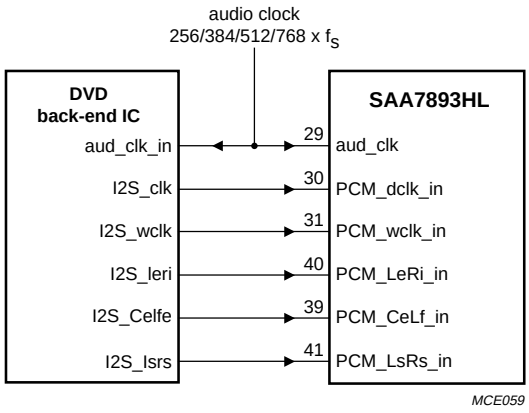



**Fig 48. Audio I²S-PCM input interface connection.**

## 11.2 Audio output interface

The 6-channel outputs can be either DSD format or PCM-I²S format. The connections are given in Table 31.

The SAA7893HL has 12 output lines: 8 lines are allocated for connection to a 6-channel DAC and 4 are for connection to a 2-channel DAC or a 75 Hz reference signal. The DSD data on the MCH output lines are outputted 6412 clocks after the positive edge of the 75 Hz signal, if no additional post-processing is done.

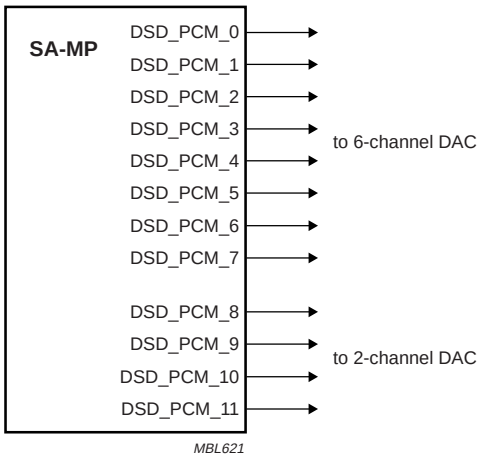



**Fig 49. SA-MP output line allocation.**

The SA-MP delivers extra flexibility when connecting to different DAC types, which can be: DSD only, PCM only or multi standard (DSD + PCM)]. In Table 31 the signal allocation is given for the 6-channel output in DSD and in PCM-I$^2$S mode.

**Table 31: Connection to a 6-channel DAC**

| Output line | Pin number | Mode = DSD | Mode = PCM |
|---|---|---|---|
| DSD_PCM_0 | 108 | left channel | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_1 | 109 | right channel | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_2 | 110 | center channel | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_3 | 111 | LFE channel | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_4 | 113 | left surround | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_5 | 114 | right surround | $L_f + R_f$; $L_s + R_s$; C + LFE; 0 or 1; PCM data/word clock |
| DSD_PCM_6 | 115 | DSD clock or 0 or 1 | PCM data/word clock |
| DSD_PCM_7 | 116 | DSD clock or 0 or 1 | PCM data/word clock |

In Table 32 the signal allocation is given for the DSD/PCM signals to be connected to the stereo DAC.

**Table 32: Connection to a 4-channel DAC**

| Output line | Pin number | Mode = DSD | Mode = PCM | Mode = 75 Hz |
|---|---|---|---|---|
| DSD_PCM_8 | 117 | DSD clock | PCM data/word clock | 0 or 1 |
| DSD_PCM_9 | 120 | 0 or 1 | PCM data/word clock | 0 or 1 |
| DSD_PCM_10 | 119 | left channel | $L_f + R_f$; 0 or 1 | 75 Hz |
| DSD_PCM_11 | 121 | right channel | $L_f + R_f$; 0 or 1 | 0 or 1 |

Both tables show that DSD has a fixed allocation while PCM outputs are selectable. The I²S-bus bit stream, generated by the SAA7893HL decimation filter, is in the Philips format as can be seen in the timing diagrams. The number of data bits is always 24.

**Table 33: Serial bit clock frequency**

| Audio input clock | I²S output 'wclk' frequency | DCLK (data bit) frequency | Remark |
|---|---|---|---|
| $256f_s$ | $2f_s$ | $128f_s$ | |
| | $4f_s$ | $256f_s$ | |
| $384f_s$ | $2f_s$ | $128f_s$ | no symmetrical bit clock |
| | $4f_s$ | $384f_s$ | 48 clocks for a word identification |
| $512f_s$ | $2f_s$ | $128f_s$ | |
| | $4f_s$ | $256f_s$ | |
| $768f_s$ | $2f_s$ | $128f_s$ | |
| | $4f_s$ | $256f_s$ | |

The wclk identification is always active for 32 clocks for each left and right sample, except when the input clock is $384f_s$ and the output sample frequency is $4f_s$; then the wclk is 48 samples active.

### 11.2.1 DSD output

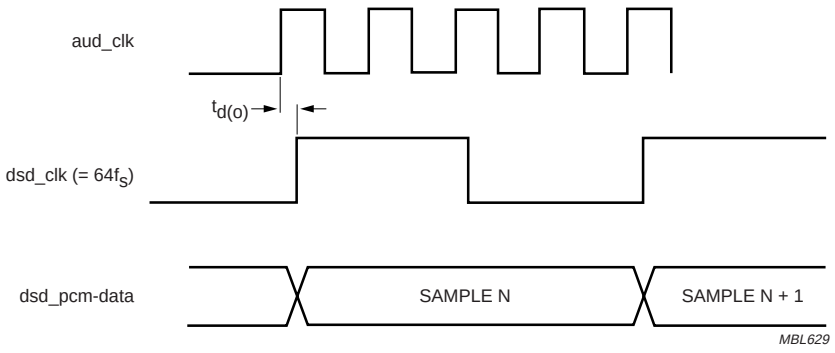



**Fig 50. Audio I²S-bus output timing.**

**Remark:** in this example timing of the aud_clk is $256 \times f_s$ and DSD clock phase is set to logic 0. If phase is set to logic 1, the dsd_clk signal will be inverted.

**Table 34: Timing numbers in DSD audio**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{d(o)}$ | output delay time with respect to the audio clock | 4 | 20 | ns |

### 11.2.2 I²S-PCM generated by the SAA7893HL

In Figure 51 and Figure 52 the timing diagrams are given when the internal PCM generator of the SAA7893HL generates the I²S-PCM output signals.

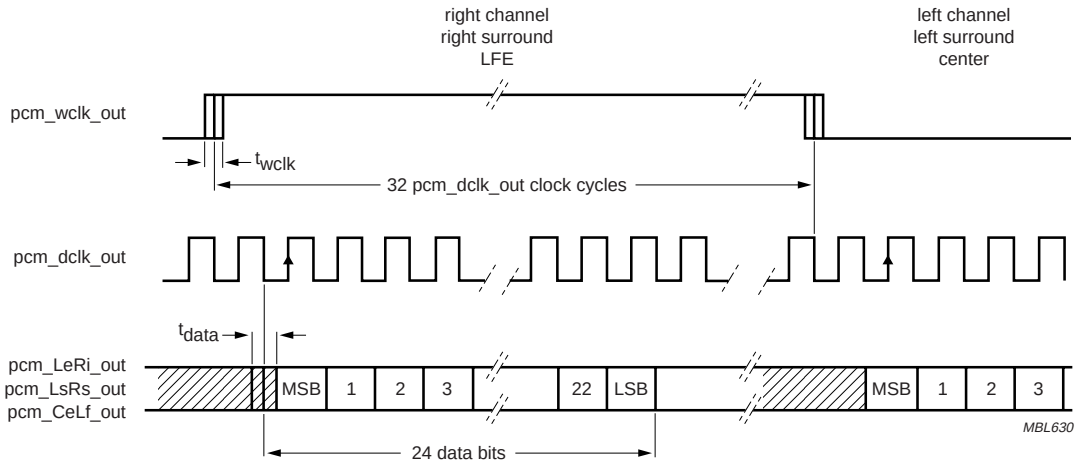



**Fig 51. Audio I²S-bus output timing in Philips format.**

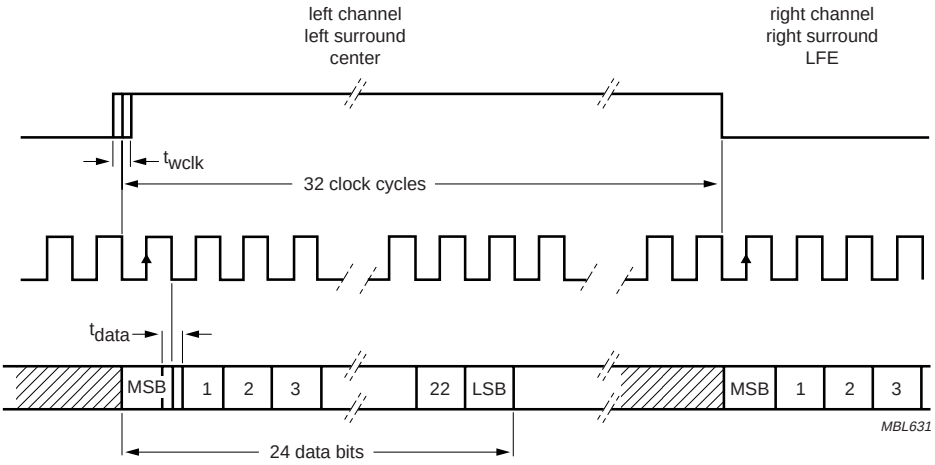



**Fig 52. Audio I²S-bus output timing in left justified format.**

**Table 35: Timing numbers for PCM-I²S output**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{wclk}$ | pcm_wclk_out timing with respect to negative edge of pcm_dclk_out | –10 | +10 | ns |
| $t_{data}$ | pcm_data_out timing with respect to negative edge of pcm_dclk_out | –10 | +10 | ns |

## 11.3 Audio output application diagrams

### 11.3.1 Hybrid DAC connection

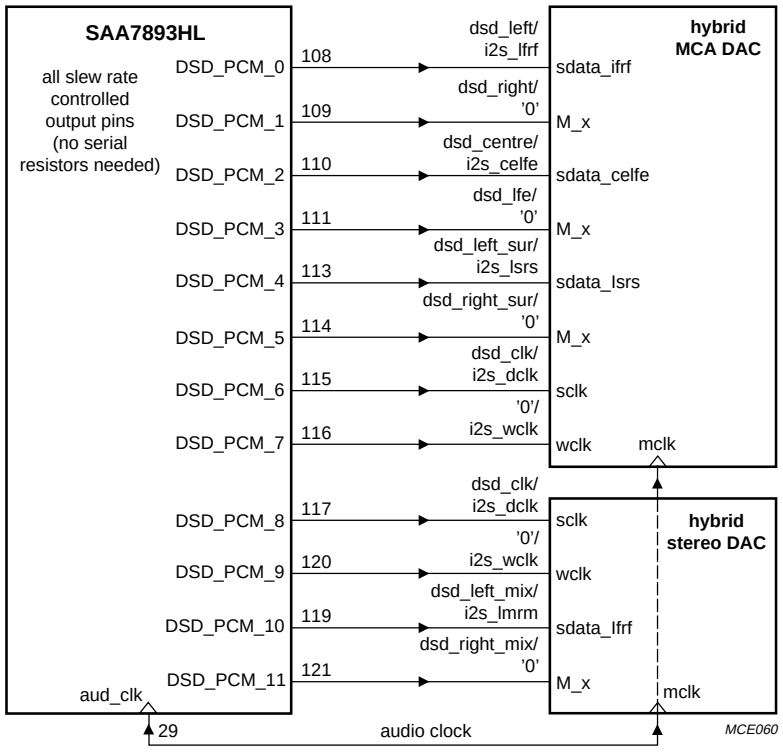



**Fig 53. Hybrid DAC interface connection.**

### 11.3.2 DSD DAC connection

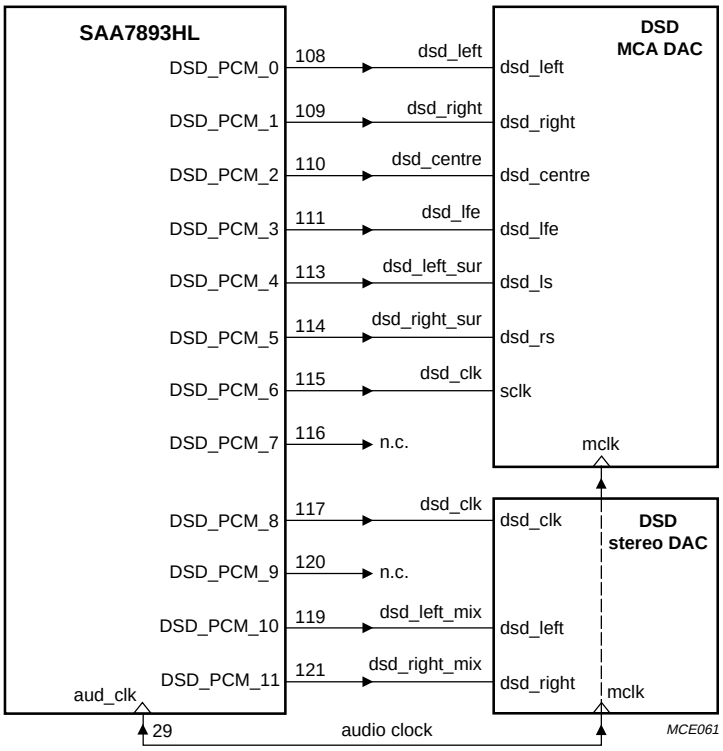



**Fig 54. DSD DAC interface connection.**

### 11.3.3 PCM DAC connection

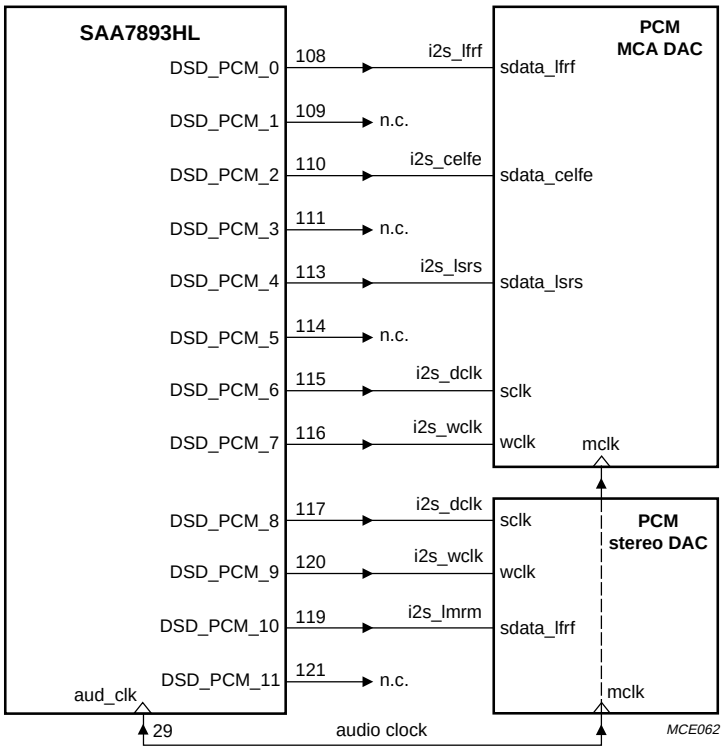



**Fig 55. PCM DAC interface connection.**

# 12. SDRAM interface

## 12.1 Writing

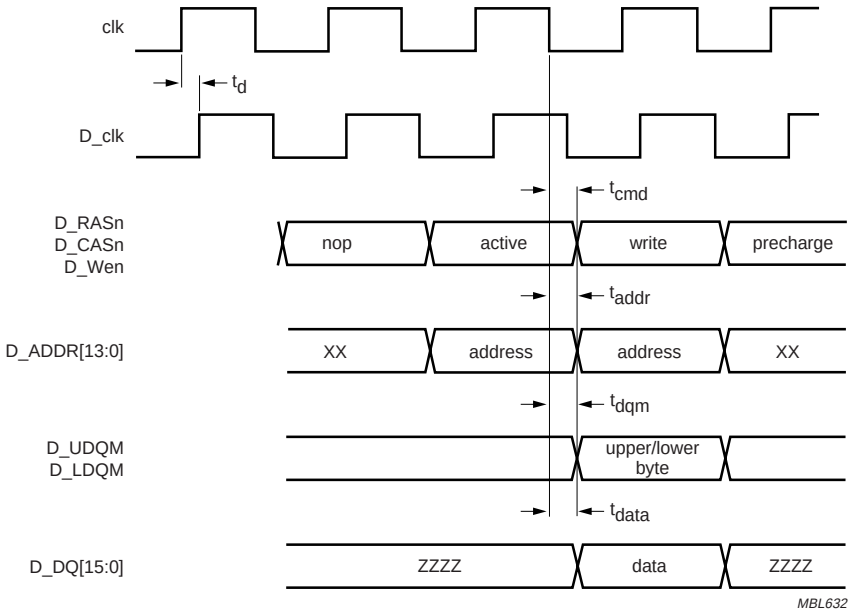



**Fig 56. SDRAM interface writing.**

**Table 36: Timing numbers of SDRAM interface writing**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_d$ | delay from clk to D_clk of SDRAM interface | D_clk is clock of SDRAM | 3 | 9 | ns |
| $t_{cmd}$ | delay from clk to control signals | | 1 | 15 | ns |
| $t_{addr}$ | delay from clk to address lines | | 1 | 15 | ns |
| $t_{dqm}$ | delay from clk to D_UDQM and D_LDQM signals | | 1 | 12 | ns |
| $t_{data}$ | delay from clk to data output signals | | 1 | 12 | ns |

## 12.2 Reading

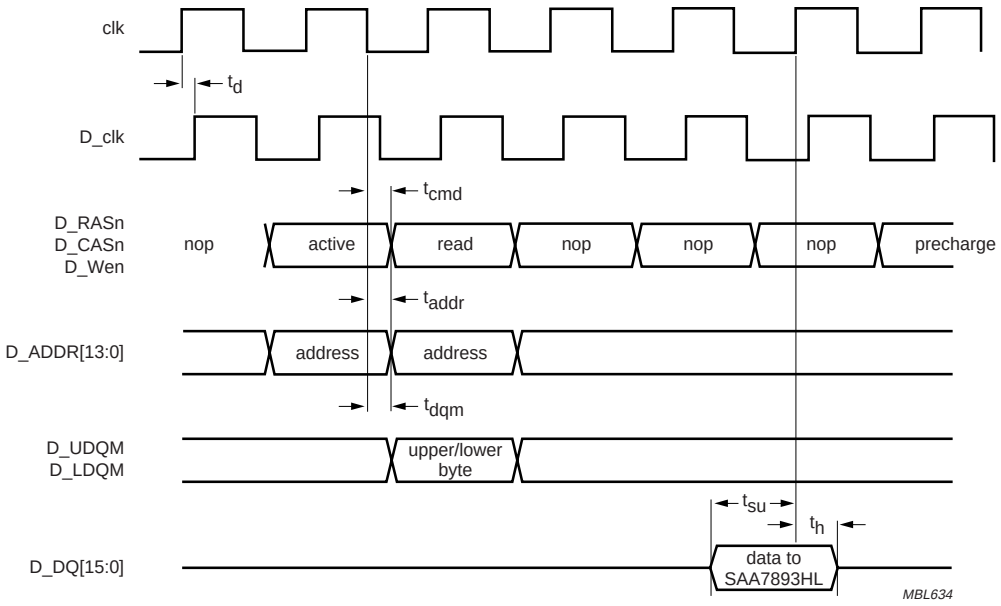



**Fig 57. SDRAM interface reading.**

**Table 37: Timing numbers of SDRAM interface reading**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_d$ | delay from clk to D_clk of SDRAM interface | D_clk is clock of SDRAM | 3 | 9 | ns |
| $t_{cmd}$ | delay from clk to control signals | | 1 | 15 | ns |
| $t_{addr}$ | delay from clk to address lines | | 1 | 15 | ns |
| $t_{dqm}$ | delay from clk to D_UDQM and D_LDQM signals | | 1 | 12 | ns |
| $t_{su}$ | set-up time of data to clk | | 3 | - | ns |
| $t_h$ | hold time of data from clk | | 3 | - | ns |

## 12.3 Interface connection

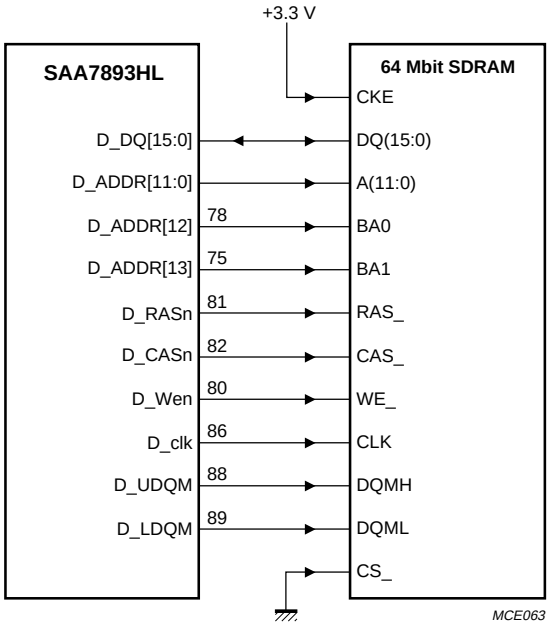



**Fig 58. SDRAM interface connection.**

## 13. Power supply connections

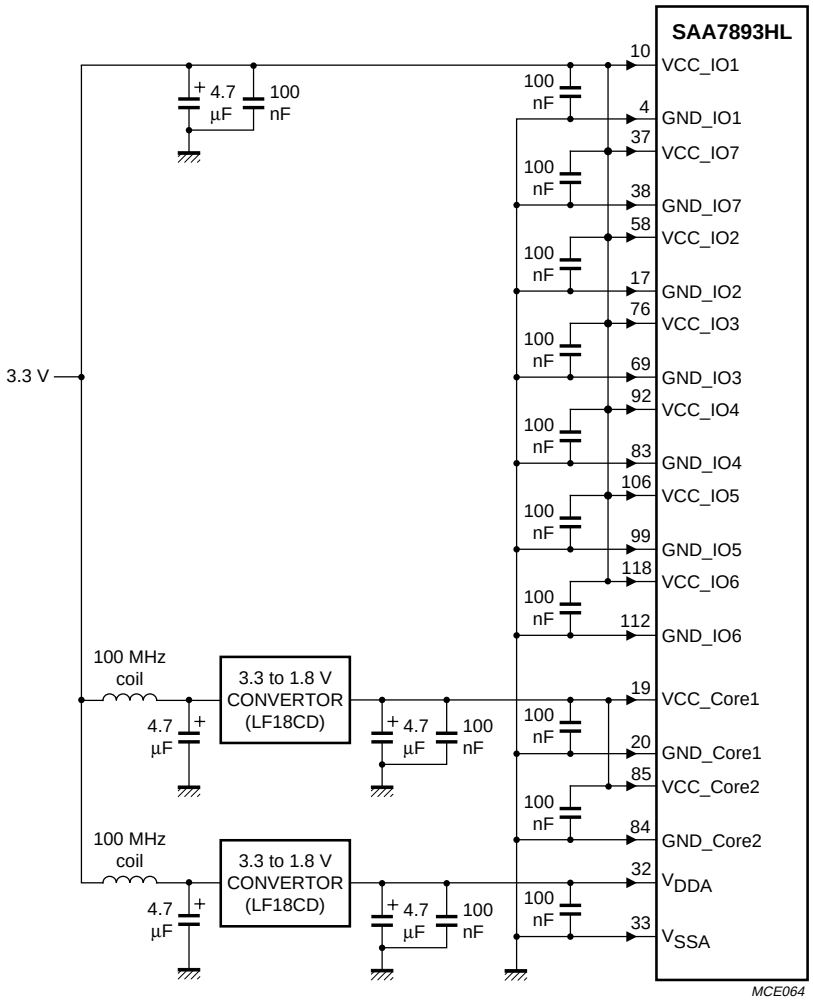



**Fig 59. Power supply connections.**

# 14. Software API

## 14.1 API provided by SA-MP

Table 38: API provided by SA-MP

| Name | Description |
|---|---|
| **Playback API** | |
| NAV_AreaSwitch | Switch SACD Area |
| NAV_PlayTrack | Start playing at the index of the track |
| NAV_PlayAtTimecode | Start playing at the given time |
| NAV_Stop | Stop playback |
| NAV_Pause | Pause playback |
| NAV_ResumePlay | Resume playback at normal speed |
| NAV_NextTrack | Continue with next track |
| NAV_PreviousTrack | Continue with previous track |
| NAV_Repeat | Set the repeat mode for playback |
| NAV_RepeatAB | Set the repeat AB mode |
| NAV_Shuffle | Play tracks in random order |
| NAV_IntroScan | Play only intro part of each track |
| NAV_ForwardScan | Start scanning forward – fast playback with burst sound |
| NAV_BackwardScan | Start scanning backward – fast playback with burst sound |
| NAV_SetPlaySequence | Set play sequence mode |
| NAV_SetProgramList | Set program list |
| NAV_GetState | Returns navigator states |
| NAV_GetPlayList | Returns navigator play list |
| **Post-processing API** | |
| APM_SetSpeakers | Select speaker configuration |
| APM_SetInputMode | Select between DSD or PCM as APM input |
| APM_SetOutputMode | Select APM output mode (DSD or PCM) |
| APM_Set6chDownMix | Set the downmix of six-channel output stream |
| APM_Set2chDownMix | Set the downmix of two-channel output stream |
| APM_SetBassFilters | Select the bass management frequency and slope |
| APM_SetAttenuation | Set attenuation of an output channel |
| APM_SetDelay | Set delay of a channel of output stream |
| APM_SetFilterMode | Set Sigma Delta modulator filter mode |
| APM_SetPcmUpsampling | Set the PCM upsampling mode |
| APM_SetPIO | Set the DAC PIO pins |
| **Text and Data API** | |
| SDI_SetAvailableCharSets | Set a list of character sets, application can handle |
| SDI_SetLanguagePreference | Set a list of preferred languages |
| SDI_GetAlbumInfo | Retrieve information about the album of active disc |
| SDI_GetAlbumText | Retrieve album text items |

**Table 38: API provided by SA-MP***…continued*

| Name | Description |
|---|---|
| SDI_GetNumberOfIndices | Retrieve number of indices for specified track |
| SDI_GetDiscInfo | Retrieve information about the active disc |
| SDI_GetDiscText | Retrieve disc text items |
| SDI_GetAreaText | Retrieve area text items |
| SDI_GetTrackInfo | Retrieve information about the specified track |
| SDI_GetTrackText | Retrieve track text items |
| **System configuration API** | |
| SDM_SetBeType | Select the front-end interface attached to SA-MP |
| SDM_SetDacPinnning | Configure the DAC pins |
| SDM_SetAudioClock | Configure the audio clock for different input stream modes |
| SDM_SetMemoryConfig | Configure the SDRAM attached to the SAA7893HL |
| SDM_GetHandler | Return the pointer to SA-MP interrupt handler |
| SDM_SetDsdClockPolarity | Configure the DSD clock polarity |
| SDM_SetSystemClock | Inform SA-MP about the system clock |
| SDM_SetBurstLength | Configure the burst length for fast play |
| **General API** | |
| SAMP_Init | Initialize SA-MP |
| SAMP_Term | Terminate SA-MP |
| SAMP_Activate | Activate SA-MP |
| SAMP_Reactivate | Reactivate SA-MP |
| SAMP_Deactivate | Deactivate SA-MP |
| SAMP_SACDDiscReq | SACD disc recognition |

## 14.2 API required by SA-MP

Software to be provided by the DVD host:

- For the front-end: Seek, GetDataArea, TransferRate (optional)
- For the operating system: Tasks, Interrupts, Semaphores, Mailboxes, Timers.

# 15. Limiting values

**Table 39: Absolute maximum ratings**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Note 1.*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VCC_Core | digital core supply voltage | –0.5 | +2.1 | V |
| VCC_IO | IO pins supply voltage | –0.5 | +3.8 | V |
| $V_{DDA}$ | analog supply voltage | –0.5 | +2.1 | V |
| $V_I$ | DC input voltage | –0.5 | +5.5 | V |
| $T_{amb}$ | ambient temperature | 0 | 70 | °C |
| $T_{stg}$ | storage temperature | –25 | +125 | °C |
| $T_j$ | junction temperature | –150 | +150 | °C |

[1] Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may effect device reliability.

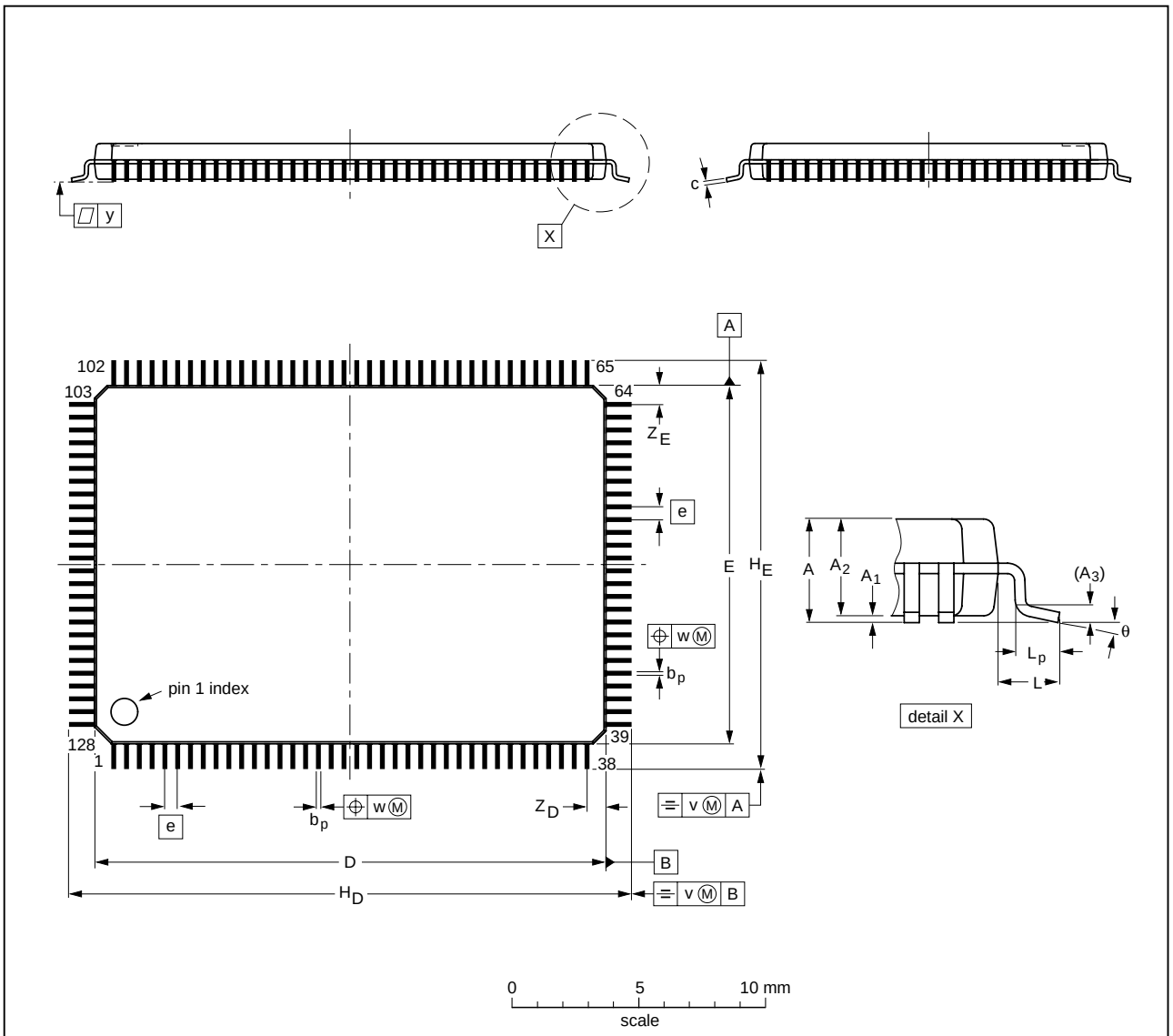
# 16. Characteristics

**Table 40: Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power supply: VCC_Core (digital core supply voltage)** | | | | | |
| VCC_Core | digital core supply voltage | 1.65 | 1.8 | 1.95 | V |
| P | power dissipation | 90 | 110 | 150 | mW |
| **Power supply: $V_{DDA}$ (analog supply voltage)** | | | | | |
| $V_{DDA}$ | analog supply voltage | 1.65 | 1.8 | 1.95 | V |
| P | power dissipation during disc recognition only | - | 40 | 60 | mW |
| **Power supply: VCC_IO (I/O pins supply voltage)** | | | | | |
| VCC_IO | I/O pins supply voltage | 3.0 | 3.3 | 3.6 | V |
| P | power dissipation during disc recognition only | - | 70 | 100 | mW |
| **Digital inputs and outputs** | | | | | |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | - | VCC_IO + 0.5 | V |
| $V_{IL}$ | LOW-level input voltage | - | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | VCC_IO – 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | - | - | 0.4 | V |
| $C_i$ | input capacitance | - | - | 10 | pF |
| $C_o$ | output capacitance | - | - | 10 | pF |
| $I_{LI}$ | input leakage current | - | - | ±10 | µA |
| $I_{i(n)}$ | input current on any pin except supplies | - | - | ±10 | mA |

## 17. Package outline

**LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm** **SOT425-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.15<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.20<br>0.09 | 20.1<br>19.9 | 14.1<br>13.9 | 0.5 | 22.15<br>21.85 | 16.15<br>15.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.81<br>0.59 | 0.81<br>0.59 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT425-1 | 136E28 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

**Fig 60. LQFP128 (SOT425-1) package outline.**

# 18. Soldering

## 18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

## 18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 $mm^3$ so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 $mm^3$ so called small/thin packages.

## 18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 18.5 Package related soldering information

**Table 41: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package[1] | Soldering method | |
|---|---|---|
| | Wave | Reflow[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended[6] | suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# 19. Revision history

**Table 42: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 02 | 20030226 | - | **Product data (9397 750 10925)**<br>Modifications:<br>• The value of the capacitor to pin Adcrefl in Figure 44 is changed from 10 nF to 100 nF<br>• The system clock definitions are added in Section 7.5.1<br>• The audio clock definitions are added in Section 7.5.2<br>• A remark is added at the end of Section 8.2.<br>• A note is added to Table 11. |
| 01 | 20021014 | - | **Product data (9397 750 10341)** |

## 20. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 21. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 10925

# Contents





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