

DATA SHEET

P80CL410; P83CL410

Low voltage 8-bit microcontrollers
with I²C-bus

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Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

CONTENTS		
1	FEATURES	
2	GENERAL DESCRIPTION	
2.1	ROMless version: P80CL410	
3	APPLICATIONS	
4	ORDERING INFORMATION	
5	BLOCK DIAGRAM	
6	FUNCTIONAL DIAGRAM	
7	PINNING INFORMATION	
7.1	Pinning	
7.2	Pin description	
8	FUNCTIONAL DESCRIPTION OVERVIEW	
8.1	General	
8.2	CPU timing	
9	MEMORY ORGANIZATION	
9.1	Program Memory	
9.2	Data Memory	
9.3	Special Function Registers (SFRs)	
9.4	Addressing	
10	I/O FACILITIES	
10.1	Ports	
10.2	Port options	
10.3	Port 0 options	
10.3.1	External memory accesses	
10.3.2	I/O Accesses	
10.4	SET/RESET options	
11	TIMERS/EVENT COUNTERS	
12	REDUCED POWER MODES	
12.1	Idle mode	
12.2	Power-down mode	
12.3	Wake-up from Power-down mode	
12.3.1	Wake-up using INT2 to INT9	
12.3.2	Wake-up using RST	
12.4	Power Control Register (PCON)	
12.5	Status of external pins	
13	I ² C-BUS SERIAL I/O	
13.1	Serial Control Register (S1CON)	
13.2	Serial Status Register (S1STA)	
13.3	Data Shift Register (S1DAT)	
13.4	Address Register (S1ADR)	
14	INTERRUPT SYSTEM	
14.1	External interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$	
14.2	Interrupt priority	
14.3	Interrupt registers	
14.3.1	Interrupt Enable Register (IEN0)	
		14.3.2 Interrupt Enable Register (IEN1)
		14.3.3 Interrupt Priority Register (IP0)
		14.3.4 Interrupt Priority Register (IP1)
		14.3.5 Interrupt Polarity Register (IX1)
		14.3.6 Interrupt Request Flag Register (IRQ1)
		15 OSCILLATOR CIRCUITRY
		16 RESET
		16.1 External reset using the RST pin
		16.2 Power-on-reset
		17 SPECIAL FUNCTION REGISTERS OVERVIEW
		18 INSTRUCTION SET
		19 LIMITING VALUES
		20 DC CHARACTERISTICS
		21 AC CHARACTERISTICS
		22 P85CL000HFZ 'PIGGY-BACK' SPECIFICATION
		22.1 General description
		22.2 Feature differences/additional features of P85CL000HFZ with respect to P83CL410
		22.3 Common specification/feature differences between P85CL000HFZ and P83CL410/P80CL51
		23 PACKAGE OUTLINES
		24 SOLDERING
		24.1 Introduction
		24.2 DIP
		24.2.1 Soldering by dipping or by wave
		24.2.2 Repairing soldered joints
		24.3 QFP
		24.3.1 Reflow soldering
		24.3.2 Wave soldering
		24.3.3 Repairing soldered joints
		24.4 Reflow soldering
		24.5 Wave soldering
		24.6 Repairing soldered joints
		25 DEFINITIONS
		26 LIFE SUPPORT APPLICATIONS
		27 PURCHASE OF PHILIPS I ² C COMPONENTS



Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

1 FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 40-lead DIP, 40-lead VSO or 44-lead QFP package
- 128 bytes on-chip RAM Data Memory
- 4 kbytes on-chip ROM Program Memory for P83CL410
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- Four 8-bit ports; 32 I/O lines
- Two 16-bit Timer/Event counters
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector, nested interrupt structure with two priority levels
- I²C-bus interface for serial transfer on two lines
- Enhanced architecture with:
 - non-page oriented instructions
 - direct addressing
 - four 8-byte RAM register banks
 - stack depth limited only by available internal RAM (maximum 128 bytes)
 - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: DC to 12 MHz
- Supply voltage: 1.8 to 6.0 V
- Very low current consumption
- Operating ambient temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

The P80CL410; P83CL410 (hereafter generally referred to as the P8xCL410) is manufactured in an advanced CMOS technology that allows the device to operate at voltages down to 1.8 V and at frequencies down to DC.

The P8xCL410 has the same instruction set as the 80C51.

The P8xCL410 features 4 kbyte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64 kbytes), four 8-bit ports, two 16-bit timer/counter, an I²C serial interface, a thirteen source two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC. The device operates over a wide range of supply voltages and has low power consumption.

The 8xCL410 has two reduced power modes that are the same as those on the standard 80C51.

The special reduced power feature of this device is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8xCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents.

If the internal oscillator is used the device cannot be stopped and started, but the Power-down mode can be used to achieve similar power savings, without loss of on-chip RAM and Special Function Register values. The Power-down mode can be terminated via an interrupt.

This data sheet details the specific properties of the P80CL410; P83CL410. For details of the 80C51 core see “*Data Handbook IC20*”.

For emulation purposes, the P85CL000 (piggy-back version) with 256 bytes of RAM is recommended. Details are given in Chapter 22.

2.1 ROMless version: P80CL410

The P80CL410 is the ROMless version of the P83CL410. The mask options on the P80CL410 are fixed as follows:

- All ports have option ‘1S’ (standard port, HIGH after reset), except ports P1.6 and P1.7 which have option ‘2S’ (open-drain, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: OFF.

3 APPLICATIONS

The P8xCL410 is an 8-bit general purpose microcontroller especially suited for battery-powered applications.

The P8xCL410 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

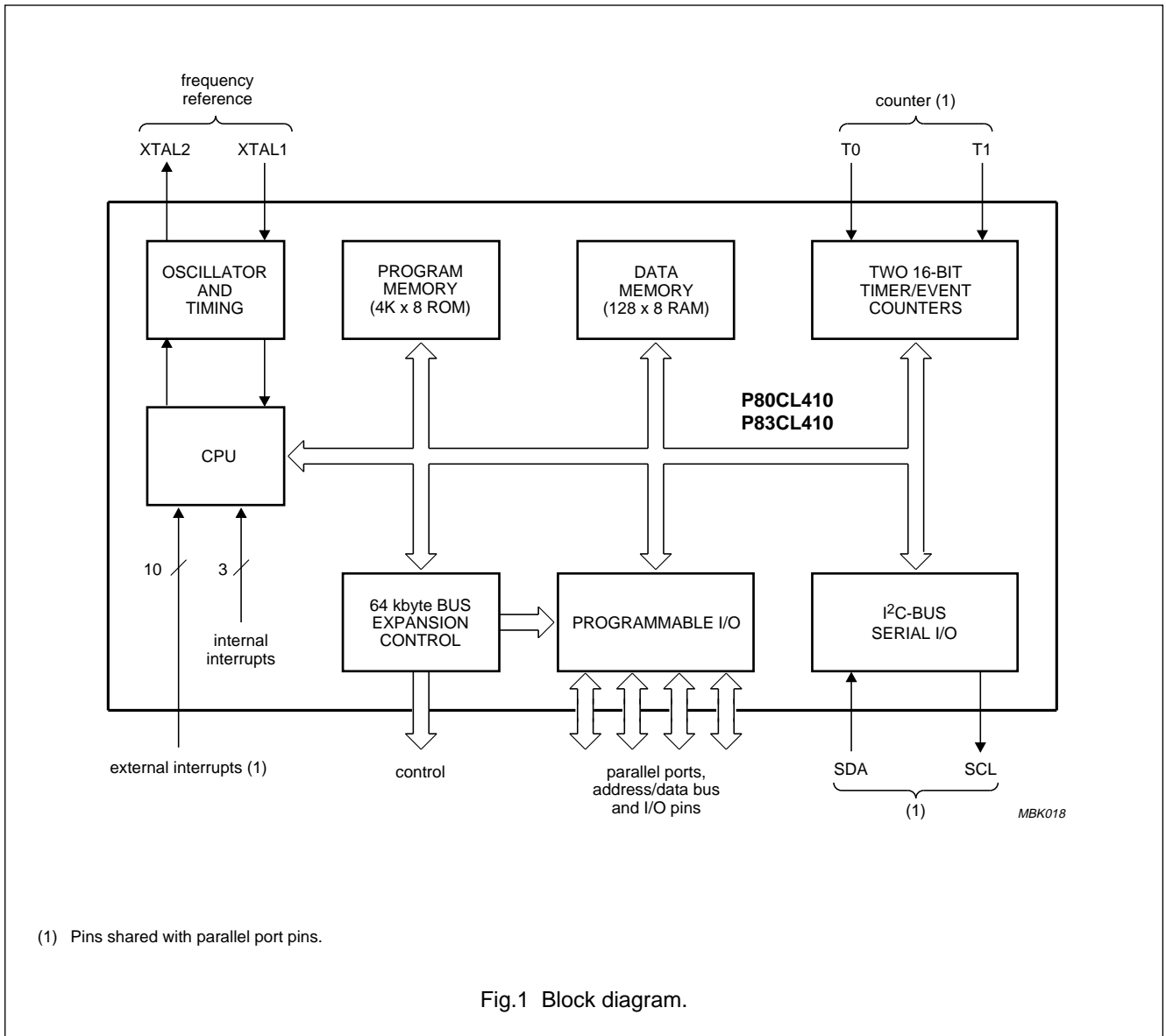
4 ORDERING INFORMATION

TYPE NUMBER ⁽¹⁾		PACKAGE		
ROMless	ROM	NAME	DESCRIPTION	VERSION
P80CL410HFP	P83CL410HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P80CL410HFT	P83CL410HFT	VSO40	plastic very small outline package; 40 leads	SOT158-1
–	P83CL410HFH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

5 BLOCK DIAGRAM



Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

6 FUNCTIONAL DIAGRAM

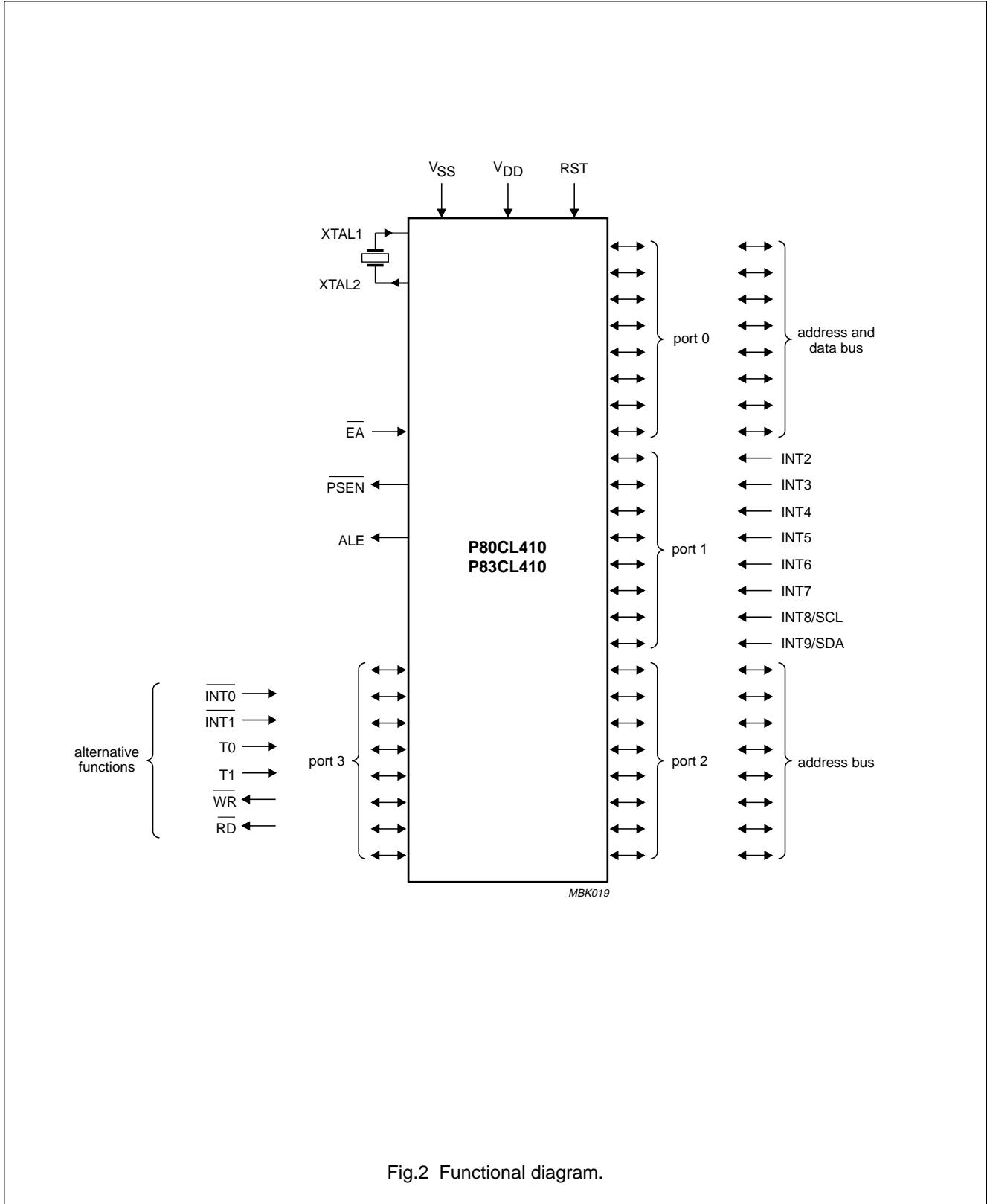


Fig.2 Functional diagram.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

7 PINNING INFORMATION

7.1 Pinning

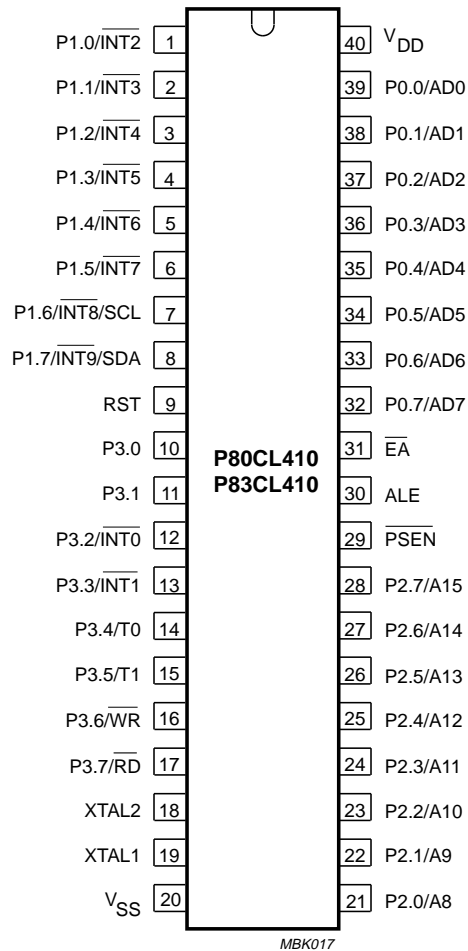


Fig.3 Pin configuration for DIP40 and VSO40 packages.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

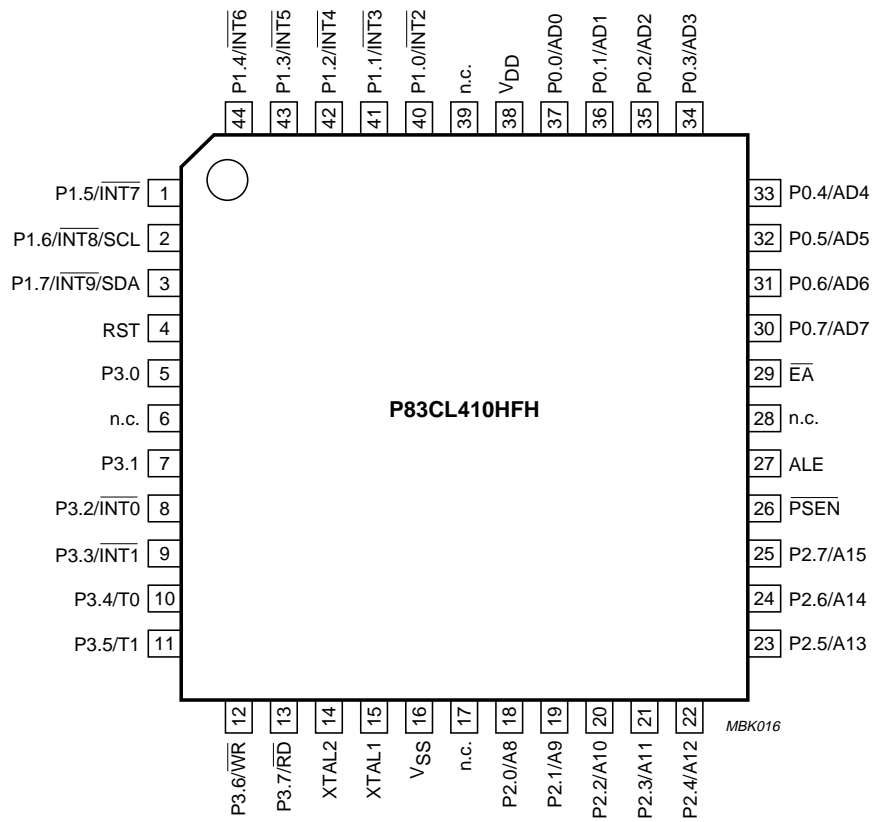


Fig.4 Pin configuration for QFP44 package.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

7.2 Pin description

Table 1 Pin description for DIP40 (SOT190-1), VSO40 (SOT319-2) and QFP44 (SOT307-2) packages

For more extensive description of the port pins see Chapter 10 "I/O facilities".

SYMBOL	PIN		DESCRIPTION
	DIP40 VSO40	QFP44	
P1.0/ $\overline{\text{INT2}}$ P1.1/ $\overline{\text{INT3}}$ P1.2/ $\overline{\text{INT4}}$ P1.3/ $\overline{\text{INT5}}$ P1.4/ $\overline{\text{INT6}}$ P1.5/ $\overline{\text{INT7}}$ P1.6/ $\overline{\text{INT8}}$ /SCL P1.7/ $\overline{\text{INT9}}$ /SDA	1 2 3 4 5 6 7 8	40 41 42 43 44 1 2 3	<ul style="list-style-type: none"> • Port 1: 8-bit bidirectional I/O port (P1.0 to P1.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}, see Chapter 20) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. • Alternative functions: <ul style="list-style-type: none"> – $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$ are external interrupt inputs – SCL and SDA are the I²C-bus clock and data lines.
RST	9	4	Reset: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P3.0 P3.1 P3.2/ $\overline{\text{INT0}}$ P3.3/ $\overline{\text{INT1}}$ P3.4/T0 P3.5/T1 P3.6/ $\overline{\text{WR}}$ P3.7/ $\overline{\text{RD}}$	10 11 12 13 14 15 16 17	5 7 8 9 10 11 12 13	<ul style="list-style-type: none"> • Port 3: 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 1. • Alternative functions: <ul style="list-style-type: none"> – $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are external interrupts 0 and 1 – T0 and T1 are external inputs for timers 0 and 1 – $\overline{\text{WR}}$ is the external Data Memory write strobe – $\overline{\text{RD}}$ is the external Data Memory read strobe.
XTAL2	18	14	Crystal oscillator output: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	19	15	Crystal oscillator input: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V _{SS}	20	16	Ground: circuit ground potential.
P2.0 to P2.7 A8 to A15	21 to 28	18 to 25	<ul style="list-style-type: none"> • Port 2: 8-bit bidirectional I/O port (P2.0 to P2.7) with internal pull-ups. Same characteristics as Port 1. • High-order addressing: Port 2 emits the high-order address byte (A8 to A15) during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
PSEN	29	26	Program Store Enable. Output read strobe to external Program Memory. When executing code out of external Program Memory, PSEN is activated twice each machine cycle. However, during each access to external Data Memory two PSEN activations are skipped.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

SYMBOL	PIN		DESCRIPTION
	DIP40 VSO40	QFP44	
ALE	30	27	Address Latch Enable. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $\frac{1}{6} \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
\overline{EA}	31	29	External Access. When \overline{EA} is held HIGH the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). Holding \overline{EA} LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
P0.0 to P0.7 AD0 to AD7	39 to 32	30 to 37	<ul style="list-style-type: none"> • Port 0: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. • Low-order addressing: Port 0 is also the multiplexed low-order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
V _{DD}	40	38	Power supply.
n.c.	–	6, 17, 28 and 39	Not connected.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

8 FUNCTIONAL DESCRIPTION OVERVIEW

This chapter gives a brief overview of the device. The detailed functional description is in the following chapters:

- Chapter 9 "Memory organization"
- Chapter 10 "I/O facilities"
- Chapter 11 "Timers/event counters"
- Chapter 12 "Reduced power modes"
- Chapter 13 "I²C-bus serial I/O"
- Chapter 14 "Interrupt system"
- Chapter 15 "Oscillator circuitry"
- Chapter 16 "Reset".

8.1 General

The P8xCL410 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of Data Memory.

The P8xCL410 contains a 4 kbytes Program Memory (ROM; P83CL410); a static 128 bytes Data Memory (RAM); 32 I/O lines; two 16-bit timer/event counters; a thirteen-source, two priority-level, nested interrupt structure and on-chip oscillator and timing circuit. An I²C-bus serial interface is also provided.

The device has two software-selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the timers, serial I/O and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μ s if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P8xCL410 has 4 kbytes of Program Memory (ROM; P83CL410 only) plus 128 bytes of Data Memory (RAM) on board. The device has separate address spaces for Program and Data Memory (see Fig.5). Using Port latches P0 and P2, the P8xCL410 can address a maximum of 64 kbytes of program memory and a maximum of 64 kbytes of data memory. The CPU generates the read (\overline{RD}) and write (\overline{WR}) signals for external Data Memory accesses, and the read strobe (\overline{PSEN}) for external Program Memory.

9.1 Program Memory

After reset the CPU begins program execution at location 0000H. The lower 4 kbytes of Program Memory can be implemented in the on-chip ROM (P83CL410 only) or in external Program Memory.

If the \overline{EA} pin is tied to V_{DD} , then Program Memory fetches from addresses 0000H to 0FFFH are directed to the internal ROM. Fetches from addresses 1000H to FFFFH are directed to external ROM. Program Counter values greater than 0FFFH are automatically addressed to external memory regardless of the state of the EA pin.

9.2 Data Memory

The P8xCL410 contains 128 bytes of internal RAM and 27 Special Function Registers (SFR). The memory map (Fig.5) shows the internal Data Memory space divided into the lower 128, the upper 128, and the SFR space. The lower 128 bytes of the internal RAM are organized as mapped in Fig.6. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions refer to these registers within a register bank as R0 through R7. Two bits in the Program Status Word select which register bank is in use. The next 16 bytes above the register banks form a block of bit-addressable memory space. The 128 bits in this area can be directly addressed by the single-bit manipulation instructions. The remaining registers (30H to 7FH) are directly and indirectly byte addressable.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

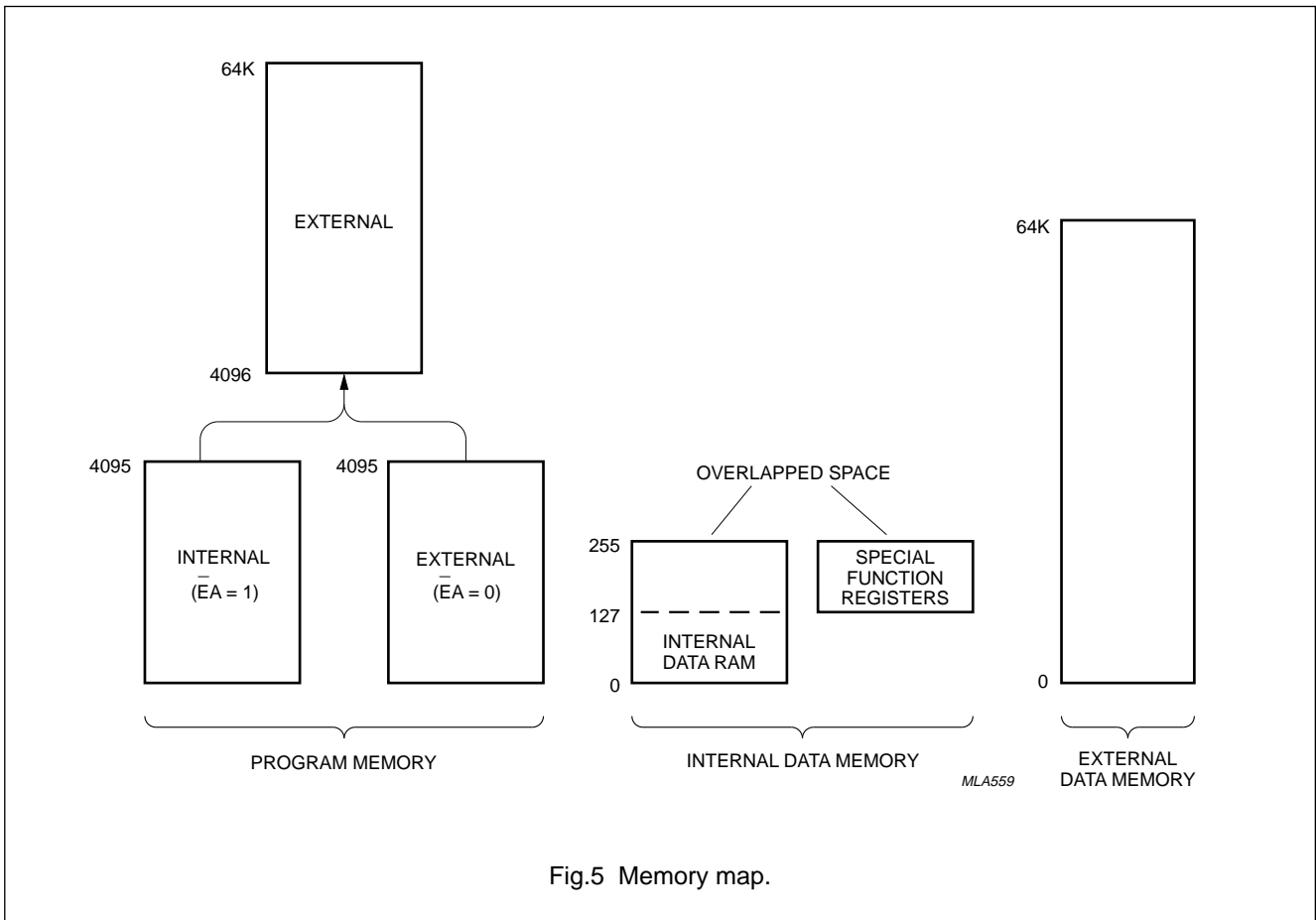


Fig.5 Memory map.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

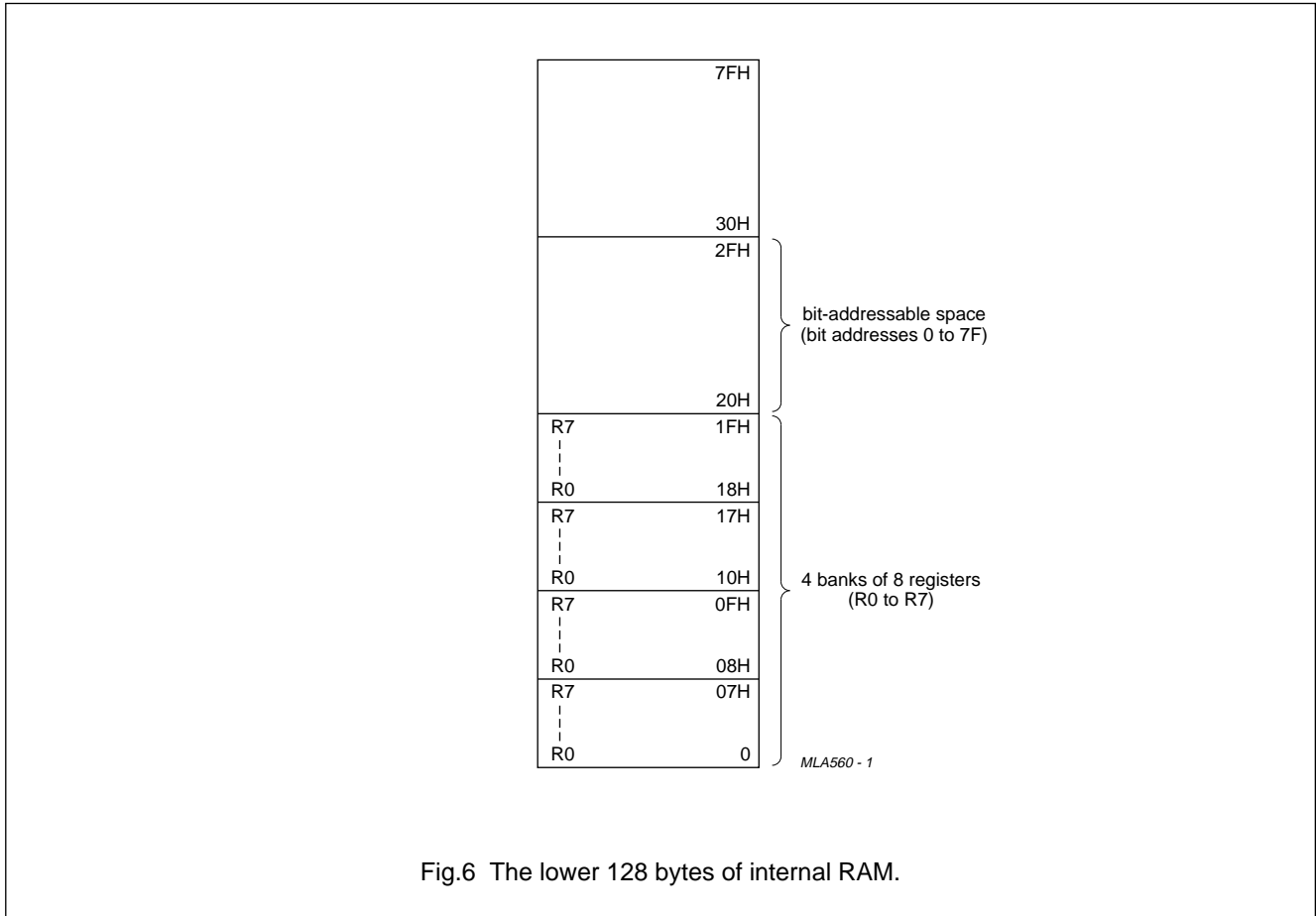


Fig.6 The lower 128 bytes of internal RAM.

9.3 Special Function Registers (SFRs)

The upper 128 bytes are the address locations of the SFRs. Figure 7 shows the SFR space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 directly addressable locations in the SFR address space (SFRs with addresses divisible by eight).

9.4 Addressing

The P8xCL410 has five methods for addressing source operands:

- Register
- Direct
- Register-indirect
- Immediate
- Base-register plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or register-indirect
- Internal RAM (128 bytes) through direct or register-indirect
- Special Function Registers through direct
- External data memory through register-indirect
- Program Memory look-up tables through base-register plus index-register-indirect.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

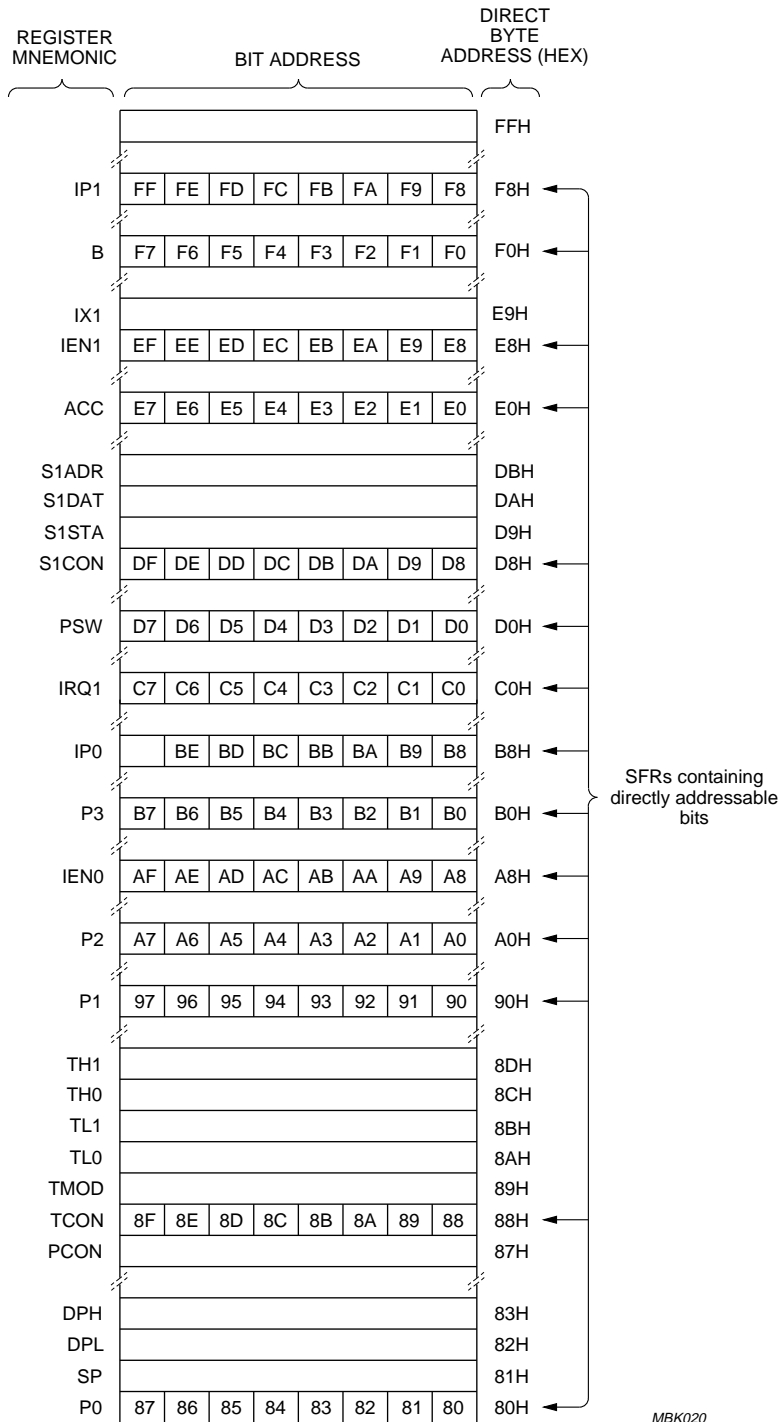


Fig.7 Special Function Register memory map.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

10 I/O FACILITIES

10.1 Ports

The P8xCL410 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the alternative functions detailed below. To enable a port pin alternate function, the port bit latch in its SFR must contain a logic 1.

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for the external interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$, and the I²C-bus interface lines SCL and SDA.

Port 2 Provides the high-order address when expanding the device with external Program or Data Memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$
- Timer/counter inputs: T1 and T0
- Control signals to read and write to external memories: RD and WR.

Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Ports 1, 2, and 3 have internal pull-ups Figure 8(a) shows that the strong transistor 'p1' is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter. This inverter and 'p3' form a latch which holds the logic 1. In Port 0 the pull-up 'p1' is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 0 bit latch leaves both output transistors switched off so that the pin can be used as a high-impedance input.

10.2 Port options

The pins of port 1 (except P1.6 and P1.7; with option 2S only), port 2 and port 3 may be individually configured with one of the following options. These options are also shown in Fig.8.

Option 1 Standard Port; quasi-bidirectional I/O with pull-up. The strong booster pull-up 'p1' is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.8(a).

Option 2 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; see Fig.8(b).

Option 3 Push-pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs; see Fig.8(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{\text{EA}} = 0$ or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 EXTERNAL MEMORY ACCESSES

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O ACCESSES

Option 1 When writing a logic 1 to the port latch, the strong pull-up 'p1' will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.8(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.8(c).

10.4 SET/RESET options

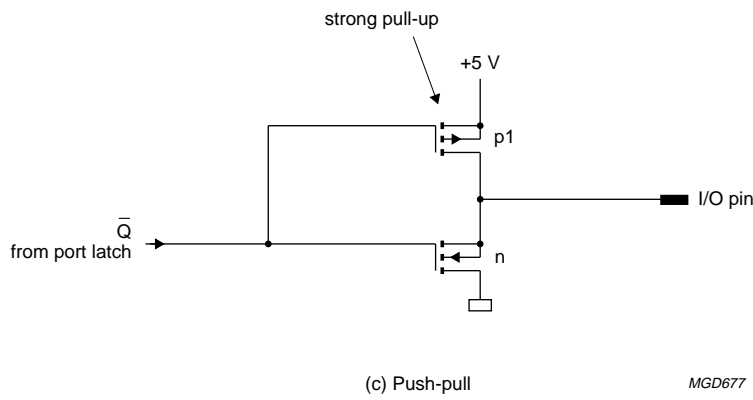
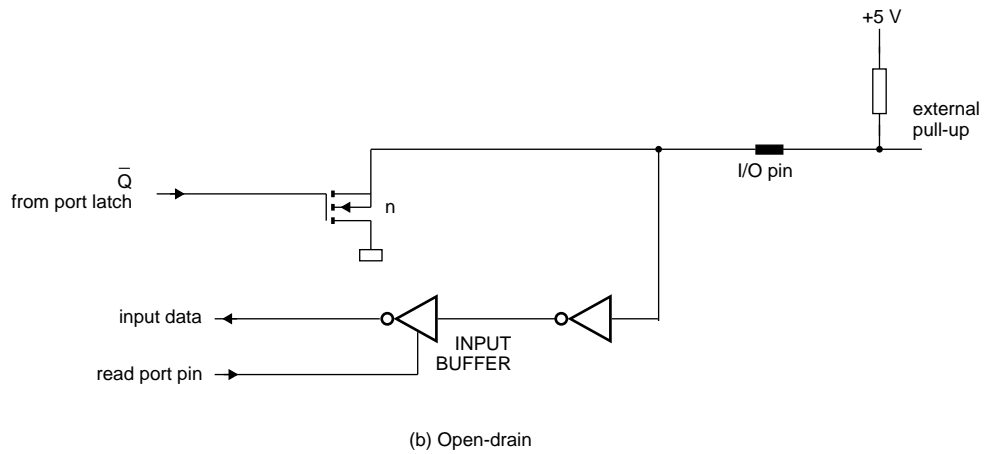
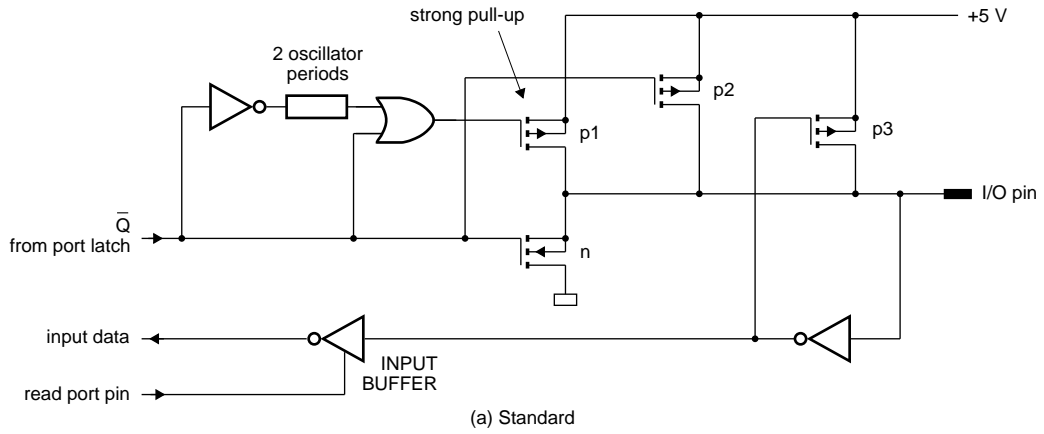
Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending 'S' or 'R' to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



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Fig.8 Port configuration options.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

11 TIMERS/EVENT COUNTERS

The P8xCL410 contains two 16-bit timer/event counter registers; Timer 0 and Timer 1, which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $\frac{1}{12} \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{24} \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

- Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.
- Mode 1 16-bit time-interval or event counter.
- Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.
- Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

12 REDUCED POWER MODES

There are two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

12.1 Idle mode

Idle mode operation permits the external interrupts, I²C-bus, and timer blocks to continue to function while the clock to the CPU is halted.

Idle mode is entered by setting the IDL bit in the Power Control Register (PCON.0, see Table 3). The instruction that sets IDL is the last instruction executed in the normal operating mode before the Idle mode is activated

Once in Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 4.

The following functions remain active during the Idle mode:

- Timer 0 and Timer 1
- I²C-bus
- External interrupt.

These functions may generate an interrupt or reset; thus ending the Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause IDL (PCON.0) to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 (PCON.2) and GF1 (PCON.3) may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

12.2 Power-down mode

Operation in Power-down mode freezes the oscillator. The internal connections which link both Idle and Power-down signals to the clock generation circuit are shown in Fig.9.

Power-down mode is entered by setting the PD bit in the Power Control Register (PCON.1, see Table 2). The instruction that sets PD is the last executed prior to going into the Power-down mode.

Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and PSEN are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

12.3 Wake-up from Power-down mode

When in Power-down mode the controller can be woken-up with either the external interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$, or a reset operation. The wake-up operation has two basic approaches as explained in Section 12.3.1; 12.3.2 and illustrated in Fig.10.

12.3.1 WAKE-UP USING $\overline{\text{INT2}}$ TO $\overline{\text{INT9}}$

If any of the interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$ are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

12.3.2 WAKE-UP USING RST

To wake-up the P8xCL410, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

12.4 Power Control Register (PCON)

See Tables 2 and 3. Idle and Power-down modes are activated by software using this SFR. PCON is not bit-addressable.

12.5 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 3. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor 'p1'; see Fig.8(a).

Table 2 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
–	–	–	–	GF1	GF0	PD	IDL

Table 3 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7, 6, 5, 4	–	reserved
3 and 2	GF1 and GF0	General purpose flag bits
1	PD	Power-down bit ; setting this bit activates the Power-down mode
0	IDL	Idle mode bit ; setting this bit activates the Idle mode

Table 4 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	port data	port data	port data	port data	port data
	external	1	1	floating	port data	address	port data	port data
Power-down	internal	0	0	port data	port data	port data	port data	port data
	external	0	0	floating	port data	port data	port data	port data

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

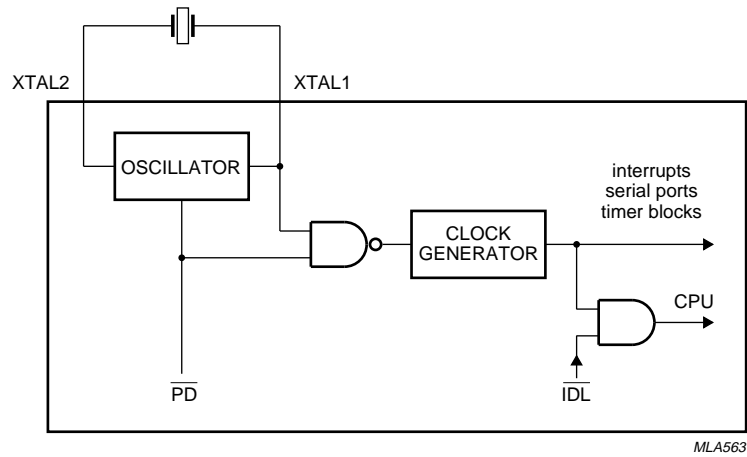


Fig.9 Internal clock control in Idle and Power-down mode.

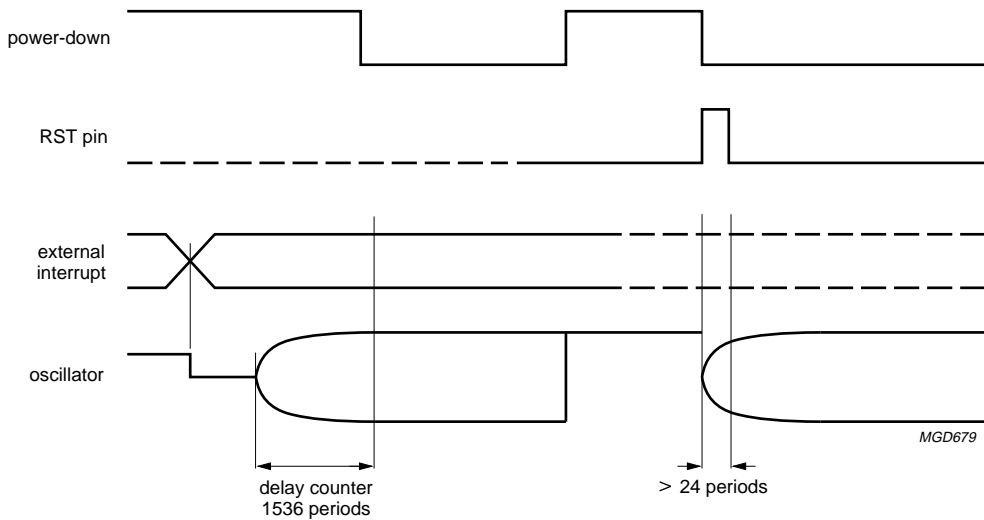


Fig.10 Wake-up operation.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

13 I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus, which consists of a serial data line (SDA) and a serial clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the Serial Control Register S1CON. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR is the Slave Address Register. Slave address recognition is performed by on-chip hardware.

Figure 11 is the block diagram of the I²C-bus serial I/O.

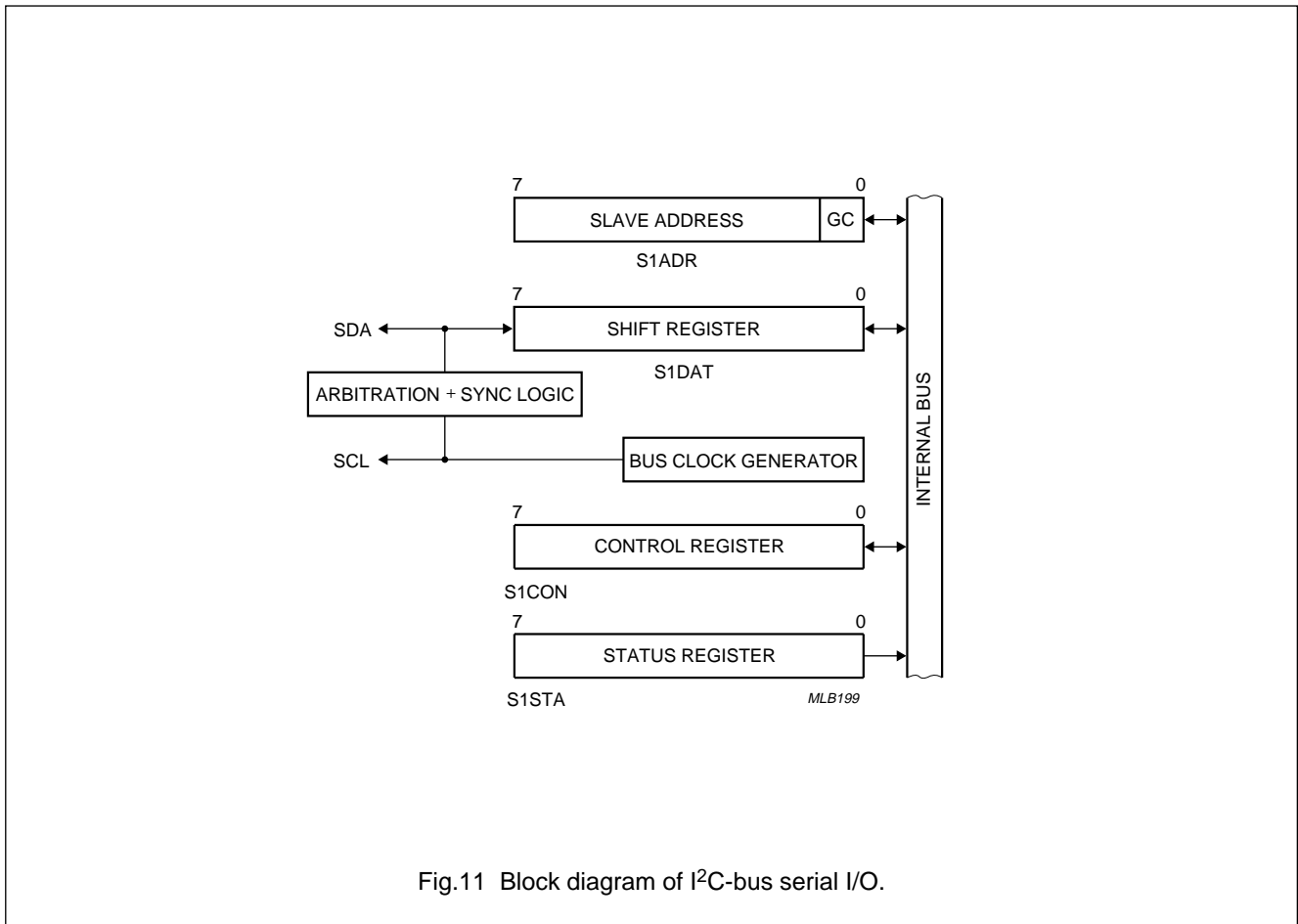


Fig.11 Block diagram of I²C-bus serial I/O.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

13.1 Serial Control Register (S1CON)

Table 5 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 6 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
7	CR2	This bit along with bits CR1 (S1CON.1) and CR0 (S1CON.0) determines the serial clock frequency when SIO is in the Master mode. See Table 7.
6	ENS1	ENABLE serial I/O. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
5	STA	START flag. When this bit is set in Slave mode, the SIO hardware checks the status of the I ² C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
4	STO	STOP flag. With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I ² C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I ² C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
3	SI	SIO interrupt flag. This flag is set, and an interrupt is generated, after any of the following events occur: <ul style="list-style-type: none"> • A START condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while GC (S1ADR.0) = 1 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A STOP or START condition is received as selected slave receiver or transmitter.
2	AA	Assert Acknowledge. When this bit is set, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the SCL line when: <ul style="list-style-type: none"> • Own slave address is received • General call address is received; GC (S1ADR.0) = 1 • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
1	CR1	These two bits along with the CR2 (S1CON.7) bit determine the serial clock frequency when SIO is in the Master mode. See Table 7.
0	CR0	

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 7 Selection of the serial clock frequency SCL in a Master mode of operation

CR2	CR1	CR0	f _{osc} DIVISOR	BIT RATE (kHz) at f _{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100.0
1	1	0	60	59.7	100.0	–
1	1	1	not allowed	–	–	–

13.2 Serial Status Register (S1STA)

S1STA is a read-only register. The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given in Tables 10 to 14.

Table 8 Serial Status Register (address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 9 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
3 to 7	SC4 to SC0	5-bit status code
0 to 2	–	these three bits are always zero

Table 10 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
38H	arbitration lost in SLA, R/W or DATA

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 11 MST/REC mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
38H	arbitration lost while returning $\overline{\text{ACK}}$
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned

Table 12 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	own SLA and W have been received, ACK returned
68H	arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
70H	general CALL has been received, ACK returned
78H	arbitration lost in SLA, R/W as MST; general CALL has been received
80H	previously addressed with own SLA; DATA byte received, ACK returned
88H	previously addressed with own SLA; DATA byte received, $\overline{\text{ACK}}$ returned
90H	previously addressed with general CALL; DATA byte has been received, ACK has been returned
98H	previously addressed with general CALL; DATA byte has been received, $\overline{\text{ACK}}$ has been returned
A0H	a STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX

Table 13 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	own SLA and R have been received, ACK returned
B0H	arbitration lost in SLA, R/W as MST; own SLA and R have been received, ACK returned
B8H	DATA byte has been transmitted, ACK received
C0H	DATA byte has been transmitted, $\overline{\text{ACK}}$ received
C8H	last DATA byte has been transmitted (AA = 0), ACK received

Table 14 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition
F8H	no relevant state information available, SI = 0

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 15 Symbols used in Tables 10 to 14

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit is logic 0)
$\overline{\text{ACK}}$	no acknowledgement (acknowledge bit is logic 1)
DATA	8-bit data byte to or from I ² C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

13.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. The MSB (bit 7) is transmitted or received first; i.e. data shifted from right to left.

Table 16 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

13.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 17 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 18 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	own slave address
0	GC	this bit is used to determine whether the general call address is recognized; when GC = 0, the general call address is not recognized; when GC = 1, the general call address is recognized

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

14 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU at unpredictable times. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The system is shown in Fig.12. The P8xCL410 acknowledges interrupt requests from thirteen sources as follows:

- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$
- Timer 0 and Timer 1
- I²C-bus
- $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. Figure 12 shows the interrupt system.

14.1 External interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$

Port 1 lines serve an alternative purpose as eight additional interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 13 shows the external interrupt configuration.

14.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If a low priority interrupt is received simultaneously with a high priority interrupt, the high priority interrupt will be dealt with first.

If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to the sequence shown in Table 19 and in Fig.12. The 'vector address' is the ROM location where the appropriate interrupt service routine starts.

Table 19 Interrupt vector polling sequence

SYMBOL	VECTOR ADDRESS (HEX)	SOURCE
X0 (first)	0003	External 0
S1	002B	I ² C port
X5	0053	External 5
T0	000B	Timer 0
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
X4	004B	External 4
X9 (last)	xt0073	External 9

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

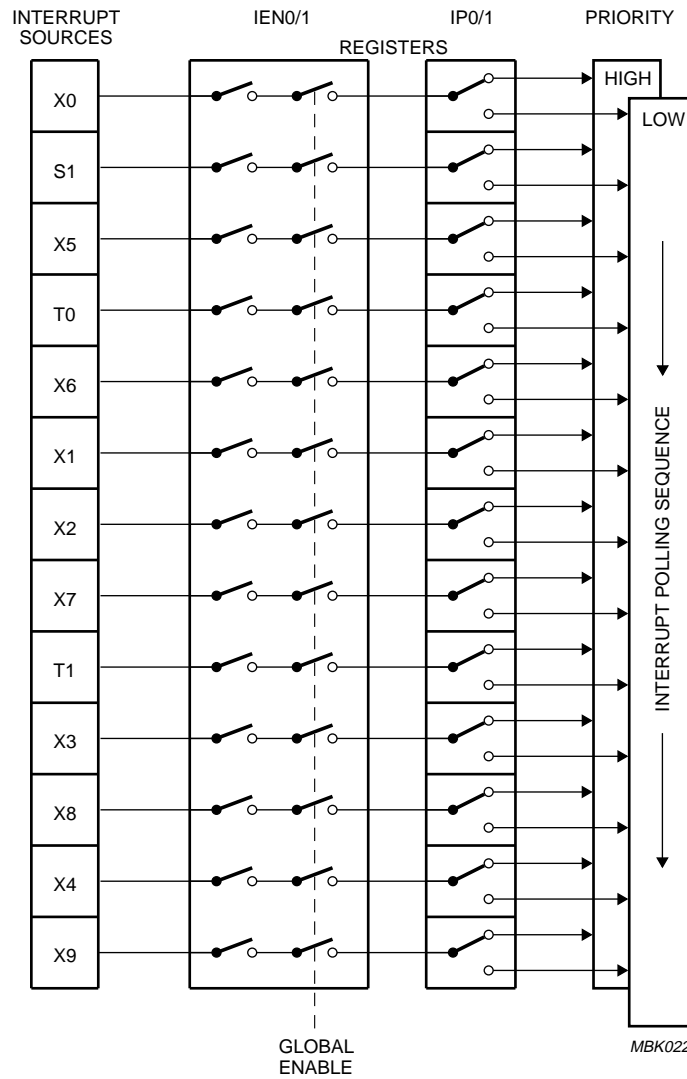
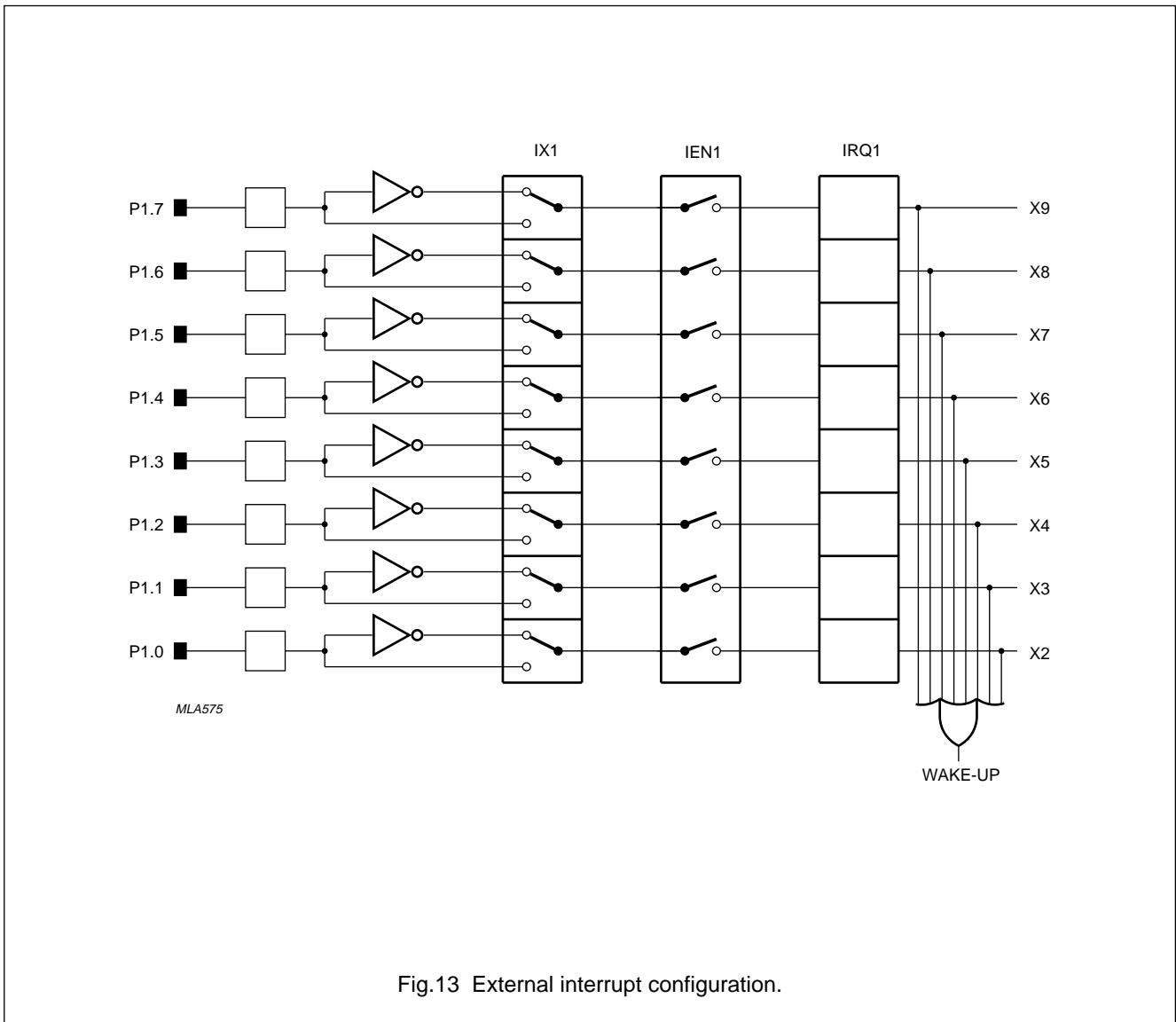


Fig.12 Interrupt system.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



14.3 Interrupt registers

The registers used in the interrupt system are listed in Table 20. Tables 21 to 32 describe the contents of these registers.

Table 20 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register ($\overline{\text{INT2}}$ to $\overline{\text{INT9}}$)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register ($\overline{\text{INT2}}$ to $\overline{\text{INT9}}$)
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

14.3.1 INTERRUPT ENABLE REGISTER (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 21 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	–	ES1	–	ET1	EX1	ET0	EX0

Table 22 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	general enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted
6	–	reserved
5	ES1	enable I ² C-bus SIO interrupt
4	–	reserved
3	ET1	enable Timer 1 interrupt (T1)
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt (T0)
0	EX0	enable external interrupt 0

14.3.2 INTERRUPT ENABLE REGISTER (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 23 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 24 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EX9	enable external interrupt 9
6	EX8	enable external interrupt 8
5	EX7	enable external interrupt 7
4	EX7	enable external interrupt 6
3	EX5	enable external interrupt 5
2	EX4	enable external interrupt 4
1	EX3	enable external interrupt 3
0	EX2	enable external interrupt 2

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

14.3.3 INTERRUPT PRIORITY REGISTER (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 25 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	–	PS1	–	PT1	PX1	PT0	PX0

Table 26 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	–	reserved
5	PS1	I ² C-bus SIO interrupt priority level
4	–	reserved
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

14.3.4 INTERRUPT PRIORITY REGISTER (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 27 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 28 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PX9	external interrupt 9 priority level
6	PX8	external interrupt 8 priority level
5	PX7	external interrupt 7 priority level
4	PX6	external interrupt 6 priority level
3	PX5	external interrupt 5 priority level
2	PX4	external interrupt 4 priority level
1	PX3	external interrupt 3 priority level
0	PX2	external interrupt 2 priority level

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

14.3.5 INTERRUPT POLARITY REGISTER (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 29 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 30 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	IL9	external interrupt 9 polarity level
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

14.3.6 INTERRUPT REQUEST FLAG REGISTER (IRQ1)

Table 31 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 32 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	IQ9	external interrupt 9 request flag
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

15 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCL410 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.15. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 33 and Fig.14).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.14.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.14(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 33 and shown in Fig.14. The required option should be stated when ordering.

Table 33 Oscillator options

OPTION	APPLICATION
Oscillator 1	for 32 kHz clock applications with external trimmer for frequency adjustment; a 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.14(c)
Oscillator 2	low-power, low-frequency operations using LC components; see Fig.14(e)
Oscillator 3	medium frequency range applications
Oscillator 4	high frequency range applications
RC oscillator	RC oscillator configuration; see Figs 14(g) and 16

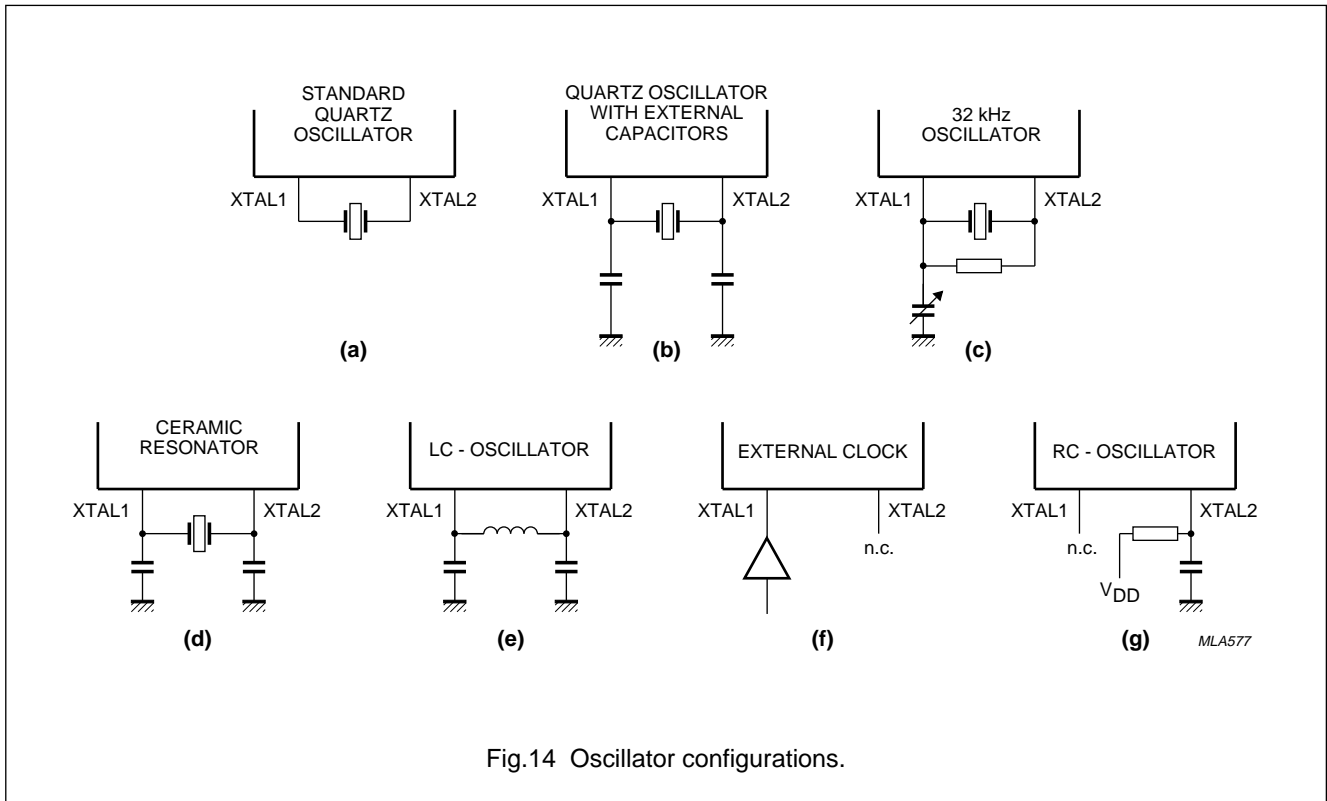


Fig.14 Oscillator configurations.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

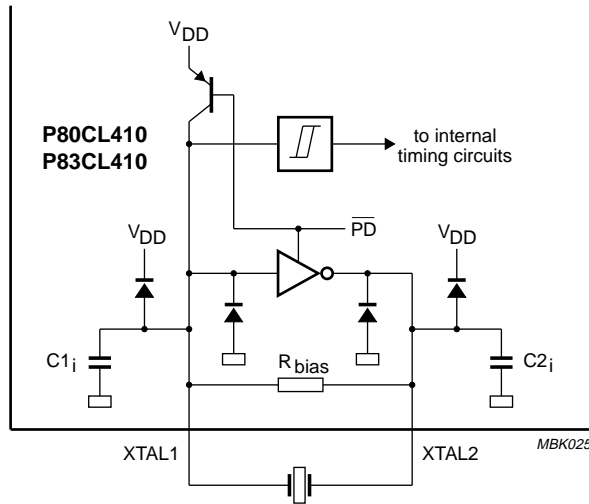
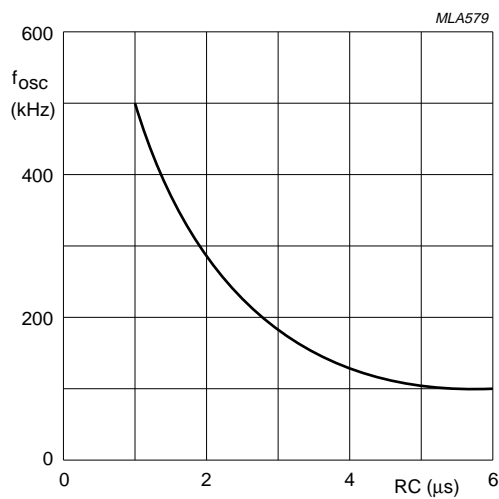


Fig.15 Standard oscillator.



RC oscillator frequency is externally adjustable; $100 \text{ kHz} \leq f_{osc} \leq 500 \text{ kHz}$.

Fig.16 RC oscillator frequency as a function of RC.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 34 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 33)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ ⁽¹⁾
	1.0	Oscillator 2	0	30	0	30	600 Ω
	3.58		0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0	Oscillator 4	0	15	0	15	60 Ω
	12.0		0	10	0	10	40 Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455	Oscillator 2	40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58		0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC	–	Oscillator 2	20	90	20	90	10 μH = 1 Ω 100 μH = 5 Ω 1 mH = 75 Ω

Note

- 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

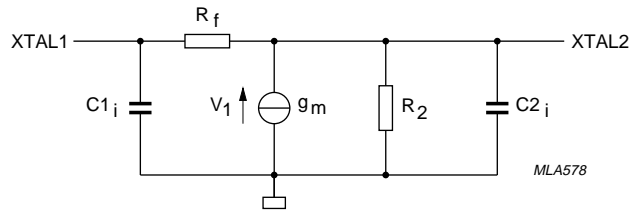


Fig.17 Oscillator equivalent circuit diagram.

Table 35 Oscillator equivalent circuit parameters

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g _m	transconductance	Oscillator 1; 32 kHz Oscillator 2 Oscillator 3 Oscillator 4	T _{amb} = +25 °C; V _{DD} = 4.5 V	– 200 400 1000	15 600 1500 4000	– 1000 4000 10000	μS μS μS μS
C _{1i}	input capacitance	Oscillator 1; 32 kHz Oscillator 2 Oscillator 3 Oscillator 4		– – – –	3.0 8.0 8.0 8.0	– – – –	pF pF pF pF
C _{2i}	output capacitance	Oscillator 1; 32 kHz Oscillator 2 Oscillator 3 Oscillator 4		– – – –	23 8.0 8.0 8.0	– – – –	pF pF pF pF
R ₂	output resistance	Oscillator 1; 32 kHz Oscillator 2 Oscillator 3 Oscillator 4		– – – –	3800 65 18 5.0	– – – –	kΩ kΩ kΩ kΩ

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

16 RESET

To initialize the P8xCL410 a reset is performed by either of three methods:

- Applying an external signal to the RST pin
- Via Power-on-reset circuitry.

A reset leaves the internal registers as shown in Chapter 17. The reset state of the port pins is mask-programmable and can be defined by the user.

16.1 External reset using the RST pin

The reset input for the P8xCL410 is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{\text{PSEN}}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

16.2 Power-on-reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation (see Fig.20).

The on-chip Power-on-reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 μF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on-reset circuitry is shown in Fig.19.

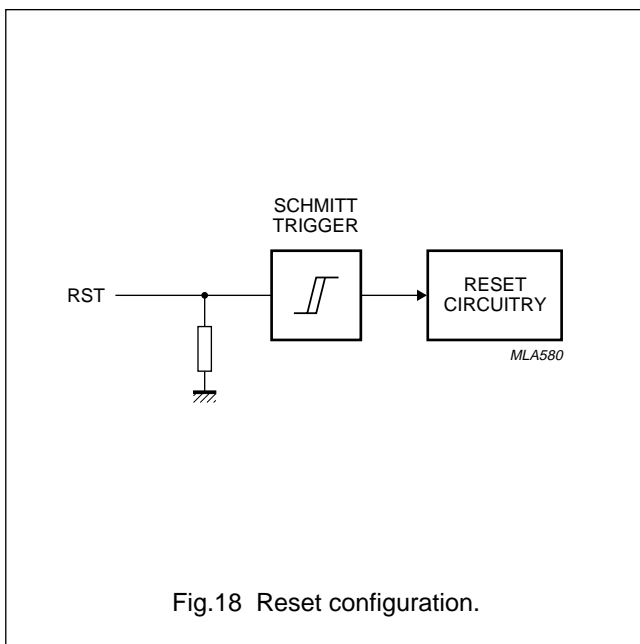


Fig.18 Reset configuration.

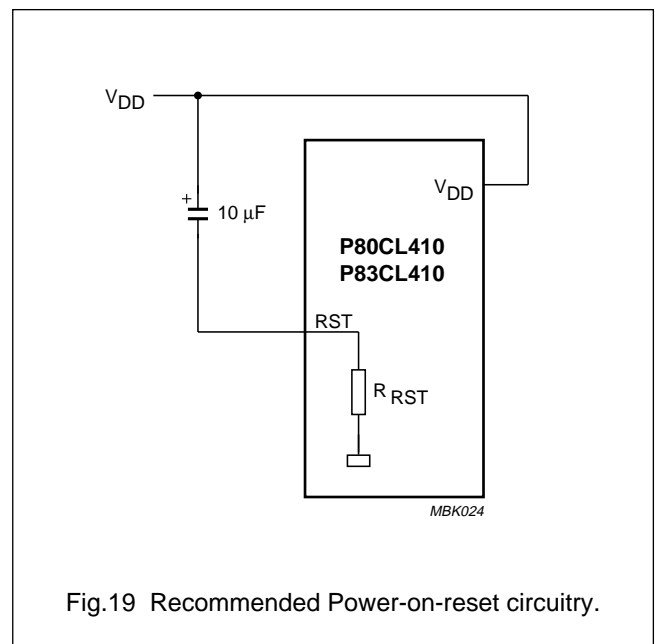


Fig.19 Recommended Power-on-reset circuitry.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

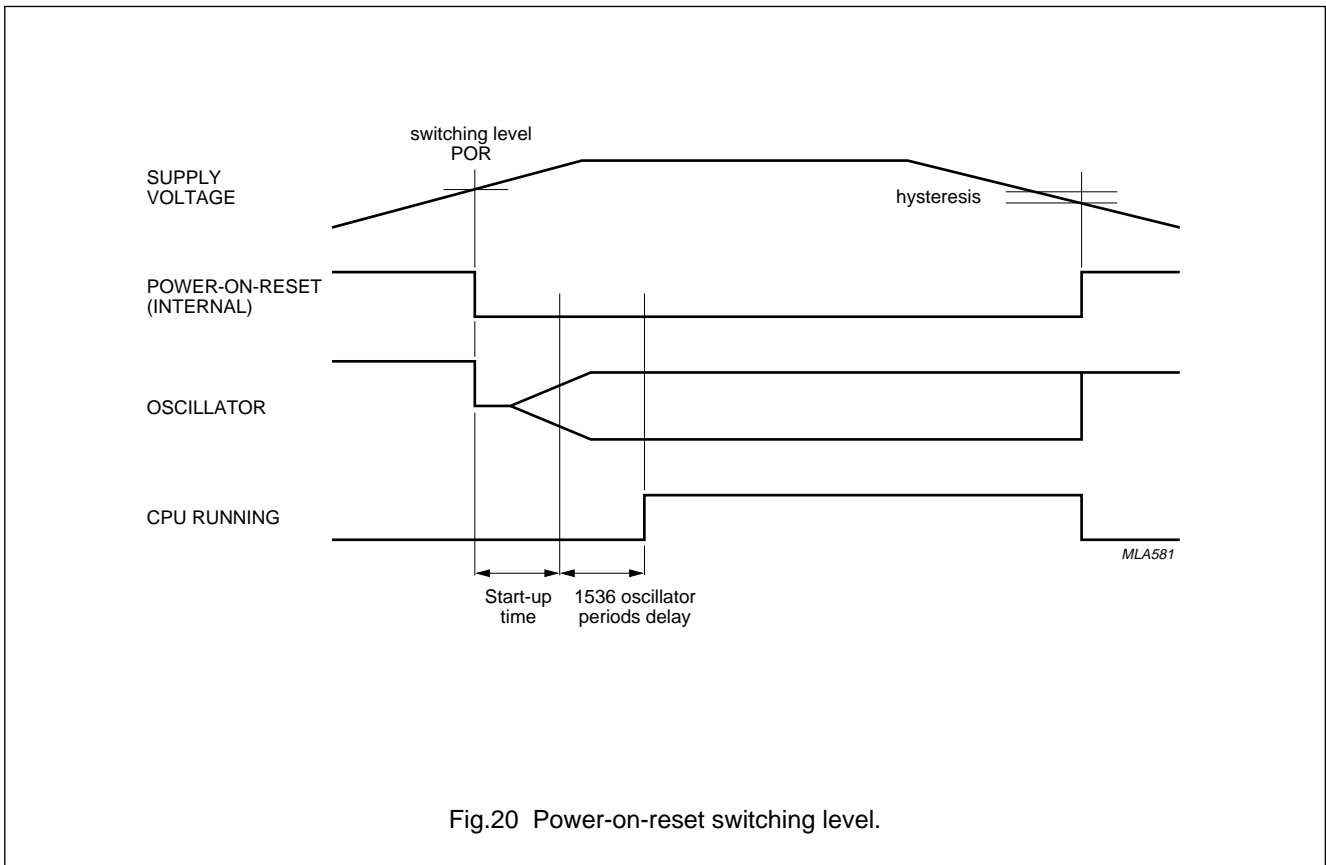


Fig.20 Power-on-reset switching level.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

17 SPECIAL FUNCTION REGISTERS OVERVIEW

The P8xCL410 has 27 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
F8	IP1 ⁽¹⁾	00000000	Interrupt Priority Register ($\overline{\text{INT2}}$ to $\overline{\text{INT9}}$)
F0	B ⁽¹⁾	00000000	B Register
E9	IX1	00000000	Interrupt Polarity Register
E8	IEN1 ⁽¹⁾	00000000	Interrupt Enable Register 1
E0	ACC ⁽¹⁾	00000000	Accumulator
DB	S1ADR	00000000	I ² C-bus Slave Address Register
DA	S1DAT	00000000	I ² C-bus Data Shift Register
D9	S1STA	1111 1000	I ² C-bus Serial Status Register
D8	S1CON ⁽¹⁾	00000000	I ² C-bus Serial Control Register
D0	PSW ⁽¹⁾	00000000	Program Status Word
C0	IRQ1 ⁽¹⁾	00000000	Interrupt Request Flag Register
B8	IP0 ⁽¹⁾	XX000000	Interrupt Priority Register 0
B0	P3 ⁽¹⁾	XXXXXXXX ⁽²⁾	Digital I/O Port Register 3
A8	IEN0 ⁽¹⁾	00000000	Interrupt Enable Register
A0	P2 ⁽¹⁾	XXXXXXXX ⁽²⁾	Digital I/O Port Register 2
90	P1 ⁽¹⁾	XXXXXXXX ⁽²⁾	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON ⁽¹⁾	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	0XX00000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0 ⁽¹⁾	XXXXXXXX ⁽²⁾	Digital I/O Port Register 0

Notes

1. Bit addressable register.
2. Port reset state determined by the customer.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

18 INSTRUCTION SET

The P8xCL410 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of

49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μ s and 45 instructions execute in 2 μ s. Multiply and divide instructions execute in 4 μ s.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 40.

Table 36 Instruction set description: Arithmetic operations

MNEMONIC	DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations				
ADD A,Rr	add register to A	1	1	2*
ADD A,direct	add direct byte to A	2	1	25
ADD A,@Ri	add indirect RAM to A	1	1	26, 27
ADD A,#data	add immediate data to A	2	1	24
ADDC A,Rr	add register to A with carry flag	1	1	3*
ADDC A,direct	add direct byte to A with carry flag	2	1	35
ADDC A,@Ri	add indirect RAM to A with carry flag	1	1	36, 37
ADDC A,#data	add immediate data to A with carry flag	2	1	34
SUBB A,Rr	subtract register from A with borrow	1	1	9*
SUBB A,direct	subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	subtract indirect RAM from A with borrow	1	1	96, 97
SUBB A,#data	subtract immediate data from A with borrow	2	1	94
INC A	increment A	1	1	04
INC Rr	increment register	1	1	0*
INC direct	increment direct byte	2	1	05
INC @Ri	increment indirect RAM	1	1	06, 07
DEC A	decrement A	1	1	14
DEC Rr	decrement register	1	1	1*
DEC direct	decrement direct byte	2	1	15
DEC @Ri	decrement indirect RAM	1	1	16, 17
INC DPTR	increment data pointer	1	2	A3
MUL AB	multiply A and B	1	4	A4
DIV AB	divide A by B	1	4	84
DA A	decimal adjust A	1	1	D4

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 37 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	exclusive-OR register to A	1	1	6*
XRL	A,direct	exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	exclusive-OR immediate data to A	2	1	64
XRL	direct,A	exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	exclusive-OR immediate data to direct byte	3	2	63
CLR	A	clear A	1	1	E4
CPL	A	complement A	1	1	F4
RL	A	rotate A left	1	1	23
RLC	A	rotate A left through the carry flag	1	1	33
RR	A	rotate A right	1	1	03
RRC	A	rotate A right through the carry flag	1	1	13
SWAP	A	swap nibbles within A	1	1	C4

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 38 Instruction set description: Data transfer

MNEMONIC	DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer				
MOV A,Rr	move register to A	1	1	E*
MOV A,direct (note 1)	move direct byte to A	2	1	E5
MOV A,@Ri	move indirect RAM to A	1	1	E6, E7
MOV A,#data	move immediate data to A	2	1	74
MOV Rr,A	move A to register	1	1	F*
MOV Rr,direct	move direct byte to register	2	2	A*
MOV Rr,#data	move immediate data to register	2	1	7*
MOV direct,A	move A to direct byte	2	1	F5
MOV direct,Rr	move register to direct byte	2	2	8*
MOV direct,direct	move direct byte to direct	3	2	85
MOV direct,@Ri	move indirect RAM to direct byte	2	2	86, 87
MOV direct,#data	move immediate data to direct byte	3	2	75
MOV @Ri,A	move A to indirect RAM	1	1	F6, F7
MOV @Ri,direct	move direct byte to indirect RAM	2	2	A6, A7
MOV @Ri,#data	move immediate data to indirect RAM	2	1	76, 77
MOV DPTR,#data 16	load data pointer with a 16-bit constant	3	2	90
MOVC A,@A+DPTR	move code byte relative to DPTR to A	1	2	93
MOVC A,@A+PC	move code byte relative to PC to A	1	2	83
MOVX A,@Ri	move external RAM (8-bit address) to A	1	2	E2, E3
MOVX A,@DPTR	move external RAM (16-bit address) to A	1	2	E0
MOVX @Ri,A	move A to external RAM (8-bit address)	1	2	F2, F3
MOVX @DPTR,A	move A to external RAM (16-bit address)	1	2	F0
PUSH direct	push direct byte onto stack	2	2	C0
POP direct	pop direct byte from stack	2	2	D0
XCH A,Rr	exchange register with A	1	1	C*
XCH A,direct	exchange direct byte with A	2	1	C5
XCH A,@Ri	exchange indirect RAM with A	1	1	C6, C7
XCHD A,@Ri	exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

- MOV A,ACC is not permitted.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 39 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	clear carry flag	1	1	C3
CLR	bit	clear direct bit	2	1	C2
SETB	C	set carry flag	1	1	D3
SETB	bit	set direct bit	2	1	D2
CPL	C	complement carry flag	1	1	B3
CPL	bit	complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	move direct bit to carry flag	2	1	A2
MOV	bit,C	move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	absolute subroutine call	2	2	•1
LCALL	addr16	long subroutine call	3	2	12
RET		return from subroutine	1	2	22
RETI		return from interrupt	1	2	32
AJMP	addr11	absolute jump	2	2	♦1
LJMP	addr16	long jump	3	2	02
SJMP	rel	short jump (relative address)	2	2	80
JMP	@A+DPTR	jump indirect relative to the DPTR	1	2	73
JZ	rel	jump if A is zero	2	2	60
JNZ	rel	jump if A is not zero	2	2	70
JC	rel	jump if carry flag is set	2	2	40
JNC	rel	jump if carry flag is not set	2	2	50
JB	bit,rel	jump if direct bit is set	3	2	20
JNB	bit,rel	jump if direct bit is not set	3	2	30
JBC	bit,rel	jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	decrement direct and jump if not zero	3	2	D5
NOP		no operation	1	1	00

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

Table 40 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	working register R0-R7
direct	128 internal RAM locations and any special function register (SFR)
@Ri	indirect internal RAM location addressed by register R0 or R1 of the actual register bank
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR
addr16	16-bit destination address. Used by LCALL and LJMP; the branch will be anywhere within the 64 kbytes Program Memory address space
addr11	11-bit destination address. Used by ACALL and AJMP; the branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction
rel	signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps; range is -128 to +127 bytes relative to first byte of the following instruction
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F
•	1, 3, 5, 7, 9, B, D, F
♦	0, 2, 4, 6, 8, A, C, E

Low voltage 8-bit microcontrollers with
I²C-bus

P80CL410; P83CL410

Table 41 Instruction map
 First hexadecimal character of opcode ← Second hexadecimal character of opcode →

→	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri	0	0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri	0	0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri	0	0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri	0	0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri	0	0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri	0	0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri	0	0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data	0	0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri	0	0	1	2	3	4	5	6	7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri	0	0	1	2	3	4	5	6	7
A	ORL C,bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct	0	0	1	2	3	4	5	6	7
B	ANL C,bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel	0	0	1	2	3	4	5	6	7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri	0	0	1	2	3	4	5	6	7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri	0	0	1	2	3	4	5	6	7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri	MOVX A,@Ri	CLR A	MOV A,direct ⁽¹⁾	MOV A,@Ri	0	0	1	2	3	4	5	6	7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A	MOVX @Ri,A	CPL A	MOV direct,A	MOV @Ri,A	0	0	1	2	3	4	5	6	7

Note

- MOV A, ACC is not a valid instruction.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

19 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DD}	supply voltage	-0.5	+6.5	V
V _I	input voltage on any pin with respect to ground (V _{SS})	-0.5	V _{DD} + 0.5	V
I _I	DC current on any input	-5.0	+5.0	mA
I _O	DC current on any output	-5.0	+5.0	mA
P _{tot}	total power dissipation	-	300	mW
T _{stg}	storage temperature	-65	+150	°C
T _{amb}	operating ambient temperature	-40	+85	°C
T _j	operating junction temperature	-	+125	°C

20 DC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = -40 to +85 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DD}	supply voltage				
	operating	V _{SS} = 0 V	1.8	6.0	V
	RAM retention in Power-down mode		1.0	-	V
Operating supply current (note 1, note 2)					
I _{DD}	operating supply current	Oscillator 1; f _{clk} = 32 kHz; V _{DD} = 1.8 V; T _{amb} = 25 °C	-	50	µA
		Oscillator 2; f _{clk} = 3.58 MHz; V _{DD} = 3 V	-	2.5	mA
		Oscillator 2; f _{clk} = 10 MHz; V _{DD} = 5 V	-	14	mA
		Oscillator 3; f _{clk} = 12 MHz; V _{DD} = 5 V	-	16	mA
		Oscillator 4; f _{clk} = 12 MHz; V _{DD} = 5 V	-	20	mA
Supply current (Idle mode) (note 2, note 3)					
I _{DD(idle)}	supply current (Idle mode)	Oscillator 1; f _{clk} = 32 kHz; V _{DD} = 1.8 V; T _{amb} = 25 °C	-	25	µA
		Oscillator 2; f _{clk} = 3.58 MHz; V _{DD} = 3 V	-	1.0	mA
		Oscillator 2; f _{clk} = 10 MHz; V _{DD} = 5 V	-	5.0	mA
		Oscillator 3; f _{clk} = 12 MHz; V _{DD} = 5 V	-	7.0	mA
		Oscillator 4; f _{clk} = 12 MHz; V _{DD} = 5 V	-	8.5	mA

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

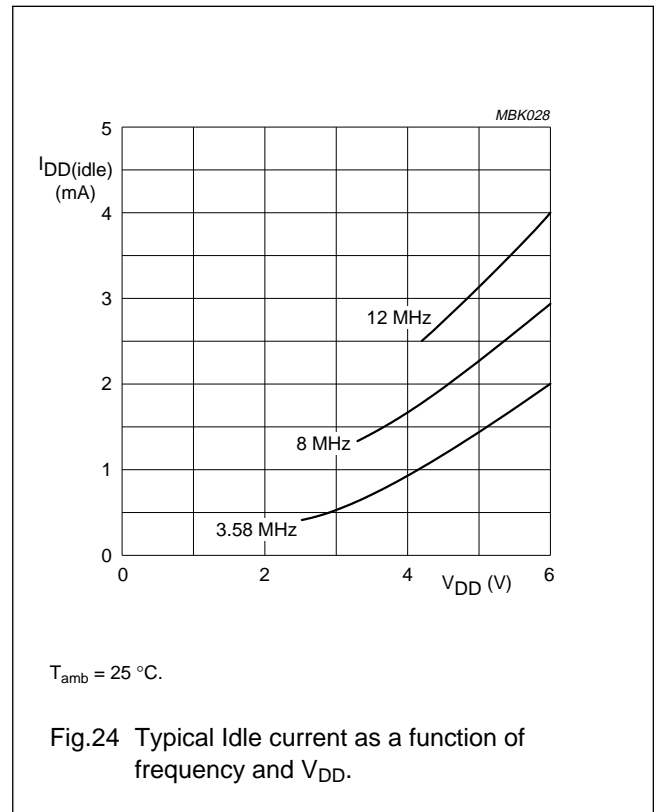
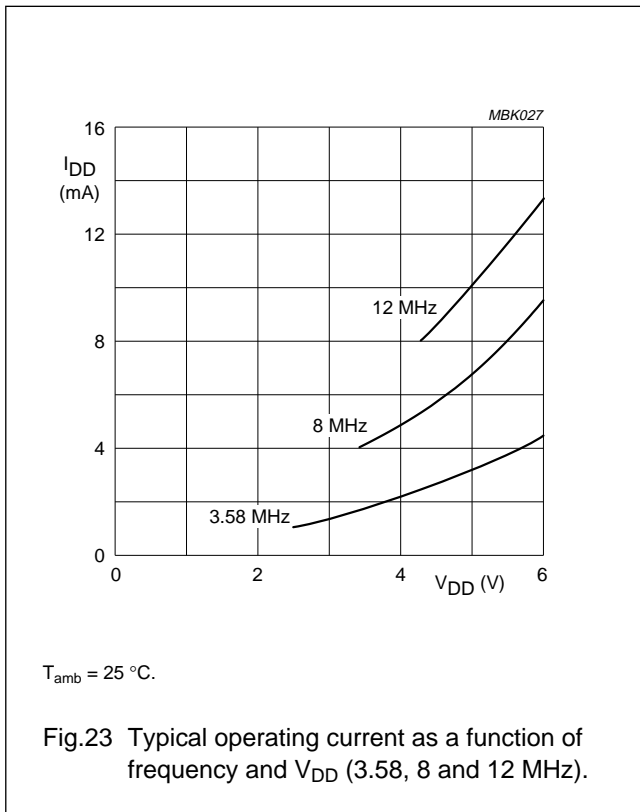
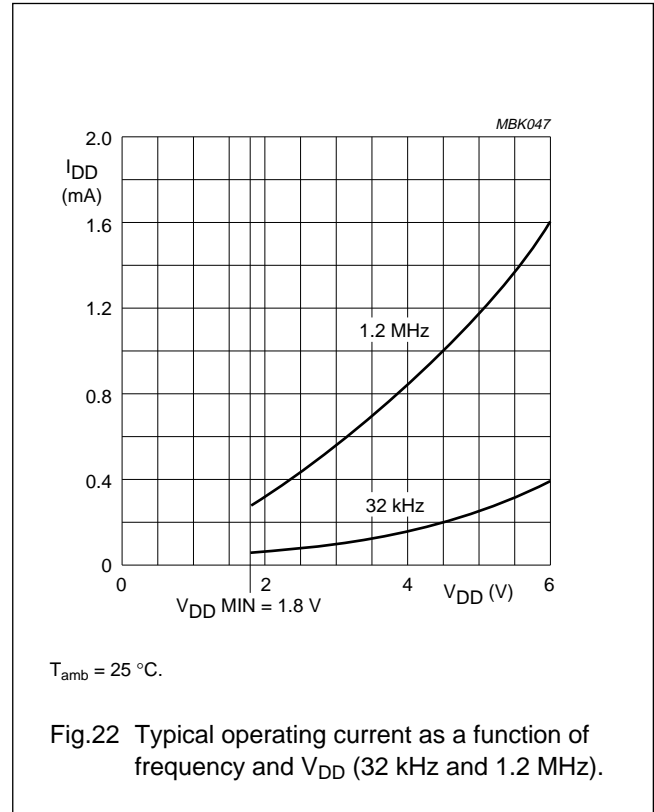
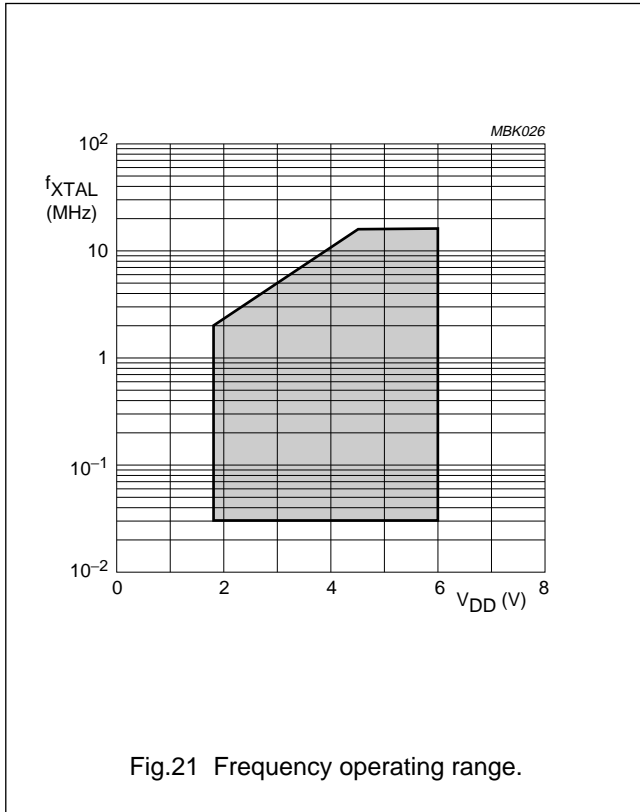
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply current (Power-down mode) (note 2, note 4)					
I _{DD(pd)}	supply current (Power-down mode)	V _{DD} = 1.8 V; T _{amb} = 25 °C	–	10	μA
Inputs					
V _{IL}	LOW level input voltage		V _{SS}	0.3V _{DD}	V
V _{IH}	HIGH level input voltage		0.7V _{DD}	V _{DD}	V
I _{IL}	input current logic 0 (port 1,2,3)	V _{DD} = 5 V; V _I = 0.4 V	–	–100	μA
		V _{DD} = 2.5 V; V _I = 0.4 V	–	–50	μA
I _{ITL}	input current logic 0, HIGH- to-LOW transition (port 1,2,3)	V _{DD} = 5 V; V _I = 0.5V _{DD}	–	–1.0	mA
		V _{DD} = 2.5 V; V _I = 0.5V _{DD}	–	–500	μA
I _{LI}	input leakage current (port 0, \overline{EA})	V _{SS} < V _I < V _{DD}	–	10	μA
Port outputs					
I _{OL}	LOW level output current (except SDA; SCL)	V _{DD} = 5 V; V _{OL} = 0.4 V	1.6	–	mA
		V _{DD} = 2.5 V; V _{OL} = 0.4 V	0.7	–	mA
I _{OL}	LOW level output current (SDA; SCL)	V _{DD} = 5 V; V _{OL} = 0.4 V	3.0	–	mA
I _{OH}	HIGH level output current (push-pull options)	V _{DD} = 5 V; V _{OH} = V _{DD} – 0.4 V	–1.6	–	mA
		V _{DD} = 2.5 V; V _{OH} = V _{DD} – 0.4 V	–0.7	–	mA
R _{RST}	RST pull-down resistor		10	200	kΩ

Notes

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with t_r = t_f = 10 ns; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL 2 not connected; \overline{EA} = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. Circuits with Power-on-reset option 'OFF' are tested at V_{DD(min)} = 1.8 V; within option 'ON' (typically 1.3 V) they are tested at V_{DD(min)} = 2.3 V. Please note, option 'ON' is only available on P83CL410.
3. The Idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with t_r = t_f = 10 ns; V_{IL} = V_{SS}. XTAL 2 not connected; \overline{EA} = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
4. The Power-down current is measured with all output pins disconnected; XTAL 1 not connected; \overline{EA} = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.

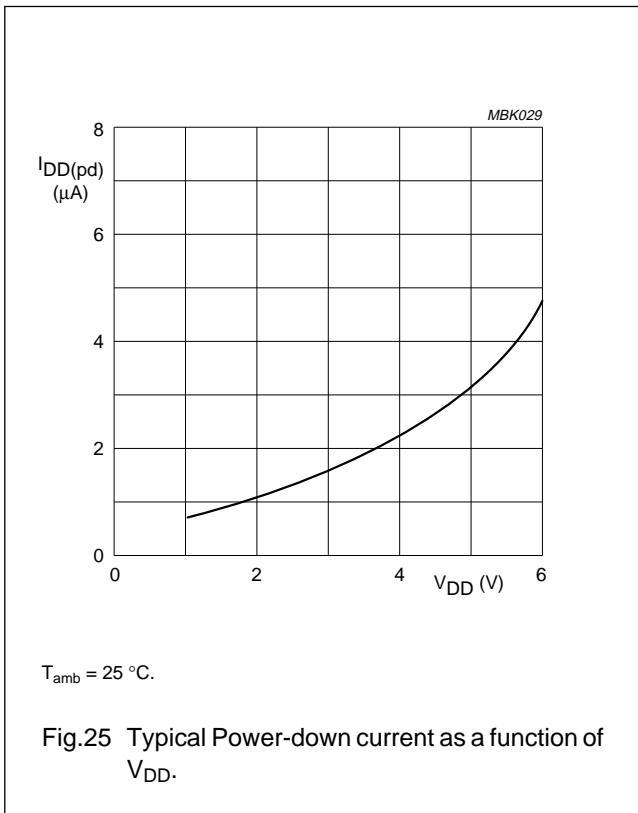
Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

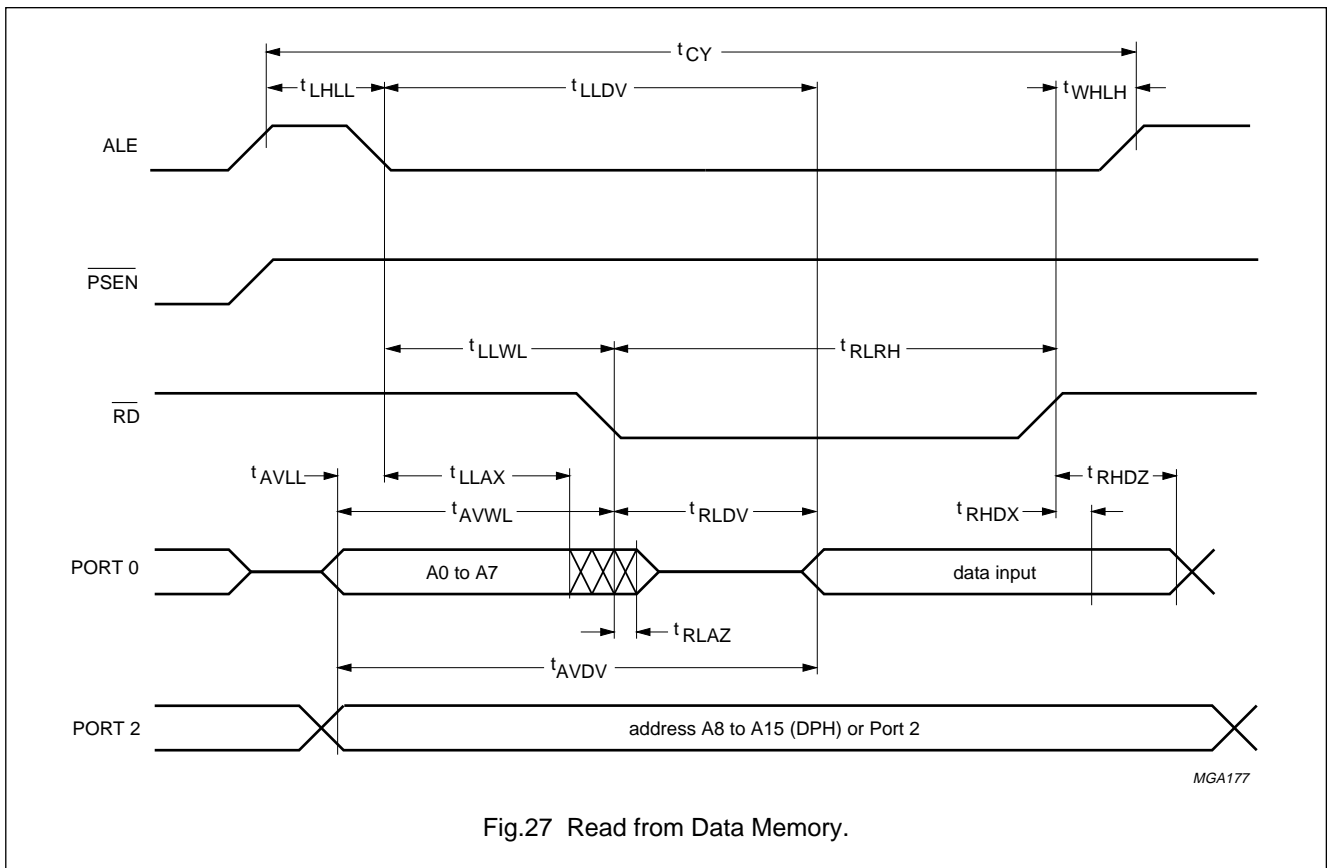
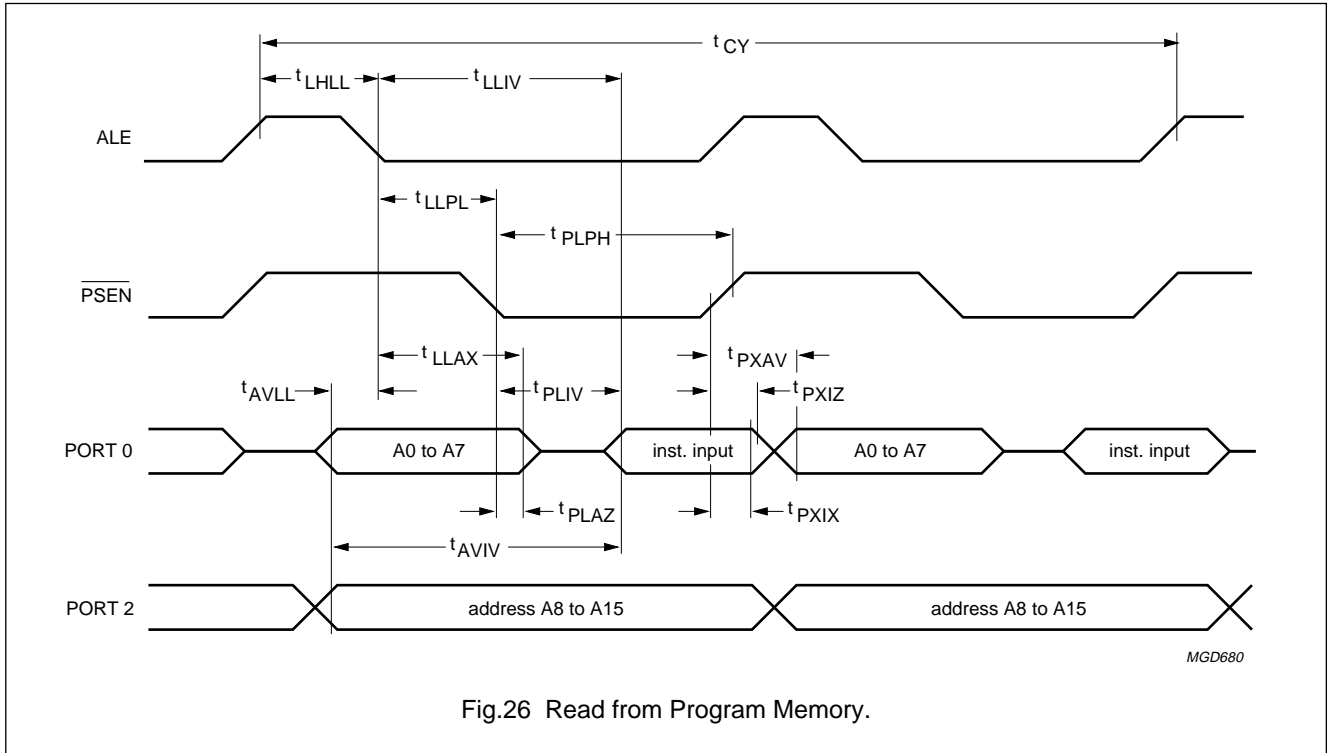
21 AC CHARACTERISTICS

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$ for Port 0, ALE and $\overline{\text{PSEN}}$; $C_L = 40\text{ pF}$ for all other outputs unless specified; $t_{CLK} = 1/f_{CLK}$.

SYMBOL	PARAMETER	$f_{osc} = 12\text{ MHz}$		$f_{osc} = \text{VARIABLE}$		UNIT
		MIN.	MAX.	MIN.	MAX.	
Program Memory (Fig.26)						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{\text{PSEN}}$ LOW	58	–	$t_{CLK} - 25$	–	ns
t_{PLPH}	$\overline{\text{PSEN}}$ pulse width	215	–	$3t_{CLK} - 35$	–	ns
t_{PLIV}	$\overline{\text{PSEN}}$ LOW to valid instruction in	–	125	–	$3t_{CLK} - 125$	ns
t_{PXIX}	input instruction hold after $\overline{\text{PSEN}}$	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{\text{PSEN}}$	–	63	–	$t_{CLK} - 20$	ns
t_{PXAV}	$\overline{\text{PSEN}}$ to address valid	75	–	$t_{CLK} - 8$	–	ns
t_{AVIV}	address to valid instruction in	–	302	–	$5t_{CLK} - 115$	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ LOW to address float	12	–	0	–	ns
External Data Memory (Figs 27 and 28)						
t_{RLRH}	$\overline{\text{RD}}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{\text{WR}}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{RLDV}	$\overline{\text{RD}}$ LOW to valid data in	–	150	–	$5t_{CLK} - 165$	ns
t_{RHDZ}	data float after $\overline{\text{RD}}$	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	517	–	$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ LOW	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ LOW	203	–	4	–	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ HIGH to ALE HIGH	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{\text{WR}}$ transition	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{\text{WR}}$ HIGH	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{\text{WR}}$	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{\text{RD}}$ LOW to address float	–	12	–	12	ns

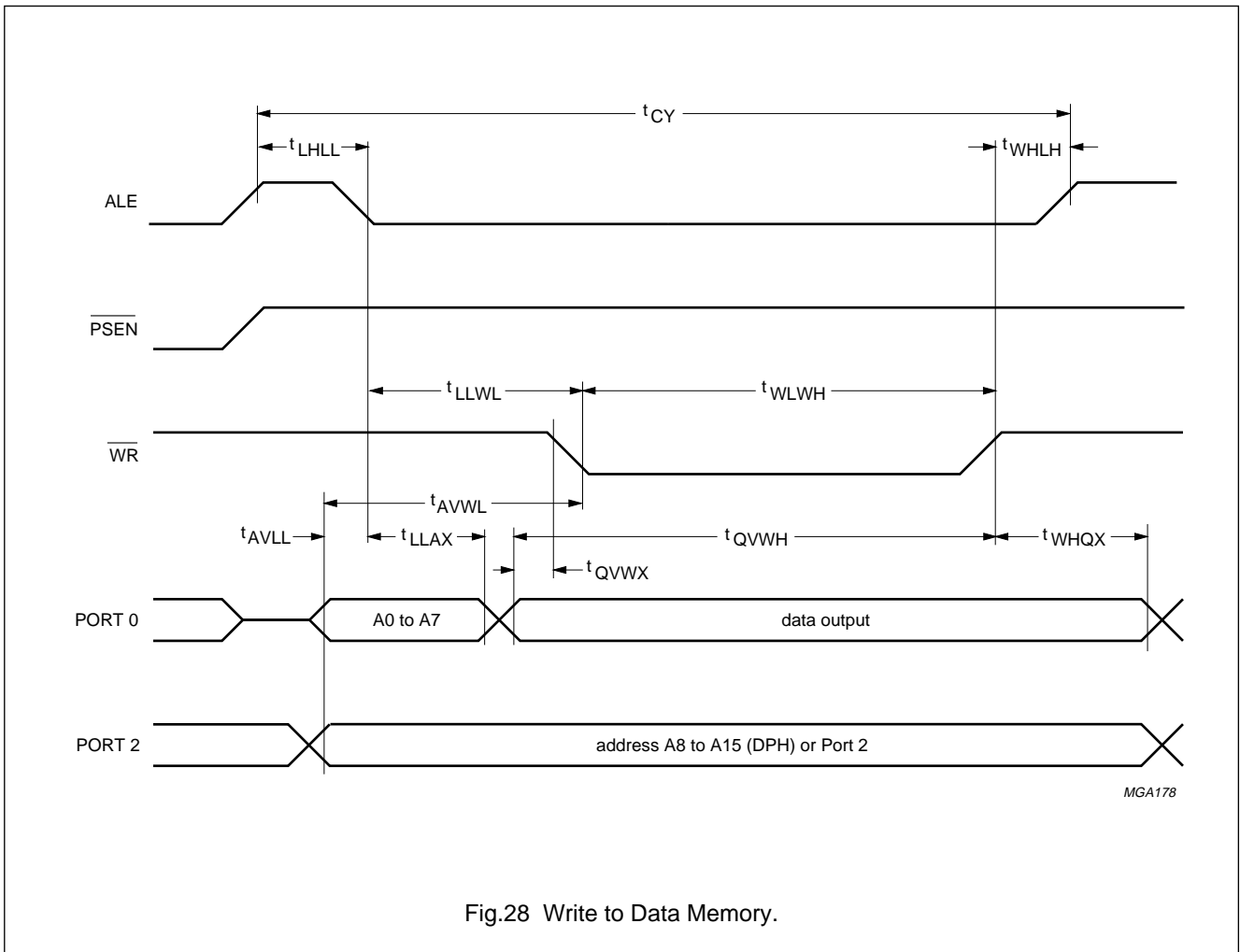
Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410



Low voltage 8-bit microcontrollers with I²C-bus

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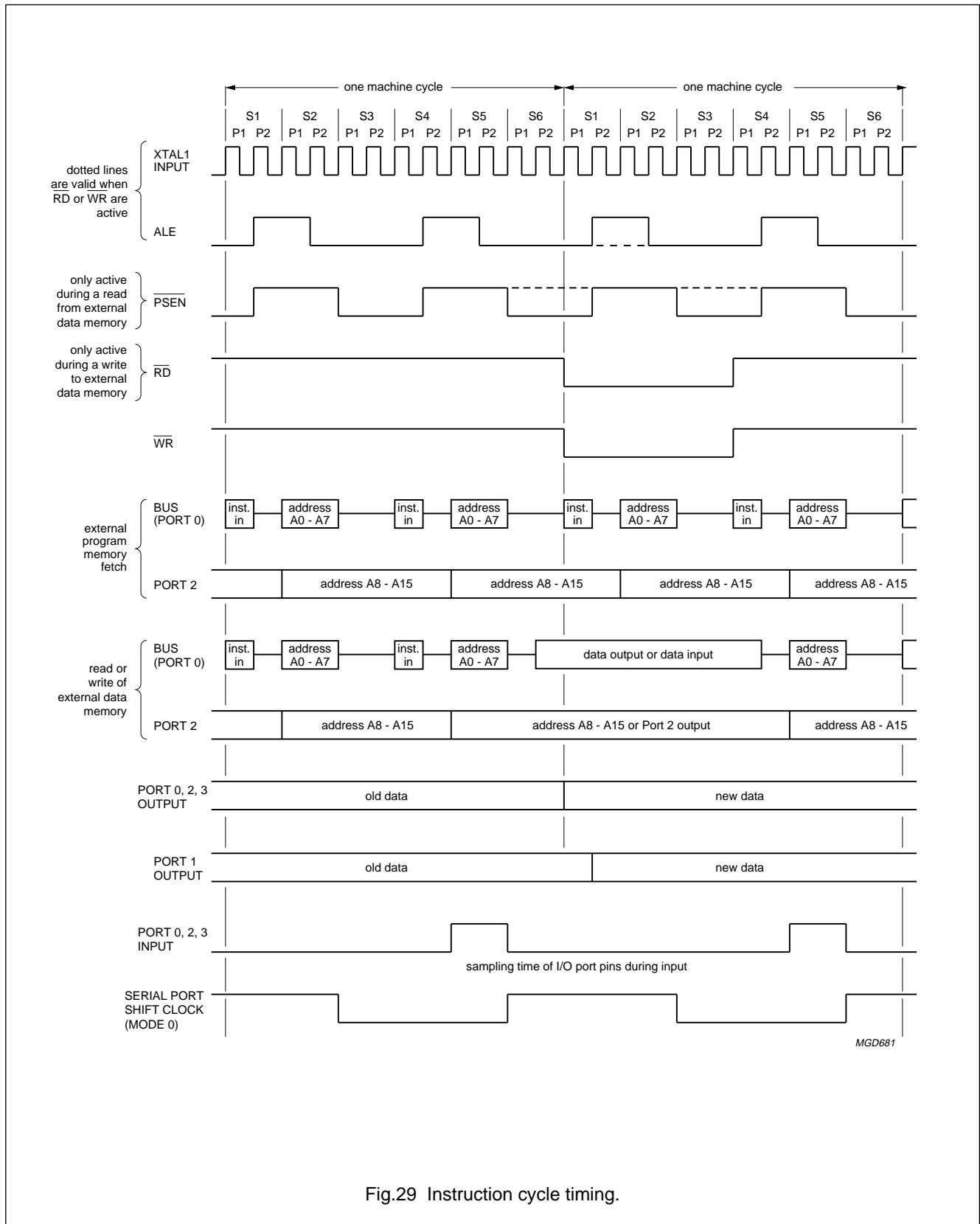


Fig.29 Instruction cycle timing.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

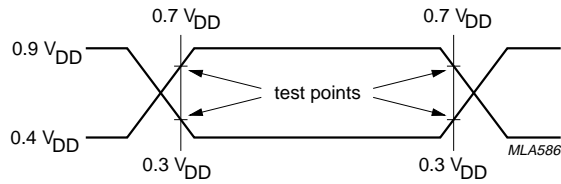


Fig.30 AC testing input waveform.

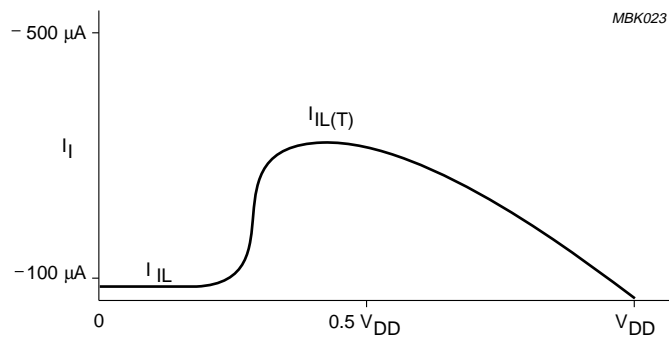


Fig.31 Input current.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

22 P85CL000HFZ 'PIGGY-BACK' SPECIFICATION

The differences between the masked version and the piggy-back are described below.

22.1 General description

The P85CL000HFZ is a piggy-back version with 256 bytes of RAM used for emulation of the P83CL410 and the P80CL51 microcontrollers. The P85CL000HFZ is manufactured in an advanced CMOS technology. The instruction set of the P85CL000HFZ is based on that of the 8051. The device has low power consumption and a wide supply voltage range. The P85CL000HFZ has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. For timing and AC/DC characteristics, please refer to the P83CL410 specifications.

22.2 Feature differences/additional features of P85CL000HFZ with respect to P83CL410

- No internal ROM
- 8-bit CPU, RAM, I/O in a single 40-lead package with DIP pin-out
- Socket for up to 16 kbytes external EPROM
- 256 bytes RAM, expandable externally to 64 kbytes
- UART interface
- On-chip oscillator: Oscillator 4 option only.

22.3 Common specification/feature differences between P85CL000HFZ and P83CL410/P80CL51

PARAMETER	P83CL410/P80CL51	P85CL000HFZ 'PIGGY-BACK'
RAM size	128	256
ROM size	4K	EPROM size dependent (max. 16K)
Port options	1, 2, 3	1
Oscillator options	Oscillator 1, 2, 3, 4, RC	Oscillator 4
Mechanical dimensions	standard dual in-line, small outline	same pin-out as SOT129-1, but larger package size
Current consumption	I _{DD}	I _{DD} (Oscillator 4) + I _{EPROM}
Voltage range	full	full, limited by EPROM
ESD	specification	not tested (different package)

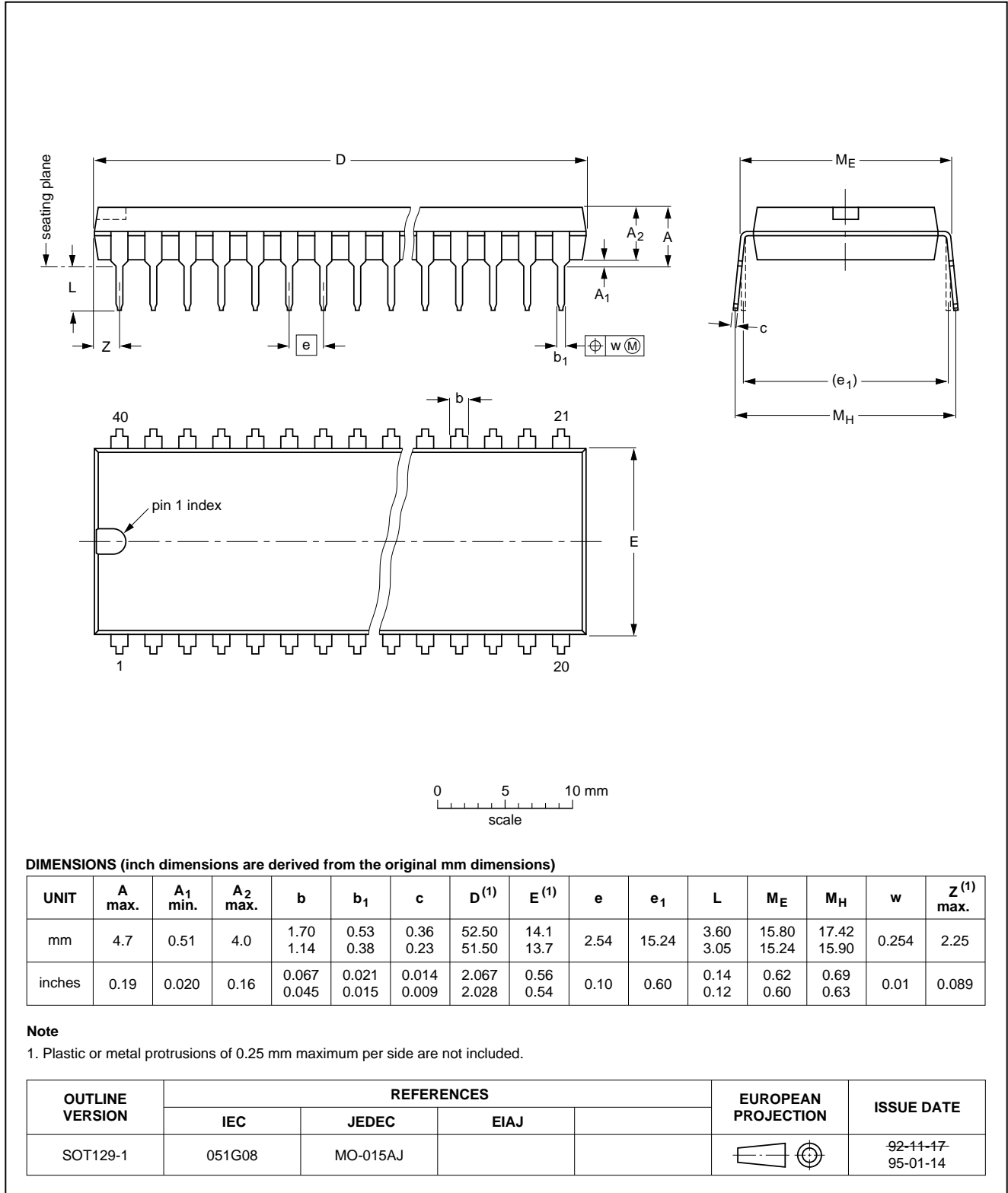
Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

23 PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1

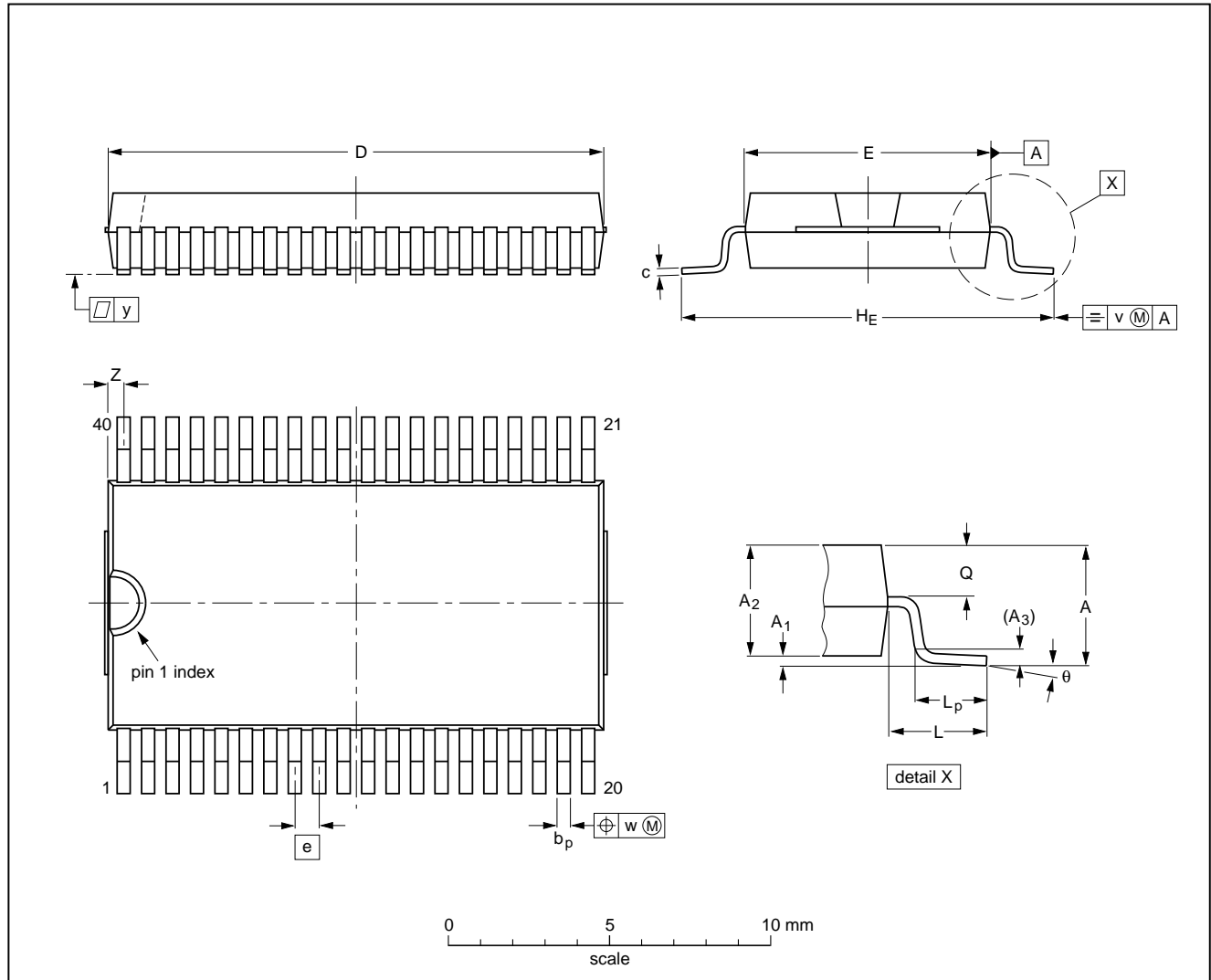


Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

VSO40: plastic very small outline package; 40 leads

SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

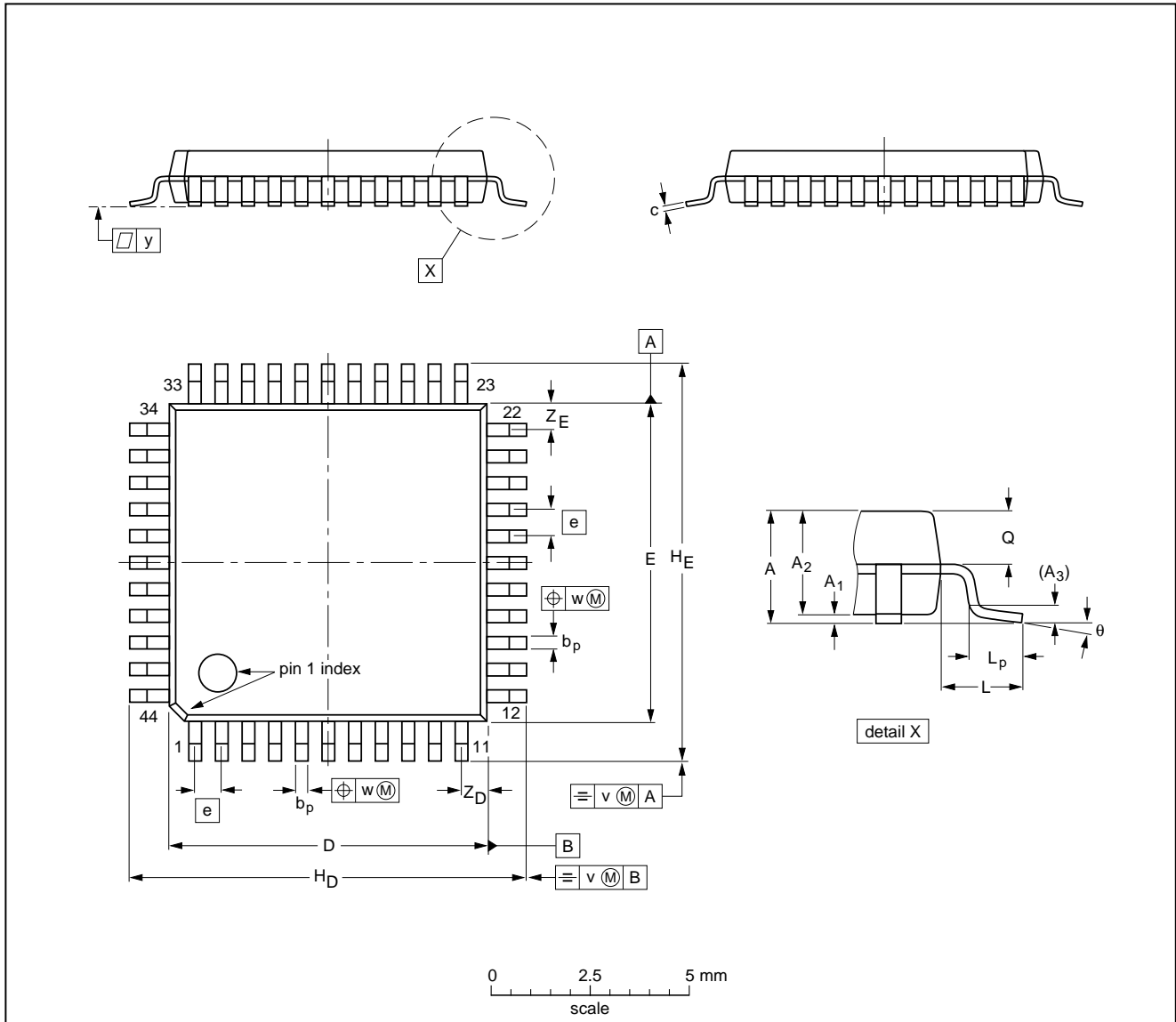
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT158-1					92-11-17 95-01-24

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	Q	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						92-11-17 95-02-04

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

24 SOLDERING

24.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

24.2 DIP

24.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

24.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

24.3 QFP

24.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our "Quality Reference Handbook" (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

24.3.2 WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

24.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

24.4 Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

24.5 Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

24.6 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Low voltage 8-bit microcontrollers with I²C-bus

P80CL410; P83CL410

25 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

26 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

27 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Low voltage 8-bit microcontrollers with
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P80CL410; P83CL410

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