



# ISP1102

## Advanced Universal Serial Bus transceiver

Rev. 05 — 11 December 2007

Product data sheet

## 1. General description

The ISP1102 Universal Serial Bus (USB) transceiver is fully compliant with *Universal Serial Bus Specification Rev. 2.0*. The ISP1102 can transmit and receive USB data at full-speed (12 Mbit/s).

The transceiver allows USB Application-Specific Integrated Circuits (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 V to 3.6 V to interface with the physical layer of the USB. The transceiver has an integrated 5 V-to-3.3 V voltage regulator for direct powering through USB supply line  $V_{BUS}$ . The transceiver has an integrated voltage detector to detect the presence of the  $V_{BUS}$  voltage ( $V_{CC(5V0)}$ ). When  $V_{CC(5V0)}$  or VREG3V3 is lost, the DP and DM pins can be shared with other serial protocols.

The transceiver is a bidirectional differential interface and is available in HBCC16 and HVQFN14 packages.

The transceiver is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, Personal Digital Assistants (PDAs) and Information Appliances (IAs).

## 2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports data transfer at full-speed (12 Mbit/s)
- Integrated 5 V-to-3.3 V voltage regulator to power through USB line  $V_{BUS}$
- $V_{BUS}$  voltage presence indication on pin VBUSDET
- VP and VM pins function in bidirectional mode, allowing pin count saving for the ASIC interface
- Used as USB device transceiver or USB host transceiver
- Stable RCV output during Single-Ended Zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports I/O voltage range from 1.65 V to 3.6 V
- $\pm 12$  kV ElectroStatic Discharge (ESD) protection (for the ISP1102W) at the DP, DM,  $V_{CC(5V0)}$  and GND pins
- Full industrial operating temperature range from  $-40$  °C to  $+85$  °C
- Available in HBCC16 and HVQFN14 lead-free and halogen-free packages

### 3. Applications

- Portable electronic devices, such as:
  - ◆ Mobile phone
  - ◆ Digital still camera
  - ◆ Personal Digital Assistant (PDA)
  - ◆ Information Appliance (IA)

### 4. Ordering information

Table 1. Ordering information

| Type number | Package |   | Version  |
|-------------|---------|---|----------|
|             | Name    | Description   |          |
| ISP1102W    | HBCC16  | plastic thermal enhanced bottom chip carrier; 16 terminals;<br>body 3 × 3 × 0.65 mm                       | SOT639-2 |
| ISP1102BS   | HVQFN14 | plastic thermal enhanced very thin quad flat package; no leads; 14 terminals;<br>body 2.5 × 2.5 × 0.85 mm | SOT773-1 |

### 5. Block diagram

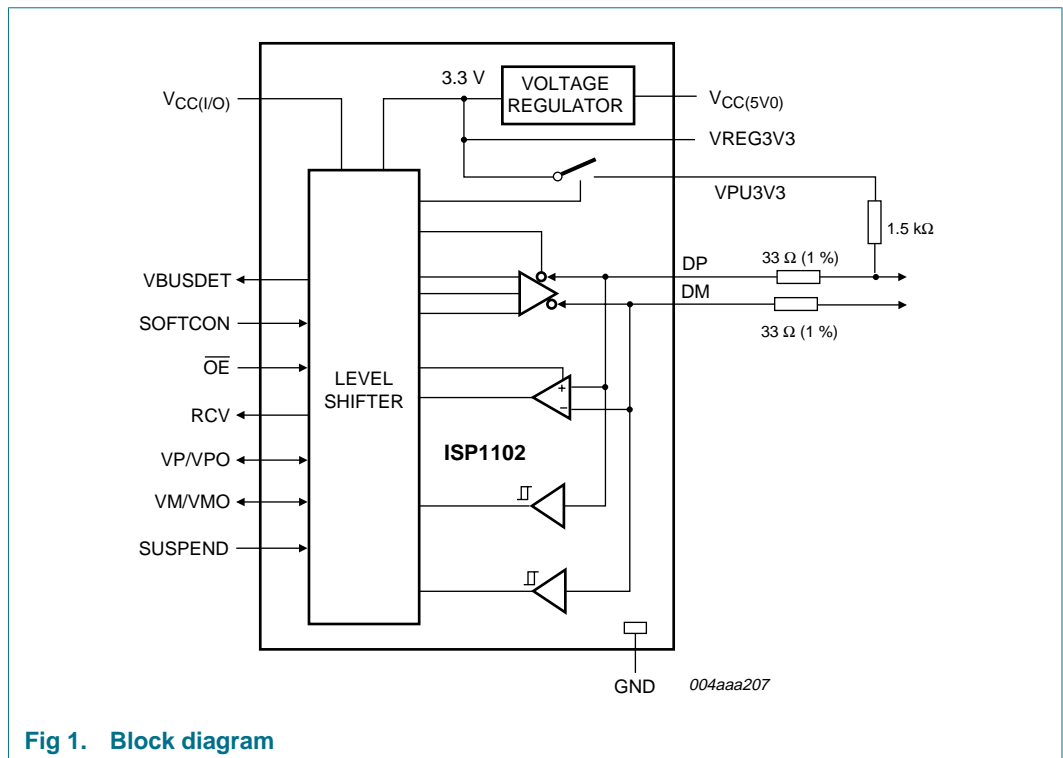


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning

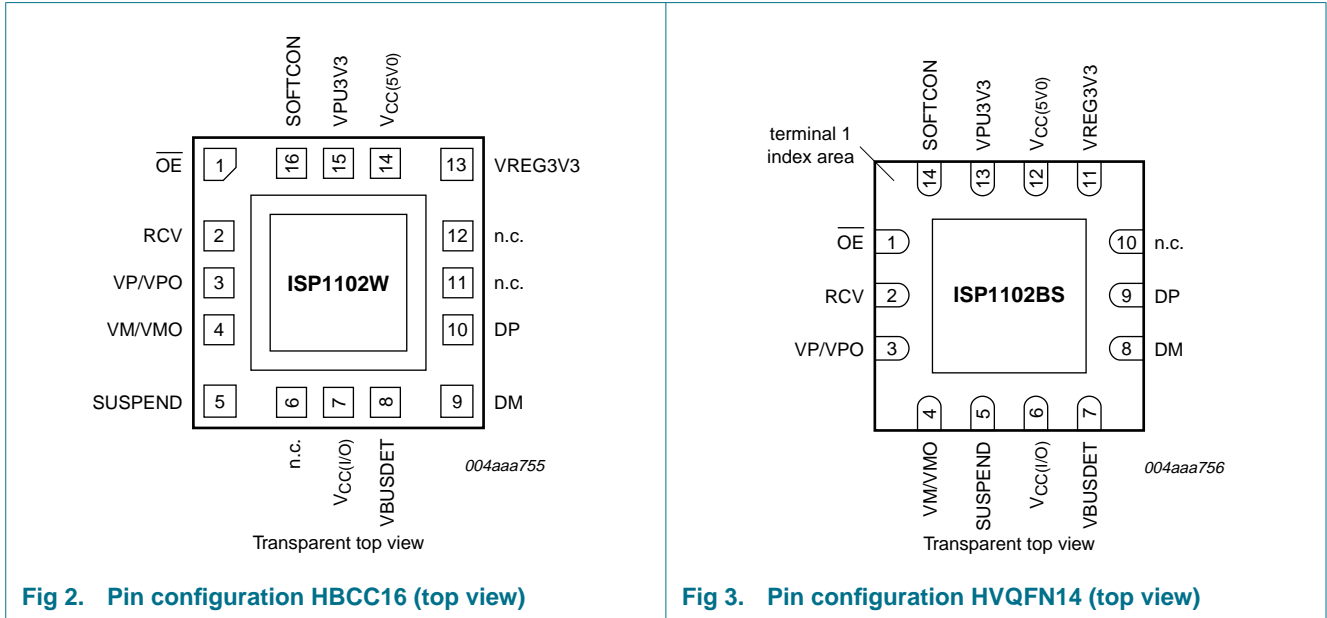


Fig 2. Pin configuration HBCC16 (top view)

Fig 3. Pin configuration HVQFN14 (top view)

### 6.2 Pin description

Table 2. Pin description

| Symbol <sup>[1]</sup> | Pin    |         | Type | Description   |
|-----------------------|--------|---------|------|---|
|                       | HBCC16 | HVQFN14 |      |   |
| OE                    | 1      | 1       | I    | input for output enable (CMOS level with respect to $V_{CC(I/O)}$ , active LOW); enables the transceiver to transmit data on the USB bus  |
| RCV                   | 2      | 2       | O    | input pad; push pull; CMOS<br>differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$ ); driven LOW when input SUSPEND is HIGH; the output state of RCV is preserved and stable during an SE0 condition   |
| VP/VPO                | 3      | 3       | I/O  | output pad; push pull; 4 mA output drive; CMOS<br>single-ended DP receiver output VP (CMOS level with respect to $V_{CC(I/O)}$ ); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VPO; see <a href="#">Table 3</a> and <a href="#">Table 4</a>                              |
| VM/VMO                | 4      | 4       | I/O  | bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS<br>single-ended DM receiver output VM (CMOS level with respect to $V_{CC(I/O)}$ ); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VMO; see <a href="#">Table 3</a> and <a href="#">Table 4</a> |
|                       |        |         |      | bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS   |

Table 2. Pin description ...continued

| Symbol <sup>[1]</sup> | Pin             |                 | Type | Description  |
|-----------------------|-----------------|-----------------|------|--|
|                       | HBCC16          | HVQFN14         |      |  |
| SUSPEND               | 5               | 5               | I    | suspend input (CMOS level with respect to $V_{CC(I/O)}$ ); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level<br>input pad; push pull; CMOS   |
| n.c.                  | 6               | -               | -    | not connected  |
| $V_{CC(I/O)}$         | 7               | 6               | -    | supply voltage for digital I/O pins (1.65 V to 3.6 V). When $V_{CC(I/O)}$ is not connected, the DP and DM pins are in 3-state. This supply pin is totally independent of $V_{CC(5V0)}$ and VREG3V3 and must never exceed the VREG3V3 voltage.  |
| VBUSDET               | 8               | 7               | O    | $V_{BUS}$ indicator output (CMOS level with respect to $V_{CC(I/O)}$ ); when $V_{BUS} > 4.1$ V, VBUSDET = HIGH and when $V_{BUS} < 3.6$ V, VBUSDET = LOW; when SUSPEND = HIGH, the VBUSDET function is invalid<br>output pad; push pull; 4 mA output drive; CMOS   |
| DM                    | 9               | 8               | AI/O | negative USB data bus connection (analog, differential)  |
| DP                    | 10              | 9               | AI/O | positive USB data bus connection (analog, differential)  |
| n.c.                  | 11              | -               | -    | not connected  |
| n.c.                  | 12              | -               | -    | not connected  |
| n.c.                  | -               | 10              | -    | not connected  |
| VREG3V3               | 13              | 11              | -    | <b>internal regulator option:</b> regulated supply voltage output (3.0 V to 3.6 V) during 5 V operation; a decoupling capacitor of at least 0.1 $\mu$ F is required<br><b>regulator bypass option:</b> used as a supply voltage input (3.3 V $\pm$ 10 %) for 3.3 V operation   |
| $V_{CC(5V0)}$         | 14              | 12              | -    | <b>internal regulator option:</b> supply voltage input (4.0 V to 5.5 V); can be directly connected to USB line $V_{BUS}$<br><b>regulator bypass option:</b> connect to VREG3V3   |
| VPU3V3                | 15              | 13              | -    | pull-up supply voltage (3.3 V $\pm$ 10 %); connect an external 1.5 k $\Omega$ resistor on DP (full-speed)<br>This pin function is controlled by the SOFTCON input:<br><b>SOFTCON = LOW</b> — VPU3V3 floating (high-Z); ensures zero pull-up current<br><b>SOFTCON = HIGH</b> — VPU3V3 = 3.3 V; internally connected to VREG3V3 |
| SOFTCON               | 16              | 14              | I    | software controlled USB connection input; a HIGH level applies 3.3 V to pin VPU3V3, which is connected to an external 1.5 k $\Omega$ pull-up resistor; this allows USB connect or disconnect signaling to be controlled by software<br>input pad; push pull; CMOS  |
| GND                   | exposed die pad | exposed die pad | -    | ground supply; down bonded to the exposed die pad (heat sink); to be connected to the PCB ground   |

[1] Symbol names with an overscore (for example,  $\overline{OE}$ ) indicate active LOW signals.

## 7. Functional description

### 7.1 Function selection

Table 3. Function selection

| SUSPEND | $\overline{OE}$ | DP, DM                   | RCV                     | VP/VPO    | VM/VMO    | Function  |
|---------|-----------------|--------------------------|-------------------------|-----------|-----------|---|
| LOW     | LOW             | driving or receiving     | active                  | VPO input | VMO input | normal driving (differential receiver active)           |
| LOW     | HIGH            | receiving <sup>[1]</sup> | active                  | VP output | VM output | receiving   |
| HIGH    | LOW             | driving                  | inactive <sup>[2]</sup> | VPO input | VMO input | driving during suspend (differential receiver inactive) |
| HIGH    | HIGH            | high-Z <sup>[1]</sup>    | inactive <sup>[2]</sup> | VP output | VM output | low-power state   |

[1] Signal levels on the DP and DM pins are determined by other USB devices and external pull-up or pull-down resistors.

[2] In suspend mode (SUSPEND = HIGH), the differential receiver is inactive and output RCV is always LOW. The resume signaling is detected through single-ended receivers VP/VPO and VM/VMO.

### 7.2 Operating functions

Table 4. Driving function using differential input data interface (pin  $\overline{OE}$  = LOW)

| VM/VMO | VP/VPO | Data                 |
|--------|--------|----------------------|
| LOW    | LOW    | SE0                  |
| LOW    | HIGH   | differential logic 1 |
| HIGH   | LOW    | differential logic 0 |
| HIGH   | HIGH   | illegal state        |

Table 5. Receiving function (pin  $\overline{OE}$  = HIGH)

| DP, DM               | RCV                 | VP/VPO | VM/VMO |
|----------------------|---------------------|--------|--------|
| Differential logic 0 | LOW                 | LOW    | HIGH   |
| Differential logic 1 | HIGH                | HIGH   | LOW    |
| SE0                  | RCV* <sup>[1]</sup> | LOW    | LOW    |

[1] RCV\* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

### 7.3 Power supply configurations

The ISP1102 can be used with various power supply configurations, which can be changed dynamically. [Table 7](#) provides an overview of power supply configurations.

**Normal mode** —  $V_{CC(I/O)}$  is connected.  $V_{CC(5V0)}$  is connected only, or  $V_{CC(5V0)}$  and VREG3V3 are connected.

For the 5 V operation,  $V_{CC(5V0)}$  is connected to a 5 V source (4.0 V to 5.5 V). The internal voltage regulator then produces 3.3 V for USB connections.

For the 3.3 V operation, both  $V_{CC(5V0)}$  and VREG3V3 are connected to a 3.3 V source (3.0 V to 3.6 V).

$V_{CC(I/O)}$  is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.

**Sharing mode** —  $V_{CC(I/O)}$  is connected only,  $V_{CC(5V0)}$  is  $< 3.6$  V and  $V_{REG3V3}$  is  $< 2.4$  V. In this mode, the DP and DM pins are 3-stated and the ISP1102 allows external signals of up to 3.6 V to share the DP and DM lines. The internal circuits of the ISP1102 ensure that virtually no current (maximum 10  $\mu$ A) is drawn through the DP and DM lines. The power consumption through pin  $V_{CC(I/O)}$  drops to the low-power (suspended) state level.

Pins  $V_{BUSDET}$  and  $RCV$  are driven to LOW to indicate this mode. The  $V_{BUSDET}$  function is ignored during suspend mode of the ISP1102.

Some hysteresis is built into the detection of  $V_{REG3V3}$  lost.

**Table 6. Pin states in sharing mode**

| Pin                                | Sharing mode          |
|------------------------------------|-----------------------|
| $V_{CC(5V0)}$                      | $< 3.6$ V             |
| $V_{REG3V3}$                       | $< 2.4$ V             |
| $V_{CC(I/O)}$                      | 1.65 V to 3.6 V input |
| $V_{PU3V3}$                        | high-Z (off)          |
| DP, DM                             | high-Z                |
| VP/VPO, VM/VMO <sup>[1]</sup>      | high-Z                |
| $RCV$                              | LOW                   |
| $V_{BUSDET}$                       | LOW                   |
| $\overline{OE}$ , SUSPEND, SOFTCON | high-Z                |

[1] VP/VPO and VM/VMO are bidirectional pins.

**Table 7. Power supply configuration overview**

| $V_{CC(5V0)}$ | Configuration | Special characteristics                                   |
|---------------|---------------|---|
| Connected     | normal mode   | -   |
| $< 3.6$ V     | sharing mode  | DP, DM and $V_{PU3V3}$ high-Z; $V_{BUSDET}$ is driven LOW |

## 7.4 Power supply input options

The ISP1102 has two power supply input options.

**Internal regulator** — Pin  $V_{CC(5V0)}$  is connected to 4.0 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). The VREG3V3 pin becomes a 3.3 V output reference.

**Regulator bypass** — Pins  $V_{CC(5V0)}$  and VREG3V3 are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from pin VREG3V3. The voltage range is 3.0 V to 3.6 V to comply with *Universal Serial Bus Specification Rev. 2.0*.

The supply voltage range for each input option is specified in [Table 8](#).

**Table 8. Power supply input options**

| Input option       | $V_{CC(5V0)}$  | VREG3V3                                       | $V_{CC(I/O)}$                                       |
|--------------------|--|---|---|
| Internal regulator | supply input for internal regulator (4.0 V to 5.5 V)                     | voltage reference output (3.3 V, 300 $\mu$ A) | supply input for digital I/O pins (1.65 V to 3.6 V) |
| Regulator bypass   | connected to VREG3V3 with maximum voltage drop of 0.3 V (2.7 V to 3.6 V) | supply input (3.0 V to 3.6 V)                 | supply input for digital I/O pins (1.65 V to 3.6 V) |

## 8. ElectroStatic Discharge (ESD)

### 8.1 ESD protection

For the HBCC package, the pins that are connected to the USB connector (DP, DM,  $V_{CC(5V0)}$  and GND) have a minimum of  $\pm 12$  kV ESD protection. The  $\pm 12$  kV measurement is limited by the test equipment. Capacitors of  $4.7 \mu\text{F}$  connected from VREG3V3 to GND and  $V_{CC(5V0)}$  to GND are required to achieve this  $\pm 12$  kV ESD protection (see [Figure 4](#)).

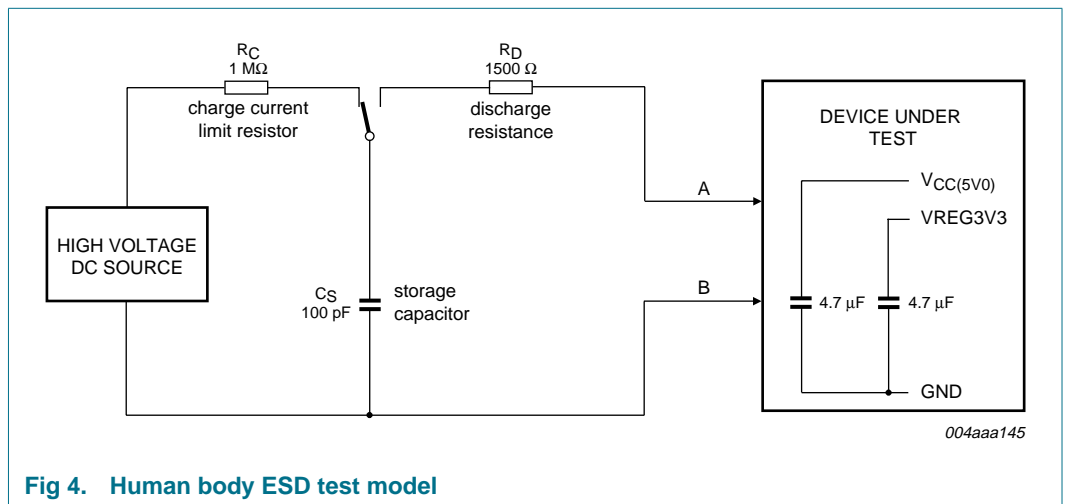


Fig 4. Human body ESD test model

**Remark:** For the HVQFN package, the pins that are connected to the USB connector (DP, DM,  $V_{CC(5V0)}$  and GND) have a minimum of  $\pm 7$  kV ESD protection.

### 8.2 ESD test conditions

A detailed report on test set up and results is available on request.



## 9. Limiting values

**Table 9. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol        | Parameter                       | Conditions  | Min    | Max                 | Unit         |   |
|---------------|---------------------------------|---|--------|---------------------|--------------|---|
| $V_{CC(5V0)}$ | supply voltage (5.0 V)          |   | -0.5   | +6.0                | V            |   |
| $V_{CC(I/O)}$ | input/output supply voltage     |   | -0.5   | +4.6                | V            |   |
| $V_I$         | input voltage                   |   | -0.5   | $V_{CC(I/O)} + 0.5$ | V            |   |
| $I_{lu}$      | latch-up current                | $V_I = -1.8$ V to +5.4 V  | -      | 100                 | mA           |   |
| $V_{esd}$     | electrostatic discharge voltage | pins DP, DM, $V_{CC(5V0)}$ and GND;<br>$I_{LI} < 3$ $\mu$ A for HBCC package  | [1][2] | -12000              | +12000       | V |
|               |                                 | pins DP, DM, $V_{CC(5V0)}$ and GND;<br>$I_{LI} < 3$ $\mu$ A for HVQFN package | [2]    | -7000               | +7000        | V |
|               |                                 | all other pins; $I_{LI} < 1$ $\mu$ A  | [2]    | -2000               | +2000        | V |
| $T_{stg}$     | storage temperature             |   | -40    | +125                | $^{\circ}$ C |   |

[1] Testing equipment limits measurement to only  $\pm 12$  kV. Capacitors needed on  $V_{CC(5V0)}$  and VREG3V3 (see [Section 8](#)).

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  resistor (Human Body Model).

## 10. Recommended operating conditions

**Table 10. Recommended operating conditions**

| Symbol        | Parameter                        | Conditions        | Min  | Typ | Max           | Unit         |
|---------------|----------------------------------|-------------------|------|-----|---------------|--------------|
| $V_{CC(5V0)}$ | supply voltage (5.0 V)           |                   | 4.0  | 5.0 | 5.5           | V            |
| $V_{CC(I/O)}$ | input/output supply voltage      |                   | 1.65 | -   | 3.6           | V            |
| $V_I$         | input voltage                    |                   | 0    | -   | $V_{CC(I/O)}$ | V            |
| $V_{IA(I/O)}$ | input voltage on analog I/O pins | on pins DP and DM | 0    | -   | 3.6           | V            |
| $T_j$         | junction temperature             |                   | -40  | -   | +125          | $^{\circ}$ C |
| $T_{amb}$     | ambient temperature              |                   | -40  | -   | +85           | $^{\circ}$ C |

## 11. Static characteristics

**Table 11. Static characteristics: supply pins**

$V_{CC(5V0)} = 4.0$  V to 5.5 V or  $V_{(VREG3V3)} = 3.0$  V to 3.6 V;  $V_{CC(I/O)} = 1.65$  V to 3.6 V;  $V_{GND} = 0$  V; see [Table 8](#) for valid voltage level combinations;  $T_{amb} = -40$   $^{\circ}$ C to +85  $^{\circ}$ C; unless otherwise specified.

| Symbol              | Parameter                                     | Conditions   | Min    | Typ | Max | Unit    |         |
|---------------------|---|--|--------|-----|-----|---------|---------|
| $V_{(VREG3V3)}$     | voltage on pin VREG3V3                        | internal regulator option;<br>$I_{load} \leq 300$ $\mu$ A                            | [1][2] | 3.0 | 3.3 | 3.6     | V       |
| $I_{CC}$            | supply current                                | transmitting and receiving at<br>12 Mbit/s; $C_L = 50$ pF on<br>pins DP and DM       | [3]    | -   | 4   | 8       | mA      |
| $I_{CC(I/O)}$       | supply current on pin $V_{CC(I/O)}$           | transmitting and receiving at<br>12 Mbit/s   | [3]    | -   | 1   | 2       | mA      |
| $I_{CC(idle)}$      | idle and SE0 supply current                   | idle: $V_{DP} > 2.7$ V, $V_{DM} < 0.3$ V;<br>SE0: $V_{DP} < 0.3$ V, $V_{DM} < 0.3$ V | [4]    | -   | -   | 300     | $\mu$ A |
| $I_{CC(I/O)(stat)}$ | static supply current on<br>pin $V_{CC(I/O)}$ | idle, SE0 or suspend   | -      | -   | 20  | $\mu$ A |         |

**Table 11. Static characteristics: supply pins ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{(VREG3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 8](#) for valid voltage level combinations;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                 | Parameter   | Conditions   | Min     | Typ  | Max | Unit          |
|------------------------|---|--|---------|------|-----|---------------|
| $I_{CC(susp)}$         | suspend supply current                                | SUSPEND = HIGH   | [4] -   | -    | 20  | $\mu\text{A}$ |
| $I_{CC(I/O)(sharing)}$ | sharing mode supply current on pin $V_{CC(I/O)}$      | $V_{CC(5V0)} < 3.6\text{ V}$   | -       | -    | 20  | $\mu\text{A}$ |
| $I_{load(sharing)DM}$  | sharing mode load current on pin DM                   | $V_{CC(5V0)} < 3.6\text{ V}$ ; SOFTCON = LOW; $V_{DM} = 3.6\text{ V}$  | -       | -    | 10  | $\mu\text{A}$ |
| $I_{load(sharing)DP}$  | sharing mode load current on pin DP                   | $V_{CC(5V0)} < 3.6\text{ V}$ ; SOFTCON = LOW; $V_{DP} = 3.6\text{ V}$  | -       | -    | 10  | $\mu\text{A}$ |
| $V_{CC(5V0)th}$        | supply voltage detection threshold (5.0 V)            | $1.65\text{ V} \leq V_{CC(I/O)} \leq 3.6\text{ V}$   |         |      |     |               |
|                        |   | supply lost  | -       | -    | 3.6 | V             |
|                        |   | supply present   | 4.1     | -    | -   | V             |
| $V_{CC(5V0)hys}$       | supply voltage detection hysteresis (5.0 V)           | $V_{CC(I/O)} = 1.8\text{ V}$   | -       | 70   | -   | mV            |
| $V_{CC(I/O)th}$        | supply voltage detection threshold (I/O)              | $V_{(VREG3V3)} = 2.7\text{ V to }3.6\text{ V}$   |         |      |     |               |
|                        |   | supply lost  | -       | -    | 0.5 | V             |
|                        |   | supply present   | 1.4     | -    | -   | V             |
| $V_{CC(I/O)(hys)}$     | supply voltage detection hysteresis (I/O)             | $V_{(VREG3V3)} = 3.3\text{ V}$   | -       | 0.45 | -   | V             |
| $V_{REG(3V3)th}$       | regulated supply voltage detection threshold (3.3 V)  | $1.65\text{ V} \leq V_{CC(I/O)} \leq V_{(VREG3V3)}$ ;<br>$2.7\text{ V} \leq V_{(VREG3V3)} \leq 3.6\text{ V}$ |         |      |     |               |
|                        |   | supply lost  | -       | -    | 0.8 | V             |
|                        |   | supply present   | [5] 2.4 | -    | -   | V             |
| $V_{REG(3V3)hys}$      | regulated supply voltage detection hysteresis (3.3 V) | $V_{CC(I/O)} = 1.8\text{ V}$   | -       | 0.45 | -   | V             |

[1]  $I_{load}$  includes the pull-up resistor current through pin VPU3V3.

[2] The minimum voltage is 2.7 V in suspend mode.

[3] Maximum value characterized only, not tested in production.

[4] Excluding any load current and VPU3V3 or  $V_{SW}$  source current to the 1.5 k $\Omega$  and 15 k $\Omega$  pull-up and pull-down resistors (200  $\mu\text{A}$  typ.).

[5] When  $V_{CC(I/O)} < 2.7\text{ V}$ , the minimum value for  $V_{REG(3V3)th} = 2.0\text{ V}$  for supply present condition.

**Table 12. Static characteristics: digital pins**

$V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol  | Parameter                 | Conditions                        | Min                  | Typ | Max              | Unit |
|---|---------------------------|-----------------------------------|----------------------|-----|------------------|------|
| <b><math>V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}</math></b> |                           |                                   |                      |     |                  |      |
| <b>Input levels</b>   |                           |                                   |                      |     |                  |      |
| $V_{IL}$  | LOW-level input voltage   |                                   | -                    | -   | $0.3V_{CC(I/O)}$ | V    |
| $V_{IH}$  | HIGH-level input voltage  |                                   | $0.6V_{CC(I/O)}$     | -   | -                | V    |
| <b>Output levels</b>  |                           |                                   |                      |     |                  |      |
| $V_{OL}$  | LOW-level output voltage  | $I_{OL} = 100\text{ }\mu\text{A}$ | -                    | -   | 0.15             | V    |
|   |                           | $I_{OL} = 2\text{ mA}$            | -                    | -   | 0.4              | V    |
| $V_{OH}$  | HIGH-level output voltage | $I_{OH} = 100\text{ }\mu\text{A}$ | $V_{CC(I/O)} - 0.15$ | -   | -                | V    |
|   |                           | $I_{OH} = 2\text{ mA}$            | $V_{CC(I/O)} - 0.4$  | -   | -                | V    |

**Table 12. Static characteristics: digital pins ...continued** $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol  | Parameter                 | Conditions                  | Min    | Typ | Max  | Unit          |
|---|---------------------------|-----------------------------|--------|-----|------|---------------|
| <b>Leakage current</b>  |                           |                             |        |     |      |               |
| $I_{LI}$  | input leakage current     |                             | [1] -1 | -   | +1   | $\mu\text{A}$ |
| <b>Capacitance</b>  |                           |                             |        |     |      |               |
| $C_{in}$  | input capacitance         | pin to GND                  | -      | -   | 10   | pF            |
| <b>Example 1: <math>V_{CC(I/O)} = 1.8\text{ V} \pm 0.15\text{ V}</math></b> |                           |                             |        |     |      |               |
| <b>Input levels</b>   |                           |                             |        |     |      |               |
| $V_{IL}$  | LOW-level input voltage   |                             | -      | -   | 0.5  | V             |
| $V_{IH}$  | HIGH-level input voltage  |                             | 1.2    | -   | -    | V             |
| <b>Output levels</b>  |                           |                             |        |     |      |               |
| $V_{OL}$  | LOW-level output voltage  | $I_{OL} = 100\ \mu\text{A}$ | -      | -   | 0.15 | V             |
|   |                           | $I_{OL} = 2\ \text{mA}$     | -      | -   | 0.4  | V             |
| $V_{OH}$  | HIGH-level output voltage | $I_{OH} = 100\ \mu\text{A}$ | 1.5    | -   | -    | V             |
|   |                           | $I_{OH} = 2\ \text{mA}$     | 1.25   | -   | -    | V             |
| <b>Example 2: <math>V_{CC(I/O)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>  |                           |                             |        |     |      |               |
| <b>Input levels</b>   |                           |                             |        |     |      |               |
| $V_{IL}$  | LOW-level input voltage   |                             | -      | -   | 0.7  | V             |
| $V_{IH}$  | HIGH-level input voltage  |                             | 1.7    | -   | -    | V             |
| <b>Output levels</b>  |                           |                             |        |     |      |               |
| $V_{OL}$  | LOW-level output voltage  | $I_{OL} = 100\ \mu\text{A}$ | -      | -   | 0.15 | V             |
|   |                           | $I_{OL} = 2\ \text{mA}$     | -      | -   | 0.4  | V             |
| $V_{OH}$  | HIGH-level output voltage | $I_{OH} = 100\ \mu\text{A}$ | 2.15   | -   | -    | V             |
|   |                           | $I_{OH} = 2\ \text{mA}$     | 1.9    | -   | -    | V             |
| <b>Example 3: <math>V_{CC(I/O)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>  |                           |                             |        |     |      |               |
| <b>Input levels</b>   |                           |                             |        |     |      |               |
| $V_{IL}$  | LOW-level input voltage   |                             | -      | -   | 0.9  | V             |
| $V_{IH}$  | HIGH-level input voltage  |                             | 2.15   | -   | -    | V             |
| <b>Output levels</b>  |                           |                             |        |     |      |               |
| $V_{OL}$  | LOW-level output voltage  | $I_{OL} = 100\ \mu\text{A}$ | -      | -   | 0.15 | V             |
|   |                           | $I_{OL} = 2\ \text{mA}$     | -      | -   | 0.4  | V             |
| $V_{OH}$  | HIGH-level output voltage | $I_{OH} = 100\ \mu\text{A}$ | 2.85   | -   | -    | V             |
|   |                           | $I_{OH} = 2\ \text{mA}$     | 2.6    | -   | -    | V             |

[1] If  $V_{CC(I/O)} \geq V_{(VREG3V3)}$ , then the leakage current will be higher than the specified value.**Table 13. Static characteristics: analog I/O pins DP and DM** $V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{(VREG3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                       | Parameter                      | Conditions                | Min | Typ | Max | Unit |
|------------------------------|--------------------------------|---------------------------|-----|-----|-----|------|
| <b>Input levels</b>          |                                |                           |     |     |     |      |
| <b>Differential receiver</b> |                                |                           |     |     |     |      |
| $V_{DI}$                     | differential input sensitivity | $ V_{I(DP)} - V_{I(DM)} $ | 0.2 | -   | -   | V    |

**Table 13. Static characteristics: analog I/O pins DP and DM ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{(VREG3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                       | Parameter                          | Conditions  | Min        | Typ | Max | Unit          |
|------------------------------|------------------------------------|---|------------|-----|-----|---------------|
| $V_{CM}$                     | differential common mode voltage   | includes $V_{DI}$ range                           | 0.8        | -   | 2.5 | V             |
| <b>Single-ended receiver</b> |                                    |   |            |     |     |               |
| $V_{IL}$                     | LOW-level input voltage            |   | -          | -   | 0.8 | V             |
| $V_{IH}$                     | HIGH-level input voltage           |   | 2.0        | -   | -   | V             |
| $V_{hys}$                    | hysteresis voltage                 |   | 0.4        | -   | 0.7 | V             |
| <b>Output levels</b>         |                                    |   |            |     |     |               |
| $V_{OL}$                     | LOW-level output voltage           | $R_L = 1.5\text{ k}\Omega\text{ to }3.6\text{ V}$ | -          | -   | 0.3 | V             |
| $V_{OH}$                     | HIGH-level output voltage          | $R_L = 15\text{ k}\Omega\text{ to GND}$           | [1] 2.8    | -   | 3.6 | V             |
| <b>Leakage current</b>       |                                    |   |            |     |     |               |
| $I_{LZ}$                     | off-state leakage current          |   | -1         | -   | +1  | $\mu\text{A}$ |
| <b>Capacitance</b>           |                                    |   |            |     |     |               |
| $C_{in}$                     | input capacitance                  | pin to GND  | -          | -   | 20  | pF            |
| <b>Resistance</b>            |                                    |   |            |     |     |               |
| $Z_{DRV}$                    | driver output impedance            | steady-state drive                                | [2] 34     | 39  | 44  | $\Omega$      |
| $Z_{INP}$                    | input impedance                    |   | 10         | -   | -   | M $\Omega$    |
| $R_{swon(VPU3V3)}$           | switch-on resistance on pin VPU3V3 |   | -          | -   | 10  | $\Omega$      |
| <b>Termination</b>           |                                    |   |            |     |     |               |
| $V_{TERM}$                   | termination voltage                | for upstream port pull-up ( $R_{pu}$ )            | [3][4] 3.0 | -   | 3.6 | V             |

[1]  $V_{OH(min)} = V_{(VREG3V3)} - 0.2\text{ V}$ .

[2] Includes external resistors of  $33\ \Omega \pm 1\%$  on both pins DP and DM.

[3] This voltage is available at pins VREG3V3 and VPU3V3.

[4] The minimum voltage is 2.7 V in suspend mode.

## 12. Dynamic characteristics

**Table 14. Dynamic characteristics: analog I/O pins DP and DM**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{(VREG3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 8](#) for valid voltage level combinations;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                        | Parameter                                 | Conditions   | Min     | Typ | Max   | Unit |
|-------------------------------|---|--|---------|-----|-------|------|
| <b>Driver characteristics</b> |   |  |         |     |       |      |
| $t_{FR}$                      | rise time                                 | $C_L = 50\text{ pF to }125\text{ pF}$ ;<br>10 % to 90 % of $ V_{OH} - V_{OL} $ ;<br>see <a href="#">Figure 5</a> | 4       | -   | 20    | ns   |
| $t_{FF}$                      | fall time                                 | $C_L = 50\text{ pF to }125\text{ pF}$ ;<br>90 % to 10 % of $ V_{OH} - V_{OL} $ ;<br>see <a href="#">Figure 5</a> | 4       | -   | 20    | ns   |
| FRFM                          | differential rise time/fall time matching | excluding the first transition from idle state   | 90      | -   | 111.1 | %    |
| $V_{CRS}$                     | output signal crossover voltage           | excluding the first transition from idle state; see <a href="#">Figure 6</a>                                     | [1] 1.3 | -   | 2.0   | V    |

**Table 14. Dynamic characteristics: analog I/O pins DP and DM ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{(VREG3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 8](#) for valid voltage level combinations;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

| Symbol                       | Parameter                                    | Conditions  | Min | Typ | Max | Unit |
|------------------------------|--|---|-----|-----|-----|------|
| <b>Driver timing</b>         |  |   |     |     |     |      |
| $t_{PLH(drv)}$               | driver propagation delay (LOW to HIGH)       | VPO, VMO to DP, DM; see <a href="#">Figure 6</a> and <a href="#">Figure 9</a>         | -   | -   | 18  | ns   |
| $t_{PHL(drv)}$               | driver propagation delay (HIGH to LOW)       | VPO, VMO to DP, DM; see <a href="#">Figure 6</a> and <a href="#">Figure 9</a>         | -   | -   | 18  | ns   |
| $t_{PHZ}$                    | HIGH to OFF-state propagation delay          | $\overline{OE}$ to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a> | -   | -   | 15  | ns   |
| $t_{PLZ}$                    | LOW to OFF-state propagation delay           | $\overline{OE}$ to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a> | -   | -   | 15  | ns   |
| $t_{PZH}$                    | OFF-state to HIGH propagation delay          | $\overline{OE}$ to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a> | -   | -   | 15  | ns   |
| $t_{PZL}$                    | OFF-state to LOW propagation delay           | $\overline{OE}$ to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a> | -   | -   | 15  | ns   |
| <b>Receiver timings</b>      |  |   |     |     |     |      |
| <b>Differential receiver</b> |  |   |     |     |     |      |
| $t_{PLH(rcv)}$               | receiver propagation delay (LOW to HIGH)     | DP, DM to RCV; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>             | -   | -   | 15  | ns   |
| $t_{PHL(rcv)}$               | receiver propagation delay (HIGH to LOW)     | DP, DM to RCV; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>             | -   | -   | 15  | ns   |
| <b>Single-ended receiver</b> |  |   |     |     |     |      |
| $t_{PLH(se)}$                | single-ended propagation delay (LOW to HIGH) | DP, DM to VP/VPO, VM/VMO; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>  | -   | -   | 18  | ns   |
| $t_{PHL(se)}$                | single-ended propagation delay (HIGH to LOW) | DP, DM to VP/VPO, VM/VMO; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>  | -   | -   | 18  | ns   |

[1] Characterized only, not tested. Limits guaranteed by design.

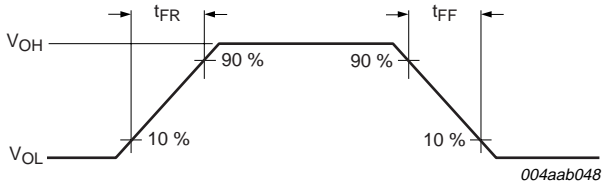


Fig 5. Rise time and fall time

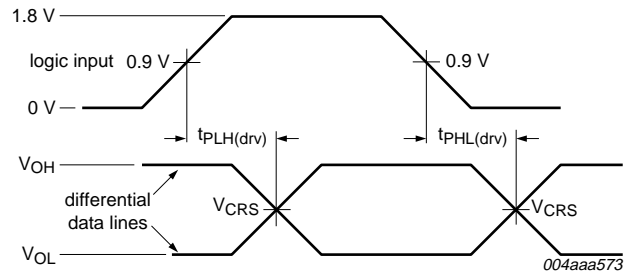


Fig 6. Timing of VPO and VMO to DP and DM

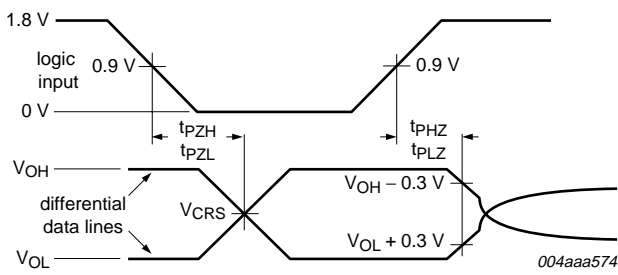


Fig 7. Timing of OE to DP and DM

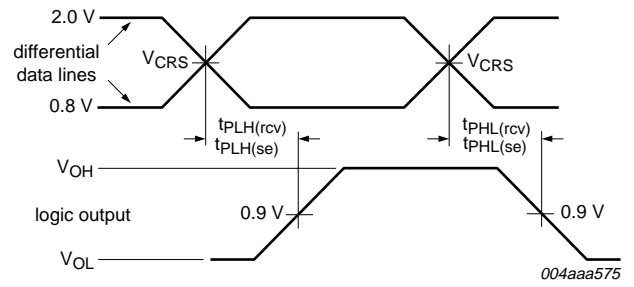
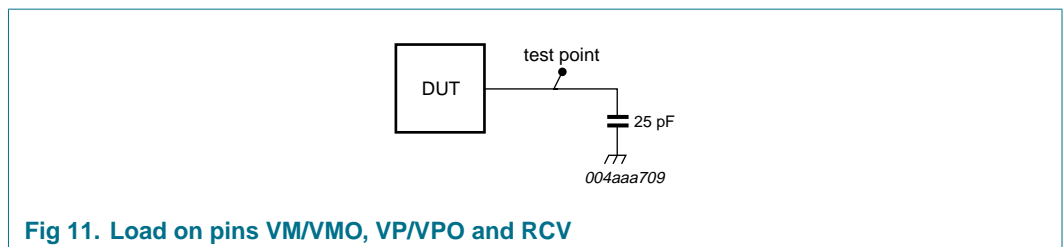
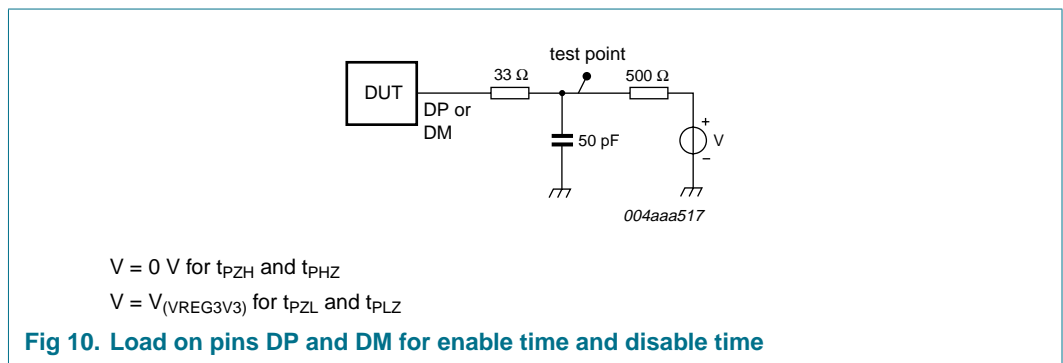
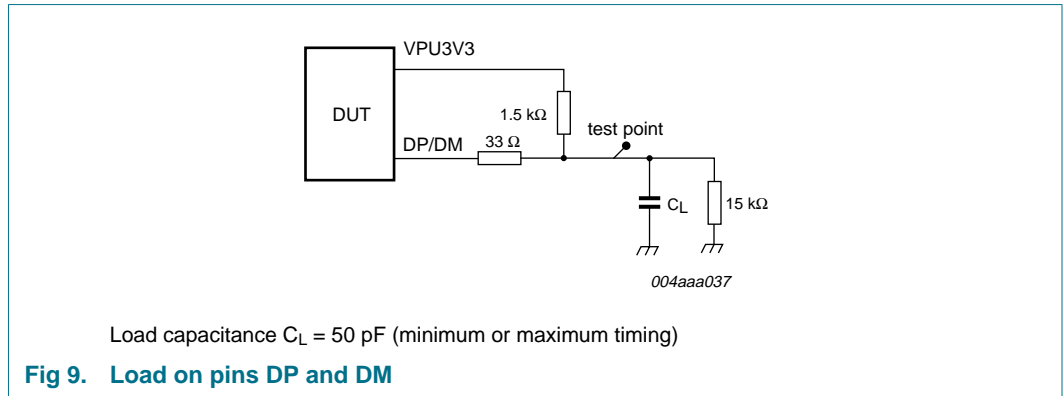


Fig 8. Timing of DP and DM to RCV, VP/VPO and VM/VMO

### 13. Test information



14. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm

SOT639-2

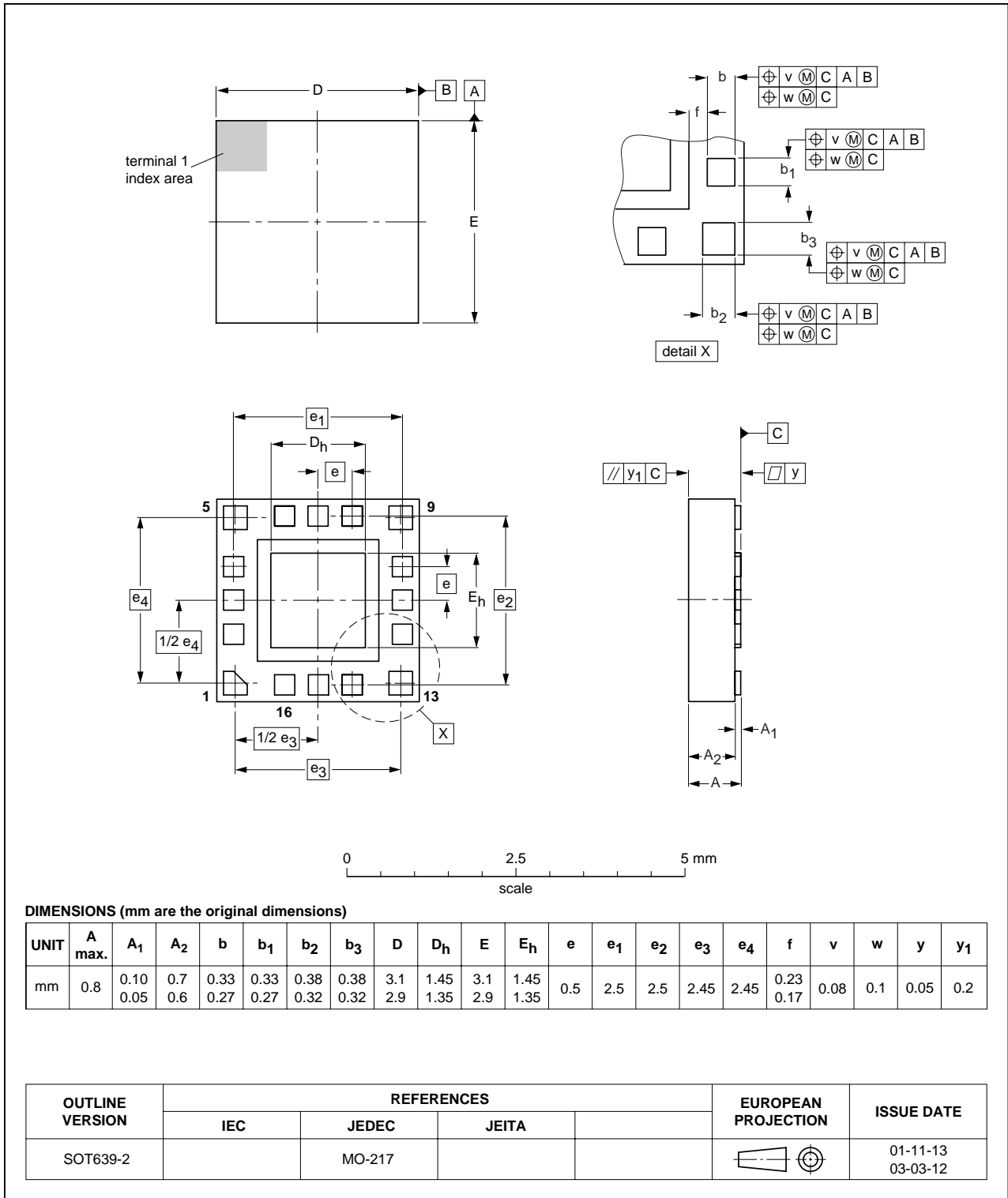


Fig 12. Package outline SOT639-2 (HBCC16)



**HVQFN14: plastic thermal enhanced very thin quad flat package; no leads;**  
**14 terminals; body 2.5 x 2.5 x 0.85 mm**

SOT773-1

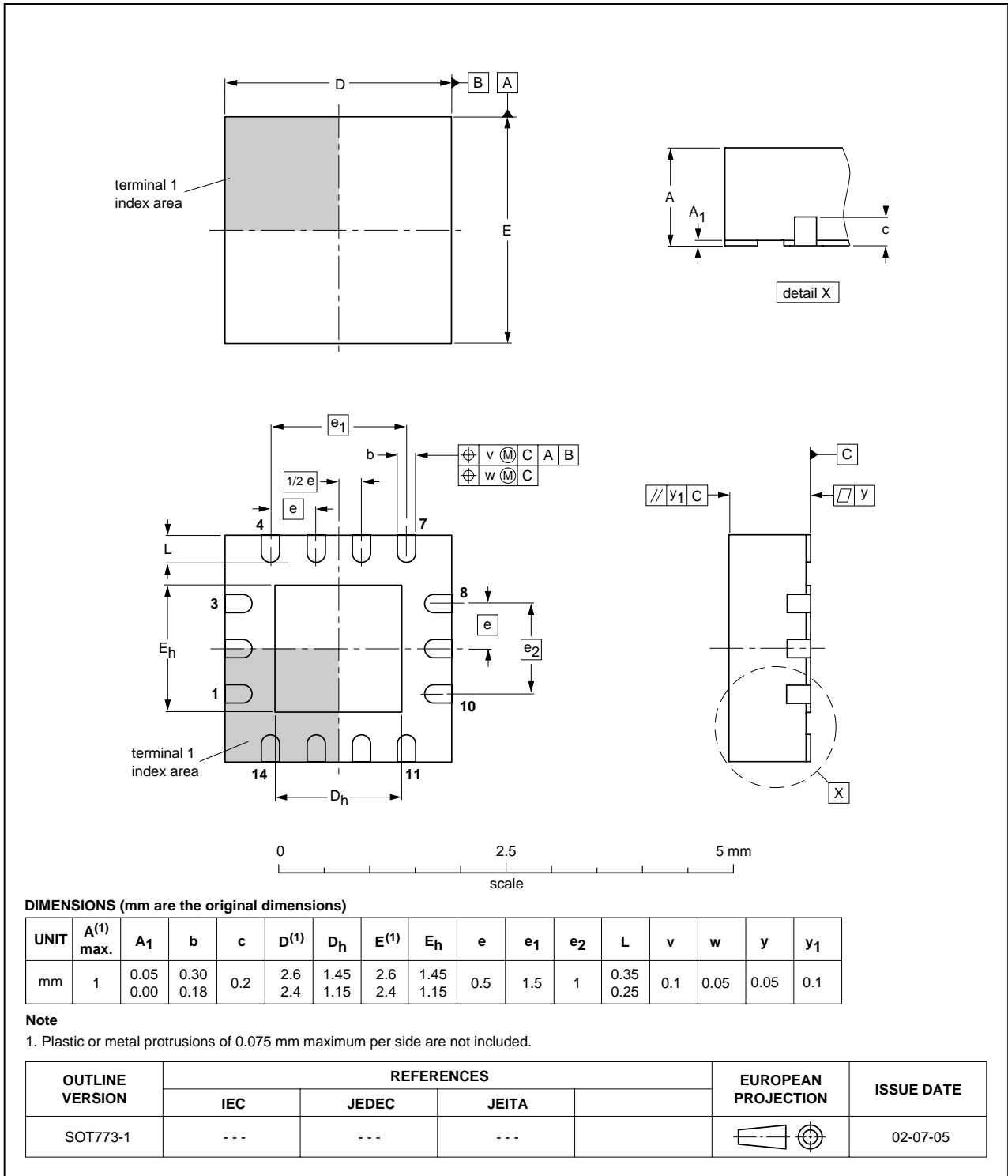


Fig 13. Package outline SOT773-1 (HVQFN14)

## 15. Packing information

The ISP1102W (HBCC16 package) is delivered on a Type A carrier tape, see [Figure 14](#). The tape dimensions are given in [Table 15](#).

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in baking process.

The cumulative tolerance of 10 successive sprocket holes is  $\pm 0.02$  mm. The camber must not exceed 1 mm in 100 mm.

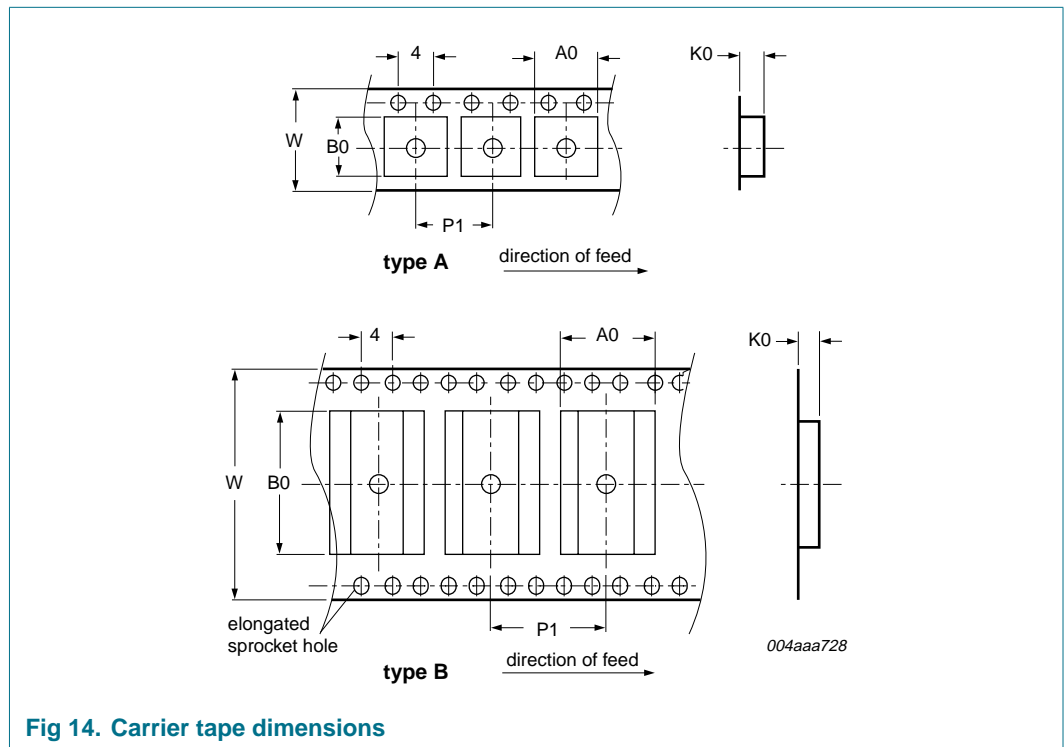


Fig 14. Carrier tape dimensions

Table 15. Type A carrier tape dimensions for the ISP1102W

| Dimension | Value          | Unit |
|-----------|----------------|------|
| A0        | 3.3            | mm   |
| B0        | 3.3            | mm   |
| K0        | 1.1            | mm   |
| P1        | 8.0            | mm   |
| W         | $12.0 \pm 0.3$ | mm   |

## 16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "Surface mount reflow soldering description".

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a PbSn process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#) and [17](#)

**Table 16. SnPb eutectic process (from J-STD-020C)**

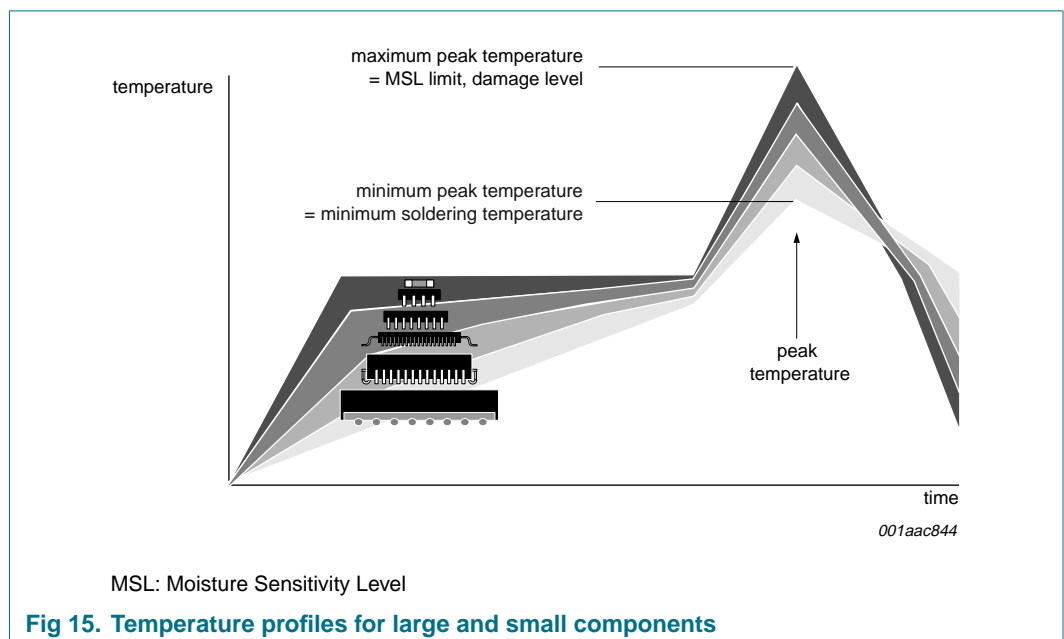
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 17. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 17. Abbreviations

**Table 18. Abbreviations**

| Acronym | Description                             |
|---------|---|
| ASIC    | Application-Specific Integrated Circuit |
| CMOS    | Complementary Metal-Oxide Semiconductor |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| SEO     | Single-Ended Zero                       |
| USB     | Universal Serial Bus                    |

## 18. Revision history

**Table 19. Revision history**

| Document ID                    | Release date  | Data sheet status  | Change notice | Supersedes |
|--------------------------------|---|--------------------|---------------|------------|
| ISP1102_5                      | 20071211  | Product data sheet | -             | ISP1102_4  |
| Modifications:                 | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 7.3 “Power supply configurations”</a> and <a href="#">Table 11 “Static characteristics: supply pins”</a>: changed <math>V_{CC(5V0)}</math> to &lt; 3.6 V.</li> <li><a href="#">Section 7.3 “Power supply configurations”</a>: changed VREG3V3 to &lt; 2.4 V.</li> <li><a href="#">Table 10 “Recommended operating conditions”</a>: added <math>T_j</math>.</li> </ul> |                    |               |            |
| ISP1102_4                      | 20060703  | Product data sheet | -             | ISP1102-03 |
| ISP1102-03<br>(9397 750 11228) | 20030902  | Product data       | -             | ISP1102-02 |
| ISP1102-02<br>(9397 750 10397) | 20030106  | Product data       | -             | ISP1102-01 |
| ISP1102-01                     | 20000524  | Objective data     | -             | -          |

## 19. Legal information

### 19.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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