DATA SHEET

SAA4990H
Progressive scan-Zoom and Noise reduction IC (PROZONIC)

Preliminary specification
File under Integrated Circuits, IC02

1996 Oct 25

Progressive scan-Zoom and Noise reduction IC (PROZONIC)

SAA4990H

FEATURES

- Progressive scan conversion (262.5 to 525 or 312.5 to 625 lines/field)
- Field rate up-conversion (50 to 100 Hz or 60 to 120 Hz)
- Line flicker reduction
- Noise and cross-colour reduction
- Variable vertical sample rate conversion
- Movie phase detection
- Synchronous No parity Eight bit Reception and Transmission (SNERT) interface.

GENERAL DESCRIPTION

The Progressive scan-Zoom and Noise reduction IC, abbreviated as PROZONIC, is designed for applications together with:

SAA4951WP Economy Controller (ECO3)

SAA4952H (memory controller)

SAA7158WP Back END IC (BENDIC)

SAA4995WP PANorama IC (PANIC)

SAA4970T ECOnomical video processing Back END IC (ECOBENDIC)

TMS4C2970/71 (serial field memories)

TDA8755/8753A (A/D converter 4 : 1 : 1 format)

83C652/54 type of microcontroller.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.5	V
T_{amb}	operating ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4990H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

BLOCK DIAGRAM

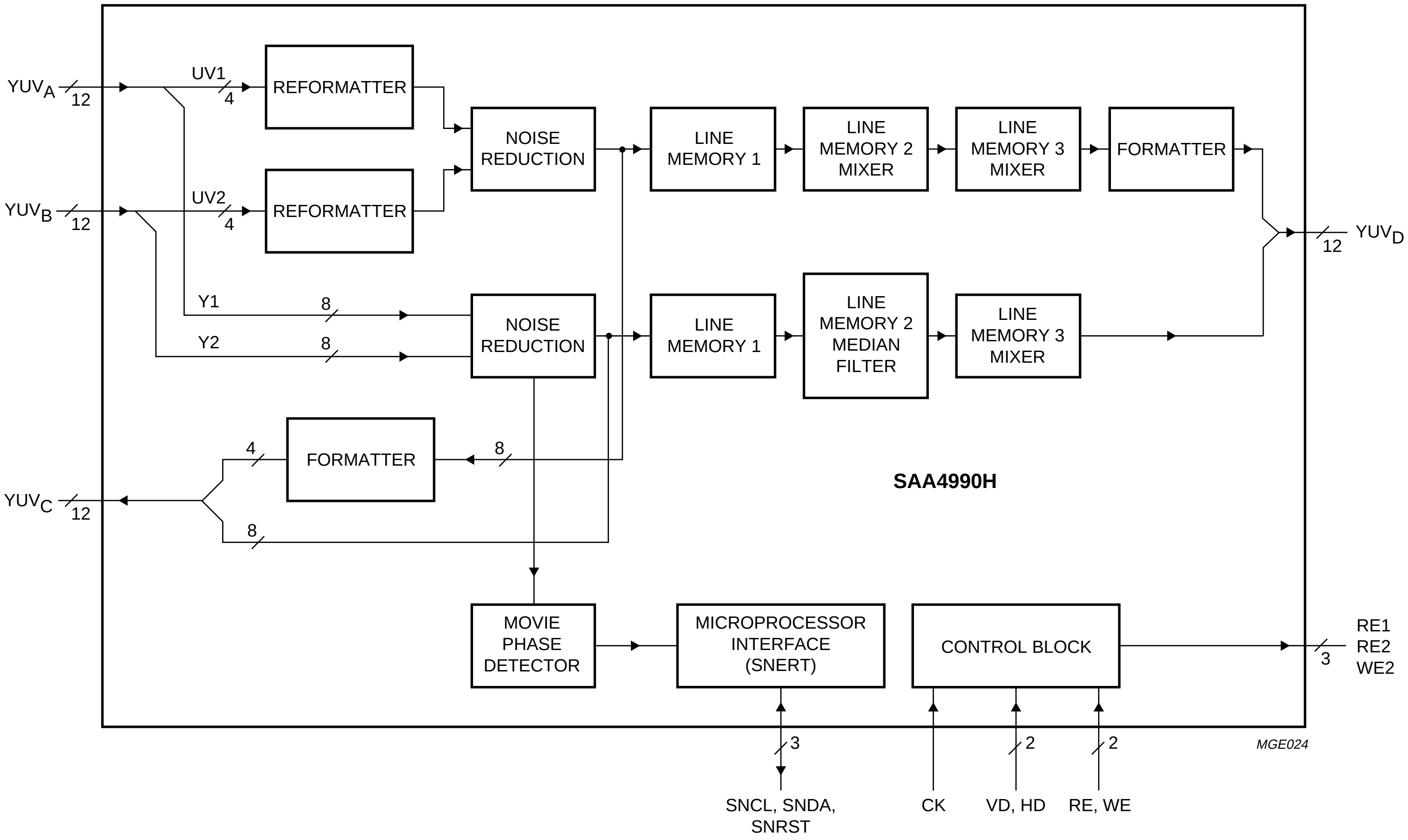


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
TEST1/AP	1	input	action pin for testing, to be connected to V_{SS}
TEST2/SP	2	input	shift pin for testing, to be connected to V_{SS}
RE1	3	output	read enable to FM1
V_{SS1}	4	ground	ground 1
V_{DD1}	5	supply	supply voltage 1
YUV_{C7}	6	output	Y bit 7 to FM2
YUV_{C6}	7	output	Y bit 6 to FM2
YUV_{C5}	8	output	Y bit 5 to FM2
YUV_{C4}	9	output	Y bit 4 to FM2
YUV_{C3}	10	output	Y bit 3 to FM2
V_{SS2}	11	ground	ground 2
V_{DD2}	12	supply	supply voltage 2
YUV_{C2}	13	output	Y bit 2 to FM2
YUV_{C1}	14	output	Y bit 1 to FM2
YUV_{C0}	15	output	Y bit 0 to FM2
YUV_{C11}	16	output	UV bit 3 to FM2
YUV_{C10}	17	output	UV bit 2 to FM2
YUV_{C9}	18	output	UV bit 1 to FM2
YUV_{C8}	19	output	UV bit 0 to FM2
CK	20	input	master clock, nominal 27 or 32 MHz
V_{SS3}	21	ground	ground 3
V_{DD3}	22	supply	supply voltage 3
WE2	23	output	write enable to FM2
RE2	24	output	read enable to FM2
YUV_{B8}	25	input	UV bit 0 from FM2
YUV_{B9}	26	input	UV bit 1 from FM2
YUV_{B10}	27	input	UV bit 2 from FM2
YUV_{B11}	28	input	UV bit 3 from FM2
YUV_{B0}	29	input	Y bit 0 from FM2
YUV_{B1}	30	input	Y bit 1 from FM2
YUV_{B2}	31	input	Y bit 2 from FM2
YUV_{B3}	32	input	Y bit 3 from FM2
V_{DD4}	33	supply	supply voltage 4
V_{SS4}	34	ground	ground 4
YUV_{B4}	35	input	Y bit 4 from FM2
YUV_{B5}	36	input	Y bit 5 from FM2
YUV_{B6}	37	input	Y bit 6 from FM2
YUV_{B7}	38	input	Y bit 7 from FM2
RE	39	input	master read enable
VD	40	input	field frequent reset, vertical display

SYMBOL	PIN	TYPE	DESCRIPTION
HD	41	input	horizontal reference signal
YUV_{D8}	42	output	UV bit 0
YUV_{D9}	43	output	UV bit 1
YUV_{D10}	44	output	UV bit 2
V_{DD5}	45	supply	supply voltage 5
V_{SS5}	46	ground	ground 5
YUV_{D11}	47	output	UV bit 3
YUV_{D0}	48	output	Y bit 0
YUV_{D1}	49	output	Y bit 1
YUV_{D2}	50	output	Y bit 2
V_{DD6}	51	supply	supply voltage 6
V_{SS6}	52	ground	ground 6
YUV_{D3}	53	output	Y bit 3
YUV_{D4}	54	output	Y bit 4
YUV_{D5}	55	output	Y bit 5
YUV_{D6}	56	output	Y bit 6
YUV_{D7}	57	output	Y bit 7
V_{DD7}	58	supply	supply voltage 7
V_{SS7}	59	ground	ground 7
SNRST	60	input	field frequent reset from microcontroller; reset for SNERT interface
SNDA	61	I/O	data for SNERT interface
SNCL	62	input	clock for SNERT interface
AUX	63	output	spare output from line-sequencer
H_O	64	output	output hold to e.g. LC display
n.c.	65	–	not connected
n.c.	66	–	not connected
YUV_{A7}	67	input	Y bit 7 from FM1
YUV_{A6}	68	input	Y bit 6 from FM1
YUV_{A5}	69	input	Y bit 5 from FM1
YUV_{A4}	70	input	Y bit 4 from FM1
YUV_{A3}	71	input	Y bit 3 from FM1
YUV_{A2}	72	input	Y bit 2 from FM1
V_{SS8}	73	ground	ground 8
V_{DD8}	74	supply	supply voltage 8
YUV_{A1}	75	input	Y bit 1 from FM1
YUV_{A0}	76	input	Y bit 0 from FM1
YUV_{A11}	77	input	UV bit 3 from FM1
YUV_{A10}	78	input	UV bit 2 from FM1
YUV_{A9}	79	input	UV bit 1 from FM1
YUV_{A8}	80	input	UV bit 0 from FM1

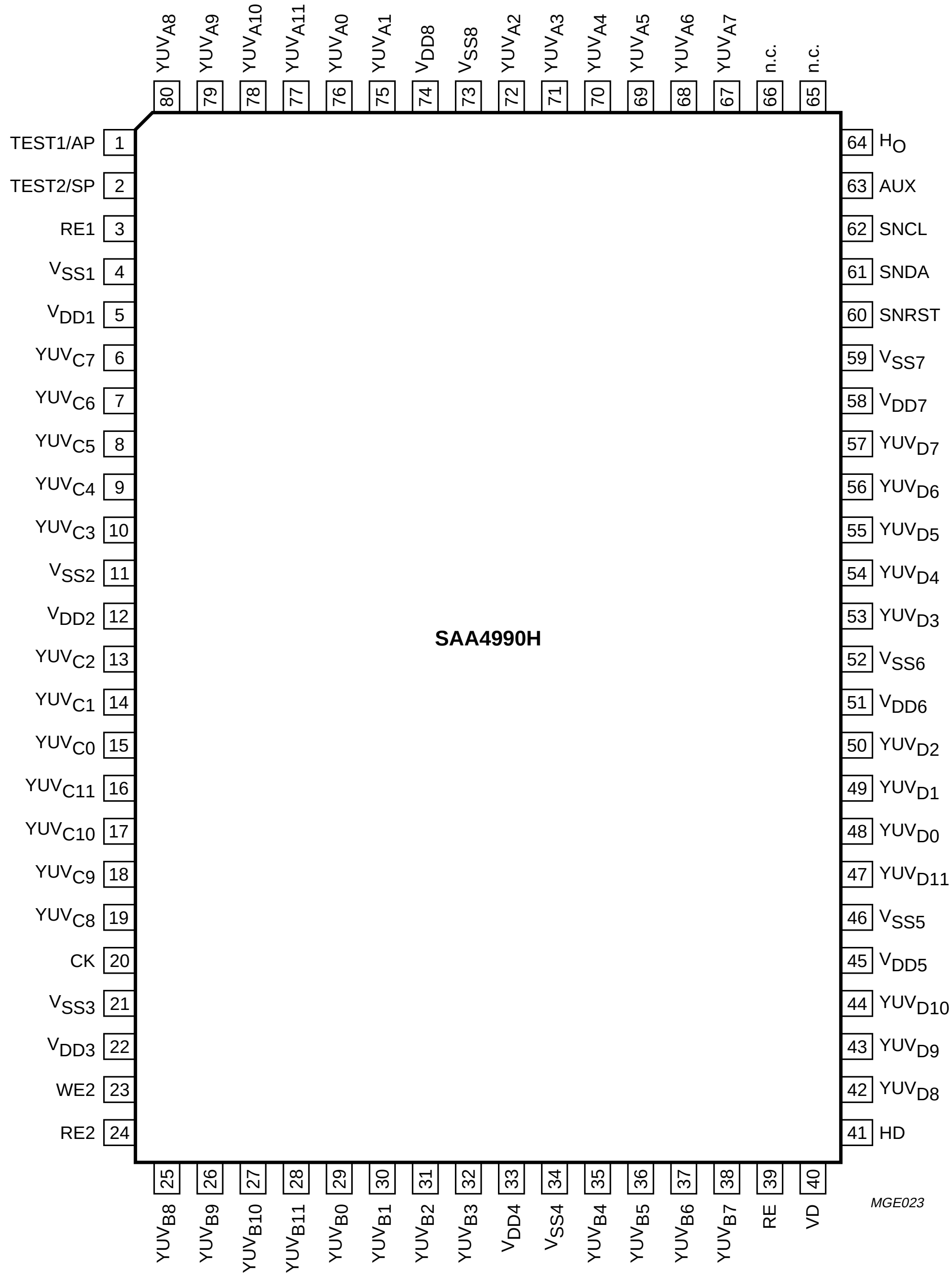


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Field rate up-conversion with line flicker reduction

The line flicker reduction in conjunction with field rate up-conversion is performed by generating a 50 Hz interlace on the 100 Hz field rate display. Median filtering supplies the data for the interlaced output fields.

DEFINITIONS

$Frame_l$: l is the number of an input/output frame temporarily combinating an A and B field.

$Field_n^x$: x is the field raster where A means an odd field and B means an even field.

$Frame_{l,\,k}$: l is the number of an output frame temporarily combinating an origin/interpolated A and B field;
k indicates the origin input field with
k = 1: odd input field and raster A
k = 2: even input field and raster B within $frame_l$.

$Field_{n,\,m}^x$: n, m = lines of $field_{n,\,m}$ are interpolated by 2 lines of $field_n$ and 1 line of $field_m$ using the median filter (see Fig.3); x is the field raster where A means an odd field and B means an even field.

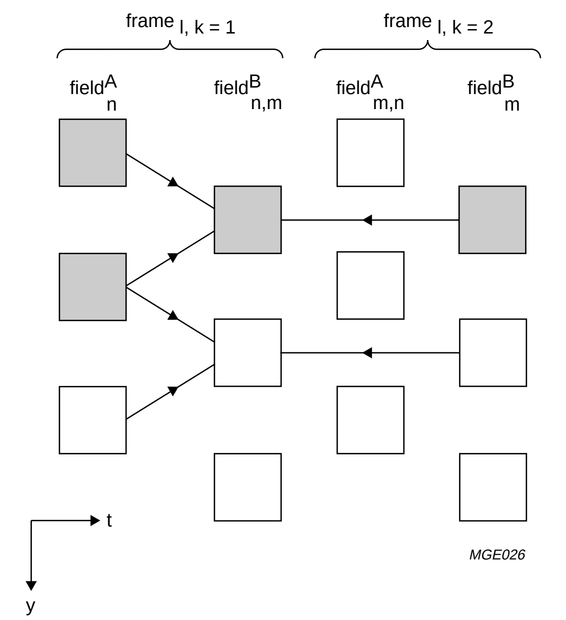


Fig.3 Generation of $field_{n,\,m}^B$ (median filter).

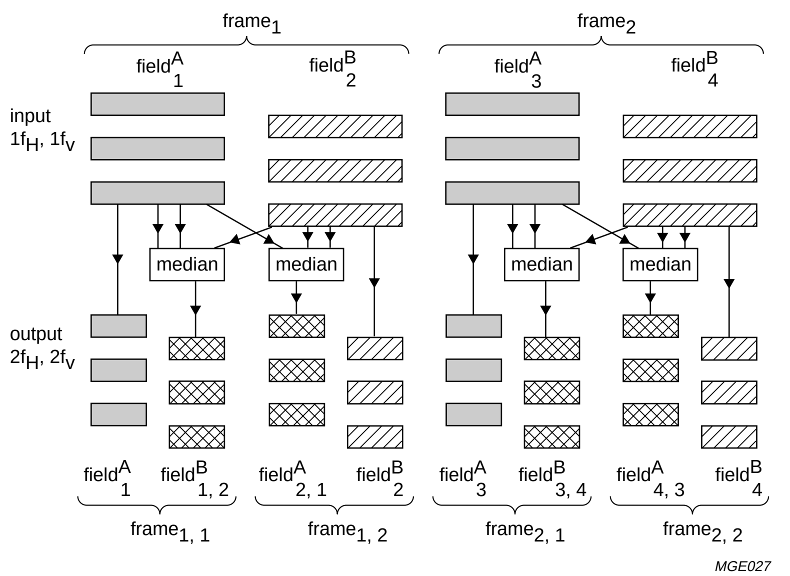


Fig.4 Scan rate up-conversion.

Progressive scan

Progressive scan conversion produces a double number of lines per field on the output. The field frequency is not changed, while the line frequency is doubled.

Processing for progressive scan is different for two successive output fields, e.g. the first output field has a median operation on the odd lines, while the second has the median operation on the even lines.

NON-INTERLACE MODE

With non-interlaced progressive scan output, line flicker is removed because interlace is removed.

INTERLACE MODE

With interlaced progressive scan the output line structure and line flicker is less visible (projection TV).

PROGRESSIVE SCAN CONVERSION

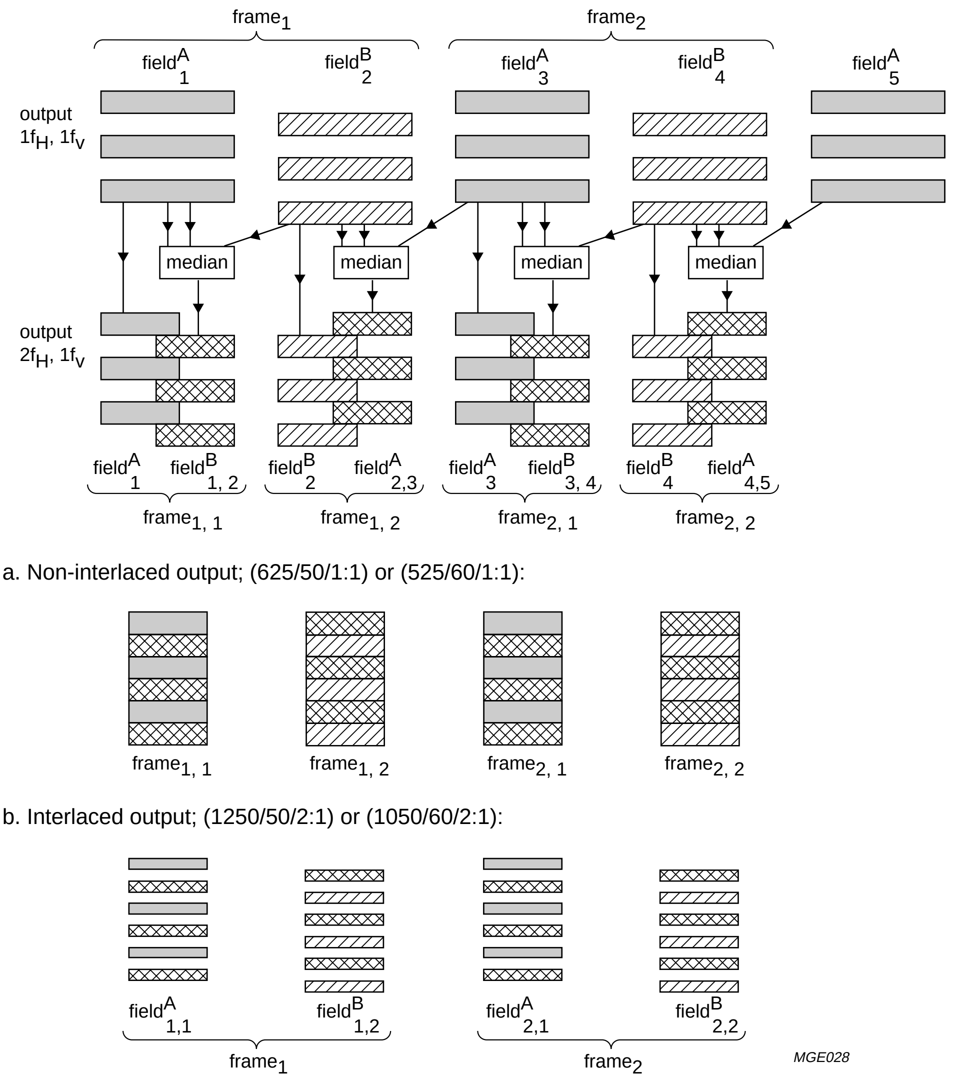


Fig.5 Progressive scan conversion.

Noise and cross-colour reduction

The noise reduction is field recursive with an average ratio between fresh and over previous fields averaged luminance and chrominance.

Two operating modes can be used in principal: the fixed and the adaptive mode (see Table 6).

In the fixed mode, the averaging produces a constant linear combination of the inputs. Except for k = 1, the fixed mode should not be used for normal operation, because of its smearing effects.

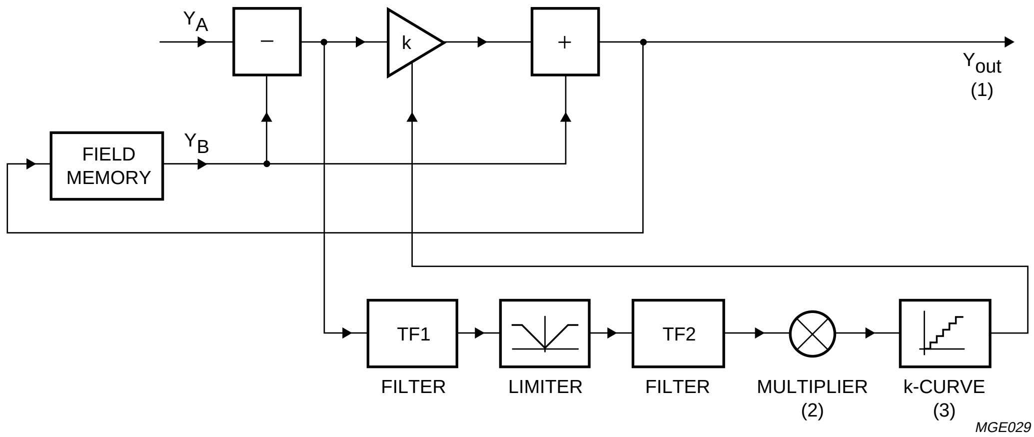
In the adaptive mode, the averaging ratio switches softly on the basis of absolute differences in luminance among the inputs. When the absolute difference is low, only a small part of the fresh data will be added. When the difference is high, much of the fresh data will be taken. This occurs in either the situation of movement or where a significant vertical contrast is seen.

To latter remark, note that recursion is done over a field, and the pixel positions one field apart always have a vertical offset of one frame line. So averaging is not only done in the dimension of time but also in the vertical direction. Therefore averaging vertically on e.g. a vertical black to white edge would provide a grey result if this was not adapted for.

The averaging in chrominance is slaved to the luminance averaging. This implies that differences in the chrominance are not taken into account for the k-factor setting.

The noise reduction scheme effectively decreases both noise and cross-colour patterns.

The cross-colour pattern does not produce an increase of the measured luminance difference, therefore this pattern will be averaged over many fields.



(1) $Y_{out} = Y_A \times k + Y_B \times (1 - k)$.
(2) see Table 9.
(3) see Fig.11.

Fig.6 Noise reduction scheme.

Vertical sample rate conversion

The variable vertical sample rate conversion is performed on top of the noise reduced and progressively scanned data.

The vertical sample rate conversion is intended to cope with the various letter box formats, to be displayed on displays with e.g. 16:9 aspect ratio. For this sample rate conversion, which usually has both a vertical and a horizontal component, the vertical sample rate conversion is taken care of in the PROZONIC, while the horizontal compression can be done in e.g. TDA8753A or SAA4995WP.

The vertical sample rate conversion can also be used to convert from an NTSC 525 lines source to a 625 line display, by setting a vertical sample rate conversion factor of $^6/_5$ and necessarily some line-time reduction.

Conversion from 625 to 525 lines is possible with progressive scan output, by setting a vertical sample rate conversion of $^5/_6$.

The principle of vertical sample rate conversion is based on linear interpolation from two successive lines of video in a frame to produce an output line in either a field or a frame.

The vertical sample rate conversion factor can be switched to the following settings for increasing the number of output lines w.r.t. the number of input lines; see Table 1.

Table 1 Vertical sample rate conversion factor

INPUT LINES	OUTPUT LINES	FACTOR
2	2	1.00
14	16	1.14
12	14	1.16
10	12	1.20
8	10	1.25
6	8	1.33
10	14	1.40
4	6	1.50
10	16	1.60
6	10	1.67
8	14	1.75
2	4	2.00

Decreasing the number of lines on the display w.r.t. the number of input lines is only possible with progressive scan output.

Movie phase detection

While processing video, that was originally film (25 movement phases per second in the case of 50 Hz field rates), median filtering is not needed when fields are combined that have the same movement phase. As this phase is not generally known, the PROZONIC has a detection circuit to help determine it. The detection is based on measurement of absolute luminance differences between successive input fields, pixel by pixel. These differences are summed over all active video and give a number every field. In case of video from film with sufficient movement, the measured number will alternately be HIGH and LOW. With the controlling microcontroller, this data can be filtered appropriately to switch to movie processing in the correct phase.

The PROZONIC has a provision to generate a rectangular box, which is position and size programmable. This box can be used to enable the measurement in the movie phase detection circuit, only within this rectangle. Otherwise, the active video part in a field is marked with a derivative of the RE pulse.

Box generation

A rectangular box is defined by the coordinates of the left-upper edge (hor_start_box, vert_start_box) and the right-lower edge (hor_stop_box, vert_stop_box). The reference for the coordinates are the HD positive edge (with some processing delay) for the horizontal direction and the VD positive edge for the vertical.

The box can serve the following purposes:

- Switch between adaptive and fixed k in noise reduction. If k-fixed is set to 0, then the box switches between adaptive noise reduced and fully still picture areas. This provides an option for producing multi picture (still) images. If no noise reduction is desired in the area where NR is adaptive, the adaptive setting can be programmed with k steps to all zeros.
- Switch the movie phase detect measurement to a defined area of the video.

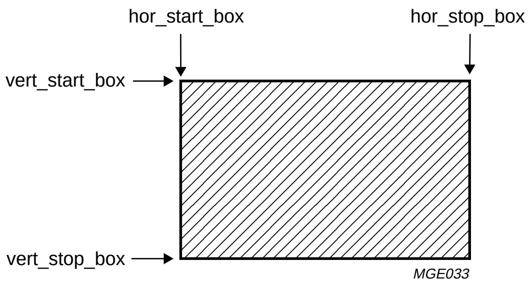


Fig.7 Box dimensions and position.

Control and microcontroller (SNERT-) interface

CONTROL SIGNALS

CK

Line-locked clock of nominal 27 or 32 MHz. This is the system clock, nominally 864 or 1024 $\times$ f_h, where f_h is the line frequency. Within the PROZONIC, CK is distributed to different blocks.

HD

Horizontal reference signal. This signal defines with its rising edge the start phase of the UV 4 : 1 : 1 format. If the HD signal has a period equal to 4 clock periods, the UV data will remain in phase without disruptions, once it has become in phase. For any mismatch between the applied HD to the UV data phase, an appropriate HD delay can be set in the PROZONIC. HD is also used to count lines for boxing.

RE

Master read enable from memory controller or ECOBENDIC. This signal controls the memory read enable if only one field memory is present. To control two field memories, the PROZONIC generates RE1, RE2 and WE2 from RE. The vertical sample rate conversion function has a major influence on these signals.

RE1

Read enable for FM1, processed from RE by PROZONIC.

RE2

Read enable for FM2, processed from RE by PROZONIC.

WE2

Write enable for FM2, processed from RE by PROZONIC.

H_O

Holds the writing of the LC display when active.

AUX

Spare output from line-sequencer.

VD

Field frequent reset signal, used in PROZONIC to reset line counting for boxing. The rising edge of VD is taken as reference. This may be the display related vertical pulse.

SNRST

Field frequent asynchronous reset signal, used in PROZONIC to reset the communication with microcontroller. After the rising edge of SNRST, communication is in its defined state. SNRST is also used to define the initial phase of the line-sequencer.

SNCL

microcontroller interface clock signal. This signal is transferred asynchronous to CK by a microcontroller (UART of 8051 family, mode 0) as communication clock signal at a frequency of 1 MHz.

SNDA

microcontroller interface data signal. This signal is transferred or received (asynchronous to CK) by a microcontroller (UART of 8051 family, mode 0) as communication data signal at 1 MBaud, related to SNCL.

EXTERNAL CONTROL

The PROZONIC is controlled via the microcontroller (SNERT) interface, by sending an address byte and a data byte to it, with the controllable items as in the register descriptions in Tables 2 and 3.

Table 2 Write registers

REGISTER	BIT	NAME	FUNCTION
Register 10H to 13H (Kstep)			
10H	0 to 3	Kstep0	step in adaptive curve from k = $^{1}/_{16}$ to k = $^{1}/_{8}$; weight of 1
	4 to 7	Kstep1	step in adaptive curve from k = $^{1}/_{8}$ to k = $^{2}/_{8}$; weight of 1
11H	0 to 3	Kstep2	step in adaptive curve from k = $^{2}/_{8}$ to k = $^{3}/_{8}$; weight of 2
	4 to 7	Kstep3	step in adaptive curve from k = $^{3}/_{8}$ to k = $^{4}/_{8}$; weight of 2
12H	0 to 3	Kstep4	step in adaptive curve from k = $^{4}/_{8}$ to k = $^{5}/_{8}$; weight of 4
	4 to 7	Kstep5	step in adaptive curve from k = $^{5}/_{8}$ to k = $^{6}/_{8}$; weight of 4
13H	0 to 3	Kstep6	step in adaptive curve from k = $^{6}/_{8}$ to k = $^{7}/_{8}$; weight of 8
	4 to 7	Kstep7	step in adaptive curve from k = $^{7}/_{8}$ to k = $^{8}/_{8}$; weight of 8
Register 14H (fixed_k)			
14H	0 to 3	fixed_k	determines k value in fixed k mode; see Table 8
	4 to 5	mult	weighting of TF2 output; see Table 9
	6	_upbox	microcontroller (_upbox = 0) or box controlled (_upbox = 1); see Table 6
	7	_adfix	adaptive (_adfix = 0) or fixed k (_adfix = 1); see Table 6
Register 15H (Tfilter)			
15H	0 to 1	Tfilter1_select	determines filter1 characteristic; see Table 5
	2 to 7	Tfilter2_select	determines filter2 characteristic; see Table 7
Register 16H (hor_start_box)			
16H	0 to 7	hor_start_box	horizontal start position of box w.r.t. picture
Register 17H (hor_stop_box)			
17H	0 to 7	hor_stop_box	horizontal stop position of box w.r.t. picture
Register 18H and 19H (vert_start_box)			
18H (bit 8 = 0) 19H (bit 8 = 1)	0 to 7	vert_start_box	vertical start position of box w.r.t. picture; bit 8 (MSB) is encoded in the address
Register 1AH and 1BH (vert_stop_box)			
1AH (bit 8 = 0) 1BH (bit 8 = 1)	0 to 7	vert_stop_box	vertical stop position of box w.r.t. picture; bit 8 (MSB) is encoded in the address
Register 1CH (box generation and UV processing)			
1CH	0	UV8bit	U/V signals are taken from input as 8-bit values instead of 7-bit
	1	UVbin	U/V signals are taken from input as binary signals instead of twos complement
	2	inv_box	inversion of box signal (inv_box = 1)
	3	en_box	overall enable box signal
	4	en_box_mpd	enable box signal to define movie phase detection area
	5	boxPSC	box generation for progressive scan with more than 511 lines
	6, 7		reserved
Register 1DH (reserved)			

REGISTER	BIT	NAME	FUNCTION
Register 1EH (horizontal delay)			
1EH	0 to 2	in_del	programmable horizontal delay (0 to 7 clock periods) of the luminance data input in comparison to the U/V data input (from FM1)
	3, 4	HD_del	determines 1 to 4 clock pulse shift for horizontal reference HD
	5, 6	WE2_del	determines 1 to 4 clock pulse shift for WE2 output
	7		reserved
Register 1FH (sequence data)			
1FH	0 to 2	mix	setting of mixer to 0, $\frac{1}{4}$, $\frac{1}{4}$, $\frac{1}{2}$, $\frac{1}{2}$, $\frac{3}{4}$, $\frac{3}{4}$, 1; setting per line in 1 to 16 lines of line sequencer
	3	post_zoom	setting of multiplexer pre or post LM_zoom to MIX; setting per line in 1 to 16 lines of line sequencer
	4	post_lfr	setting of multiplexer pre or post LM_lfr to MIX; setting per line in 1 to 16 lines of line sequencer
	5	mem_hold	setting of field and line memory hold; setting per line in 1 to 16 lines of line sequencer
	6	o_hold	setting of output hold, may stop e.g. LC display; setting per line in 1 to 16 lines of line sequencer
	7	aux	setting of auxiliary sequencer output signal; setting per line in 1 to 16 lines of line sequencer
Register 20H (sequence length)			
20H	0 to 3	seq_length	setting of sequence length to 1, 2, 3 to 16 lines
	4 to 7		reserved
Register 21H (field control 1); note 1			
21H	0	FCM4	see Fig.12 and Table 10
	1	FCM23	
	2	FCM1	
	3, 4	fixselUV	defines UV data output; see Fig.12 and Table 11
	5, 6	fixselY	defines Y data output; see Fig.12 and Table 11
	7	RAM1wr	selects RAM1 for write operation; note 2; see Fig.13
Register 22H (field control 2); note 1			
22H	0	WE2act	activates field controlled write enable 2 for FM2
	1, 2	RE1del	line delay for read enable 1 (FM1) w.r.t. RE input (pin 39)
	3, 4	RE2del	line delay for read enable 2 (FM2) w.r.t. RE input (pin 39)
	5, 6	WE2del	line delay for write enable 2 (FM2) w.r.t. RE input (pin 39)
	7	UV_av	UV averaged while luminance signal is median filtered

Notes

1. Data will be active after next VD pulse (pin 40).
2. In normal conditions control bit should be toggled field by field.

Table 3 Read registers

REGISTER	BIT	NAME
Register 26H (MPD_LSB)		
26H	0 to 7	MPD_LSB
Register 27H (MPD_MSB)		
27H	0 to 7	MPD_MSB

Table 4 Output multiplex control

output_mux[2:0]	THROUGHPUT
000	video
011	grey
111	sawtooth

Table 5 Filter1 characteristic

Tfilter1_select[1:0]	Tfilter1-TRANSFER (z)
00	1
01	$\frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1}$
10	$\frac{1}{2}$
11	$\frac{1}{2} \times z + \frac{1}{2} + \frac{1}{2} \times z^{-1}$

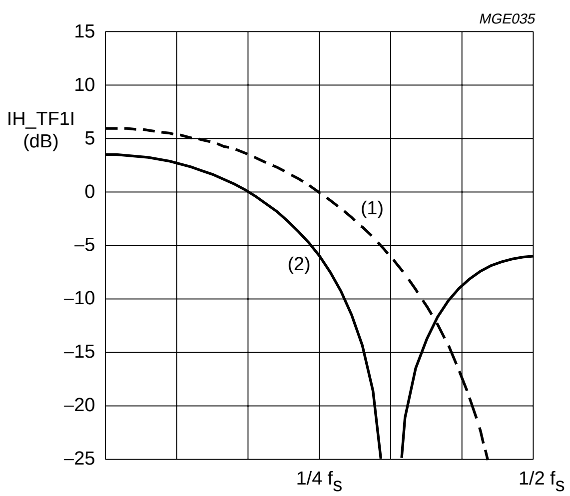
Table 6 Adaptive/fixed_k selection

Dynamic box signal, active in user defined rectangular part of the picture, enable with en_box, may be inverted with inv_box.

_upbox	_adfix	box	k
0	0	X(1)	adapt
0	0	X(1)	adapt
0	1	X(1)	fixed
0	1	X(1)	fixed
1	X(1)	0	fixed
1	X(1)	1	adapt
1	X(1)	0	fixed
1	X(1)	1	adapt

Note

1. X = don’t care bits.



$TF1(z) = \frac{1}{2} z + a + \frac{1}{2} z^{-1}$.

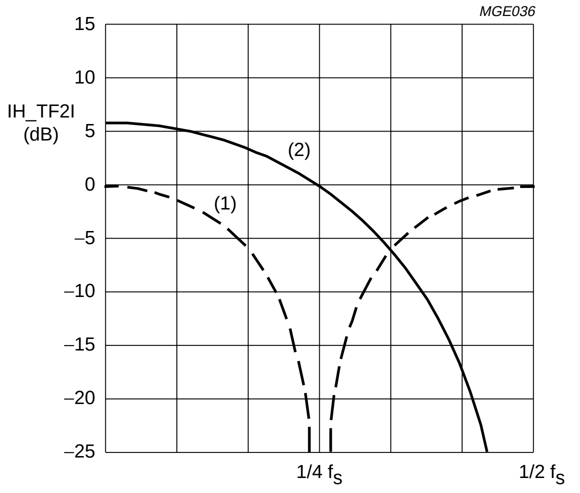
(1) a = 1.

(2) a = ½.

Fig.8 Characteristic pre-filter TF1.

Table 7 Filter2 characteristic

Tfilter2_select[5:0]		Tfilter2-TRANSFER (z)
HEX	**DECIMAL**	
00	00	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
01	01	$1 \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
02	02	$0 \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
04	04	$\frac{1}{2} \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
05	05	$1 \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + 1 \times z^{-2}$
06	06	$0 \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + 0 \times z^{-2}$
08	08	$\frac{1}{2} \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
09	09	$1 \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + 1 \times z^{-2}$
0A	10	$0 \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + 0 \times z^{-2}$
10	16	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
11	17	$1 \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
12	18	$0 \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
14	20	$\frac{1}{2} \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
15	21	$1 \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + 1 \times z^{-2}$
16	22	$0 \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + 0 \times z^{-2}$
18	24	$\frac{1}{2} \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
19	25	$1 \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + 1 \times z^{-2}$
1A	26	$0 \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + 0 \times z^{-2}$
20	32	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
21	33	$1 \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
22	34	$0 \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
24	36	$\frac{1}{2} \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
25	37	$1 \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + 1 \times z^{-2}$
26	38	$0 \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + 0 \times z^{-2}$
28	40	$\frac{1}{2} \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
29	41	$1 \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + 1 \times z^{-2}$
2A	42	$0 \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + 0 \times z^{-2}$

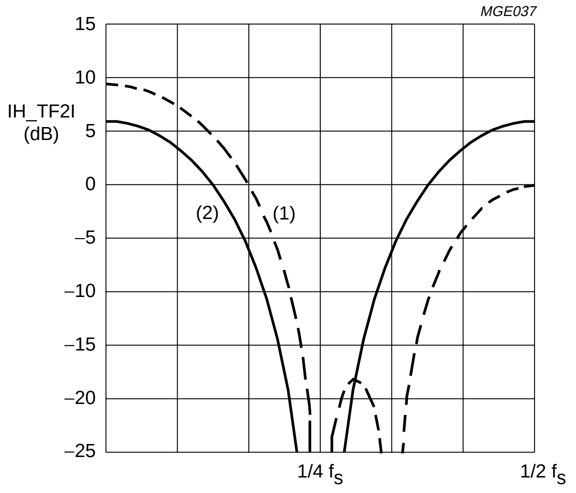


$TF2(z) = a\,z^{2} + b\,z + 2\,c + b\,z^{-1} + a\,z^{-2}$.

(1) c = 0.

(2) c = 1.

Fig.9 Characteristic pre-filter TF2 (a = 0; b = 1).



$TF2(z) = a\,z^{2} + b\,z + 2\,c + b\,z^{-1} + a\,z^{-2}$.

(1) b = 1.

(2) b = 0.

Fig.10 Characteristic pre-filter TF2 (a = 1; c = 1).

Table 8 Fixed_k setting

Fixed_k SETTING [3:0]		k
HEX	DECIMAL	
00	00	0
01	01	1⁄16
02	02	2⁄16
03	03	3⁄16
04	04	4⁄16
05	05	5⁄16
06	06	6⁄16
07	07	7⁄16
08	08	8⁄16
09	09	9⁄16
0A	10	10⁄16
0B	11	11⁄16
0C	12	12⁄16
0D	13	13⁄16
0E	14	14⁄16
0F	15	16⁄16

Table 9 Mult setting

MULT SETTING [1:0]		FACTOR
HEX	DECIMAL	
00	00	1
01	01	2
02	02	4
03	03	8

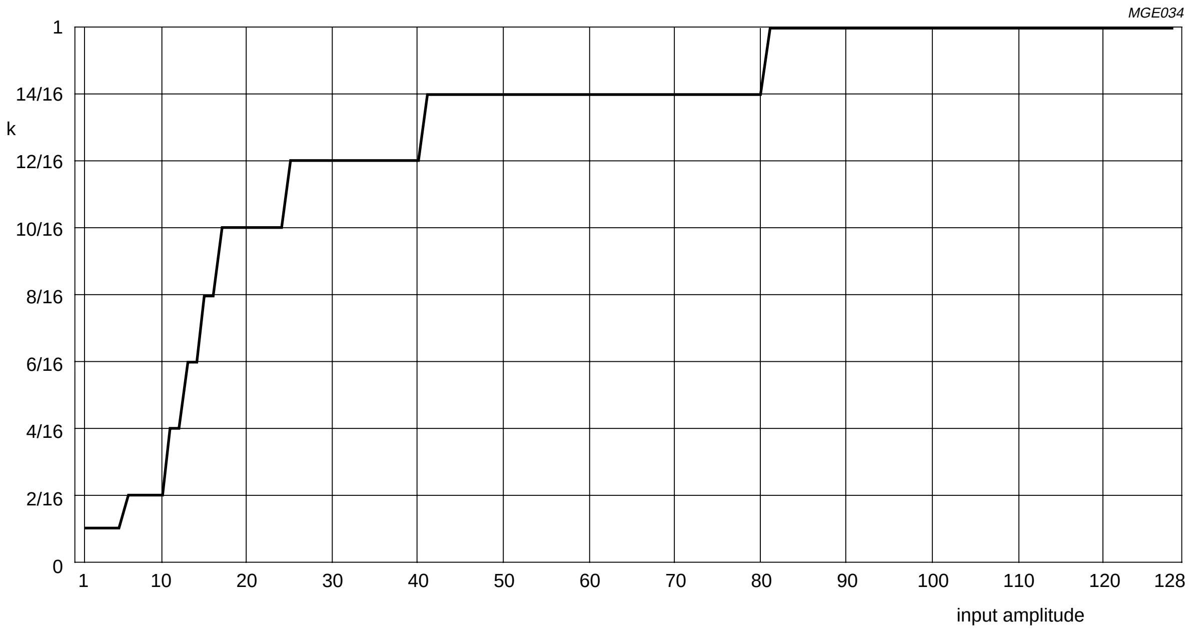
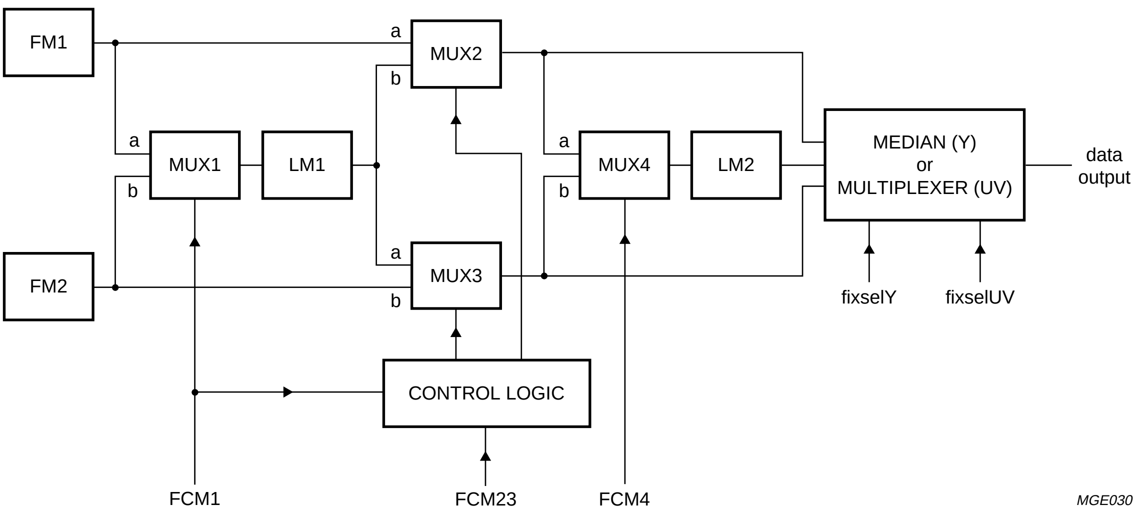


Fig.11 k factor curve (example) from filter TF2 and multiplier (see Fig.6).



FM1 and FM2: field memories (external).
LM1 and LM2: line memories.

Fig.12 Extract of the Progressive scan-Zoom and Noise reduction IC (PROZONIC) data path.

Table 10 Field controlled output

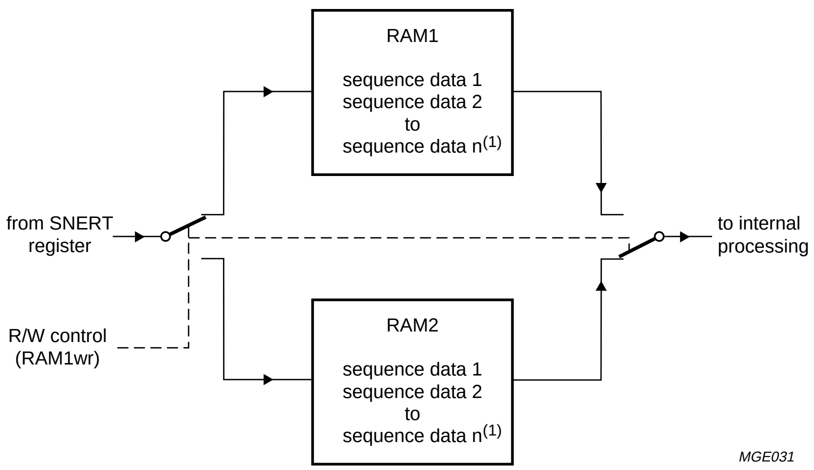
FCM23(1)	FCM1(2)	FCM4(3)	FIELD CONTROLLED OUTPUT TO MEDIAN (Y) OR MULTIPLEXER (UV)			
			MUX1	MUX2	MUX3	MUX4
0	X	0	X	FM1	FM2	FM1
0	X	1	X	FM1	FM2	FM2
1	0	0	FM2	FM1	FM2/1H delay	FM1
1	0	1	FM2	FM1	FM2/1H delay	FM2/1H delay
1	1	0	FM1	FM1/1H delay	FM2	FM1/1H delay
1	1	1	FM1	FM1/1H delay	FM2	FM2

Notes

1. FCM23 is the field controlled MUX2, MUX3.
2. FCM1 is the field controlled MUX1.
3. FCM4 is the field controlled MUX4.

Table 11 Data output

fixselY/fixselUV		DATA OUTPUT FROM
HEX	DECIMAL	
00	00	MUX2
01	01	MUX4/1H delay
02	02	MUX3
03	03	MEDIAN (Y)/median controlled MULTIPLEXER (UV)



(1) n = sequence length + 1

Fig.13 Internal RAM control.

Microcontroller interface (SNERT)

In the microcontroller interface the external signals SNDA and SNCL are processed to address and data. Data enable pulses are derived from the received addresses. The data enable pulses are used elsewhere for input enabling the delivered data into various control registers.

The microcontroller interface operates in a few stages:

1. SNCL positive and negative edges are sampled
2. on each negative edge of SNCL and SNDA data is shifted in a shift register
3. starting from phase 0, a counter counts positive edges of SNCL
4. during phase 7, but waited for a negative edge of SNCL, so after the 8th negative edge of SNCL, an address latch enable pulse is made, whereby the shift register contents are taken over in the address register
5. in the address range 10H to 27H, the addresses are decoded in two steps
6. during phase 15, but waited for a negative edge of SNCL, so after the 16th negative edge of SNCL, the address has been decoded and will be passed to any of the data enable pulses.

For each of the functions vert_start_box and vert_stop_box, two addresses are used, in which the LSB from the address is taken as an extra MSB for the data. This is done because vert_start_box and vert_stop_box must be supplied with 9-bit data. All other data from the SNERT-bus has only relevance in the 7:0 range.

During the data phases (phase 8 to 15), each negative edge produces a shift pulse for the movie phase detect circuit that produces output data on the SNDA signal. The data enables for the movie phase detect circuit are active in all of the data phases, when an address 26 or 27 has been decoded.

After an MPD read transmission it is necessary to send a second (dummy) transmission to the PROZONIC.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_I	input voltage	–0.5	+7	V
V_{DDD}	digital supply voltage	–0.5	+7	V
V_{DDA}	analog supply voltage	–0.5	+7	V
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	0	70	°C

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	supply voltage		4.5	5.5	V
I_{DDD}	supply current		–	180	mA
Digital inputs					
V_{IL}	LOW level input voltage except CK		–0.5	+0.8	V
	LOW level input voltage for CK		–0.5	+0.6	V
V_{IH}	HIGH level input voltage except CK		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage for CK		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	10	μA
C_I	input capacitance		–	10	pF
Digital outputs					
V_{OH}	HIGH level output voltage	note 1	2.4	V_{DDD}	V
V_{OL}	LOW level output voltage	note 1	0	0.6	V
Timing					
T_{cyCK}	CK cycle time		27	–	ns
δ_{CK}	CK duty factor t_{CKH}/t_{CKL}		40	60	%
t_r	CK rise time		–	5	ns
t_f	CK fall time		–	6	ns
t_{SU}	input data set-up time		–	3	ns
t_{HD}	input data hold time		–	3	ns
t_{OH}	output data hold time	note 1	3	–	ns
t_{OD}	output data delay time	note 1	–	23	ns
Data output loads (3-state outputs)					
C_L	output load capacitance		10	20	pF
	output load capacitance for RE1, RE2, WE2 and SNDA		10	35	pF

Note

1. Timings and levels have to be measured with load circuits 1.2 kΩ connected to 3.0 V (TTL load) and C_L = 20 pF.

Input/output timing

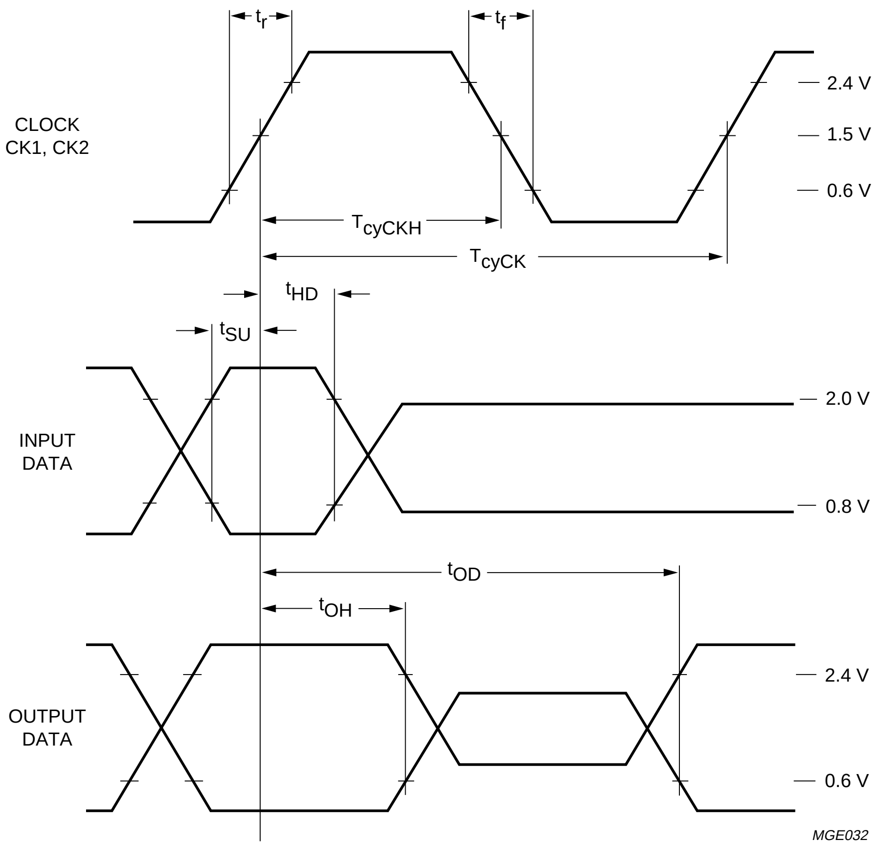


Fig.14 Timing diagram.

APPLICATION INFORMATION

The basic application of PROZONIC in a feature box is shown in Fig.15. Here, apart from the data streams, the ‘timed control data’ streams indicate that some memory control signals have to be processed by the PROZONIC, in order to let the vertical sample rate conversion function correctly.

Horizontal scaling factors are performed by the memory controller SAA4951WP/SAA4952H.

All basic clock signals in the feature box are provided by the memory controller, nominal frequencies on the double scan parts of the system are 27, 32 or 36 MHz. In any case the display frequency is decoupled from the acquisition clock.

The memory controller supplies the deflection processor with clock, horizontal and vertical pulses.

The SNERT-bus is used to control the PROZONIC at a data rate of typically 1 Mbits/s.

Table 12 Abbreviations used in Fig.15

BLND	horizontal blanking signal, display related
HDFL	horizontal synchronization signal, deflection related
HA	horizontal synchronization signal, acquisition related
HRA	horizontal reference signal, acquisition related
HRD	horizontal reference signal, display related
HRDFL	horizontal reference signal, deflection related
IE	input enable signal
LLA	line locked clock signal, acquisition related
LLD	line locked clock signal, display related
LLDFL	line locked clock signal, deflection related
RE	read enable signal
RSTR	reset read signal
RSTW	reset write signal
SCL	serial clock signal (I^2C-bus)
SDA	serial data signal (I^2C-bus)
SNERT	synchronous no parity eight bit reception and transmission (serial control bus)
SRC	serial read clock signal
SWC	serial write clock signal
VA	vertical synchronization signal, acquisition related
VDFL	vertical synchronization signal, deflection related

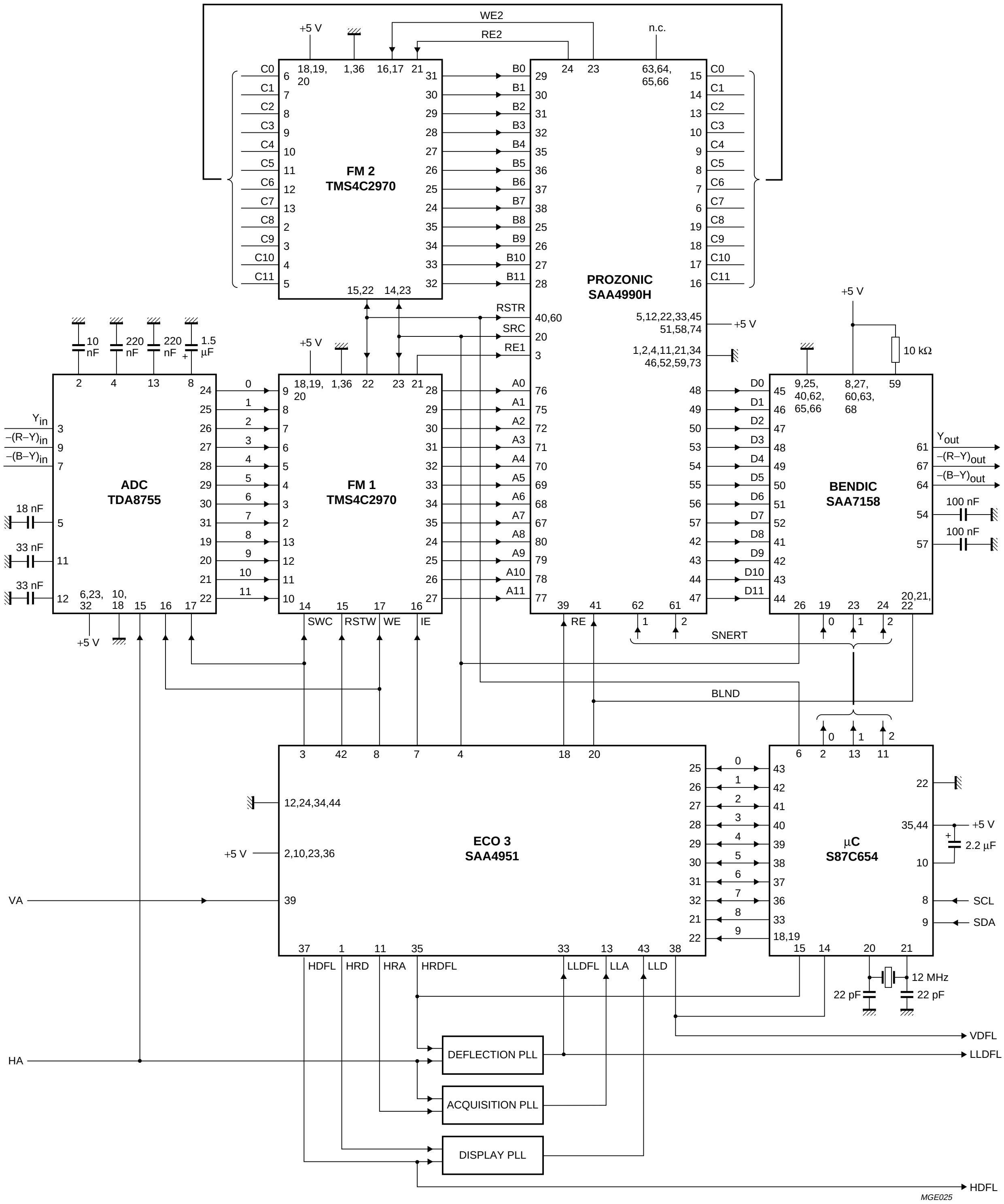
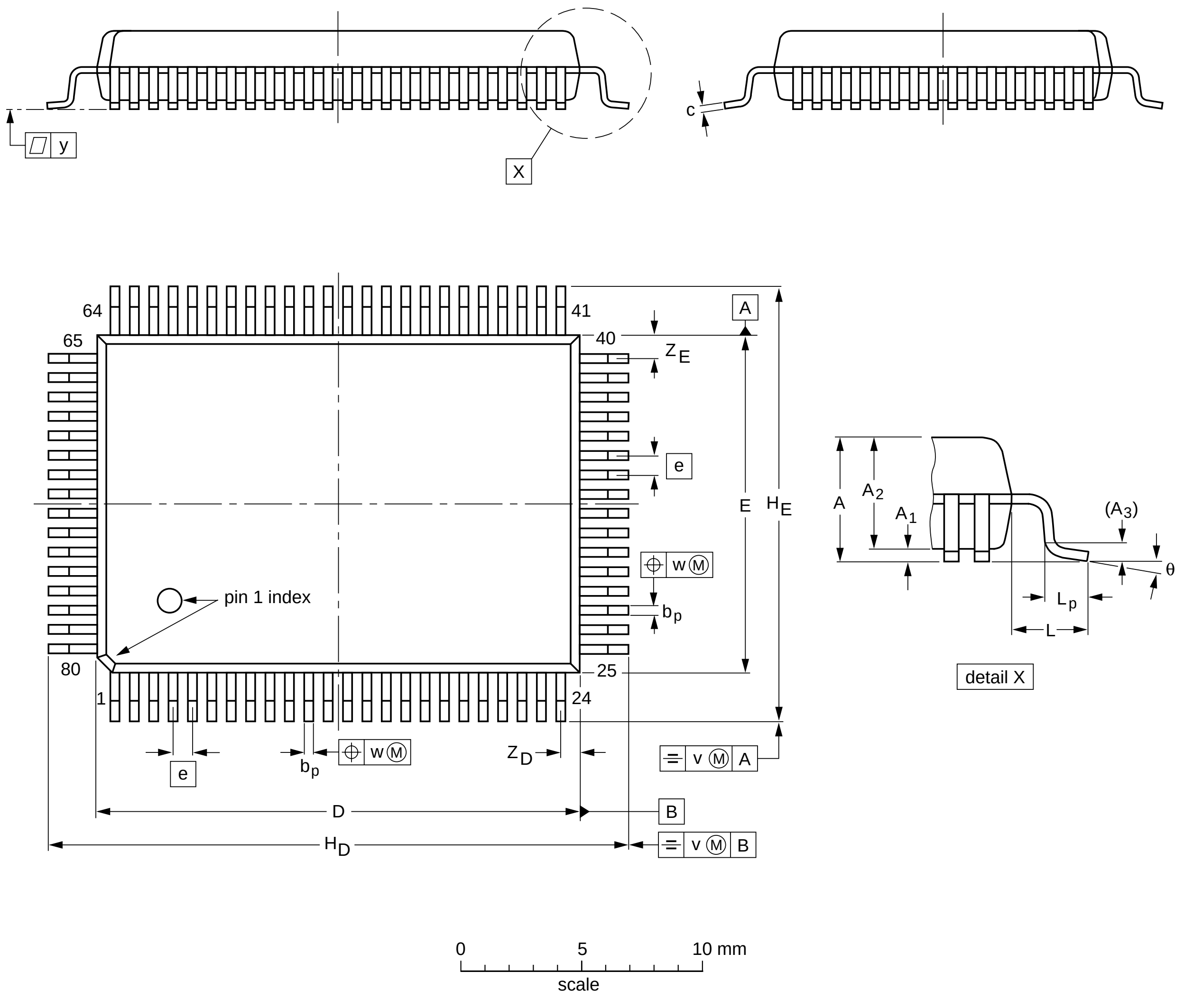


Fig.15 Application circuit.

PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands   537021/1200/01/pp28   Date of release: 1996 Oct 25   Document order number: 9397 750 01435

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