DATA SHEET

TDA8260TW
Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

Product specification
Supersedes data of 2004 Sep 03

2005 Jan 11

Philips
Semiconductors

PHILIPS

Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

TDA8260TW

FEATURES

- Direct conversion Quadrature Phase Shift Keying (QPSK) and 8-Phase Shift Keying (8PSK) demodulation (Zero-IF)
- Frequency range: 950 to 2175 MHz
- High level asymmetrical RF input
- 0 to 50 dB variable gain with AGC control
- Loop-controlled 0 to 90° phase shifter
- High AGC linearity (<1 dB per bit with an 8-bit DAC), AGC voltage variable between 0 and 3 V
- Integrated 5th-order matched baseband filters for in-phase (I) and quadrature (Q) signal paths
- Controlled I-to-Q gain balance
- I^2C-bus controlled PLL frequency synthesizer
- Low phase noise
- Operation from a 4 MHz crystal (allowing the use of an SMD crystal)
- Five frequency steps from 125 kHz to 2 MHz
- Crystal frequency output to drive the demodulator IC
- Compatible with 5, 3.3 and 2.5 V I^2C-bus
- Fully compatible and easy to interface with Philips Semiconductors family of digital satellite demodulators
- +5 V DC supply voltage
- 38-pin high heat dissipation package.

APPLICATIONS

- Direct Broadcasting Satellite (DBS) QPSK demodulation
- Digital Video Broadcasting (DVB) QPSK demodulation
- BS digital 8PSK demodulation.

GENERAL DESCRIPTION

The direct conversion QPSK demodulator is the front-end receiver dedicated to digital TV broadcasting, satisfying both DVB and DBS TV standards. The wide range oscillator (from 950 to 2175 MHz) covers the American, European and Asian satellite bands, as well as the SMA-TV US standard.

The Zero-IF concept discards traditional IF filtering and intermediate conversion techniques. It also simplifies the signal path.

Optimum signal level is guaranteed by gain-controlled amplifiers in the RF path. The 0 to 50 dB variable gain is controlled by the signal returned from the Satellite Demodulator and Decoder (SDD) and applied to pin AGCIN.

The PLL synthesizer is built on a dual-loop concept. The first loop controls a fully integrated L-band oscillator, using as a reference the LC VCO which runs at a quarter of the synthesized frequency.

The second loop controls the tuning voltage of the VCO and improves the phase noise of the carrier within the loop bandwidth. The step size is equal to the comparison frequency. The input of the main divider of the PLL synthesizer is connected internally to the VCO output.

The comparison frequency of the second loop is obtained from an oscillator driven by an external 4 MHz crystal. The 4 MHz output available at pin XTOUT may be used to drive the crystal inputs of the SDD, thereby saving an additional crystal in the application.

Both the divided and the comparison frequencies of the second loop are compared in a fast phase detector which drives the charge pump. The TDA8260TW includes a loop amplifier with an internal high-voltage transistor to drive an external 33 V tuning voltage.

Control data is entered via the I^2C-bus. The I^2C-bus voltage can be 5.0, 3.3 or 2.5 V, thus allowing compatibility with most existing microcontrollers.

A 5-byte frame is required to address the device and to program the main divider ratio, the reference divider ratio, the charge pump current and the operating mode.

A flag is set when the loop is ‘in-lock’, this can be read during READ operations, as well as the Power-on reset flag.

The device has four selectable I^2C-bus addresses. The selection is done by applying a specific voltage to pin AS. This feature gives the possibility to use up to four TDA8260TW ICs in the same system.

Performance summary

TDA8260TW performance:

- Noise figure at maximum gain = +18 dB
- High linearity; IP2 = +19 dBm and IP3 = +14 dBm
- Low phase noise on baseband outputs: –78 dBc/Hz (f_{offset} = 1 and 10 kHz; f_{COMP} = 1 MHz)
- 0 to 50 dB variable gain with AGC control
- AGC linearity <1 dB/bit with an 8-bit DAC
- Maximum I-to-Q amplitude mismatch = 1 dB
- Maximum I-to-Q phase mismatch = 3°
- Signal rates from 1 to 45 MSymbol/s.

System performance, for example, in a tuner application with the IC placed after a low-cost discrete LNA (see Fig.11):

- Noise figure at maximum gain = 8 dB
- High linearity; IP2 = +15 dBm and IP3 = +5 dBm
- 0 to 50 dB variable gain with AGC control.

Specification limitation

The content of this specification is applies to the device TDA8260TW with versions C2 and above. Version C1 is not covered by this document. Please contact your Philips semiconductors representative for further information.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current		–	155	–	mA
f_{osc}	oscillator frequency		950	–	2175	MHz
$\lvert Eq \rvert$	quadrature error (absolute value)	V_{AGC} = 1.5 V; $V_{o(p-p)}$ = 750 mV; measured in baseband	–	0	3	deg
$V_{o(p-p)}$	recommended output voltage (peak-to-peak value)		–	750	–	mV
LPF_{CO}	LPF cut-off frequency		–	36	–	MHz
φ_n	phase noise on baseband outputs	f_{offset} = 1 and 10 kHz; f_{COMP} = 1 MHz with appropriate loop filter and charge pump setting	–	–	–78	dBc/Hz
ΔG_v	AGC range	V_{AGC} = 0 to 3 V	48	50	–	dB
$V_{XTOUT(p-p)}$	AC output voltage on pin XTOUT (peak-to-peak value)	T_2 = 1, T_1 = 0, T_0 = 0; driving a load of C_L = 10 pF, R_L = 1 MΩ	500	650	–	mV
T_{amb}	ambient temperature		–20	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8260TW	HTSSOP38	plastic thermal enhanced thin shrink small outline package; 38 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT633-3

BLOCK DIAGRAM

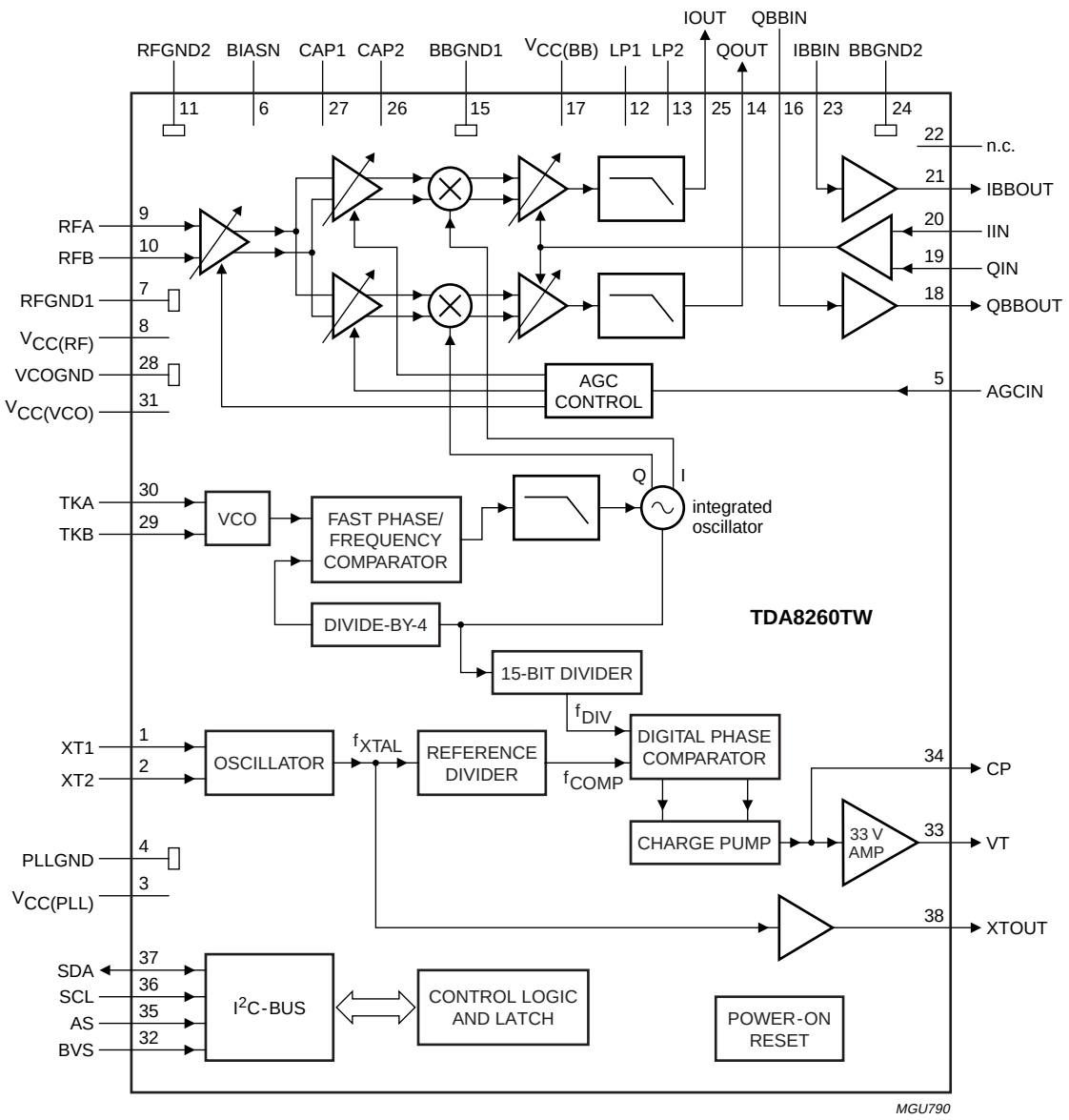


Fig.1 Block diagram.

PINNING INFORMATION

SYMBOL	PIN	DESCRIPTION
XT1	1	4 MHz crystal oscillator input 1
XT2	2	4 MHz crystal oscillator input 2
$V_{CC(PLL)}$	3	supply voltage for PLL circuit (+5 V)
PLLGND	4	ground for PLL circuit
AGCIN	5	AGC input from satellite demodulator and decoder
BIASN	6	RF isolation input (+5 V)
RFGND1	7	ground 1 for RF circuit
$V_{CC(RF)}$	8	supply voltage for RF stage (+5 V)
RFA	9	RF signal input A
RFB	10	RF signal input B
RFGND2	11	ground 2 for RF circuit
LP1	12	low-pass filter loop filtering output
LP2	13	low-pass filter loop filtering input
QOUT	14	quadrature output for AC coupling to pin 16
BBGND1	15	ground 1 for baseband stage
QBBIN	16	quadrature baseband AC-coupled input from pin 14
$V_{CC(BB)}$	17	supply voltage for baseband stage (+5 V)
QBBOUT	18	quadrature baseband output to satellite demodulator and decoder
QIN	19	quadrature input for auto-amplitude matching
IIN	20	in-phase input for auto-amplitude matching
IBBOUT	21	in-phase baseband output to satellite demodulator and decoder
n.c.	22	not connected
IBBIN	23	in-phase AC-coupled baseband input from pin 25
BBGND2	24	ground 2 for baseband stage
IOUT	25	in-phase output for AC-coupling to pin 23
CAP2	26	amplitude matching loop filtering output 2
CAP1	27	amplitude matching loop filtering output 1
VCOGND	28	ground for VCO circuit
TKB	29	VCO tank circuit input B
TKA	30	VCO tank circuit input A
$V_{CC(VCO)}$	31	supply voltage for VCO circuit (+5 V)
BVS	32	bus voltage select input
VT	33	tuning voltage output for VCO
CP	34	charge pump output
AS	35	address selection input
SCL	36	I^2C-bus clock input
SDA	37	I^2C-bus data input/output
XTOUT	38	4 MHz crystal oscillator output to satellite demodulator and decoder

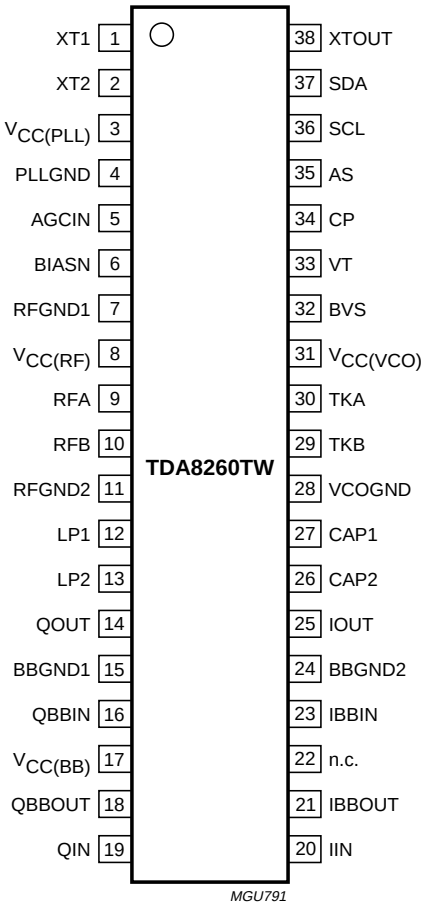


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8260TW contains the core of the RF analog part of a digital satellite receiver. The signal coming from the Low Noise Block (LNB) is coupled through a Low Noise Amplifier (LNA) to the RF inputs. The internal circuitry performs the Zero-IF quadrature frequency conversion and the two in-phase (IBBOUT) and quadrature (QBBOUT) output signals can be used directly to feed a Satellite Demodulator and Decoder circuit (SDD).

The TDA8260TW has a gain-controlled amplifier in the converter circuit. The gain is controlled by the AGCIN input from the SDD.

An external VCO tank circuit is connected between pins TKA and TKB. The main elements of the external tank circuit are an SMD coil and a varactor diode. The tuning voltage of 0 to 30 V covers the whole frequency range from 237.5 to 543.75 MHz. The internal loop controls a fully integrated VCO to cover the range 950 to 2175 MHz. The VCO provides both in-phase and quadrature signals to drive the two mixers.

Except for the 4 MHz crystal and the loop filter, all circuit components necessary to control the varactor-tuned oscillator are integrated in the TDA8260TW. The tuning circuit includes a fast phase detector with a high comparison frequency in order to achieve the lowest possible level of phase noise in the local oscillator.

The f_{DIV} output of the15-bit programmable divider passes through the fast phase comparator where it is compared in both phase and frequency with the comparison frequency (f_{COMP}). The frequency f_{COMP} is derived from the signal present at the XT1/XT2 pins (f_{XTAL}) divided-down by the reference divider. The buffered XTOUT signal can drive the crystal frequency input of the SDD, thereby saving a crystal in the application.

The output of the phase comparator drives the charge pump and loop amplifier section. The loop amplifier includes a high voltage transistor to handle the 30 V tuning voltage at pin VT, this drives a variable capacitance diode in the external circuit of the voltage controlled oscillator. Pin CP is the output of the charge pump. The loop filter is connected between pins CP and VT and the post-filter section is connected between pin VT and the variable capacitance diode.

For test and alignment purposes, it is possible to release the tuning voltage output and apply an external voltage to pin VT, also to select the charge pump function to sink current, source current or to be switched off.

PROGRAMMING

The programming of the TDA8260TW is performed through the I²C-bus. The read/write selection is made through the R/$\overline{W}$ bit (address LSB). The TDA8260TW fulfils the I²C-bus fast mode, according to the Philips I²C-bus specification, see document *"9398 393 40011"*.

I²C-bus voltage

The I²C-bus lines SCL and SDA can be connected to an I²C-bus system tied either to 2.5, 3.3 or 5.0 V, that will allow direct connection to most existing microcontrollers. The choice of the threshold voltage for the I²C-bus lines is made with pin BVS that needs to be left open-circuit, connected to supply voltage or connected to ground; see Table 1.

Table 1 I²C-bus voltage selection

PIN BVS	I²C-BUS VOLTAGE (V)
GND	2.5
Open-circuit	3.3
V_{CC}	5

I²C-bus write mode

I²C-bus write mode: R/$\overline{W}$ = logic 0; see Table 2.

After transmission of the address (first byte), four data bytes can be sent to fully program the TDA8260TW. The transmission sequence is one address byte followed by four data bytes PD1, PD2, CD1 and CD2.

The I²C-bus transceiver has an auto-increment facility that permits the TDA8260TW to be programmed within a single transmission.

The TDA8260TW can be partly programmed provided that the first data byte following the address is PD1 or CD1. The first bit of the first data byte transmitted indicates whether PD1 (first bit = logic 0) or CD1 (first bit = logic 1) will follow.

Additional data bytes can be entered without the need to re-address the device until an I²C-bus STOP condition is sent by the controller. Each byte is loaded after the corresponding 8th clock pulse.

Programmable divider data (contents of PD1 and PD2) become valid only after the 8th clock pulse of PD2, or after a STOP condition if only PD1 needs to be programmed.

Table 2 I²C-bus write data format

BYTE	(MSB)(1)			BITS(2)				(LSB)	ACK(3)
Programmable address	1	1	0	0	0	MA1	MA0	0	A
Programmable divider (PD1)	0	N14	N13	N12	N11	N10	N9	N8	A
Programmable divider (PD2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control data (CD1)	1	T2	T1	T0	R2	R1	R0	X	A
Control data (CD2)	C1	C0	X	X	X	X	X	X	A

Notes

1. MSB is transmitted first.
2. X = undefined.
3. Acknowledge bit (A).

Programmable addresses

The programmable address bits MA1 and MA0 offer the possibility of having up to four TDA8260TW devices in the same system. The relationship between the voltage applied to pin AS and the value of bits MA1 and MA0 is given in Table 3.

Table 3 I^2C-bus address selection

V_{AS}	MA1	MA0
0 to $0.1V_{CC}$	0	0
open-circuit	0	1
$0.4V_{CC}$ to $0.6V_{CC}$	1	0
$0.9V_{CC}$ to V_{CC}	1	1

Programmable main divider ratio

Program bytes PD1 and PD2 contain the fifteen bits N14 to N0 that set the main divider ratio. The ratio $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$.

Operating and test modes

The mode of operation is set using bits T2, T1 and T0 in control byte CD1; see Table 4.

Table 4 Mode selection

T2	T1	T0	MODE	XTOUT
0	0	0	normal operation	OFF
0	0	1	POR state = CP sink(1)	f_{XTAL}
0	1	0	$^1/_2 \times f_{DIV}$	$^1/_2 \times f_{DIV}$
0	1	1	CP sink	f_{XTAL}
1	0	0	normal operation	f_{XTAL}
1	0	1	$2 \times f_{ref}$	$2 \times f_{ref}$
1	1	0	CP OFF	f_{XTAL}
1	1	1	CP source	f_{XTAL}

Note

1. Status at power-on: the tuning voltage output is released and pin VT is in the high-impedance state.

Reference divider

Five reference divider ratios allow the adjustment of the comparison frequency to different values depending on the compromise that has to be found between step size and phase noise. The reference divider ratios and the corresponding comparison frequencies are programmed using bits R2, R1 and R0; see Table 5.

Table 5 Reference divider ratio

R2	R1	R0	DIVIDER RATIO	COMPARISON FREQUENCY
0	0	0	2	2 MHz
0	0	1	4	1 MHz
0	1	0	8	500 kHz
0	1	1	not allowed	
1	0	0	not allowed	
1	0	1	16	250 kHz
1	1	0	not allowed	
1	1	1	32	125 kHz

Charge pump current

Four values of charge pump current can be chosen using bits C1 and C0; see Table 6.

Table 6 Charge pump current

C1	C0	TYPICAL CHARGE PUMP CURRENT ABSOLUTE VALUES (μA)
0	0	420
0	1	900
1	0	1360
1	1	2320

I²C-bus read mode

I²C-bus read mode: R/$\overline{W}$ = logic 1 (address LSB; see Table 7).

When a read sequence is started, all eight bits of the status byte must be read.

Data can be read from the TDA8260TW by setting the R/$\overline{W}$ bit to logic 1. After recognition of its slave address, the TDA8260TW generates an acknowledge pulse and transfers the status byte onto the SDA line (MSB first). Data is valid on the SDA line when the SCL clock signal is HIGH.

A second data byte can be read from the TDA8260TW if the microcontroller generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge is received from the microcontroller. The TDA8260TW will then release the data line to allow the microcontroller to generate a STOP condition.

The POR flag (Power-on reset) is set to logic 1 at power-on and when V_{CC} goes below 2.7 V. It is reset to logic 0 when an end-of-data condition is detected by the TDA8260TW (end of a READ sequence).

The in-lock flag FL indicates that the loop is phase-locked when set to logic 1.

Table 7 I²C-bus read data format

BYTE	(MSB)			BITS				(LSB)	ACK(1)
Address	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR	FL(2)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	–

Notes

1. Acknowledge bit (A).
2. FL is valid only in normal mode.
3. X can be 1 or 0 and needs to be masked in the microcontrollers' software; MSB is transmitted first.

POWER-ON RESET

Power-on reset flag POR = 1 at power-on.

At power-on, or when the supply voltage drops below 2.7 V, internal registers are reset as shown in Table 8.

Table 8 Status at Power-on reset

BYTE	(MSB)			BITS(1)				(LSB)
Programmable divider (PD1)	0	N14 = X	N13 = X	N12 = X	N11 = X	N10 = X	N9 = X	N8 = X
Programmable divider (PD2)	N7 = X	N6 = X	N5 = X	N4 = X	N3 = X	N12 = X	N1 = X	N0 = X
Control data (CD1)	1	T2 = 0	T1 = 0	T0 = 1	R2 = X	R1 = X	R0 = X	X
Control data (CD2)	C1 = X	C0 = X	X	X	X	X	X	X

Note

1. X = not set.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); see note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
$V_{i(max)}$; $V_{o(max)}$	maximum input or output voltage on all pins except SDA, SCL and VT	–0.3	V_{CC} + 0.3	V
$V_{i(SDA)}$; $V_{o(SDA)}$	data input or data output voltage	–0.3	+6.0	V
$V_{i(SCL)}$	clock input voltage	–0.3	+6.0	V
$V_{o(tune)}$	tuning voltage output	–0.3	+35	V
T_{amb}	ambient temperature	–20	+85	°C
T_{stg}	IC storage temperature	–40	+150	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C
$t_{sc(max)}$	maximum short-circuit time; each pin; short-circuit to V_{CC} or GND	–	10	s

Note

1. Maximum ratings cannot be exceeded, not even momentarily, without causing irreversible damage to the IC. Maximum ratings cannot be accumulated.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	39	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

ESD specification:

- Every pin withstands 2000 V in the ESD test in accordance with *JEDEC specification EIA/JESD-A114A*, HBM model (category 2); except pin $V_{CC(RF)}$ (pin 8).
- Identically every pin withstands 200 V in the ESD test in accordance with *JEDEC specification EIA/JESD22-A115A*, MM model (category B).

CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 5 V; R_L = 1 kΩ and $V_{o(p-p)}$ = 750 mV on baseband output pins IBBOUT and QBBOUT; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.75	5.00	5.25	V
I_{CC}	supply current		–	155	–	mA
$V_{CC(POR)}$	supply voltage threshold for POR active		–	2.7	–	V
Performance from RF inputs to I, Q outputs (from pins RFA, RFB to pins IBBOUT, QBBOUT)						
$P_{L(LO)}$	LO power leakage through pins RFA and RFB		–	–75	–	dBm
$G_{v(RF-BBOUT)(max)}$	maximum voltage gain from pins RFA, RFB to IBBOUT, QBBOUT	V_{AGC} = 3 V	55	57	–	dB
ΔG_v	AGC range	V_{AGC} = 0 to 3 V	48	50	–	dB
$V_{o(p-p)}$	output voltage (peak-to-peak value)	recommended value	–	750	–	mV
IP2i	2nd-order interception point	at RF input; V_{AGC} = 0 V	–	19	–	dBm
IP3i	3rd-order interception point	at RF input; V_{AGC} = 0 V	–	14	–	dBm
F	noise figure	at maximum gain; V_{AGC} = 3 V	–	18	–	dB
$\Delta G_{v(IQ)}$	voltage gain mismatch between I and Q	in 22.5 MHz band	–	–	1	dB
$\lvert Eq \rvert$	quadrature error (absolute value)	V_{AGC} = 1.5 V; $V_{o(p-p)}$ = 750 mV; measured in baseband	–	0	3	deg
$G_{v(IQ)ripple}$	voltage gain ripple for I or Q	in 30 MHz band	–	–	2	dB
$t_{d(g)(IQ)(R)}$	group delay ripple for I or Q	in 22.5 MHz band	–	5	–	ns
RR_{60}	ripple rejection for I and Q	f_{ripple} = 60 MHz	30	–	–	dB
Pulling sensitivity						
3/4LO	sensitivity to pulling on the third harmonic of the external VCO	see Table 9	–	–40	–35	dBc
5/4LO	sensitivity to pulling on the fifth harmonic of the external VCO	see Table 9	–	–40	–35	dBc
VCO and synthesizer						
f_{osc}	oscillator frequency range		950	–	2175	MHz
$\varphi_{n(osc)}$	oscillator phase noise	in the satellite band; f_{offset} = 100 kHz; out of PLL loop bandwidth	–	–100	–94	dBc/Hz
φ_n	phase noise on baseband outputs	f_{offset} = 1 and 10 kHz; f_{COMP} = 1 MHz with appropriate loop filter and charge pump setting	–	–	–78	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MDR	main divider ratio		64	–	32767	
$\lvert Z_{osc} \rvert$	crystal oscillator negative impedance (absolute value)		1.0	1.5	–	kΩ
f_{XTAL}	crystal frequency		–	4	–	MHz
$V_{XTOUT(p-p)}$	AC output voltage on pin XTOUT (peak-to-peak value)	T_2 = 1, T_1 = 0, T_0 = 0; driving a load of C_L = 10 pF, R_L = 1 MΩ	500	650	–	mV
Z_{XTAL}	crystal series impedance	recommended value	–	–	200	Ω
Charge pump output; pin CP						
$I_{L(CP)}$	charge pump leakage current	T_2 = 1; T_1 = 1; T_0 = 0	–10	0	+10	nA
Tuning voltage output; pin VT						
$I_{LO(off)}$	leakage current when pin VT is in high-impedance off-state	T_2 = 0; T_1 = 0; T_0 = 1; V_{tune} = 33 V	–	–	10	μA
V_o	output voltage when the loop is locked	normal mode; V_{tune} = 33 V	0.2	–	32.7	V
Bus voltage select input; pin BVS						
I_{LIH}	HIGH-level input leakage current	$V_{BVS} = V_{CC}$	–	–	100	μA
I_{LIL}	LOW-level input leakage current	V_{BVS} = 0 V	–100	–	–	μA
SCL and SDA inputs						
V_{IL}	LOW-level input voltage	pin BVS floating	–	–	$0.2V_{CC}$	V
		V_{BVS} = 0 V	–	–	$0.15V_{CC}$	V
		V_{BVS} = 5 V	–	–	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage	pin BVS floating	$0.46V_{CC}$	–	–	V
		V_{BVS} = 0 V	$0.35V_{CC}$	–	–	V
		V_{BVS} = 5 V	$0.6V_{CC}$	–	–	V
I_{LIH}	HIGH-level leakage current	V_{IH} = 5.5 V; V_{CC} = 5.5 V	–	–	10	μA
		V_{IH} = 5.5 V; V_{CC} = 0 V	–	–	10	μA
I_{LIL}	LOW-level leakage current	V_{IL} = 0 V; V_{CC} = 5.5 V	–10	–	–	μA
$f_{SCL(max)}$	maximum input clock frequency		400	–	–	kHz
SDA output						
V_{ACK}	output voltage during acknowledge	I_{sink} = 3 mA	–	–	0.4	V
AS input						
I_{IH}	HIGH-level input current	$V_{AS} = V_{CC}$	–	–	10	μA
I_{IL}	LOW-level input current	V_{AS} = 0 V	–10	–	–	μA

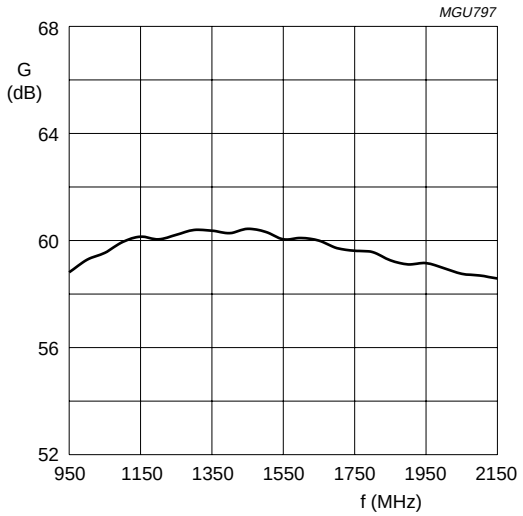


Fig.3 Overall maximum gain as a function of frequency.

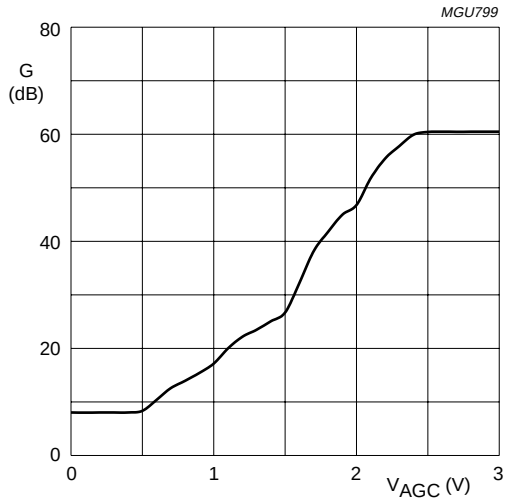


Fig.4 Overall gain as a function of AGC voltage.

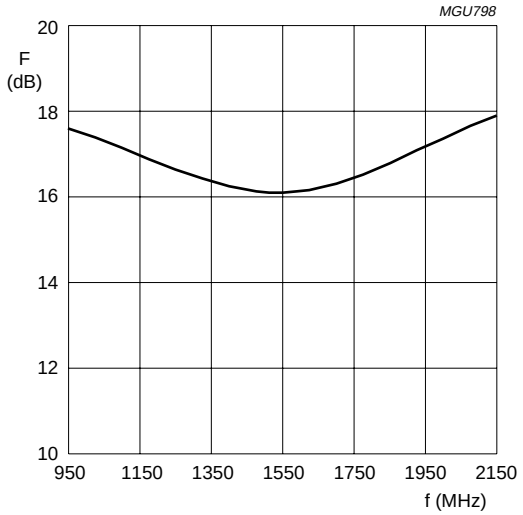
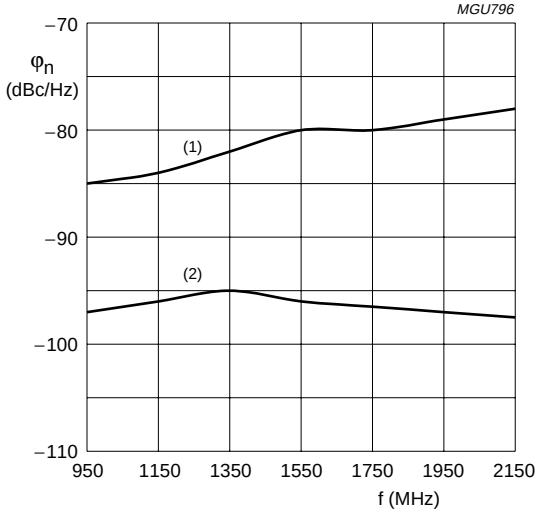


Fig.5 Noise figure at maximum gain as a function of frequency.



(1) f_{offset} = 10 kHz; f_{COMP} = 1 MHz.
(2) f_{offset} = 100 kHz; f_{COMP} = 1 MHz.

Fig.6 Phase noise on I and Q baseband outputs as a function of frequency.

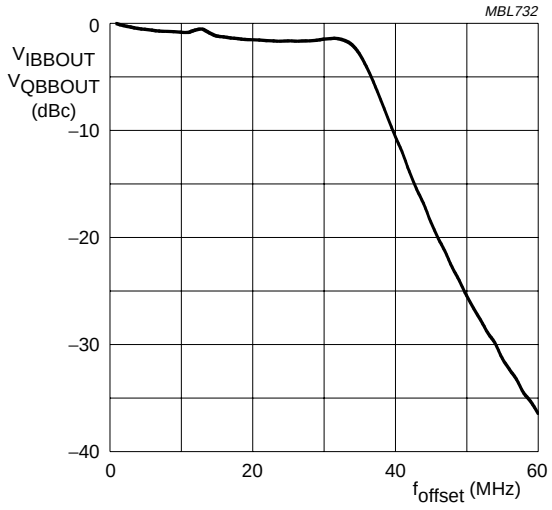


Fig.7 Baseband output filters.

Measurement method for pulling sensitivity

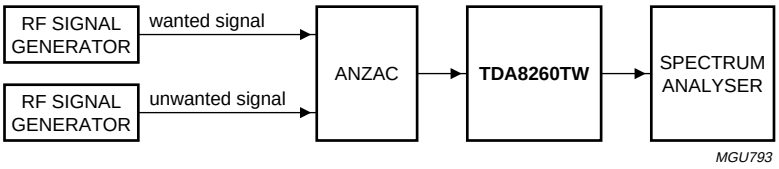


Fig.8 Test set-up.

Table 9 Test signal conditions for pulling measurements

TEST	SIGNAL	FREQUENCY	LEVEL	CONTENT (see Fig.9)
3/4LO test	wanted	f_w = 2161 MHz	–10 dBm	$f_w = f_{LO}$ + 11 MHz
	unwanted	f_{uw} = 1613 MHz	–2 dBm	$f_{uw} = f_{LO} \times {}^3/_4$ + 500 kHz
	local oscillator	f_{LO} = 2150 MHz	–	–
5/4LO test	wanted	f_w = 1761 MHz	–10 dBm	$f_w = f_{LO}$ + 11 MHz
	unwanted	f_{uw} = 2188 MHz	–2 dBm	$f_{uw} = f_{LO} \times {}^5/_4$ + 500 kHz
	local oscillator	f_{LO} = 1750 MHz	–	–

The level of the wanted and unwanted signals given in Table 9 are measured at the outputs of the RF signal generators. The sensitivity to pulling is measured in baseband by the difference expressed in dB (Δ) between the level of the wanted signal and the spurious signal that has been generated by pulling. The ANZAC reference is HH128.

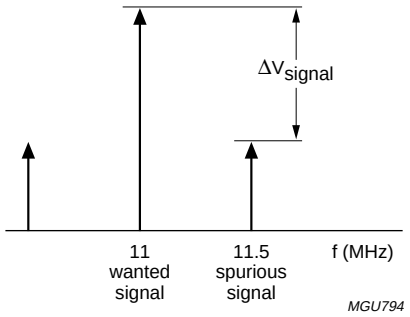


Fig.9 Baseband spectrum.

APPLICATION INFORMATION

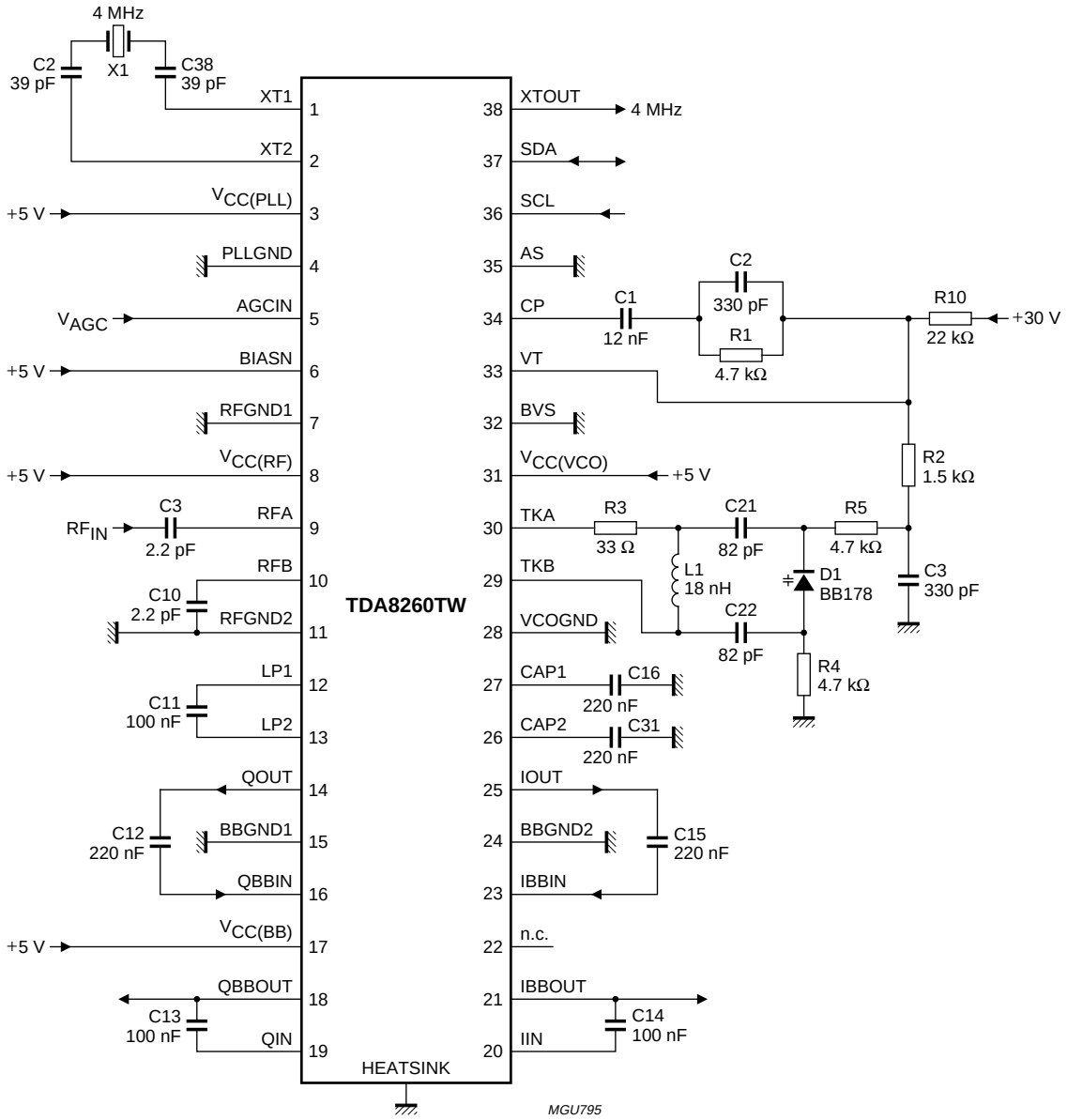


Fig.10 Typical application circuit.

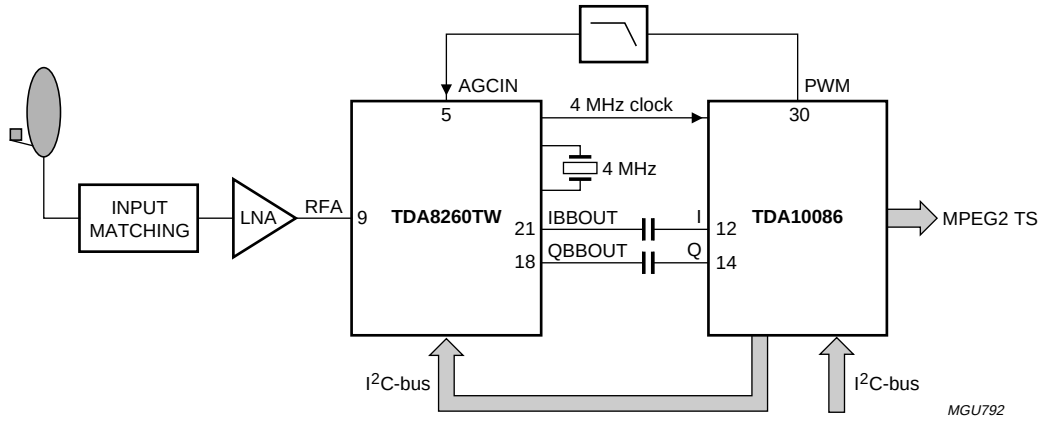


Fig.11 Tuner configuration of the TDA8260TW.

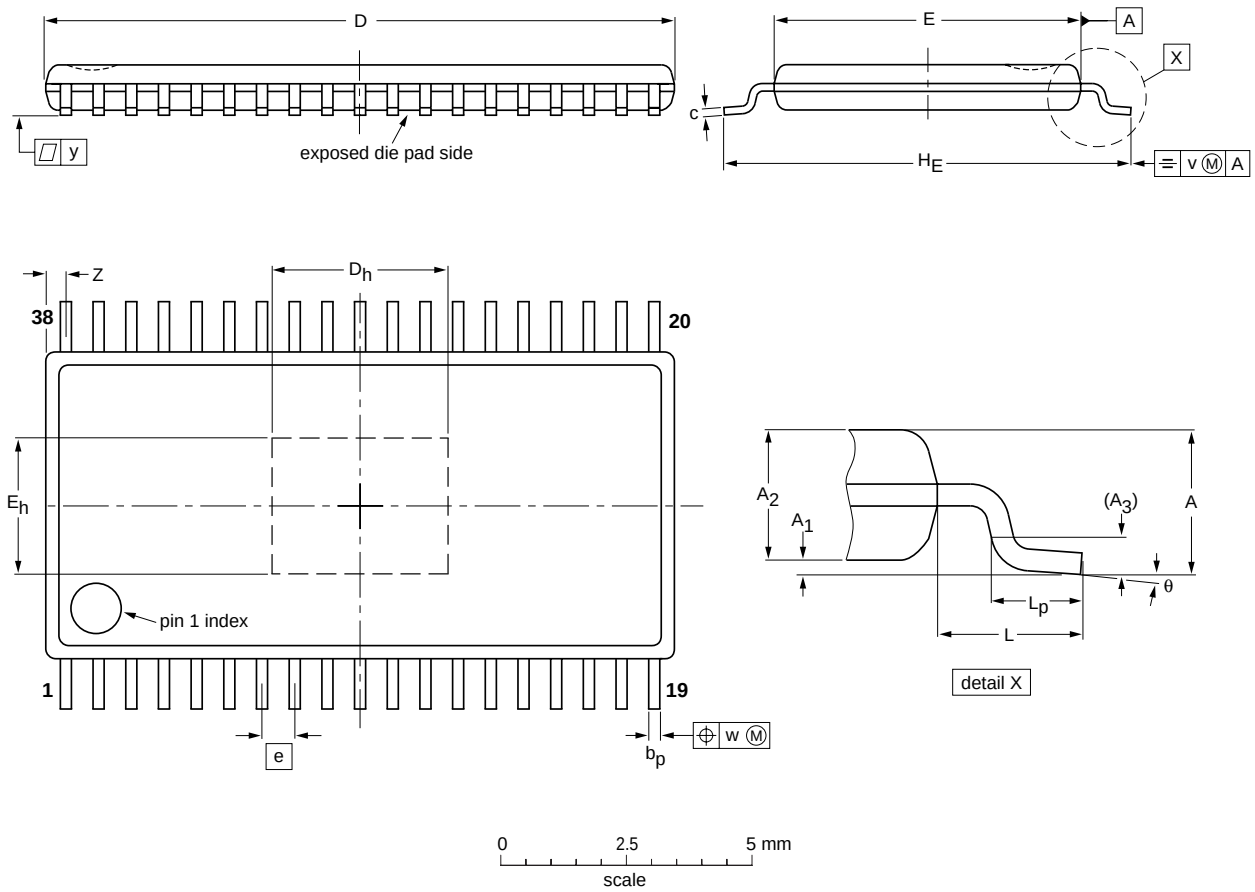
Application design

The performance of the application using the TDA8260TW strongly depends on the application design itself. Furthermore the printed-circuit board design and the soldering conditions should take into account the exposed die pad underneath the device, as this requires an optimum electrical ground path for electrical performance, together with the capability to dissipate into the application the heat created in the device. Philips Semiconductors can provide support through reference designs and application notes for TDA8260TW together with associated channel decoders. Please contact your local Philips Semiconductors sales office for more information.

Wave soldering is not suitable for the TDA8260TW package. This is because the heatsink needs to be soldered to the printed-circuit board underneath the package but with wave soldering the solder cannot penetrate between the printed-circuit board and the heatsink.

PACKAGE OUTLINE

HTSSOP38: plastic thermal enhanced thin shrink small outline package; 38 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad **SOT633-3**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	D_h	E(2)	E_h	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.80	0.25	0.30 0.19	0.20 0.09	12.6 12.4	3.65 3.45	6.2 6.0	2.85 2.65	0.65	8.3 7.9	1	0.75 0.45	0.2	0.1	0.1	0.6 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT633-3	- - -	- - -	- - -			04-01-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar soldering or manual soldering is suitable for PMFP packages.

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SCA77

Printed in The Netherlands R25/03/pp23 Date of release: 2005 Jan 11 Document order number: 9397 750 14556

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