# DATA SHEET

# PCF50732
## GSM baseband and audio interface

Product specification
Supersedes data of 1999 May 03
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Philips
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**CONTENTS**

## 1 FEATURES

- Low power and low voltage device in 0.25 micron CMOS technology; supply voltage: analog 2.7 V (typical) and digital 1.5 V (typical)
- Compatible with GSM phase 2 and DCS1800 recommendations
- Complete in-phase and quadrature component interface paths between the Digital Signal Processor (DSP) and RF circuitry
- Complete linear PCM CODEC for audio signal conversion between earphone/microphone and DSP
- Four auxiliary analog inputs for measurement purposes (e.g. battery monitoring)
- Three auxiliary analog outputs for control purposes (i.e. AFC, AGC and power ramping control)
- Separate baseband, audio and control serial interfaces
- Voice band Signal Processor (VSP) for flexible audio data processing.

## 2 APPLICATIONS

Wireless telephone handsets conforming to the GSM recommendations phases 1 and 2, DCS1800 and PCS1900.

## 3 GENERAL DESCRIPTION

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the Digital Signal Processor (DSP). It consists of three parts:

- The **receive path**, which transforms the quadrature signals from the RF (I/Q) to digital signals
- The **transmit path**, which transforms a bitstream to analog quadrature signals for the RF devices
- The digital **Baseband Serial Interface (BSI)**, which exchanges baseband data between the PCF50732 and the digital signal processor. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

The voice band CODEC is a complete analog front-end circuit. It consists of four parts:

- The **receive path**, which converts a digital signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives the analog external signal from a microphone and converts it into a digital signal
- The **Voice band Signal Processor (VSP)**, which filters the voice band data
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to an external DSP. The voice band data is coded in 16-bit linear PCM two's complement words.

The **auxiliary Analog-to-Digital Converter (ADC)** section consists of four input channels specified for battery management applications.

The **auxiliary Digital-to-Analog Converter (DAC)** section consists of three DACs for Automatic Gain Control (AGC), for Automatic Frequency Control (AFC) and for power ramping.

The **Control Serial Interface (CSI)** is used to program a set of control registers, to store the power amplifier ramping characteristics into the dedicated RAM and to transmit auxiliary ADC values to the DSP. It also controls switches, modes and power status of the different parts of the IC.

## 4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| PCF50732H | LQFP48 | plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm | SOT313-2 |

## 5 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage | | 1.0 | 1.5 | 2.75 | V |
| $V_{DDA}$ | analog supply voltage | $V_{DDA} \geq V_{DDD}$ | 2.5 | 2.7 | 2.75 | V |
| $I_{DDA}$ | analog supply current | $V_{DDD}$ = 1.5 V; $V_{DDA}$ = 2.7 V; RXON active | – | 3.5 | – | mA |
| $P_{av}$ | average power consumption | $V_{DDD}$ = 1.5 V; $V_{DDA}$ = 2.7 V; note 1 | – | 15 | – | mW |
| $I_{stb(tot)}$ | total standby current | | – | 10 | – | µA |
| $f_{clk}$ | master clock frequency | | – | 13.0 | – | MHz |
| $T_{amb}$ | ambient temperature | | –40 | +27 | +85 | °C |

**Note**

1. Without load on audio outputs EARP, EARN, AUXSP and BUZ.

## 6 BLOCK DIAGRAM

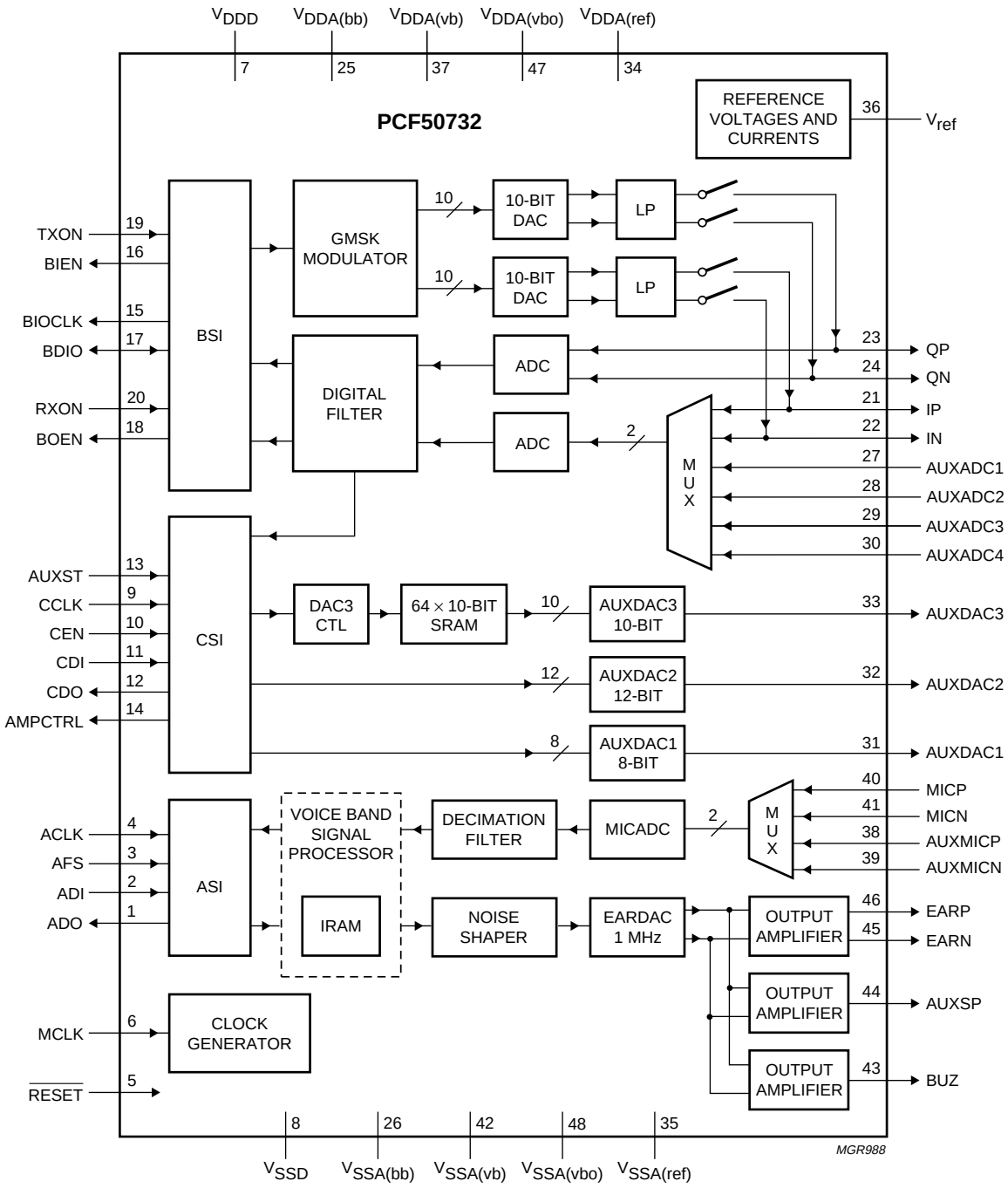



Fig.1 Block diagram.

## 7 PINNING

| SYMBOL | PIN | TYPE[1] | ACTIVE LEVEL | ACTIVE EDGE | $I_{DD}$ | DESCRIPTION |
|---|---|---|---|---|---|---|
| ADO | 1 | O/TS | – | – | 1.5 mA | audio digital interface PCM data output to DSP |
| ADI | 2 | I | – | – | – | audio digital interface PCM data input from DSP |
| AFS | 3 | I | – | rising | – | audio digital interface PCM frame synchronization signal input from DSP |
| ACLK | 4 | I | – | rising | – | audio digital interface PCM clock signal input from DSP |
| $\overline{\text{RESET}}$ | 5 | I | LOW | – | – | asynchronous reset input |
| MCLK | 6 | I | – | rising | – | low-swing master clock input; $f_{clk}$ = 13 MHz; integrated capacitive coupling |
| $V_{DDD}$ | 7 | P | – | – | – | digital supply voltage |
| $V_{SSD}$ | 8 | G | – | – | – | digital ground supply |
| CCLK | 9 | I | – | falling | – | control bus clock input from DSP |
| CEN | 10 | I | LOW | – | – | control bus data enable input from DSP |
| CDI | 11 | I | – | – | – | control bus data input from DSP |
| CDO | 12 | O/TS | – | – | 1.5 mA | control bus data output to DSP |
| AUXST | 13 | I | HIGH | – | – | status control signal input for activation of AUXDAC1, AUXDAC2 and MCLK input |
| AMPCTRL | 14 | O | – | – | 1.5 mA | general purpose output pin |
| BIOCLK | 15 | O/TS | – | – | 3 mA | baseband interface data clock output |
| BIEN | 16 | O | LOW | – | 1.5 mA | baseband transmit interface data enable signal output |
| BDIO | 17 | I/O | – | – | 1.5 mA | baseband interface data I/O from and to DSP |
| BOEN | 18 | O | LOW | – | 1.5 mA | baseband receive interface data enable signal output |
| TXON | 19 | I | HIGH | – | – | baseband transmit path activation signal input |
| RXON | 20 | I | HIGH | – | – | baseband receive path activation signal input |
| IP | 21 | I/O | – | – | – | baseband-I differential positive input/output to IF circuit |
| IN | 22 | I/O | – | – | – | baseband-I differential negative input/output to IF circuit |
| QP | 23 | I/O | – | – | – | baseband-Q differential positive input/output to IF circuit |
| QN | 24 | I/O | – | – | – | baseband-Q differential negative input/output toIF circuit |
| $V_{DDA(bb)}$ | 25 | P | – | – | – | baseband supply voltage (analog) |
| $V_{SSA(bb)}$ | 26 | G | – | – | – | baseband ground supply (analog) |
| AUXADC1 | 27 | I | – | – | – | auxiliary ADC input 1 for battery voltage measurement |
| AUXADC2 | 28 | I | – | – | – | auxiliary ADC input 2 |
| AUXADC3 | 29 | I | – | – | – | auxiliary ADC input 3 |
| AUXADC4 | 30 | I | – | – | – | auxiliary ADC input 4 |
| AUXDAC1 | 31 | O | – | – | – | auxiliary DAC output for AGC; maximum load 50 pF // 2 kΩ |
| AUXDAC2 | 32 | O | – | – | – | auxiliary DAC output for AFC; maximum load 50 pF // 10 kΩ |
| AUXDAC3 | 33 | O | – | – | – | auxiliary DAC output for power ramping; maximum load 50 pF, ±600 μA |
| $V_{DDA(ref)}$ | 34 | P | – | – | – | reference voltage supply voltage (analog) |

| SYMBOL | PIN | TYPE(1) | ACTIVE LEVEL | ACTIVE EDGE | $I_{DD}$ | DESCRIPTION |
|---|---|---|---|---|---|---|
| $V_{SSA(ref)}$ | 35 | G | – | – | – | reference voltage ground supply (analog) |
| $V_{ref}$ | 36 | I/O | – | – | – | band gap reference voltage noise decoupling |
| $V_{DDA(vb)}$ | 37 | P | – | – | – | voice band voltage supply voltage |
| AUXMICP | 38 | I | – | – | – | auxiliary microphone differential positive input |
| AUXMICN | 39 | I | – | – | – | auxiliary microphone differential negative input |
| MICP | 40 | I | – | – | – | microphone differential positive input |
| MICN | 41 | I | – | – | – | microphone differential negative input |
| $V_{SSA(vb)}$ | 42 | G | – | – | – | voice band ground supply |
| BUZ | 43 | O | – | – | – | buzzer output |
| AUXSP | 44 | O | – | – | – | auxiliary speaker output |
| EARN | 45 | O | – | – | – | earphone differential negative output |
| EARP | 46 | O | – | – | – | earphone differential positive output |
| $V_{DDA(vbo)}$ | 47 | P | – | – | – | voice band output buffer supply voltage (analog) |
| $V_{SSA(vbo)}$ | 48 | G | – | – | – | voice band output buffer ground supply (analog) |

**Note**

1. O/TS = 3-state output; I = input; P = power supply; G = ground supply; I/O = input/output.

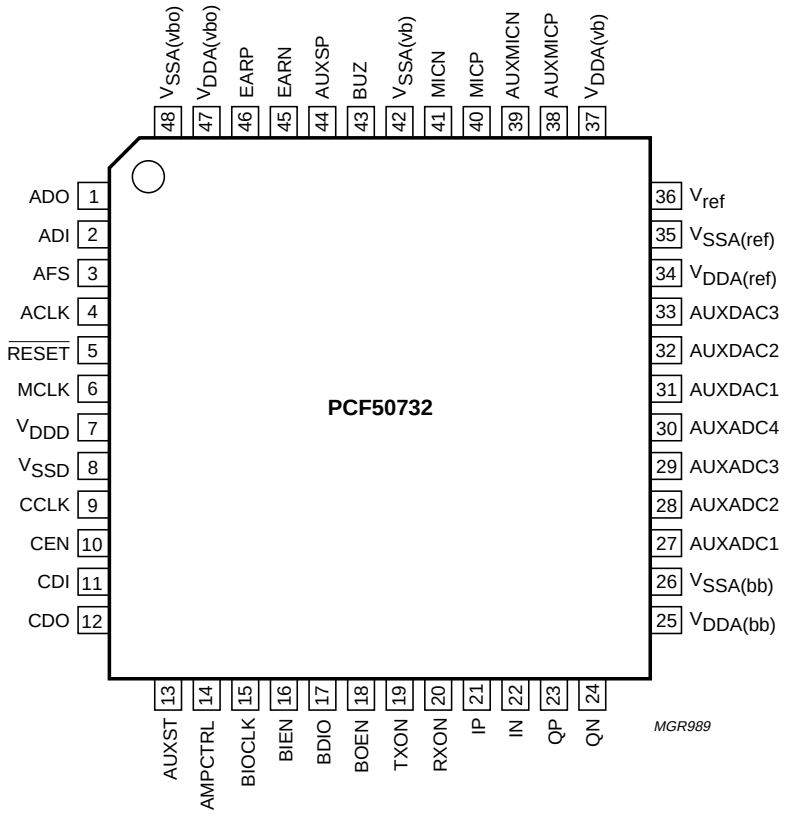



Fig.2 Pin configuration.

## 8 FUNCTIONAL DESCRIPTION

This chapter gives a brief overview of the device. The detailed functional description can be found in the following chapters:

Chapter 9 “Baseband CODEC”

Chapter 10 “Voice band CODEC”

Chapter 11 “Auxiliary functions”

Chapter 12 “Control Serial Interface (CSI)”

Chapter 13 “Voice band Signal Processor (VSP)”.

### 8.1 General

As low power consumption in mobile telephones is a very important issue, all the circuit parts in the PCF50732 can be powered-on/off either by means of the external signals AUXST, TXON or RXON, or by programming the respective register bits in the Control Serial Interface (CSI).

The most important signal for the digital and analog circuit functions in the PCF50732 is the DAC enable signal AUXST, which allows to activate AUXDAC1 (AGC) and AUXDAC2 (AFC), as well as the low-swing master clock input MCLK. AUXST must be active (HIGH) and **$V_{DDA}$ must be stable** (see also Section 18.1) to allow the master clock to access different circuit parts after a reset ($\overline{\text{RESET}}$ active). AUXDAC1 and AUXDAC2 are only activated if their related power-on bit is set. AUXDAC1 is default off, AUXDAC2 is default on.

$\overline{\text{RESET}}$ must be active during at least 3 MCLK cycles, with AUXST active, to ensure a correct initialization of all the digital circuitry of the PCF50732. Since $\overline{\text{RESET}}$ is asynchronous, even small spikes of a few nanoseconds can cause partial resets.

For power supply noise interference reduction, a pair of supply voltage and ground supply pins are provided for the:

- Baseband analog: $V_{DDA(bb)}$ and $V_{SSA(bb)}$
- Voice band analog: $V_{DDA(vb)}$ and $V_{SSA(vb)}$
- Voice band output drivers: $V_{DDA(vbo)}$ and $V_{SSA(vbo)}$
- DC reference voltages and currents: $V_{DDA(ref)}$ and $V_{SSA(ref)}$
- Digital circuitry: $V_{DDD}$ and $V_{SSD}$.

All $V_{SS}$ pins are connected internally. $V_{DDD}$ is the digital supply. $V_{DDA(bb)}$, $V_{DDA(vb)}$, $V_{DDA(vbo)}$, and $V_{DDA(ref)}$ are analog supplies, and are referred to as $V_{DDA}$ throughout this document. These analog supplies must be connected externally.

### 8.2 Baseband and voice band reference voltages

The reference voltage $V_{ref}$ is generated on-chip by a band gap voltage reference circuit and is available at pin $V_{ref}$.

As $V_{ref}$ is used as reference for most of the internal analog circuitry, noise must be kept as low as possible by connecting an external decoupling capacitor at this pin.

The voltage at $V_{ref}$ is buffered to generate the baseband and voice band reference voltage $V_{ref}$ as well as internal references for the different functions, such as the auxiliary and the transmit DACs.

## 9 BASEBAND CODEC

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the digital signal processor. It consists of three parts:

- The **transmit path**, which converts a bitstream to analog quadrature signals for the RF devices
- The **receive path**, which transforms the quadrature signals of the IF circuit (I/Q) to digital signals
- The digital **baseband serial interface**, which exchanges baseband data between the PCF50732 and the DSP. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

### 9.1 Baseband transmit path

The baseband transmit path consists of three parts:

- **GMSK modulator:** generation of a Gaussian Minimum Shift Keying (GMSK) signal
- **10-bit DACs:** digital-to-analog converters for the I and Q components of the GMSK signal
- **Low-pass filters:** analog reconstruction low-pass filters for the output of the DACs.

The requirements of the transmit path of a GSM terminal are given by *“GSM recommendation 05.05”*:

- Phase RMS error <5°
- Phase peak error <20°
- Amplitude error < ±1 dB.

Nevertheless the performance of the PCF50732 is far better than these figures indicate; see Section 18.1.

#### 9.1.1 GMSK MODULATOR

The input signal of the GMSK modulator is a bitstream coming from the baseband serial interface with a sampling frequency of 270.833 kHz. Typically 148 bits are modulated during a normal burst, and 88 bits during an access burst. Using this bitstream, the GMSK modulator generates digital I and Q components as described in *"GSM recommendation 05.04"*.

This is done in three steps:

1. First the incoming bitstream is differentially encoded by an EXOR operation on the actual bit and the previous bit.
2. The instantaneous phase (φ) is calculated using a gaussian filter with an impulse response of 4 taps.
3. A look-up table provides the cosine (I component) and the sine values (Q component) of the phase (φ).

   The look-up table also interpolates the signal to a 16 times higher frequency (4.333 MHz).

#### 9.1.2 10-BIT DACS

The two 10-bit DACs are working at a sampling rate of 4.3333 MHz. They convert the digital I and Q components of the GMSK modulator to differential analog I and Q signals.

#### 9.1.3 LOW-PASS FILTER

The analog output signals of the DACs are filtered by analog reconstruction low-pass filters.

These filters remove high frequency components of the DAC output signals and attenuate components around the 4.3333 MHz sampling frequency. The low-pass filters have a cut-off frequency of approximately 300 kHz, with very linear phase behaviour in the pass band.

### 9.2 Baseband receive path

The baseband receive path consists of two parts:

- **Receive ADC:** ΣΔ analog-to-digital converters
- **Decimator**: digital decimators for I and Q.

The baseband receive section can be switched between two modes of operation:

- ZIF (zero IF) mode for radio sections, which convert the receive signal down to baseband. In this mode the ADC is sampled at 6.5 MHz, the decimator samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers $2 \times 12$-bit values for I and Q components at 270.833 kHz.
- NZIF (near zero IF) mode for radio sections, which converts the receive signal down to a centre frequency of 100 kHz. In this mode the ADC is sampled at 13 MHz, the decimator samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers $2 \times 12$-bit values for I and Q components at 541.667 kHz.

#### 9.2.1 RECEIVE ADC

The receive ADCs are ΣΔ analog-to-digital converters that convert differential input signals into1-bit data streams with a sampling frequency of 6.5 or 13 MHz.

#### 9.2.2 DIGITAL DECIMATOR

Digital filtering is required for:

- Suppression of out-of-band noise produced by the ΣΔ ADC
- Decimation of the sampling rate (6.5 or 13 MHz) by 24
- System level filtering.

The digital filtering is performed by a digital FIR filter with a group delay for this running average filter of approximately 23 or 11.5 μs respectively. The filter uses two's complement arithmetic.

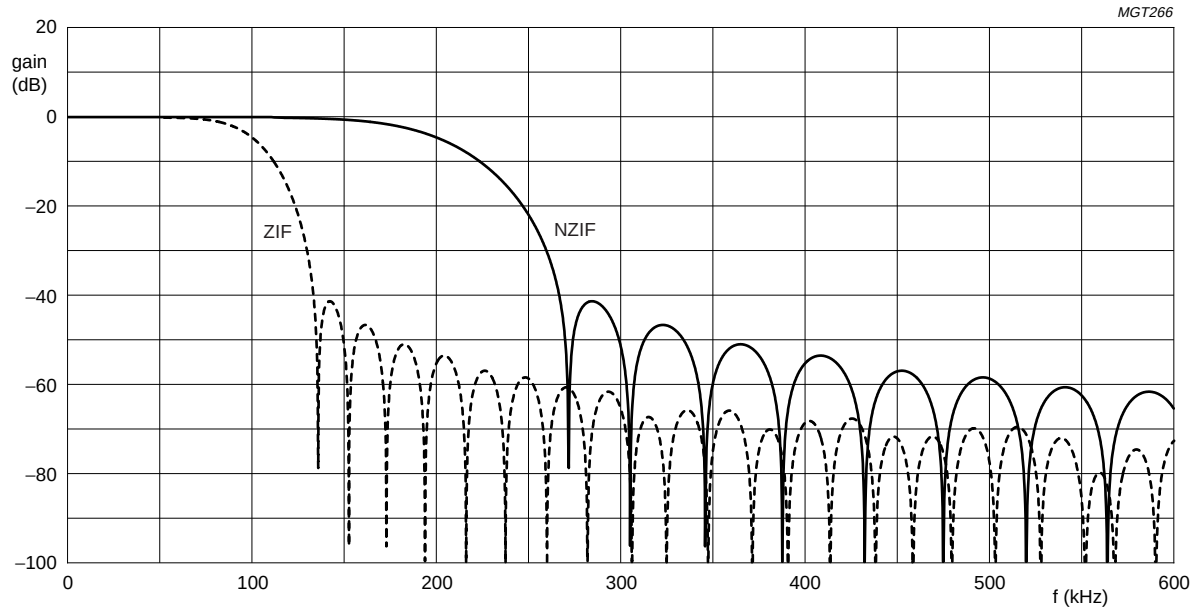



Fig.3 Transfer functions for the baseband receive filter.

### 9.3 Baseband Serial Interface (BSI)

#### 9.3.1 Overview

The digital part of the baseband interface consists of a receive section and a transmit section. The receive section is a FIR filter that reduces the 6.5 MHz (13 MHz for NZIF mode) bitstream from the sigma-delta converters into 2 × 12-bit values at 270.833 kHz (541.667 kHz for NZIF mode).

The transmit section converts the 270.833 kHz data stream from the DSP into a GMSK signal sampled at 4.333 MHz. The 10-bit I and Q signals are then fed into two 10-bit DACs. The power ramping signal is also generated by the transmit section with the 10-bit AUXDAC3 block.

#### 9.3.2 Transmit path block description

##### *9.3.2.1 Transmit serial interface*

The power-up of the BSI transmit path is controlled via the TXON pin. When TXON is pulled HIGH, the transmit path recovers from power-down. The MCLK/48 = 270.833 kHz output signal BIOCLK is activated. When the BIEN0 period has elapsed the output signal BIEN goes LOW and the bits to be transmitted are clocked out of the DSP.

BIEN0 must be at least 10 quarterbits long to allow settling of the analog filters. Bits are clocked out of the DSP by the falling edge and clocked into the PCF50732 by the rising edge of BIOCLK. After the BIEN1 period has elapsed, BIEN is set HIGH again and transmission from the DSP ends. Logic 1s are modulated whenever BIEN is HIGH and the baseband transmit (BBTX) block is active. Values for BIEN0 and BIEN1 can be set in the Burst control register.

Figure 5 shows the timing for the BSI data transmission. In Power-down mode the de-asserted value of BIOCLK is high-Z and BIEN is HIGH. Typical connection to the system DSP is defined in Table 1.

**Table 1** Connection of BSI transmit signals to PCF5087X

| PCF50732 | | PCF5087X | |
|---|---|---|---|
| **PIN** | **I/O** | **PIN** | **I/O** |
| TXON | I | RFSIG[y] | O |
| BDIO | I/O | SIOXD | I/O |
| BIEN | O | SOXEN_N | I |
| BIOCLK | O | SIOXCLK | I |

*9.3.2.2 Power ramping controller*

The PCF50732 fully supports all multislot modes which do not require full duplex operation or more than two consecutive transmit bursts. In this specification double burst mode is used for all supported multislot modes while single burst mode supports the normal GSM modes.

The power ramping controller drives the power amplifier output envelope.

In each transmit (TX) burst one ramp-up and one ramp-down will be carried out. In multislot mode one intermediate ramp will be carried out in addition to ramp-up and ramp-down. Each ramp consists of 16 discrete step values that are sent to the DAC3. The duration of each step is 2 quarterbits which translates into 8-bit long ramps. The DAC3 output is pulled LOW whenever DAC3 is powered down. The ramping step values are stored in a $64 \times 10$-bit RAM as shown in Table 2.

In order to initialize AUXDAC3 it is necessary to write into the RAM all 32 (or 48 in multislot mode) DAC3 output values. Filling the RAM is normally done by writing a logic 0 to the address sub-register of the burst control register, after which 32 or 48 values, depending on multislot mode, can be written into the data sub-register of the burst control register. Writing to the DAC3 RAM is only possible when the DAC3 is powered off.

Total number of CSI accesses is therefore 33 for a normal burst and 49 for a double burst.

An auto-increment feature will store these data into the correct RAM positions.

The value after power-up of DAC3 will always be equal to the value of RAM location 47.

AUXDAC3 timing is controlled by the Burst control register. This contains the following sub-registers:

- The **RU register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-up ramping; default value is 0
- The **RM register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the intermediate power ramp; default value is 0. RM is only used in case of multislot mode
- The **RD register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-down ramping; default value is 0
- DAC3 burst RAM address register
- DAC3 burst RAM data register
- Single/double burst mode register: normal mode or multislot mode selection flag.

After TXON goes HIGH and a time equal to RU quarterbit periods has elapsed, power ramp-up is done.

After a time period equal to RD quarterbits has elapsed, power ramp-down is initiated.

The AUXDAC3 output is also shown in Fig.4.

Values for RU (ramp-up) and RD (ramp-down) can be set in the burst control register of the control serial interface. RD must be greater than RU + 32. RU and RD range from 0 to 4000 QB (quarterbit). The register offers the possibility to enter codes up to 4095.

The GMSK modulator is active for a period of 2 clock cycles after the ramp-down or for the length of the TXON burst, whichever is longer.

Multislot (high-speed switched data mode) can be selected by setting the appropriate bit in the burst control register. In multislot mode an intermediate ramping step is done. This intermediate step is started after a time period equal to RM quarterbits has elapsed. A value for RM (intermediate ramp) is also set using the burst control register. The following conditions must be true:

RU + 32 < RM and RM + 32 < RD

In single slot mode the condition is:

RU + 32 < RD

**Table 2** AUXDAC3 RAM contents

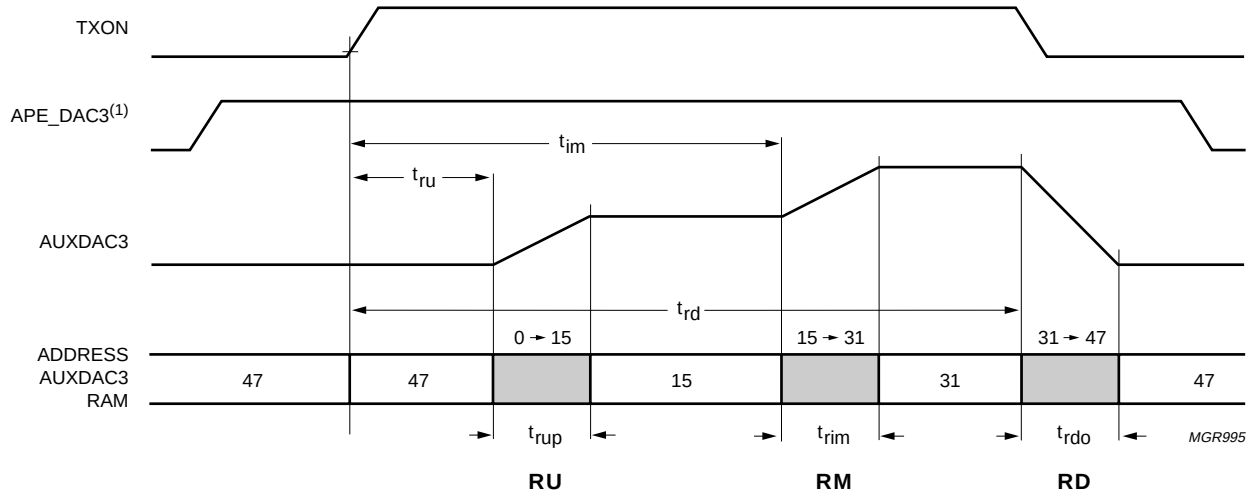
| RAM ADDRESS | DATA |
|---|---|
| 0 to 15 | ramp-up data |
| 16 to 31 | intermediate ramp data |
| 32 to 47 | ramp-down data |
| 48 to 64 | not used |

**Table 3** Power ramping timing characteristics

| SYMBOL | VALUE | COMMENTS(1) |
|---|---|---|
| $t_1$ | 76.9 ns | MCLK cycle time |
| $t_0$ | $12t_1$ | 1 QB |
| $t_{ru}$ | RU register | 0 to 4000 QB |
| $t_{im}$ | RM register | RU + 32 to 4000 QB |
| $t_{rd}$ | RD register | RM + 32 to 4000 QB |
| $t_{rup}$, $t_{rim}$, $t_{rdo}$ | $32t_0$ | 8 bits; 32 QB |

**Note**

1. QB: Quarterbit, usually referred to the time needed for one quarter of a GSM baseband bit, i.e. a frequency of $^1/_{12} \times 13$ MHz.




(1) APE_DAC3: Analog Power Enable signal for the AUXDAC3.

Fig.4 Power ramping timing characteristics (multislot mode).

### 9.3.3 RECEIVER PATH BLOCK DESCRIPTION

#### *9.3.3.1 Receive serial interface*

The baseband serial interface sends the digital signal of the receive path to a digital signal processor. It also takes the digital bitstream from the digital signal processor and transmits it via the baseband CODEC.

The baseband reception and transmission are active in bursts. A normal burst has a length of 548 μs. The frame rate of bursts is 4.615 ms. Using a normal traffic channel, one burst for each frame is transmitted and two bursts are received. To save as much power as possible, the transmit path and the receive path of the PCF50732 are in power-up mode only during the transmission or reception bursts respectively.

The power-up of the receive section is controlled via the pin RXON or bit RXON. When RXON is driven HIGH, the receive section recovers from power-down and the output clock BIOCLK is activated. After a settling delay of 52 μs (ZIF mode, analog circuitry + decimator settling time), BOEN goes LOW to transfer the first 12-bit I and Q words. The settling time is only 26 μs in NZIF mode.

Bits are clocked out of the PCF50732 by the falling edge, and clocked into the DSP by the rising edge of BIOCLK. In normal bursts 148 I/Q pairs are read from the PCF50732.

When RXON goes LOW, the last pair of I and Q values will be sampled and transferred to the baseband processor (both I and Q components). BIOCLK stops after additional 16 BIOCLK cycles. The receive path is powered down again. In power-down the BIOCLK output is put in 3-state and the BOEN output is HIGH.

The output format is $2 \times 12$-bit I/Q (two's complement). Transmission occurs MSB first, I followed by Q. The serial clock signal BIOCLK will run at 6.5 MHz, or 13 MHz in the NZIF mode. Figure 6 shows the timing of the BSI data reception.

An automatic offset compensation mechanism is provided in order to achieve the required performance. This mechanism will short the receive (RX) inputs internally and measure the resulting offset value. This offset value will be subtracted from all subsequent I/Q output words.
The offset inherent to the device can thereby be reduced to a few millivolts. Default value for both I- and Q-offset is zero.

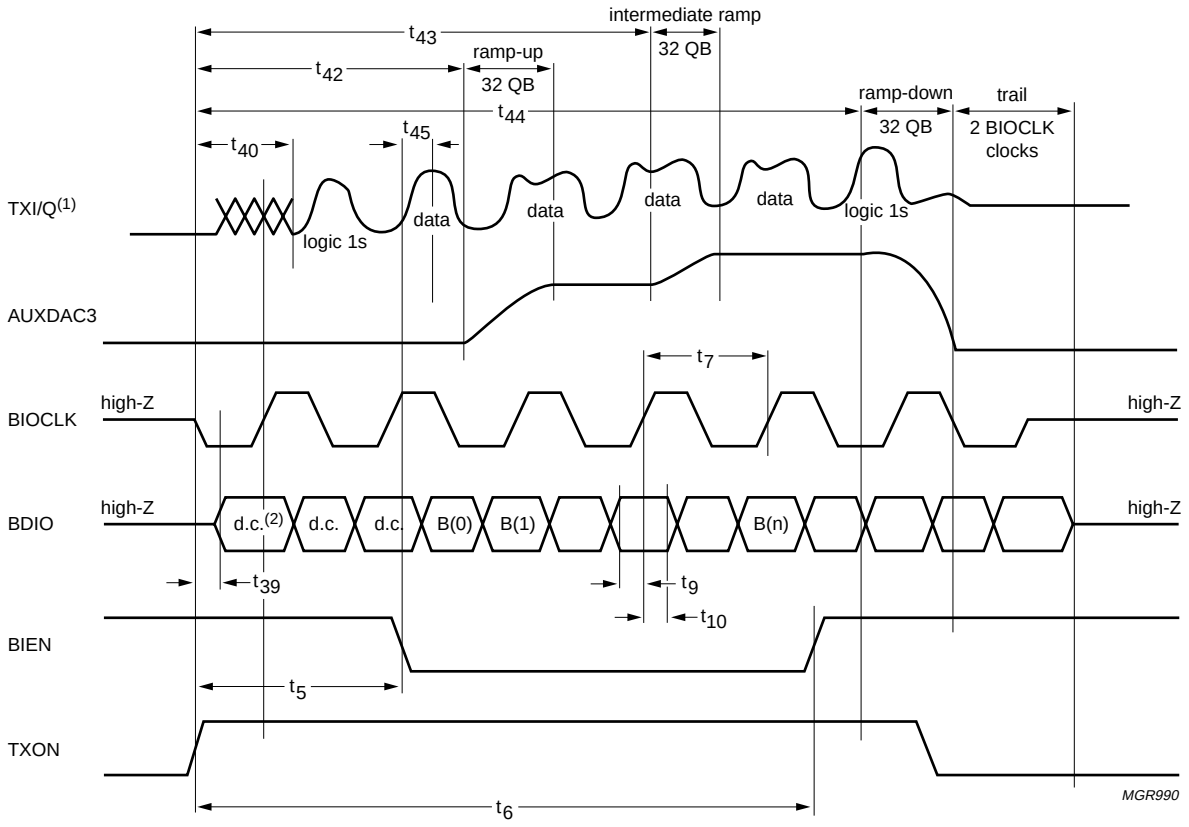
Offset compensation measurement can be done on three channels separately: baseband receive I channel, baseband receive Q channel and AUXADC channel. All AUXADC channels use the same offset compensation value. Starting an offset measurement is done by writing a logic 1 into the offset trigger register for each channel that needs calibration. If the value '7' (decimal) is written into the offset trigger register offsets will be measured for I, Q and AUXADC channels.

Offsets can also be read or written directly. Each offset measurement is implemented internally as an AUXADC measurement and takes approximately 100 µs.
Offsets from –256 up to +255 can be compensated.

**Table 4** Connection of BSI receive signals to the PCF5087X

| PCF50732 | | PCF5087X | |
|---|---|---|---|
| **PIN** | **I/O** | **PIN** | **I/O** |
| RXON | I | RFSIG[z] | O |
| BDIO | I/O | SIOXD | I/O |
| BOEN | O | SIXEN_N | I |
| BIOCLK | O | SIOXCLK | I |

### 9.3.4 Baseband Serial Interface (BSI) timing characteristics




(1) TXI/Q = transmit I or Q.
(2) d.c. = don't care; will be overwritten with logic 1.

Fig.5 Timing of the baseband serial interface transmit path; for the timing values see Table 5.

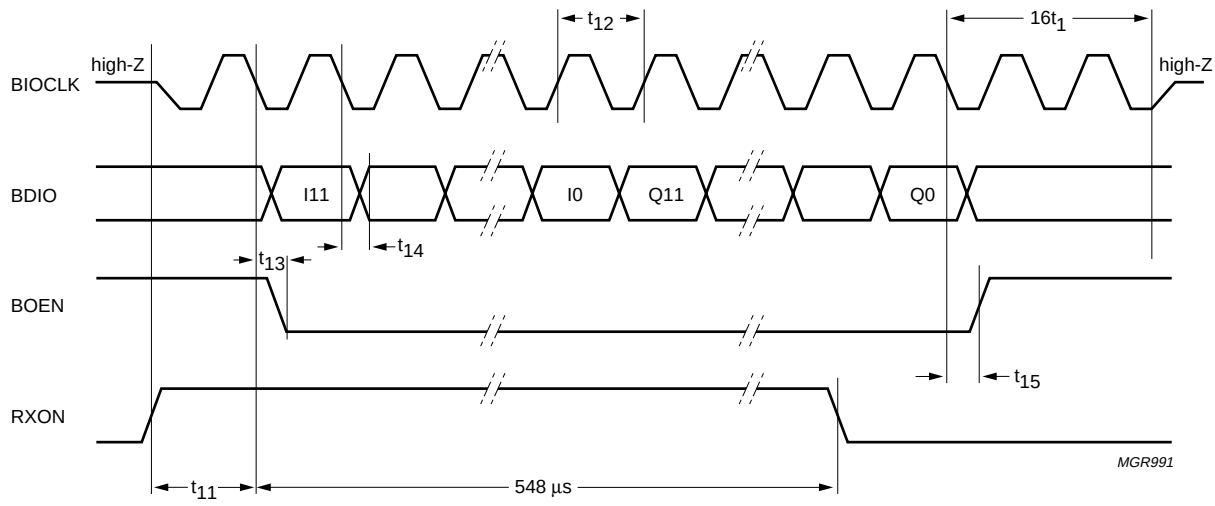



Fig.6 Timing of the baseband serial interface receive path; for the timing values see Table 5.

**Table 5** BSI timing characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Master clock** | | | | | |
| $t_1$ | MCLK cycle time | – | 76.9 | – | ns |
| $t_2$ | MCLK LOW time | 30 | $\frac{1}{2}t_1$ | – | ns |
| $t_3$ | MCLK HIGH time | 30 | $\frac{1}{2}t_1$ | – | ns |
| $t_4$ | $\overline{\text{RESET}}$ LOW time | $3t_1$ | – | – | ns |
| **Baseband Serial Interface (BSI) transmit path** (see Fig.5) | | | | | |
| $t_5$ | BIEN0 value | 10 | – | 511 | QB |
| $t_6$ | BIEN1 value | $t_5$ | – | 4000 | QB |
| $t_7$ | BIOCLK cycle time | – | $48t_1$ | – | ns |
| $t_9$ | data set-up time | 20 | – | – | ns |
| $t_{10}$ | data hold time | 20 | – | – | ns |
| $t_{39}$ | BIOCLK active after TXON rising edge | – | – | $t_1$ | ns |
| $t_{40}$ | analog TX and GMSK power-up time | – | – | 17.4 | QB |
| $t_{42}$ | ramp-up value | 0 | – | 3940 | QB |
| $t_{43}$ | intermediate ramp value | $32 + t_{42}$ | – | 3980 | QB |
| $t_{44}$ | ramp-down value | | | | |
| | normal mode | $32 + t_{42}$ | – | 4020 | QB |
| | double burst mode | $32 + t_{43}$ | – | 4020 | QB |
| $t_{45}$ | first data out after BIEN falling edge | – | 10 | – | µs |

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Baseband Serial Interface (BSI) receive path** (see Fig.6) | | | | | |
| $t_{11}$ | analog power-up and filter settling time | | | | |
| | ZIF mode | – | 52 | – | µs |
| | | – | 120 | – | QB |
| | NZIF mode | – | 26 | – | µs |
| | | – | 60 | – | QB |
| $t_{12}$ | BIOCLK cycle time | | | | |
| | ZIF mode | – | $2t_1$ | – | ns |
| | NZIF mode | – | $t_1$ | – | ns |
| $t_{13}$ | BOEN LOW after falling clock edge | – | – | 15 | ns |
| $t_{14}$ | BIOCLK falling edge to data valid | – | – | 15 | ns |
| $t_{15}$ | BOEN HIGH after falling clock edge | – | – | 15 | ns |

## 10 VOICE BAND CODEC

The voice band CODEC is a complete analog front-end circuit. It consists of three parts:

- The **receive path**, which converts a digital linear PCM signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives an analog signal from a microphone or an auxiliary input and converts it into a digital linear PCM signal
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to a digital signal processor.

Various functions and characteristics of the voice band CODEC can be selected by programming the corresponding control registers in the Control register block (see also Tables 11, 22, 23, 24 and 26).

### 10.1 Voice band receive path

The voice band receive path consists of the following parts:

- The receive part of the voice band signal processor
- **NOISE SHAPER:** 3rd-order digital ΣΔ modulator, generates a bitstream at 1 MHz to drive the EARDAC
- **EARDAC:** digital-to-analog converter including low-pass filter for high frequency noise content of noise shaper
- **EARAMP:** amplifier for an earpiece
- **AUXAMP:** amplifier for an auxiliary loudspeaker
- **BUZAMP:** amplifier for a buzzer output.

Linearity of receiver equipment (to earpiece) at EARPGA = 0 dB and a volume control (VOLPGA and EARAMP or AUXAMP) of −12 dB, signal-to-total harmonic distortion ratio according to *“GSM recommendation II.11.10 V.4.16.1”*.

#### 10.1.1 RXVOL

RXVOL controls the volume of the voice band receive path. In conjunction with EARAMP, AUXAMP and BUZAMP it allows a gain variation from +6 to −30 dB in 64 steps; see Table 26. RXVOL also provides a mute selection of the three outputs EARP/EARN, AUXSP and BUZ respectively. At $\overline{\text{RESET}}$ the volume is automatically set to −12 dB.

#### 10.1.2 RXPGA

RXPGA controls the gain of the voice band receive path within a range of −24 to +12 dB in 64 steps for calibration purposes.

#### 10.1.3 RXFILTER

RXFILTER is a digital band-pass filter with a pass band from 300 to 3400 Hz. It is realized by a programmable structure (voice band signal processor).

#### 10.1.4 EARDAC

EARDAC is a DAC operating at a sampling frequency of 1 MHz. It converts the bitstream input to a sampled differential analog signal and it is a low-pass filter for the output signal at the same time.

#### 10.1.5 EARAMP

EARAMP is an amplifier, capable of driving a standard earpiece with a minimum impedance of 8 Ω in single-ended mode or 16 Ω in differential mode.

#### 10.1.6 AUXAMP

AUXAMP is an amplifier for connection to an external loudspeaker amplifier of minimum 8 Ω (hands-free car kit).

An **'auxiliary speaker external amplifier control'** (pin AMPCTRL) can be used to switch on/off an external amplifier (hands-free car kit). The status of AMPCTRL is programmable via the control serial interface; its default value is on.

#### 10.1.7 BUZAMP

BUZAMP is an amplifier for connection to an external buzzer of minimum 8 Ω. It has the same output characteristics as the AUXAMP and can hence be used as a second auxiliary output amplifier. It is switched on/off by a dedicated control bit in the Control register block.

### 10.2 Voice band transmit path

The voice band transmit path consists of the following parts:

- **MICMUX:** microphone input multiplexer
- **MICADC:** ΣΔ analog-to-digital converter
- **DECIMATOR:** decimates the incoming bitstream from 1 MHz to 40 kHz
- **TXFILTER:** band-pass filter for the digital transmit signal and down-sampling
- **TXPGA/LIM:** fine-programmable gain for calibration, limiter
- **SidePGA:** voice band sidetone programmable gain amplifier.

Linearity of transmitter equipment, signal-to-total harmonic distortion ratio according to *"GSM recommendation II.11.10 V.4.16.1"*.

#### 10.2.1 MICMUX

MICMUX is used to select between a differential signal at pins MICP and MICN and a differential signal at pins AUXMICP and AUXMICN.

Values are specified for a standard electret microphone with a sensitivity of −64 ±3 dB for high gain or for an external microphone with an amplifier sensitivity of −26 ±3 dB (0 dB ≡ 1 V/0.1 Pa = 1 V/μbar; at 1 kHz).

#### 10.2.2 MICADC

MICADC is a ΣΔ analog-to-digital converter which generates a 1 MHz bitstream.

#### 10.2.3 DECIMATOR AND TXFILTER

The decimator is a digital filter, which performs a signal processing to a lower sampling rate at the output compared to the input.

The bitstream with a sampling frequency of 1 MHz is low-pass filtered and down-sampled to 40 kHz by a FIR filter.

A digital high-pass filter and a digital low-pass filter (both IIR filters) process the 14-bit input samples to achieve a band-pass with a pass band from 300 to 3400 Hz. These filters run on the on-chip voice band signal processor (see Fig.7). Its program is down-loaded into the instruction memory (IRAM) via the CSI (see Table 28).

The output of the TXFILTER is down-sampled to a sampling frequency of 8 kHz with a word length of 16 bits.

#### 10.2.4 TXPGA

TXPGA adapts the analog signals coming from MICMUX within a range of −30 to +6 dB. It is designed for calibration purposes.

#### 10.2.5 SIDEPGA

SidePGA loops part of the voice band transmit signal back into the receive path. There are 64 gain steps from mute to +6 dB.

### 10.3 Voice band digital circuitry

The voice band digital circuitry is responsible for converting a 16-bit PCM signal at 8 kHz sample rate to and from a 1-bit, 1 MHz signal. It also contains a band-pass filter for 300 to 3400 Hz and a sidetone engine. Various volume settings are calculated inside this block. Figure 7 shows the block diagram of the voice band signal processor.

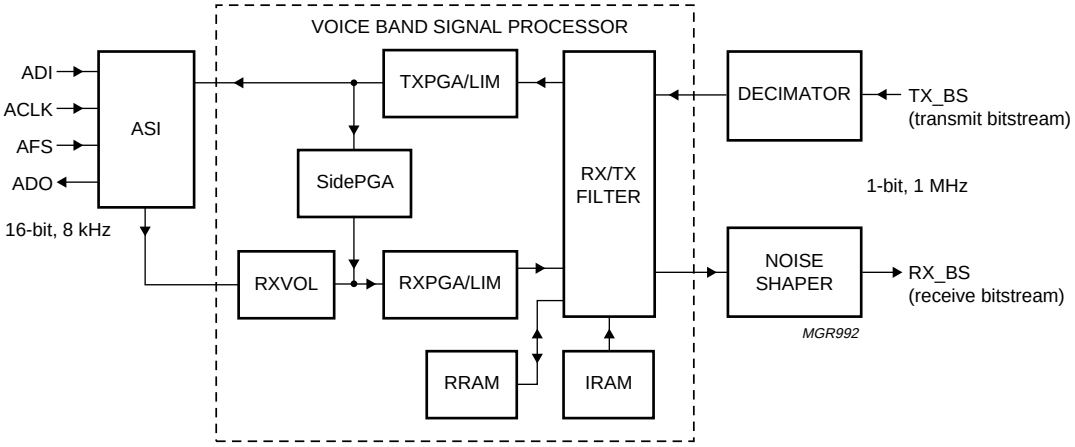



Fig.7 Block diagram of the voice band signal processor.

### 10.3.1 Volume control block

The volume control block contains the RXPGA, SidePGA, TXPGA and both limiter blocks. The possible settings can be found in the description of the CSI block. All digital volume control blocks, i.e. RXPGA, SidePGA, and TXPGA, will allow settings from +6 to –30 dB and mute in 64 steps. However, not all combinations of settings for these blocks will be meaningful. The limiter will always clip signals with overflow to the maximum or minimum allowable value.

### 10.3.2 Audio Serial Interface (ASI) block

The ASI is the voice band serial interface which provides the connection for the exchange of PCM data in both receive and transmit directions, between the baseband digital signal processor and the PCF50732. The data is coded in 16-bit linear PCM two's complement words.

A frame start is defined by the first falling edge of ACLK after a rising AFS. This first falling edge is used to clock in the first data bit on both the baseband and the DSP device.

Data on pin ADI is clocked in (MSB first) on the falling edge of the ACLK clock. Data is clocked out (MSB first) on pin ADO on the rising edge of the ACLK clock.

Pin ADO is put in 3-state after the LSB of the transmit word, independent of the length of the AFS pulse. If the channel position 0 (see Section 10.3.2.1) is selected, then the MSB must be output directly after AFS becomes a logic 1, even if no rising edge on ACLK has been given yet.

The following modes of operation are programmable:

- Channel position
- ACLK clock mode.

#### *10.3.2.1 Channel position mode*

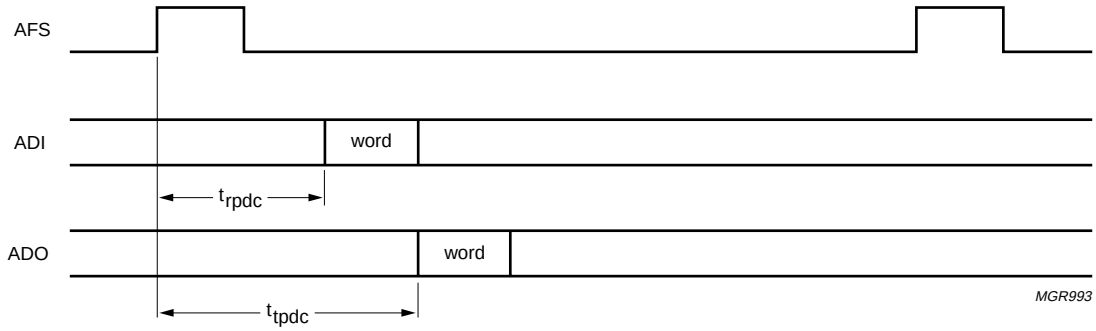
Depending on a programmable register value n (n = 0 to 15) 1 of 16 channels can be selected (see Table 22). The ASI can add a delay of 16 × n-bit clocks between the assertion of AFS and the start of the MSB of the PCM values. This delay is independently programmable for transmit and receive mode.

#### *10.3.2.2 ACLK clock mode*

Single or double clock mode can be selected. Double clock mode implies two clock pulses per data bit and is used for communication with IOM2 compatible devices. In double clock mode data must be output on the first rising edge and be read on the last falling edge.

**Table 6** Pin connection of the ASI to the PCF5087X

| PCF50732 | | PCF5087X | |
|---|---|---|---|
| **PIN** | **I/O** | **PIN** | **I/O** |
| ADI | I | DD | O |
| ADO | O | DU | I |
| ACLK | I | DCL | O |
| AFS | I | FSC | O |




$t_{rpdc}$: receive path data channel delay.
$t_{tpdc}$: transmit path data channel delay.

Fig.8 Frame structure of the Audio Serial Interface (ASI).

*10.3.2.3 Audio Serial Interface (ASI) timing characteristics*

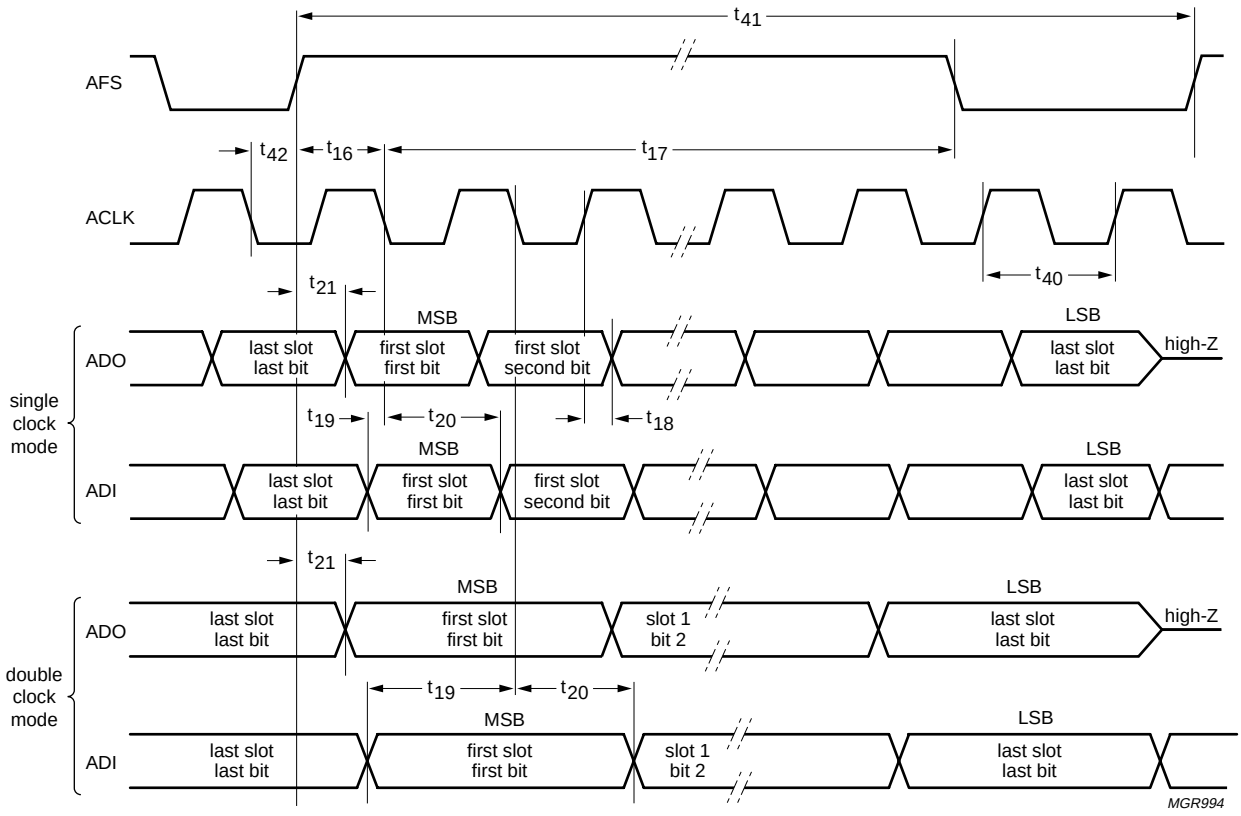



Fig.9 Timing of the Audio Serial Interface (ASI).

**Table 7** ASI timing characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $t_{16}$ | frame sync (AFS) set-up time to falling edge of ACLK | 70 | – | – | ns |
| $t_{17}$ | frame sync (AFS) hold time from falling edge of ACLK | 40 | – | – | ns |
| $t_{18}$ | ACLK rising edge to data (ADO) valid | –30 | – | +30 | ns |
| $t_{19}$ | data (ADI) set-up time to falling edge of ACLK | 50 | – | – | ns |
| $t_{20}$ | data (ADI) hold time from falling edge of ACLK | 80 | – | – | ns |
| $t_{21}$ | first data valid (ADO) after AFS rising edge | 0 | – | 60 | ns |
| $t_{40}$ | ACLK period | | | | |
| | single clock mode | 0.5 | – | 7.8 | µs |
| | double clock mode | 0.5 | – | 3.9 | µs |
| $t_{41}$ | AFS period | – | 125 | – | µs |
| $t_{42}$ | ACLK LOW before AFS rising edge | 40 | – | – | ns |

## 11 AUXILIARY FUNCTIONS

The auxiliary functions part consists of three digital-to-analog converters and a 4 input analog-to-digital converter with a 12-bit range. The DACs are for:

- Automatic Gain Control (AGC): AUXDAC1
- Automatic Frequency Control (AFC): AUXDAC2
- Power ramping: AUXDAC3.

### 11.1 Automatic Gain Control (AGC): AUXDAC1

The AUXDAC1 is an 8-bit binary coded, guaranteed monotonic digital-to-analog converter.

The status of AUXDAC1 is controlled by the signal AUXST and a power-up bit in the Power control register. The signal that switches the external VCXO can also be used to control the AUXST pin of the PCF50732. The AUXDAC1 output is pulled-down in Power-down mode (AUXST = LOW). The input MCLK is then deactivated.

When AUXST goes HIGH, AUXDAC1 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC1 output pin.

If a write access to the AUXDAC1 register occurs, the DAC is activated with the new content of the DAC register (see Table 14 and 15). The AUXDAC1 must be powered-up by setting the correct bit in the power control register. At reset AUXDAC1 is powered-down.

### 11.2 Automatic Frequency Control (AFC): AUXDAC2

The AUXDAC2 is a 12-bit binary coded, guaranteed monotonic digital-to-analog converter. This DAC is used to control the frequency of an external master clock VCXO.

The status of AUXDAC2 is controlled by the signal AUXST and a power-up bit in the power control register. The signal that switches the external VCXO can also be used to control the pin AUXST of the PCF50732. The AUXDAC2 output is pulled-down in Power-down mode (AUXST = LOW). When AUXST goes HIGH, AUXDAC2 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC2 output pin.

The default value for AUXDAC2 is 1.1 V which corresponds to a 800H code in the AUXDAC2 register. At reset AUXDAC2 is powered-up.

### 11.3 Power ramping: AUXDAC3

AUXDAC3 is a 10-bit binary coded digital-to-analog converter designed for power ramping purposes. AUXDAC3 is default off. The power ramping behaviour is described in Section 9.3.2.2.

### 11.4 Auxiliary analog-to-digital converter (AUXADC)

The AUXADC is specified for voltage and temperature measurements. It contains 4 input channels required for $\Delta T$ and $\Delta V$ measurements, as well as battery type recognition:

- $\Delta T$: battery temperature, ambient temperature (measured across sensor)
- $\Delta V$: peak battery voltage, battery voltage during transmit burst.

Five 12-bit registers are available in which results of auxiliary analog-to-digital conversions can be stored. Two registers are dedicated to the input AUXADC1 and one to each of AUXADC2, AUXADC3 and AUXADC4.

The AUXADC1 input can be used for battery voltage measurement. In the AUXADC1A register the voltage during a transmit time slot can be stored. The AUXADC1B register can store the voltage during other time slots. If a read request to one of these registers is executed by loading its address into the read request register, the actual contents of the addressed register are given to the control interface and a new measurement is performed in the next appropriate time slot.

A multiplexer connects each of the AUXADC inputs to a channel of the receive ADC depending on read access to the corresponding register.

Thus an auxiliary analog-to-digital conversion is only possible, if the baseband receive section is not in use (RXON is LOW). At each read request to one of the AUXADC registers, a flag is set in the AUXADC flag register indicating that an analog-to-digital conversion is to be performed. When one of the registers AUXADC1B, AUXADC2, AUXADC3, or AUXADC4 is being read, the baseband interface verifies that RXON is LOW, indicating that no receive burst is currently active. The baseband receive path is then powered-up. After the ADC settling time has elapsed (see $POST_{AUXADC}$ in Chapter 18), valid data is available and stored in the corresponding register.

After conversion the corresponding bit in the AUXADC flag register is reset (see Table 18). If RXON is activated during an auxiliary analog-to-digital conversion cycle, the auxiliary conversion is interrupted and restarted when RXON returns LOW, indicating no receive burst activity.

When register AUXADC1A is read, a battery voltage measurement during a transmission burst is executed.

The PCF50732 waits for a rising edge of TXON, and powers up the receive path.

After the settling time of the ADC added to the programmed AUXADC conversion delay (in 48 MCLK cycles) has elapsed, valid data is available and stored in the AUXADC1A register.

For reasons of resource sharing the baseband receive ADC is used for the auxiliary ADC function, but only positive values of its differential input range can be converted. This results in output values between 0 and 2048 bits, but to prevent instability this is reduced by 2.6 dB to a useful range of 0 to 1480 bits.

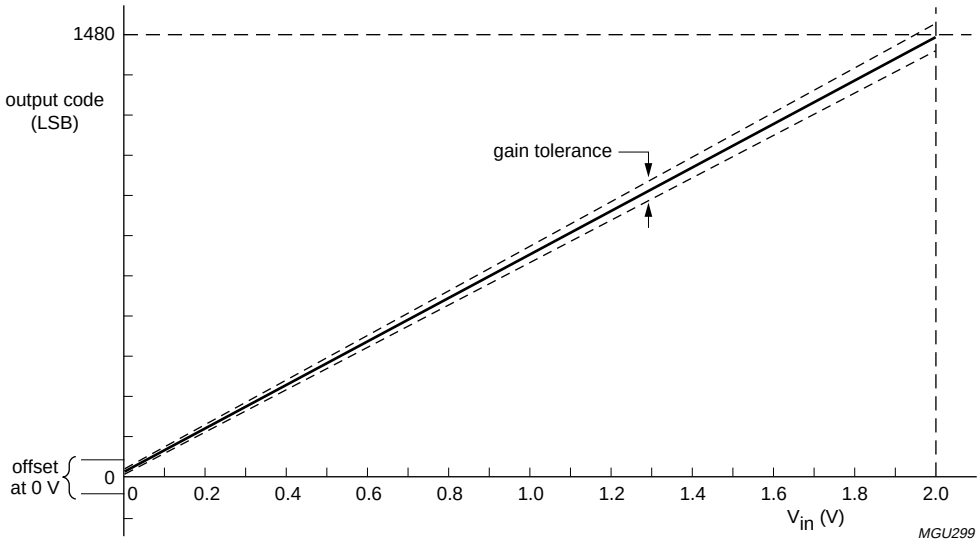



Fig.10 Typical transfer characteristics of AUXADC (output code as function of differential input voltage).

## 12 CONTROL SERIAL INTERFACE (CSI)

The Control Serial Interface block is used to set and read the status bits inside the PCF50732. It is also used to read data from the AUXADCs and to write data into the auxiliary DACs. Finally, the block is used to write the power ramping curve into a 64 × 10-bit static RAM. It should be noted that only 48 of the 64 addresses can be accessed; see Table 2.

### 12.1 The serial interface

A 4-line bidirectional serial interface is used to control the circuit. It allows access to each register of the control register block (read and/or write). The 4 lines are:

- Control Data In (CDI)
- Control Data Out (CDO)
- Control Clock (CCLK)
- Control Enable (CEN).

Table 8 lists the normal connections to the PCF5087X.

Data sent to or from the device is loaded in bursts framed by CEN. Clock edges and data bits are ignored until CEN goes active (LOW). Each data word consists of 21 bits that comprises a 4-bit device address, a 4-bit register address, a 12-bit data word and a dummy bit; see Table 9. The 21 bits are transmitted with MSB first. Figure 11 shows the valid timing for data transmission on the control interface.

Data is read in from the CDI pin on the rising edge of the CCLK clock and output on CDO on the falling edge of the CCLK clock. Data is written into the registers on the rising edge of CEN.

If the device address is equal to the chip address, the programmed information on CDI (DB11 to DB00) is loaded into the addressed register (RA3 to RA0) when CEN returns inactive HIGH.

The dummy bit in front is needed for compatibility with older baseband devices.

Reading a register is accomplished by writing the address of the required register into the read request register. The next time CEN goes LOW, the requested data will be shifted out, together with the register and device address.

**Table 8** Pin connection of the CSI to the PCF5087X

| PCF50732 | | PCF5087X | |
|---|---|---|---|
| **PIN** | **I/O** | **PIN** | **I/O** |
| CDI | I | RFDO | O |
| CDO | O | RFDI | I |
| CCLK | I | RFCLK | O |
| CEN | I | RFE_N2 | O |

**Table 9** Bit mapping of the 21-bit words

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 00 to 03 | ADD0 to ADD3 | device address; for the PCF50732 this is ‘1001’ (= 9 decimal) |
| 04 to 07 | RA0 to RA3 | register address |
| 08 to 19 | DB00 to DB11 | data value |
| 20 | dummy | don’t care |

### 12.2 Control Serial Interface (CSI) timing characteristics

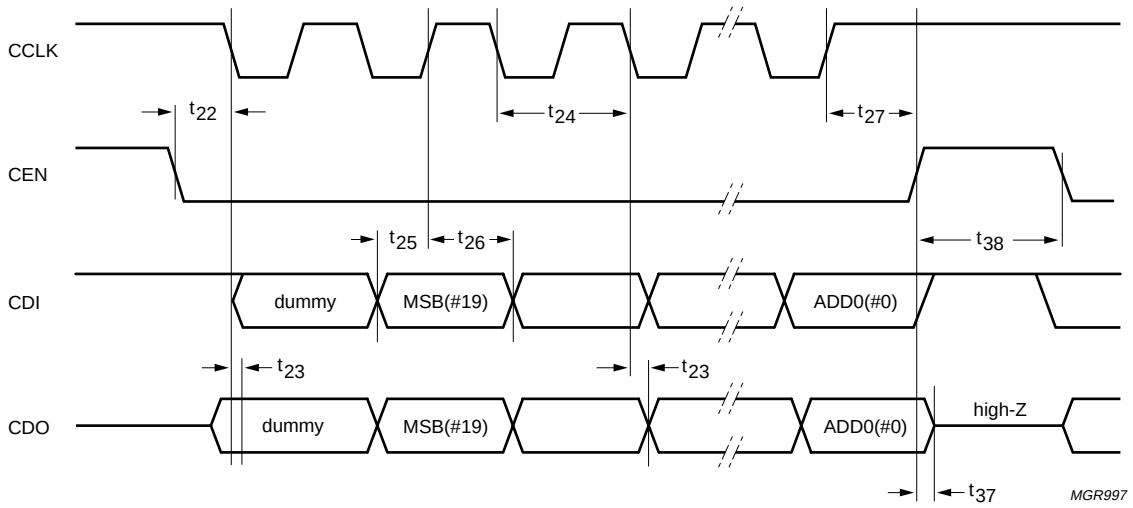



Fig.11 Timing diagram of the Control Serial Interface (CSI).

**Table 10** CSI timing characteristics
For the timing diagram see Fig.11.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $t_{22}$ | CEN set-up time | 20 | – | ns |
| $t_{23}$ | CDO data valid after falling clock edge | – | 50 | ns |
| $t_{24}$ | CCLK cycle time | 100 | – | ns |
| $t_{25}$ | data set-up time to rising edge of CCLK | 20 | – | ns |
| $t_{26}$ | data hold time from rising edge of CCLK | 30 | – | ns |
| $t_{27}$ | CEN hold time | 30 | – | ns |
| $t_{37}$ | CDO 3-state after CEN HIGH | – | 30 | ns |
| $t_{38}$ | CEN HIGH time | 50 | – | ns |

### 12.3 Control register block

This section describes the different registers that are implemented in the PCF50732. An overview is given in Table 11. Tables 12 to 30 describe all the registers of the PCF50732.

**Table 11** Control register block overview

| ADDRESS | ACCESS | REGISTER NAME |
|---|---|---|
| 0000 | W | Read request register |
| 0001 | R/W | AUXDAC1 (AGC) value register |
| 0010 | R/W | AUXDAC2 (AFC) value register |
| 0011 | R/W | Burst control register |
| 0100 | R/W | AUXADC control register |
| 0101 | R | AUXADC channel 1 register A (AUXADC1A); note 1 |
| 0110 | R | AUXADC channel 1 register B (AUXADC1B); note 1 |
| 0111 | R | AUXADC channel 2 register (AUXADC2); note 1 |
| 1000 | R | AUXADC channel 3 register (AUXADC3); note 1 |
| 1001 | R | AUXADC channel 4 register (AUXADC4); note 1 |
| 1010 | R/W | Voice band control register |
| 1011 | R/W | Voice band volume register |
| 1100 | R/W | Power control register |
| 1101 | R/W | RAM interface register |
| 1110 | R/W | Baseband receive control register |
| 1111 | R/W | Test mode register; note 2 |

**Notes**

1. See description in Section 11.4.
2. Do not use this register.

#### 12.3.1 READ REQUEST REGISTER

**Table 12** Read request register

X = don’t care during a read/or write access.

| ADDRESS | REGISTER NAME | VALUE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0000 | Read request register | X | X | X | X | r3 | r2 | r1 | r0 | s3 | s2 | s1 | s0 |

**Table 13** Read request register bit description

| VALUE OF | SYMBOL | DESCRIPTION |
|---|---|---|
| Read request register | r3 to r0 | Address of the register to be read. |
| | s3 to s0 | Subaddress that might be needed. The subaddress bits are right aligned, meaning that the subaddress always starts with bit ‘s0’ (LSB); e.g. in case of two subaddress bits, ‘s1’ and ‘s0’ are used. |

### 12.3.2 AUXDAC1 (AGC) VALUE AND AUXDAC2 (AFC) VALUE REGISTERS

**Table 14** Registers overview
X = don't care during a read/or write access.

| ADDR. | REGISTER NAME | VALUE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0001 | AUXDAC1 (AGC) value register | X | X | X | X | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0010 | AUXDAC2 (AFC) value register | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**Table 15** AUXDAC1 (AGC) value and AUXDAC2 (AFC) value registers value description

| VALUE OF | SYMBOL | DESCRIPTION |
|---|---|---|
| AUXDAC1 (AGC) value register | b7 to b0 | input value to the 8-bit AUXDAC1 (fed directly into the DAC); the default value is 85H |
| AUXDAC2 (AFC) value register | b11 to b0 | input value to the 8-bit AUXDAC2 (fed directly into the DAC); the default value is 800H |

### 12.3.3 BURST CONTROL REGISTER

The Burst control register controls the timing of the transmit burst (TX-burst). The 'lo'-registers contain the lower 8 bits, the 'hi'-registers the upper 4 bits of a 12-bit delay value. Therefore, each register has a programmable range from 0 to 4095. Not all combinations of values might make sense, e.g. ramp-down before ramp-up.

**Table 16** Burst control register (address 0011 and subaddresses)
X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | | VALUE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s3) | 10 (s2) | 9 (s1) | 8 (s0) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RU-lo | 0 | 0 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RU-hi | 0 | 0 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| RM-lo | 0 | 0 | 1 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RM-hi | 0 | 0 | 1 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| RD-lo | 0 | 1 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RD-hi | 0 | 1 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| BIEN0-lo | 0 | 1 | 1 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BIEN0-hi | 0 | 1 | 1 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| BIEN1-lo | 1 | 0 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BIEN1-hi | 1 | 0 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| Single/double burst mode[1] | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | b0 |
| DAC3 burst RAM address[1] | 1 | 0 | 1 | 1 | X | X | a5 | a4 | a3 | a2 | a1 | a0 |
| DAC3 burst RAM data[1] | 1 | 1 | d9[2] | d8[2] | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

**Notes**

1. The programming is described in Section 9.3.2.2.
2. The subaddress positions bit 9 (s1) and bit 8 (s0) do not apply to the DAC3 burst RAM data register.

**Table 17** Burst control registers value description

| VALUE OF | DESCRIPTION |
|---|---|
| RU | Value RU, consisting of RU-lo (least significant byte) and RU-hi (most significant byte), is the delay measured in quarterbits ($^1/_{12}$MCLK) between the rising edge of TXON and the start of the ramp-up on AUXDAC3. After this delay, the first 16 values of the AUXDAC3 RAM are sent to AUXDAC3. Shifting out is done at $^1/_{24}$MCLK. |
| RM | Value RM, consisting of RM-lo (least significant byte) and RM-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the intermediate ramp in multislot mode. The RM value is ignored in single slot mode. RM must be greater than RU + 32. |
| RD | Value RD, consisting of RD-lo (least significant byte) and RD-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the ramp-down on AUXDAC3. RD must be greater than RU + 32, or in case of multislot mode, greater than RM + 32. |
| BIEN0 | Value BIEN0, consisting of BIEN0-lo (least significant byte) and BIEN0-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the falling edge of BIEN. |
| BIEN1 | Value BIEN1, consisting of BIEN1-lo (least significant byte) and BIEN1-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the rising edge of BIEN. BIEN1 must be greater than BIEN0. |

Data is read back from these registers in their full 12-bit length, i.e. reading RU-lo will give the full 12-bit word RU-hi + RU-lo. Reading RU-hi will also give the same 12-bit result RU-hi + RU-lo. The same is true for RM, RD, BIEN0 and BIEN1.

The burst mode control bit b0 has a default value of 0, corresponding to single burst mode.

### 12.3.4 AUXADC CONTROL REGISTER

**Table 18** AUXADC control register (address 0100 and subaddresses)
X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUXADC conversion delay value register | 0 | 0 | 0 | X | X | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AUXADC flag register | 0 | 0 | 1 | X | X | X | auxoff | flag 4 | flag 3 | flag 2 | flag 1B | flag 1A |
| AUXADC offset value register | 1 | 0 | 0 | 9-bit signed offset compensation value | | | | | | | | |
| Offset trigger register | 1 | 1 | 1 | X | X | X | X | X | X | 0 | 0 | Aux |

**Table 19** AUXADC control registers value description

| VALUE OF | DESCRIPTION |
|---|---|
| AUXADC conversion delay value register | Actual duration of one AUXADC-1A conversion is 160 μs + AUXDLY × 3.7 μs. This duration is halved in NZIF mode. Conversions are done continually until the end of the baseband transmit burst. Default value for AUXDLY is 0. Reading out is to be done at a carefully selected time in order to have the required amount of delay between TXON and the measurement. |
| AUXADC flag register | The AUXADC flag register returns the status of the AUXADC converters. If an AUXADC is pending, the flag of the corresponding AUXADC will be set. The flag register is read only. |
| AUXADC offset value register | The offset value register contains a signed 9-bit offset compensation value. This value is subtracted automatically from all AUXADC measurements to compensate for offset errors. The compensation value can be read and written and has a default value of 0. It can also be measured by the device itself. |
| Offset trigger register | A write to the offset trigger register will trigger an offset measurement. An offset measurement is a special case of an AUXADC measurement and takes approximately 160 μs. The trigger register is write only. |

### 12.3.5 AUXADC REGISTERS

**Table 20** AUXADC registers overview

| ADDR. | REGISTER NAME | VALUE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0101 | AUXADC channel 1 register A (AUXADC1A) | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0110 | AUXADC channel 1 register B (AUXADC1B) | | | | | | | | | | | | |
| 0111 | AUXADC channel 2 register (AUXADC2) | | | | | | | | | | | | |
| 1000 | AUXADC channel 3 register (AUXADC3) | | | | | | | | | | | | |
| 1001 | AUXADC channel 4 register (AUXADC4) | | | | | | | | | | | | |

**Table 21** AUXADC registers value description

| VALUE OF | DESCRIPTION |
|---|---|
| AUXADC1A | 12-bit result of the A/D conversion on AUXADC channel 1, measured during a transmission burst |
| AUXADC1B | 12-bit result of the A/D conversion on AUXADC channel 1, measured outside a transmission burst |
| AUXADC2 | 12-bit result of the A/D conversion on AUXADC channel 2 |
| AUXADC3 | 12-bit result of the A/D conversion on AUXADC channel 3 |
| AUXADC4 | 12-bit result of the A/D conversion on AUXADC channel 4 |

### 12.3.6 VOICE BAND CONTROL REGISTER

The voice band control register is used to control the following functionality of the voice band CODEC:

- Analog input source: microphone (MICAMP) or auxiliary (AUXMIC) input
- Analog output device: earphone (EARAMP), auxiliary (AUXAMP) or buzzer (BUZAMP) output; this register allows individual control of all three output amplifiers
- EARAMP output mode: single-ended (EARP) or differential (EARN/EARP). This selects the input source for the EARAMP-N amplifier. In single-ended mode EARAMP-N will be at $V_{ref}$, in differential mode it will carry the output signal
- General purpose output pin: AMPCTRL
- Receive and transmit path delay values
- ASI clock mode
- TX gain boost (MICHI).

**Table 22** Voice band control register (address 1010 and subaddresses)
X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | | FUNCTION SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Select input source | 0 | 0 | 0 | don't care | | | | | | | | 0 | MICAMP (default) |
| | | | | | | | | | | | | 1 | AUXMIC |
| Select output amplifier | 0 | 0 | 1 | don't care | | | | | X | X | X | 0 | EARAMP-P off |
| | | | | | | | | | X | X | X | 1 | EARAMP-P on (default) |
| | | | | | | | | | X | X | 0 | X | EARAMP-N off |
| | | | | | | | | | X | X | 1 | X | EARAMP-N on (default) |
| | | | | | | | | | X | 0 | X | X | AUXAMP off (default) |
| | | | | | | | | | X | 1 | X | X | AUXAMP on |
| | | | | | | | | | 0 | X | X | X | BUZAMP off (default) |
| | | | | | | | | | 1 | X | X | X | BUZAMP on |
| EARAMP output mode | 0 | 1 | 0 | don't care | | | | | | | | 0 | single-ended |
| | | | | | | | | | | | | 1 | differential (default) |
| AMPCTRL pin polarity | 0 | 1 | 1 | don't care | | | | | | | | 0 | active LOW |
| | | | | | | | | | | | | 1 | active HIGH (default) |
| Receive path data channel | 1 | 0 | 0 | don't care | | | | | d | c | b | a | 4-bit delay value (default = 0) |
| Transmit path data channel | 1 | 0 | 1 | | | | | | d | c | b | a | |
| ASI clock mode | 1 | 1 | 0 | don't care | | | | | | | | 0 | single clock (default) |
| | | | | | | | | | | | | 1 | double clock |
| TX gain boost (MICHI) | 1 | 1 | 1 | don't care | | | | | | | | 0 | 7 dB |
| | | | | | | | | | | | | 1 | 35 dB (default) |

### 12.3.7 VOICE BAND VOLUME REGISTER

Voice band gain settings can be independently programmed for: TXPGA, RXPGA, RXVOL and SidePGA.

**Table 23** Voice band volume register (address 1011 and subaddresses)
X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | | SELECTED RANGE | DEFAULT SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| TXPGA gain | 0 | 0 | 0 | X | X | X | a | b | c | d | e | f | –24 to +12 dB | 0 dB |
| RXPGA gain | 0 | 0 | 1 | X | X | X | a | b | c | d | e | f | | |
| RXVOL gain | 0 | 1 | 0 | X | X | X | a | b | c | d | e | f | –30 to +6 dB | –12 dB |
| SidePGA gain | 0 | 1 | 1 | X | X | X | a | b | c | d | e | f | | mute |
| Clock settings (do not use) | 1 | 0 | 1 | X | X | X | X | pll | dc | dir | hf | bgb | – | "10000" |
| Voice band tuning | 1 | 1 | 0 | | | | | 0 | 0 | vbch | fdg1 | fdg0 | – | "00101" |

**Table 24** Voice band volume registers value description

| VALUE | REMARKS | DESCRIPTION |
|---|---|---|
| TXPGA gain | microphone calibration | TXPGA and RXPGA settings use the 6-bit binary fixed point value 'ab.cdef' as a multiplier for each PCM-sample. This results in a control range of +12 to –24 dB; note 1a. |
| RXPGA gain | earphone calibration | |
| RXVOL gain | customer volume control | RXVOL and SidePGA settings use the 6-bit binary fixed point value 'a.bcdef' as a multiplier for each PCM-sample. This results in a control range of +6 to –30 dB (and mute); note 1b. |
| SidePGA gain | | |
| Clock settings | | • dir: bypass clock buffer<br>• pll: clock optimizer<br>• dc: bypass clock capacitor<br>• vbch: voice band chopping<br>• hf: 26 MHz master clock input<br>• bgb: band gap boost. |
| Voice band tuning | | • vbch: voice band chopping<br>• fdg1 and fdg0: FIRDAC gain steps; note 2. |

**Notes**

1. Possible gain settings are listed in Table 26 or can be calculated using the following formulae ('n' is an integer that represents the value that is written into the register; n = 0 to 63):

   a) RXPGA and TXPGA: $\text{gain} = 20 \times \log\frac{n}{16}$ ; add 6.02 dB to each gain for RXPGA and TXPGA settings.

   b) RXVOL and SidePGA: $\text{gain} = 20 \times \log\frac{n}{32}$

2. The gain setting bits are used to control the analog gain steps in the voice band output drivers: the highest gain setting must be used to achieve the maximum output drive of 2 V (p-p) at differential outputs; for lower gain settings the output noise is reduced accordingly, see Table 25.

**Table 25** Analog gain settings

| fg1 | fg0 | GAIN PER OUTPUT DRIVER (dB) |
|---|---|---|
| 0 | 0 | –8.5 |
| 0 | 1 | –6.0 (default) |
| 1 | 0 | –2.5 |
| 1 | 1 | 0.0 |

*12.3.7.1 Possible gain selections for voice band blocks: RXPGA, TXPGA, RXVOL and SidePGA*

Table 26 shows the possible gain selections for the voice band blocks RXPGA, TXPG, RXVOL and SidePGA. It should be noted that not all possible combinations of these volume settings are meaningful; setting RXPGA, SidePGA and RXVOL to maximum will result in clipping of the output signal.

**Table 26** Gain selections

| BINARY CODE | GAIN (dB) | |
|---|---|---|
| | RXPGA/TXPGA | RXVOL/SidePGA |
| 111111 | 11.88 | 5.88 |
| 111110 | 11.74 | 5.74 |
| 111101 | 11.60 | 5.60 |
| 111100 | 11.46 | 5.46 |
| 111011 | 11.31 | 5.31 |
| 111010 | 11.17 | 5.17 |
| 111001 | 11.01 | 5.01 |
| 111000 | 10.86 | 4.86 |
| 110111 | 10.70 | 4.70 |
| 110110 | 10.54 | 4.54 |
| 110101 | 10.38 | 4.38 |
| 110100 | 10.22 | 4.22 |
| 110011 | 10.05 | 4.05 |
| 110010 | 9.88 | 3.88 |
| 110001 | 9.70 | 3.70 |
| 110000 | 9.52 | 3.52 |
| 101111 | 9.34 | 3.34 |
| 101110 | 9.15 | 3.15 |
| 101101 | 8.96 | 2.96 |
| 101100 | 8.77 | 2.77 |
| 101011 | 8.57 | 2.57 |
| 101010 | 8.36 | 2.36 |
| 101001 | 8.15 | 2.15 |
| 101000 | 7.94 | 1.94 |
| 100111 | 7.72 | 1.72 |
| 100110 | 7.49 | 1.49 |
| 100101 | 7.26 | 1.26 |
| 100100 | 7.02 | 1.02 |
| 100011 | 6.78 | 0.78 |
| 100010 | 6.53 | 0.53 |
| 100001 | 6.27 | 0.27 |
| 100000 | 6.00 | 0.00 |
| 011111 | 5.72 | –0.28 |
| 011110 | 5.44 | –0.56 |
| 011101 | 5.14 | –0.86 |
| 011100 | 4.84 | –1.16 |
| 011011 | 4.52 | –1.48 |
| 011010 | 4.20 | –1.80 |
| 011001 | 3.86 | –2.14 |
| 011000 | 3.50 | –2.50 |
| 010111 | 3.13 | –2.87 |
| 010110 | 2.75 | –3.25 |
| 010101 | 2.34 | –3.66 |
| 010100 | 1.92 | –4.08 |
| 010011 | 1.47 | –4.53 |
| 010010 | 1.00 | –5.00 |
| 010001 | 0.51 | –5.49 |
| 010000 | 0.00 | –6.02 |
| 001111 | –0.58 | –6.58 |
| 001110 | –1.18 | –7.18 |
| 001101 | –1.82 | –7.82 |
| 001100 | –2.52 | –8.52 |
| 001011 | –3.28 | –9.28 |
| 001010 | –4.10 | –10.10 |
| 001001 | –5.02 | –11.02 |
| 001000 | –6.04 | –12.04 |
| 000111 | –7.20 | –13.20 |
| 000110 | –8.54 | –14.54 |
| 000101 | –10.12 | –16.12 |
| 000100 | –12.06 | –18.06 |
| 000011 | –14.56 | –20.56 |

| BINARY CODE | GAIN (dB) | |
|---|---|---|
| | RXPGA/TXPGA | RXVOL/SidePGA |
| 000010 | −18.08 | −24.08 |
| 000001 | −24.10 | −30.10 |
| 000000 | off | off |

### 12.3.8 Power control register

The Power control register is used to control power-up and power-down of the different sections of the device.

Changing the power status is accomplished by addressing the device as shown in Table 27 and setting bit 0 (= a) according to the required state:

a = 0 → power-down

a = 1 → power-up.

Setting the baseband RX or TX flag is functionally equivalent to setting RXON or TXON respectively (logical OR function). The CSI is accessible when the band gap is powered down. Therefore no reset is required to power-up after total power-down. Pin AUXST and the complete device pin are identical in behaviour. Both must be activated to enable the device.

**Table 27** Power control register (address 1100 and subaddresses)

| FUNCTION | SUBADDRESS | | | | VALUE | | | | | | | | DEFAULT | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s3) | 10 (s2) | 9 (s1) | 8 (s0) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | VALUE | STATUS |
| AUXDAC1 | 0 | 0 | 0 | 1 | don't care | | | | | | | a | 0 | off |
| AUXDAC2 | 0 | 0 | 1 | 0 | | | | | | | | a | 1 | on |
| AUXDAC3 | 0 | 0 | 1 | 1 | | | | | | | | a | 0 | off |
| Voice band transmit | 0 | 1 | 0 | 0 | | | | | | | | a | 0 | off |
| Voice band receive | 0 | 1 | 0 | 1 | | | | | | | | a | 0 | off |
| $V_{ref}$ | 0 | 1 | 1 | 0 | | | | | | | | a | 1 | on |
| Baseband receive | 1 | 0 | 0 | 0 | | | | | | | | a | 0 | off |
| Baseband transmit | 1 | 0 | 0 | 1 | | | | | | | | a | 0 | off |
| Complete device | 1 | 1 | 1 | 1 | | | | | | | | a | 1 | on |

### 12.3.9 RAM interface register

The RAM interface register is a general purpose communication channel between the serial interface CSI and the voice band signal processor. None of the processor registers have default values.

The voice band control register is used to communicate with the voice band signal processor. Register functions with subaddress '00' to '11' can be used to program the Instruction RAM (IRAM) when the voice band processor is not running, i.e. when voice band receive and transmit sections are both powered down.

The IRAM registers are used to write into the voice band instruction RAM.

Normal operation is to write an address into the VSP instruction RAM program counter and write low and high bytes of the 16-bit instructions into their respective locations. No auto-increment is foreseen, i.e. the address register must be updated by the user. Writing to the IRAM is only possible when voice band transmit and receive sections are both powered off. If this is not the case write actions are ignored.

Reading back from the IRAM is not straightforward due to the need for an extra clock pulse when accessing RAMs; when reading back the contents of RAM locations 1, 2, 3 and 4 actual output is 'undefined' as 1, 2, 3, etc.

**Table 28** RAM interface register (address 1101 and subaddresses)
X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | VALUE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 (s1) | 10 (s0) | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSP instruction RAM data low-byte | 0 | 0 | X | X | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| VSP instruction RAM data high-byte | 0 | 1 | X | X | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| VSP instruction RAM program counter | 1 | 0 | X | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| VSP interface register | 1 | 1 | x9 | x8 | x7 | x6 | x5 | x4 | x3 | x2 | x1 | x0 |

### 12.3.10 Baseband receive control register

Normal bandwidth refers to an input signal bandwidth of 100 kHz used for ZIF operation, double bandwidth is 200 kHz used for NZIF operation. Normal sampling refers to a sampling rate of $\frac{1}{2}$MCLK, double sampling refers to sampling at MCLK.

The baseband receive control register allows the selection of one of the two operational modes for the BBRX section.

The tuning bits can be used to fine-tune operation inside the different blocks.

Bit lck is used to write-protect the VSP IRAM block. It has a default value of logic 0 and must be set after the VSP firmware has been downloaded and before the VSP is activated.

**Table 29** Baseband receive control register (address 1110)

| FUNCTION | VALUE | | | | | | | | | | | | REMARK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| ZIF operation, 100 kHz bandwidth | 0 | 0 | don't care | | | | | | | | 0 | X[1] | 271 kHz[2] |
| NZIF operation, 200 kHz bandwidth | 0 | 0 | | | | | | | | | 1 | X[1] | 542 kHz |
| Baseband transmit tune | 1 | 0 | don't care | | | | | – | lck | 0 | 0 | 0 | 00000[2] |
| Baseband receive tune | 1 | 1 | | | | | | 0 | 1 | 0 | 0 | 1 | 01001[2] |

**Notes**

1. X = don't care.
2. Default value.

### 12.3.11 TEST MODE REGISTER

Only test mode 8 (TM8) is available to the end user. It is used to mark baseband-I (BB-I) samples with a logic 0 and baseband-Q (BB-Q) samples with a logic 1 on the LSB of the 12-bit value.

**Table 30** Test mode register (address 1111)

| TEST MODE | FUNCTION | VALUE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| NM | normal mode (default) | don't care | | | | | | | | 0 | 0 | 0 | 0 |
| TM1 | baseband transmit (BBTX) I digital | | | | | | | | | 0 | 0 | 0 | 1 |
| TM2 | baseband receive (BBRX) digital | | | | | | | | | 0 | 0 | 1 | 0 |
| TM3 | voice band (VB) loop digital | | | | | | | | | 0 | 0 | 1 | 1 |
| TM4 | voice band transmit/receive (VBTX/RX) digital | | | | | | | | | 0 | 1 | 0 | 0 |
| TM5 | CSI | | | | | | | | | 0 | 1 | 0 | 1 |
| TM6 | baseband (BB) DACs | | | | | | | | | 0 | 1 | 1 | 0 |
| TM7 | voice band receive (VBRX) DAC current sources | | | | | | | | | 0 | 1 | 1 | 1 |
| TM8 | I/Q marking test | | | | | | | | | 1 | 0 | 0 | 0 |
| TM9 | voice band signal processor test mode | | | | | | | | | 1 | 0 | 0 | 1 |
| TM10 | VSP signature output mode | | | | | | | | | 1 | 0 | 1 | 0 |
| TM11 | MCLK input reflected on BDIO | | | | | | | | | 1 | 0 | 1 | 1 |
| TM12 | baseband bitstream output | | | | | | | | | 1 | 1 | 0 | 0 |
| TM13 | baseband transmit state machine output | | | | | | | | | 1 | 1 | 0 | 1 |
| TM14 | 3-state all digital outputs | | | | | | | | | 1 | 1 | 1 | 0 |
| TM15 | – | | | | | | | | | 1 | 1 | 1 | 1 |

## 13 VOICE BAND SIGNAL PROCESSOR (VSP)

### 13.1 Hardware description

The VSP used in the PCF50732 is a 30-bit fixed point VSP with separate data and instruction areas. The data path consists of two guard bits, 16 data bits before and 12 data bits behind the binary point for a total of 30 bits. Two's complement notation is used inside the data path. Intermediate results from calculations are stored in a $64 \times 30$-bit wide data RAM. Data and Programmable Gain Amplifier (PGA) settings are read in via 7 input ports and written back into 3 output ports (see Fig.12).

The instruction path uses a 16-bit format with the 4 MSBs designating the opcode (operation code) and the trailing 12 bits used to describe the operand. The VSP has 12 major instructions; some instructions use two opcodes. The addressing range is 9 bits wide, allowing for a total of 512 instructions, which is more than adequate for the filter types it is intended to calculate. Some room is available for Built-In Self Test (BIST). The ALU consists of a 30-bit subtractor, a 30-bit adder and a $30 \times 16$-bit 'modified booth'-type parallel multiplier.

The accumulator of the VSP has built-in overrange checking and will limit values to their minimum (in case of underflow) or maximum (in case of overflow) value.

The VSP engine is designed to operate at 4 MIPS on a 8 kHz PCM signal.

All instructions take one clock-cycle to complete. It should be noted that since the noise shaper operates at a sample rate of 32 kHz and the voice band filter operates at a sample rate of 40 kHz it is necessary to transfer 4 samples to the receive output and to read 5 samples from the transmit input for each frame.

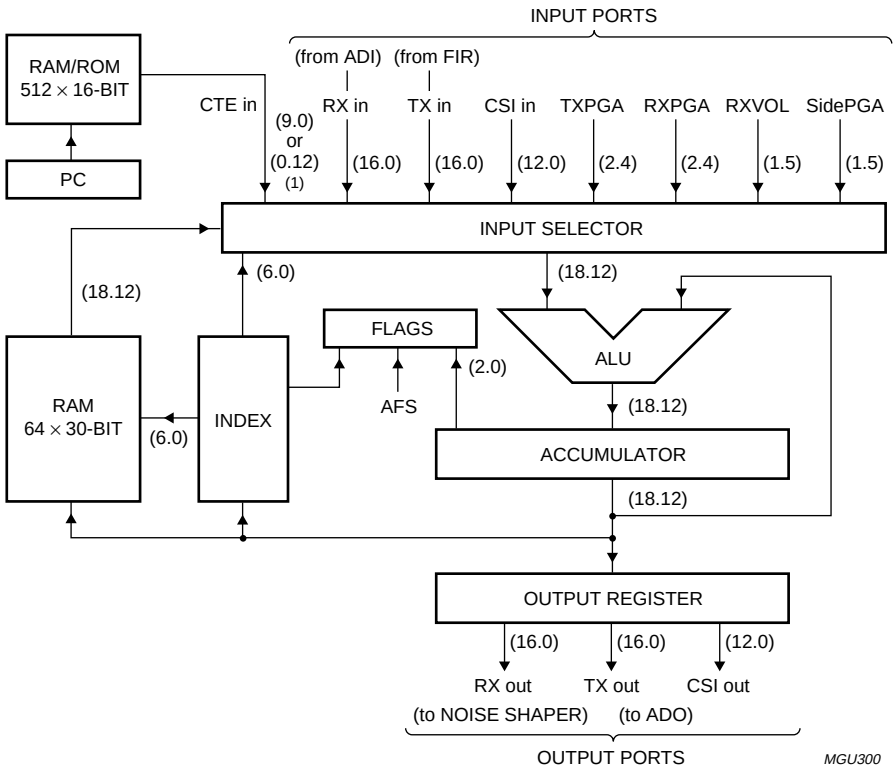
No buffering is foreseen for these samples, which means that the VSP program is responsible for proper spacing in time of the input and output samples. Failure to ensure proper spacing will result in heavily distorted signals.

Synchronization to the 8 kHz frame sync signal AFS is also done under program control. The VSP program must ensure that noise shaper and FIR filter are properly reset before actual operation is started.

A VSP emulator and a VSP assembler have been written in order to facilitate program development. The assembler generates a stream of 16-bit words that need to be loaded into the instruction RAM. This is done by repeated writes to the VSP control register. The sequence would be as follows:

1. Write address into the VSP instruction RAM program counter register
2. Write the upper 8 bits into the VSP instruction RAM data high-byte register
3. Write the lower 8 bits into the VSP instruction RAM data low-byte register.

This sequence should be repeated until the VSP is fully programmed. Programming can only be done when the VSP is not active. The VSP program counter will be set to location 0 and operation starts after enabling voice band transmit or voice band receive. See also the CSI description in Chapter 12.




The program ROM and program counter are not shown.

(1) (x.y) designates a (x + y) bits wide data stream with x bits before and y bits after the binary point.

Fig.12 Voice band Signal Processor (VSP) block diagram.

### 13.2 VSP assembler language

The stack for return addresses is only one entry deep which means that nesting of subroutines is not possible.

**Table 31** VSP instruction set

X = don't care during a read/or write access. For the description of the bit symbols see notes 1 to 7.

| MNEMONIC | INSTRUCTION | I3 | I2 | I1 | I0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LDA | load accumulator | 0 | 0 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| STO | store accumulator | 0 | 0 | 1 | 0 | m2 | m1 | m0 | X | X | X | d5 | d4 | d3 | d2 | d1 | d0 |
| RTN | return from subroutine | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X |
| ADD | add to accumulator | 0 | 1 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| SUB | subtract from accumulator | 0 | 1 | 1 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| MUL | multiply with accumulator | 1 | 0 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| JMFS | jump if flag set | 1 | 0 | 1 | 0 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JMFC | jump if flag clear | 1 | 0 | 1 | 1 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JSFS | jump subroutine if flag set | 1 | 1 | 0 | 0 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JSFC | jump subroutine if flag clear | 1 | 1 | 0 | 1 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| STF | set/clear flag | 1 | 1 | 1 | 0 | f2 | f1 | f0 | X | X | X | X | X | X | X | X | d0 |
| IDX | index operations | 1 | 1 | 1 | 1 | im2 | im1 | im0 | X | X | X | i5 | i4 | i3 | i2 | i1 | i0 |

**Notes**

1. c11 to c0 denotes a 12-bit two's complement coefficient between −1 and +1.
2. m3 to m0 denotes a 4-bit instruction mode descriptor.
3. f2 to f0 denotes a 3-bit flag descriptor.
4. a8 to a0 denotes a 9-bit address.
5. i5 to i0 denotes a 6-bit index register value.
6. X is a don't care bit.
7. im2 to im0 denotes a 3-bit instruction mode descriptor for the IDX operator.

**Table 32** Mode descriptions

| m3 | m2 | m1 | m0 | MODE NAME | OPERAND | RANGE | ASSEMBLER SHORT HAND |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | register | R(d5 to d0) | register 0 to 63 | r |
| 0 | 0 | 0 | 1 | register indexed | R((d5 to d0) + index) | register 0 to 63 | i |
| 0 | 0 | 1 | 0 | port | P(d2 to d0) | ports 0 to 7 | p |
| 0 | 0 | 1 | 1 | small integer | d8 to d0 | –256 to +255; note 1 | s |
| 0 | 1 | 0 | 0 | index | index | 0 to 63; note 1 | i |
| 1 | bits 11 to 0 form a 12-bit two's complement coefficient between –1 and +1 | | | | | | c |

**Note**

1. Value range in increments of 1.

**Table 33** Index mode descriptions

| im2 | im1 | im0 | NAME | OPERAND |
|---|---|---|---|---|
| 0 | 0 | 0 | store | index = d5 to d0 |
| 0 | 0 | 1 | increment | index = (d5 to d0) + index |
| 1 | 0 | 0 | accu | index = accu |

**Table 34** Flag descriptions

| f2 | f1 | f0 | NAME | DESCRIPTION | REMARKS | TYPE |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | ALW | always set | flag is clear in VSP test mode; used to initiate BIST | system |
| 0 | 0 | 1 | INZ | set if index not zero | used to implement loops | |
| 0 | 1 | 0 | EQ0 | set if accu is all 0 | | |
| 0 | 1 | 1 | EQ1 | set if accu is all 1 | | |
| 1 | 0 | 0 | SYNC | PCM sync signal | used to sync VSP to external PCM signal | |
| 1 | 0 | 1 | A | user flag A | | user |
| 1 | 1 | 0 | B | user flag B | | |
| 1 | 1 | 1 | C | user flag C | used to reset noise shaper and FIR filter | |

**Table 35** Port descriptions

| P2 | P1 | P0 | NAME | DIRECTION | RANGE |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Receive (RX) | read/write | –32768 to +32767 (16 bits) |
| 0 | 0 | 1 | Transmit (TX) | read/write | –32768 to +32767 (16 bits) |
| 0 | 1 | 0 | CSI | read/write | –2048 to +2047 (12 bits) |
| 0 | 1 | 1 | ZERO | read | fixed 0 |
| 1 | 0 | 0 | TXPGA | read | 0 to 63 (–24 to +12 dB) |
| 1 | 0 | 1 | RXPGA | read | 0 to 63 (–24 to +12 dB) |
| 1 | 1 | 0 | RXVOL | read | 0 to 63 (–20 to +6 dB) |
| 1 | 1 | 1 | SidePGA | read | 0 to 63 (–20 to +6 dB) |

### 13.3 Descriptions of the VSP instruction set

#### 13.3.1 CONVENTIONS

In the descriptions of the VSP instruction set:

- A = the 30-bit accumulator
- I = the 6-bit index register
- r.a. = a 6-bit register address
- p.n. = a 3-bit port number (address)
- coeff = a 12-bit coefficient
- f.l. = a 3-bit flag descriptor
- addr = a 9-bit address
- stack = a one entry deep return address stack
- PC = a 9-bit program counter
- o.a. = the 9-bit old address
- s.i. = small integer
- X = don't care during a read/or write access.

#### 13.3.2 LDA INSTRUCTION

The LDA (Load accumulator) instruction is used to load data into the accumulator of the VSP. Flags affected are EQ0 and EQ1.

**Table 36** LDA instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | coefficient | | | | | | | | | | | | coeff → A | LDA c <coeff> | load coefficient |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | R(r.a.) → A | LDA r <r.a.> | load register |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | R(r.a. + I) → A | LDA i <r.a.> | load register indexed |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | P(p.n.) → A | LDA p <p.n.> | load port |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | s.i. → A | LDA s <s.i.> | load integer |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | I → A | LDA x | load index |

#### 13.3.3 STO INSTRUCTION

The STO (Store accumulator) instruction is used to store data into register RAM or output ports. No flags are affected.

**Table 37** STO instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | A → R(r.a.) | STO r <r.a.> | store register |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | A → R(r.a. + I) | STO i <r.a.> | store register indexed |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | A → P(p.n.) | STO p <p.n.> | store port |

### 13.3.4 ADD INSTRUCTION

The ADD (Add to accumulator) instruction is used to add data to the accumulator of the VSP. Flags affected are EQ0 and EQ1.

**Table 38** ADD instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | coefficient | | | | | | | | | | | | A + coeff → A | ADD c <coeff> | add coefficient |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | A + R(r.a.) → A | ADD r <r.a.> | add register |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | A + R(r.a. + I) → A | ADD i <r.a.> | add register indexed |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | A + P(p.n.) → A | ADD p <p.n.> | add port |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | A + s.i. → A | ADD s <s.i.> | add integer |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | A + I → A | ADD x | add index |

### 13.3.5 SUB INSTRUCTION

The SUB (Subtract from accumulator) instruction is used to subtract data from the accumulator of the VSP. Flags affected are EQ0 and EQ1.

**Table 39** SUB instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | coefficient | | | | | | | | | | | | A – coeff → A | SUB c <coeff> | subtract coefficient |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | A – R(r.a.) → A | SUB r <r.a.> | subtract register |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | A – R(r.a. + I) → A | SUB i <r.a.> | subtract register indexed |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | A – P(p.n.) → A | SUB p <p.n.> | subtract port |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | A – s.i. → A | SUB s <s.i.> | subtract integer |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | A – I → A | SUB x | subtract index |

### 13.3.6 MUL INSTRUCTION

The MUL (Multiply with accumulator) instruction is used to multiply data with the accumulator of the VSP. Flags affected are EQ0 and EQ1. The second operand of the multiplication is restricted to 16-bit; e.g. R(r.a.). Range is –8.0000 to +7.9999.

**Table 40** MUL instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | coefficient | | | | | | | | | | | | A × coeff → A | MUL c <coeff> | multiply coefficient |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | A × R(r.a.) → A | MUL r <r.a.> | multiply register |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | A × R(r.a. + I) → A | MUL i <r.a.> | multiply register indexed |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | A × P(p.n.) → A | MUL p <p.n.> | multiply port |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | A × s.i. → A | MUL s <s.i.> | multiply integer |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | A × I → A | MUL x | multiply index |

### 13.3.7 JMFS INSTRUCTION

The JMFS (Jump if flag set) is used for conditional jumps. The jump is carried out when the flag is set, otherwise the PC is simply incremented.

**Table 41** JMFS instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | flag | | | address | | | | | | | | | <addr> → PC | JMFS <f.l.> <addr> |

### 13.3.8 JMFC INSTRUCTION

The JMFC (Jump if flag clear) is used for conditional jumps. The jump is carried out when the flag is clear, otherwise the PC is incremented.

**Table 42** JMFC instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | flag | | | address | | | | | | | | | <addr> → PC | JMFC <f.l.> <addr> |

### 13.3.9 JSFS INSTRUCTION

The JSFS (Jump subroutine if flag set) is used for conditional call to a subroutine. The jump is carried out when the flag is set, otherwise the PC is incremented. Note that the return stack is just one entry deep, so nesting of subroutines is not allowed.

**Table 43** JSFS instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | flag | | | address | | | | | | | | | <o.a> → stack<br><addr> → PC | JSFS <f.l.> <addr> |

### 13.3.10 JSFC INSTRUCTION

The JSFC (Jump subroutine if flag clear) is used for conditional jumps to a subroutine. The jump is carried out when the flag is clear, otherwise the PC is incremented. It should be noted that the return stack is just one entry deep, so nesting of subroutines is not allowed.

**Table 44** JSFC instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | flag | | | address | | | | | | | | | <o.a> → stack<br><addr> → PC | JSFC <f.l.> <addr> |

### 13.3.11 RTN INSTRUCTION

The RTN (Return from subroutine) is used to return from a subroutine.

**Table 45** RTN instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | stack → PC | RTN |

#### 13.3.12 STF INSTRUCTION

The STF (Set/clear flag) instruction is used to set or clear the user flags A, B or C. System flags cannot be set or reset under program control.

**Table 46** STF instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | flag | | | X | X | X | X | X | X | X | X | value | <value> → <f.l.> | STF <f.l.> <value> |

#### 13.3.13 IDX INSTRUCTION

The IDX (Index operations) instruction is used to store and increment/decrement index values. It should be noted that additions to the index register is done in modulo 64. A ‘decrement index register by one’ could therefore be programmed as ‘IDX + 63’. The ‘IDX A’ instruction loads the 6 bits to the left of the binary point into the index register, i.e. it stores the integer part modulo 64 into I.

**Table 47** IDX instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | value | | | | | | <value> → I | IDX = <value> |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | value | | | | | | I + <value> → I | IDX + <value> |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | A → I | IDX A |

### 13.4 The assembler/emulator

A 2-pass assembler and an emulator was made to assist with the development of VSP programs. The software programs are written in ‘C’ and currently run under NT, HPUX and LINUX operating systems. The assembler reads assembler source files and produces a log file, sets of VHDL or Verilog stimuli and an output file containing CSI instructions that, when loaded, will load the executable into the VSP RAM.

Requirements for the assembler source code are:

- One instruction or pseudo instruction (see Table 48) per line
- No empty lines
- A maximum of 512 instructions
- Operation always starts at instruction 0.

**Table 48** Assembler pseudo instructions

| MNEMONIC | INSTRUCTION | DEFINITION |
|---|---|---|
| . label | {<.>< ><label>} | Defines a location inside the source code. Is usually used as an argument to JMF/JSF instructions. |
| define | {<define>< ><label> < ><value> | Defines a variable and assigns a value to it. These variables can then be referenced in the assembler instructions. |
| include | {<include>< ><file name>} | Reads in another source code file and then continues with the current file. |
| -- | {<-->< ><comment> | Defines a comment; the rest of the line is skipped. |
| flag | | For debugging. |
| brk | | Breakpoint for debugging. |

## 14 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | supply voltage | –0.5 | +3.3 | V |
| $I_{DD}$ | supply current | – | 30 | mA |
| $I_{I1}$ | DC current into any pin; except EARP, EARN, AUXSP and BUZ | –10 | +10 | mA |
| $I_{I2}$ | DC current into pins EARP, EARN, AUXSP and BUZ | –100 | +100 | mA |
| $V_I$ | input voltages on all inputs | –0.5 | $V_{DD}$ + 0.5 | V |
| $P_{tot}$ | total power consumption | – | 800 | mW |
| $T_{amb}$ | ambient temperature | –40 | +85 | °C |
| $T_{stg}$ | storage temperature | –65 | +150 | °C |

## 15 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 80 | K/W |

## 16 DC CHARACTERISTICS

$T_{amb}$ = –40 to +85 °C; $V_{SS}$ = 0 V (ground supply pins must be interconnected externally); $V_{DDA} \geq V_{DDD}$; $V_{DDA(bb)} = V_{DDA(vb)} = V_{DDA(vbo)} = V_{DDA(ref)} = V_{DDA}$ = 2.5 to 2.75 V (supply pins must be interconnected externally); all voltages measured with respect to $V_{SS}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{stb(tot)}$ | total standby current | | – | 10 | – | µA |
| $P_{av}$ | average power consumption | $V_{DDD}$ = 1.5 V; $V_{DDA}$ = 2.7 V; without load on audio outputs EARP, EARN, AUXSP and BUZ | – | 15 | – | mW |
| **Digital supply voltage: pin $V_{DDD}$** | | | | | | |
| $V_{DDD}$ | digital supply voltage | | 1.0 | 1.5 | 2.75 | V |
| **Digital input: pins CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and $\overline{\text{RESET}}$** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0.0 | – | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDD}$ | – | $V_{DDD}$ | V |
| $I_{LI}$ | input leakage current | | – | ±1 | – | µA |
| **Digital output: pins BIEN, BOEN, ADO and AMPCTRL** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{sink}$ = 1.5 mA | – | – | $0.2V_{DDD}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{source}$ = 1.5 mA | $0.7V_{DDD}$ | – | – | V |
| **Digital output: pin BIOCLK** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{sink}$ = 1.5 mA | – | – | $0.2V_{DDD}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{source}$ = 1.5 mA | $0.7V_{DDD}$ | – | – | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Digital bidirectional: pins CDO and BDIO** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDD}$ | – | $V_{DDD}$ | V |
| $I_{LI}$ | input leakage current | | – | ±1 | – | µA |
| $V_{OL}$ | LOW-level output voltage | $I_{sink}$ = 1.5 mA | – | – | $0.2V_{DDD}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{source}$ = 1.5 mA | $0.7V_{DDD}$ | – | – | V |
| **Low-swing clock input: pin MCLK** | | | | | | |
| $I_{LI}$ | input leakage current | | – | ±1 | – | µA |
| **Analog supply voltage: pins $V_{DDA(bb)}$, $V_{DDA(vb)}$, $V_{DDA(vbo)}$ and $V_{DDA(ref)}$** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 2.5 | 2.7 | 2.75 | V |
| $I_{DDA}$ | analog supply current | $V_{DDD}$ = 1.5 V; $V_{DDA}$ = 2.7 V; RXON active | – | 3.5 | – | mA |
| **Analog reference: pin $V_{ref}$** | | | | | | |
| $V_{ref}$ | DC reference level | no external load | – | 1.25 | – | V |
| $I_{I(ref)}$ | input source/sink current | | – | 0.1 | – | µA |
| **Analog output: pins IP, IN, QP and QN** | | | | | | |
| $V_{bias(TXIQ)}$ | DC bias level | | 1.175 | 1.25 | 1.325 | V |
| **Analog input: pins MICP and MICN** | | | | | | |
| $V_{ref(MIC)}$ | DC input reference level | | – | $0.5V_{ref}$ | – | V |
| **Analog input: pins AUXMICP and AUXMICN** | | | | | | |
| $V_{ref(AUXMIC)}$ | DC input reference level | | – | $0.5V_{ref}$ | – | V |
| **Analog output: pins EARP and EARN** | | | | | | |
| $V_{bias(EAR)}$ | DC bias level | | – | $V_{ref}$ | – | V |
| **Analog output: pin AUXSP** | | | | | | |
| $V_{bias(AUX)}$ | DC bias level | | – | $V_{ref}$ | – | V |
| **Analog output: pin BUZ** | | | | | | |
| $V_{bias(BUZ)}$ | DC bias level | | – | $V_{ref}$ | – | V |

## 17 AC CHARACTERISTICS

$V_{DDD}$ = 1.0 to 2.75 V; $V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = −40 to +85 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $f_{clk}$ | master clock frequency | | – | 13.0 | – | MHz |
| **Digital input: pins CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and $\overline{\text{RESET}}$** | | | | | | |
| $C_i$ | input capacitance | | – | 5.0 | – | pF |
| **Digital output: pins BIOCLK, BIEN, BOEN, ADO and AMPCTRL** | | | | | | |
| $t_{dLHO}$ | output rise time | output load = 10 pF | – | 10 | – | ns |
| $t_{dHLO}$ | output fall delay | output load = 10 pF | – | 10 | – | ns |
| **Digital bidirectional: pins CDO and BDIO** | | | | | | |
| $C_i$ | input capacitance | | – | 5.0 | – | pF |
| $t_{dLHO}$ | output rise time | output load = 20 pF | – | 10 | – | ns |
| $t_{dHLO}$ | output fall delay | output load = 20 pF | – | 10 | – | ns |
| **Low-swing clock input: pin MCLK** | | | | | | |
| $V_{MCLK}$ | input amplitude | note 1 | 0.1 | – | $0.5V_{DDD}$ | V |
| $\delta_{MCLK}$ | duty factor | | 40 | – | 60 | % |
| **Analog output: pins IP, IN, QP and QN** | | | | | | |
| $t_{st(TXIQ)}$ | output settling time | output load = 10 pF // 10 kΩ, to 1 LSB, for 0.8 to 2.2 V | – | 9.6 | – | µs |
| $R_{o(TXIQ)}$ | output resistance | f < 100 kHz | – | 105 | – | Ω |
| **Analog input: pins IP, IN, QP and QN** | | | | | | |
| $R_{i(RXIQ)}$ | input resistance | differential | 200 | – | – | kΩ |
| $C_{i(RXIQ)}$ | input capacitance | | – | 5 | – | pF |
| **Analog input: pins AUXADC1, AUXADC2, AUXADC3 and AUXADC4** | | | | | | |
| $R_{i(AUXADC)}$ | input resistance | | – | 1 | – | MΩ |
| **Analog input: pins MICP and MICN** | | | | | | |
| $R_{i(eq)(MIC)}$ | equivalent input resistance | differential | 200 | 220 | 320 | kΩ |
| **Analog input: pins AUXMICP and AUXMICN** | | | | | | |
| $R_{i(eq)(AUXMIC)}$ | equivalent input resistance | | 200 | 220 | – | kΩ |
| **Analog output: pins EARP and EARN** | | | | | | |
| $R_{o(EARAMP)}$ | output resistance | f = 1 kHz | 0 | – | 1 | Ω |
| **Analog output: pin AUXSP** | | | | | | |
| $R_{o(AUXAMP)}$ | output resistance | f = 1 kHz | 0 | – | 1 | Ω |
| **Analog output: pin BUZ** | | | | | | |
| $R_{o(BUZ)}$ | output resistance | f = 1 kHz | 0 | – | 1 | Ω |

**Note**

1. Input MCLK is internally AC coupled; the signal must not go below $V_{SS}$ or above $V_{DDD}$.

## 18 FUNCTIONAL CHARACTERISTICS

### 18.1 Baseband transmit (BSI to TXI/Q)

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $RES_{TXIQ}$ | resolution of TX DACs | | – | 10 | – | bit |
| $S/N_{TXIQ}$ | signal-to-noise ratio of TX DACs | | – | 55 | – | dB |
| $FSIN_{TXIQ}$ | input sampling frequency | | – | 270.833 | – | kHz |
| $V_{O(TXIQ)(p-p)}$ | output signal amplitude (peak-to-peak value) | note 1 | 0.9 | 1.0 | 1.1 | V |
| $V_{DC(TXIQ)}$ | output DC level | | 1.15 | 1.25 | 1.35 | V |
| $AMAT_{TXIQ}$ | output amplitude matching between I and Q TX paths | note 1 | –2.0 | – | +2.0 | % |
| | | | –0.2 | – | +0.2 | dB |
| $VOFS_{TXIQ}$ | differential DC offset voltage between IP/IN or QP/QN | note 1 | –4.5 | – | +4.5 | mV |
| $FRESP_{TXIQ}$ | output spectrum for a random input signal referred to a periodic signal at 67 kHz and a measurement bandwidth of 30 kHz | f = 0 to 100 kHz | –3 | – | – | dB |
| | | f = 200 kHz | – | – | –30 | dB |
| | | f = 250 kHz | – | – | –33 | dB |
| | | f = 400 kHz | – | – | –60 | dB |
| | | f = 600 kHz | – | – | –70 | dB |
| | | f = 1200 kHz | – | – | –70 | dB |
| | | f > 1800 kHz | – | – | –70 | dB |
| $MPEI_{TXIQ}$ | maximum phase effect instance | note 2 | – | 22 | – | µs |
| $AGD_{TXIQ}$ | absolute group delay | note 1 | – | 10 | – | µs |
| $GDL_{TXIQ}$ | group delay linearity | measured at full-scale; 10 kHz < f < 100 kHz; load: 10 pF // 10 kΩ | – | 100 | – | ns |
| $GDMAT_{TXIQ}$ | group delay matching of I and Q TX paths | | – | – | 40 | ns |
| $PMAT_{TXIQ}$ | phase matching of I and Q TX paths | note 1 | – | 0.5 | – | deg |
| $PTERMS_{TXIQ}$ | RMS phase trajectory error | random input pattern; notes 1 and 3 | – | 0.5 | 0.8 | deg |
| $PTEPEAK_{TXIQ}$ | peak phase trajectory error | | – | 1.5 | 3.0 | deg |

**Notes**

1. Measured at full-scale; load: 10 pF // 10 kΩ; f = 67 kHz.
2. Not tested. Defined between the rising edge of BIOCLK which latches a data bit at BDIO to its corresponding maximum phase change on the analog outputs I and Q TX paths.
3. Not tested.

### 18.2 Baseband receive (RXI/Q to BSI)

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C; all values valid for ZIF and NZIF modes.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $RES_{RXIQ}$ | resolution | I and Q word length at BSI | – | 12 | – | bit |
| $S/N_{RXIQ}$ | signal-to-noise ratio | f = 67 kHz; $V_i$ = 3 V (p-p) | – | 66 | – | dB |
| $V_{ICM(RXIQ)}$ | input common mode voltage | (IP + IN)/2; (QP + QN)/2; referred to $V_{SS}$ | 1.0 | 1.25 | 1.5 | V |
| $V_{IDM(RXIQ)}$ | input differential voltage | (IP – IN); (QP – QN) | –1.5 | – | +1.5 | V |
| $FSIN_{RXIQ}$ | input sampling frequency | ZIF mode | – | 6.5 | – | MHz |
| | | NZIF mode | – | 13 | – | MHz |
| $FSOUT_{RXIQ}$ | output sample rate | ZIF mode | – | 270.833 | – | kHz |
| | | NZIF mode | – | 541.667 | – | kHz |
| $FRESP_{RXIQ}$ | frequency response | referred to f = 10 kHz; ZIF mode | | | | |
| | | f = 0 to 70 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | –0.8 | 0 | +0.3 | dB |
| | | f = 90 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | –2.0 | – | dB |
| | | f = 100 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | –4.5 | – | dB |
| | | f = 200 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | – | –35 | dB |
| | | f > 220 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | – | –45 | dB |
| | | referred to f = 20 kHz; NZIF mode | | | | |
| | | f = 0 to 140 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | –0.8 | 0 | +0.3 | dB |
| | | f = 180 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | –2.0 | – | dB |
| | | f = 200 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | –4.5 | – | dB |
| | | f = 400 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | – | –35 | dB |
| | | f > 440 kHz; $V_{IDM(RXIQ)}$ = 150 mV (p-p) | – | – | –45 | dB |
| $DR_{ICN\_RXIQ}$ | dynamic signal range | f = 20 Hz to 135 kHz; ZIF mode | 60 | 68 | – | dB |
| | | f = 20 Hz to 270 kHz; NZIF mode | 60 | 68 | – | dB |
| $SINAD_{RXIQ}$ | signal-to-noise and distortion ratio | f = 20 kHz; $V_{IDM(RXIQ)}$ = 2 V (p-p) | 40 | – | – | dB |
| OPC | output code in BDIO | for maximum input amplitude | – | ±1450 | – | LSB |
| $PSRR_{RXIQ}$ | power supply ripple rejection | applying a 217 Hz sine wave of 100 mV (p-p) on top of the analog supply voltage | – | 70 | – | dB |
| $GERR_{RXIQ}$ | gain error | referenced to maximum amplitude | –6 | – | +6 | % |
| | | | –0.5 | – | +0.5 | dB |
| $GMAT_{RXIQ}$ | gain matching error | at maximum input amplitude | –4 | – | +4 | % |
| | | | –0.35 | – | +0.35 | dB |
| $GDMAT_{RXIQ}$ | group delay matching of I and Q RX paths | at maximum input amplitude; 10 kHz < f < 100 kHz | – | – | 5 | ns |
| $OFFS_{RXIQ}$ | offset error | | –30 | – | +30 | mV |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $POST_{RXIQ}$ | power-on settling time | including decimator; ZIF mode | – | 111 | – | µs |
| | | | – | 120 | – | QB |
| | | including decimator; NZIF mode | – | 55.5 | – | µs |
| | | | – | 60 | – | QB |
| $FGD_{RXIQ}$ | filter group delay | ZIF mode | – | 23 | – | µs |
| | | NZIF mode | – | 11.5 | – | µs |

### 18.3 Voice band transmit (microphone to ASI)

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C; TXPGA = 0 dB; firmware version “vb10.0”; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $RES_{MICADC}$ | resolution of ADC | | – | 13 | – | bit |
| $FSIN_{MICADC}$ | internal sampling frequency | | – | 1000 | – | kHz |
| $GRAN_{TXPGA}$ | calibration gain range | | –24 | 0 | +12 | dB |
| $GSTP_{TXPGA}$ | calibration gain step size | see Table 26 | – | 64 | – | steps |
| $GTOL_{VBTX}$ | gain tolerance of coder | | –1.5 | – | +1.0 | dB |
| $FRESP_{VBTX}$ | digital filter frequency response of implemented standard VSP software (version: vb5_all) | f < 100 Hz | – | – | –20 | dB |
| | | 100 Hz < f < 200 Hz | – | – | –10 | dB |
| | | f = 300 Hz to 3.3 kHz | –1 | – | +1 | dB |
| | | f = 3.3 to 3.4 kHz | –1.5 | – | 0 | dB |
| | | f ≥ 4 kHz | – | – | –20 | dB |
| $FREJ_{VBTX}$ | out-of-band rejection | f = 4.6 kHz | 40 | 45 | – | dB |
| | | f = 6 to 30 kHz | 45 | 50 | – | dB |
| **Microphone/auxiliary signal path** | | | | | | |
| $V_{O(nom)}$ | nominal output level | f = 1 kHz at –35 dBm input level | – | –4 | – | dBFS |
| $V_{I(rms)}$ | nominal input level (RMS value) | TXPGA = 0 dB, MICHI = 1 | – | – | –35 | dBm |
| | | TXPGA = 0 dB, MICHI = 0 | – | – | –7 | dBm |
| $N_{IDLE}$ | idle noise level (pin ADO) | $T_{amb}$ = 25 °C; psophometrically weighted; note 1 | – | – | –75 | dBm0p[2] |
| THD | total harmonic distortion | f = 1 kHz; maximum input level; TXPGA = 3 dB | – | – | 1 | % |
| SINAD | signal-to-noise and distortion | ADO = 3 dBm0 | 30 | – | – | dB |
| | | ADO = 0 dBm0 | 40 | – | – | dB |
| | | ADO = –10 dBm0 | 45 | – | – | dB |
| | | ADO = –20 dBm0 | 45 | – | – | dB |
| | | ADO = –30 dBm0 | 40 | – | – | dB |
| | | ADO = –40 dBm0 | 30 | – | – | dB |
| | | ADO = –45 dBm0 | 25 | – | – | dB |
| $PSCT_{VBTX}$ | supply voltage crosstalk | applying a 437 Hz sine wave of 100 mV (p-p) on top of the analog supply voltage | – | – | 2 | LSB |
| **Audio Serial Interface (ASI)** | | | | | | |
| FDATA | PCM output bit rate | equal for ADI and ADO | 128 | – | 5000 | kbits/s |
| $FSYNC_{AFS}$ | PCM frame synchronization frequency at pin AFS | fixed to 8 kHz at pin AFS | – | 8 | – | kHz |

**Notes**

1. Psophometrical weighting: a frequency weighting curve described in *“ITU recommendation O.41”*.
2. The unit dBm0p: 0 dBm0p is generally defined as –3.14 dBFS, where dBFS denotes dB full-scale, i.e. a signal with an amplitude covering the complete range of digital values. The suffix ‘p’ refers to psophometrical weighting.

### 18.4 Voice band receive (ASI to earphone)

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C; analog gain setting = –6 dB; RXVOL = –12 dB; RXPGA = 0 dB; firmware version “vb10.0”; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $RES_{EARDAC}$ | resolution of DAC | | – | 13 | – | bit |
| $FSIN_{EARDAC}$ | internal sampling frequency | | – | 1000 | – | kHz |
| $GRAN_{VOL}$ | gain step range | | –30 | – | +6 | dB |
| $GSTP_{VOL}$ | gain step size | digital steps; see Table 26 | – | 64 | – | steps |
| $GRAN_{PGA}$ | calibration PGA range | | –24 | 0 | +12 | dB |
| $GSTP_{PGA}$ | gain step size | digital steps; see Table 26 | – | 64 | – | steps |
| $GTOL_{VBRX}$ | gain tolerance of decoder | | –1 | – | +1 | dB |
| $GMUTE_{VBRX}$ | mute attenuation of decoder | | 40 | – | – | dB |
| $FRESP_{VBRX}$ | frequency response | f = 0 to 100 Hz | – | – | –20 | dB |
| | | f = 300 to 3300 Hz | –1.0 | – | +1.0 | dB |
| | | f = 3300 to 3400 Hz | –2.0 | – | +1.0 | dB |
| | | f = 4000 Hz | – | – | –18 | dB |
| $FSPUR_{VBRX}$ | spurious out-of-band signals | f = 4600 Hz | – | – | –38 | dB |
| | | f = 28.6 kHz | – | – | –40 | dB |
| **Receive outputs: EARP and EARN** | | | | | | |
| $V_{ref(EAR)}$ | DC reference level | | – | $V_{ref}$ | – | V |
| $V_{o(EAR)(p-p)}$ | output voltage (peak-to-peak value) | load: 16 Ω differential | 4[1] | – | – | V |
| | | load: 8 Ω single-ended | 1.5[1] | – | – | V |
| $I_{o(EAR)peak}$ | output source/sink peak current | load: 8 Ω single-ended | – | 100 | – | mA |
| $OPL_{EAR}$ | nominal level between EARP and EARN for 0 dBm0 at ADI | load: 32 Ω; f = 1000 Hz | | | | |
| | | differential | –16.6 | –15.6 | –14.6 | dBm |
| | | single-ended | –22.6 | –21.6 | –20.6 | dBm |
| $GRAN_{SIDVOL}$ | total sidetone gain (from MICP and MICN to EARP and EARN) | | –30 | – | +6 | dB |
| $THD_{EAR}$ | total harmonic distortion | at maximum $V_{DD}$ | – | – | 1 | % |
| $IDLN_{EAR}$ | idle noise at EARP and EARN | A-weighted | – | – | –72 | dBm |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $SINAD_{EAR}$ | signal-to-noise and distortion ratio from ASI to earphone | psophometrically weighted(2) | | | | |
| | | at 3 dBm0 input signal level | 30 | – | – | dB |
| | | at 0 dBm0 input signal level | 35 | – | – | dB |
| | | at –10 dBm input signal level | 45 | – | – | dB |
| | | at –20 dBm input signal level | 42 | – | – | dB |
| | | at –30 dBm input signal level | 40 | – | – | dB |
| | | at –40 dBm input signal level | 30 | – | – | dB |
| | | at –45 dBm input signal level | 25 | – | – | dB |
| $PSRR_{EAR}$ | power supply ripple rejection at EARP and EARN | applying a 437 Hz sine wave of 100 mV (p-p) on top of the analog supply voltage | 70 | – | – | dB |
| **Auxiliary output: AUXSP** | | | | | | |
| $V_{ref(AUXSP)}$ | DC reference level | | – | $V_{ref}$ | – | V |
| $V_{o(AUXSP)(p-p)}$ | output voltage (peak-to-peak value) | load: 16 Ω with 47 μF in series to ground supply | 2 | – | – | V |
| | | load: 8 Ω with 100 μF in series to ground supply | 1.5 | – | – | V |
| $I_{o(AUXSP)peak}$ | output source/sink peak current | load: 16 Ω with 47 μF in series to ground supply | – | 62.5 | – | mA |
| $OPL_{AUXSP}$ | nominal level at AUXSP for 0 dBm0 at ADI | load: 16 Ω with 47 μF in series to ground supply | –22 | –21 | –20 | dBm |
| **Buzzer output: BUZ** | | | | | | |
| $V_{ref(BUZ)}$ | DC reference level | | – | $V_{ref}$ | – | V |
| $V_{o(BUZ)(p-p)}$ | output voltage (peak-to-peak value) | load: 16 Ω with 47 μF in series to ground supply | 2 | – | – | V |
| | | load: 8 Ω with 100 μF in series to ground supply | 1.5 | – | – | V |
| $I_{o(BUZ)peak}$ | output source/sink peak current | load: 16 Ω with 47 μF in series to ground supply | – | 62.5 | – | mA |
| $OPL_{BUZ}$ | nominal level at BUZ for 0 dBm0 at ADI | load: 16 Ω with 47 μF in series to ground supply | –22 | –21 | –20 | dBm |

**Notes**

1. Not tested: guaranteed by design.
2. Psophometrical weighting: a frequency weighting curve described in *“ITU recommendation O.41”*.
3. The unit dBmp: 0 dBmp refers to a voltage of a signal of 1 mW across a 600 Ω load. The suffix ‘p’ refers to psophometrical weighting.

### 18.5 Auxiliary digital-to-analog converters

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **AUXDAC1** | | | | | | |
| $RES_{DAC1}$ | resolution | | – | 8 | – | bit |
| $VOMIN_{DAC1}$ | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| $VOMAX_{DAC1}$ | maximum output voltage | register value: 0FFH | 2.1 | 2.2 | 2.3 | V |
| $VDEF_{DAC1}$ | output voltage after reset | register value: 085H | – | 1.147 | – | V |
| $MON_{DAC1}$ | monotonicity range | | – | 8 | – | bit |
| $INL_{DAC1}$ | integral non-linearity(1) | | –5.0 | – | +5.0 | LSB |
| $DNL_{DAC1}$ | differential non-linearity(2) | | –1.0 | – | +1.0 | LSB |
| $OFFS_{DAC1}$ | offset error | | –40 | – | +40 | mV |
| $FSST_{DAC1}$ | full-scale settling time | load: 50 pF // 2 kΩ to $V_{SS}$; see Fig.13a | – | 40 | – | µs |
| $LSBST_{DAC1}$ | one LSB settling time | | – | 8 | – | µs |
| **AUXDAC2** | | | | | | |
| $RES_{DAC2}$ | resolution | | – | 12 | – | bit |
| $VOMIN_{DAC2}$ | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| $VOMAX_{DAC2}$ | maximum output voltage | register value: FFFH | 2.1 | 2.2 | 2.32 | V |
| $VDEF_{DAC2}$ | output voltage after reset | register value: 800H | – | 1.1 | – | V |
| $MON_{DAC2}$ | monotonicity range | | – | 12 | – | bit |
| $INL_{DAC2}$ | integral non-linearity(1) | | –10 | – | +10 | LSB |
| $DNL_{DAC2}$ | differential non-linearity(2) | | –1.0 | – | +2.0 | LSB |
| $OFFS_{DAC2}$ | offset error | | –25 | – | +25 | mV |
| $FSST_{DAC2}$ | full-scale settling time | load: 50 pF // 10 kΩ to $V_{SS}$; see Fig.13b | – | 40 | – | µs |
| $LSBST_{DAC2}$ | one LSB settling time | | – | 8 | – | µs |
| $POST_{DAC2}$ | power-on settling time | see Section 18.1 | – | – | 4 | ms |
| **AUXDAC3** | | | | | | |
| $RES_{DAC3}$ | resolution | | – | 10 | – | bit |
| $VOMIN_{DAC3}$ | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| $VOMAX_{DAC3}$ | maximum output voltage | register value: 3FFH | 2.1 | 2.2 | 2.3 | V |
| $MON_{DAC3}$ | monotonicity range | | – | 10 | – | bit |
| $INL_{DAC3}$ | integral non-linearity(1) | | –5.0 | – | +5.0 | LSB |
| $DNL_{DAC3}$ | differential non-linearity(2) | | –1.0 | – | +1.0 | LSB |
| $OFFS_{DAC3}$ | offset error | | –40 | – | +40 | mV |
| $FSST_{DAC3}$ | full-scale settling time | load: 50 pF // 1 kΩ to $V_{SS}$; see Fig.13c | 1 | 10 | 15 | µs |
| $LSBST_{DAC3}$ | one LSB settling time | | – | 2.5 | – | µs |
| $SSC_{DAC3}$ | output source/sink current | | – | – | 2.5 | mA |

**Notes**

1. INL: the difference of the output to the best fit line. $INL_{(i)} = [V_{(i)} - (a + i \times b)]/1$ LSB; $INL = (INL_{(i)(max)} - INL_{(i)(min)})/2$.
2. DNL is the difference between individual code width and average code width (1 LSB); maximum and minimum specified. $DNL_{(i)} = [(V_{(i+1)} - V_{(i)} - 1\ LSB)/1\ LSB]$; $DNL_{(min)} > -1$ is equivalent to monotonicity $V_{(i+1)} > V_{(i)}$.

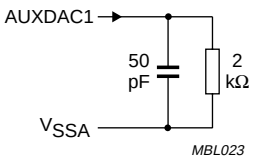
### 18.6 Auxiliary analog-to-digital converters

$V_{DDA}$ = 2.5 to 2.75 V; $T_{amb}$ = –40 to +85 °C.

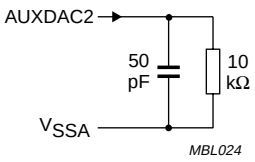
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **AUXADC1, AUXADC2, AUXADC3 and AUXADC4** | | | | | | |
| $RES_{AUXADC}$ | resolution | coded in 12 bits | – | 1480 | – | LSB |
| $VIN_{AUXADC}$ | input voltage | | 0.0 | – | 2.0 | V |
| $VIN_{AUXADCMIN}$ | $V_i$ for output code 0 | | –20 | – | +20 | mV |
| $VIN_{AUXADCMAX}$ | $V_i$ for maximum output code | after offset compensation | – | 2.0 | – | V |
| $R_{i(AUXADC)}$ | input resistance | | – | 1.0 | – | MΩ |
| $INL_{AUXADC}$ | integral non-linearity | | – | 2.5 | – | mV |
| $DNL_{AUXADC}$ | differential non-linearity | | – | 2.5 | – | mV |
| $GERR_{AUXADC}$ | gain error | $V_i$ = 2 V | –0.5 | – | + 0.5 | dB |
| $MATCH_{AUXADC}$ | matching of AUXADCs | | – | 5 | – | LSB |
| $OFFS_{AUXADC}$ | offset error after compensation | | –3 | – | +3 | LSB |
| $POST_{AUXADC}$ | power-on settling time | | – | 160 | – | µs |
| $POST_{ADCOFF}$ | settling time for offset compensation | | – | 160 | – | µs |

### 18.7 Typical output loads

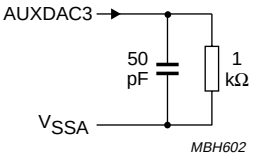
Figure 13 illustrates the typical loads for the outputs: AUXDAC1, AUXDAC2, AUXDAC3, EARP, EARN, AUXSP and BUZ.



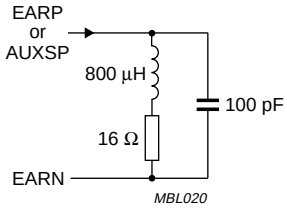

a. AUXDAC1.



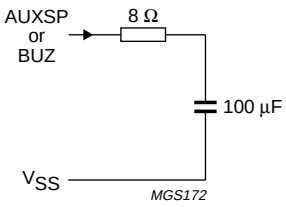

b. AUXDAC2.



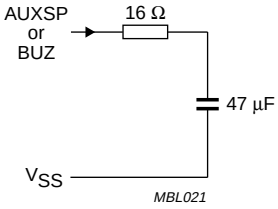

c. AUXDAC3.




d. EARP or AUXSP and EARN.




e. AUXSP or BUZ; R = 8 Ω.




f. AUXSP or BUZ; R = 16 Ω.

Fig.13 Typical output loads.

## 19 APPLICATION INFORMATION

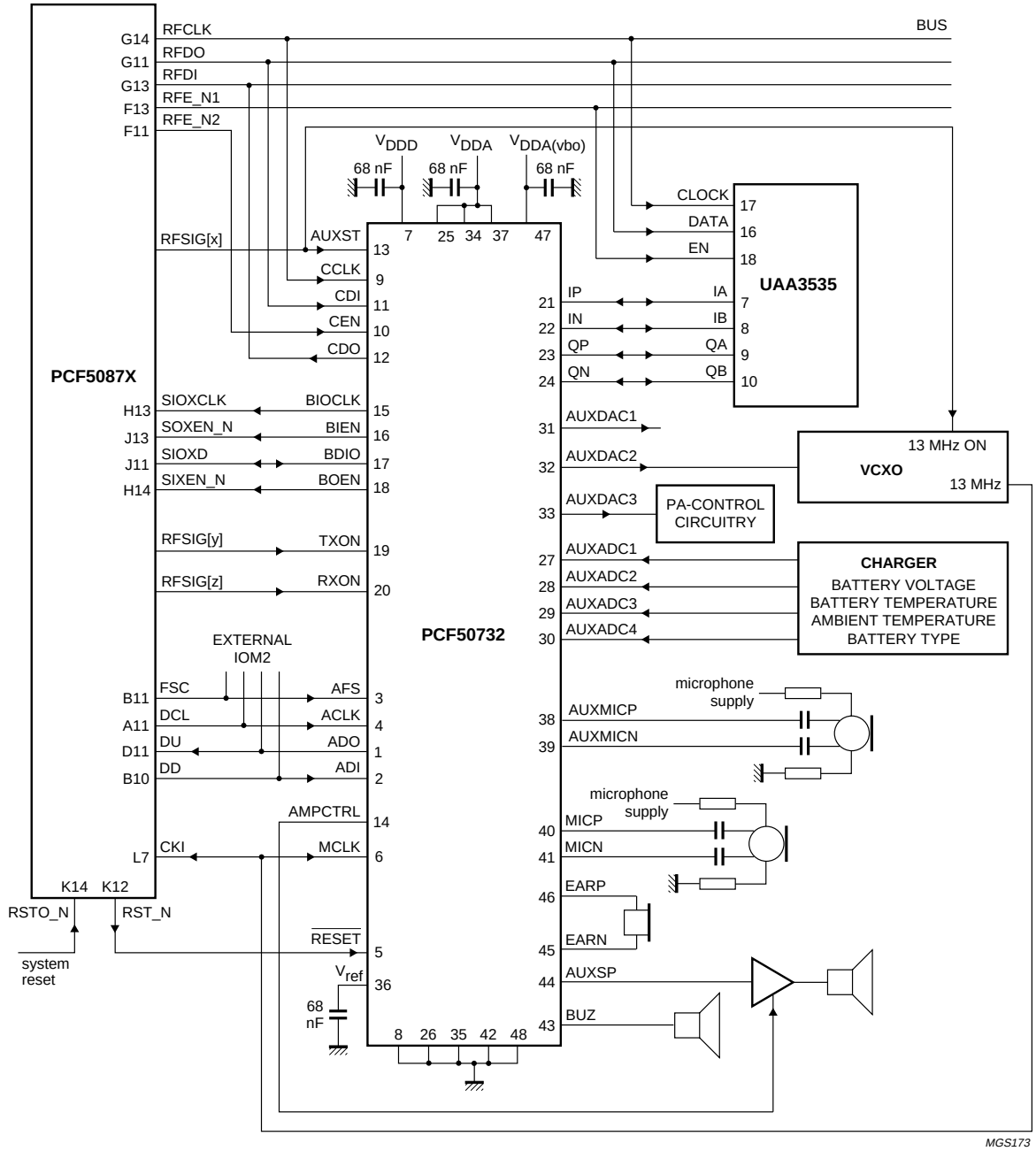



Fig.14 Application diagram.

### 19.1 Wake-up procedure from Sleep mode

Apart from being the status control signal of AUXDAC1, AUXDAC2 and the MCLK input, AUXST also starts a down-counter at each rising edge which controls the output drive capability of pin $V_{ref}$. This is important for the following considerations. For current consumption reduction during Sleep mode there are **two** possibilities as shown in Section 19.1.1 and 19.1.2.

#### 19.1.1 Possibility 1

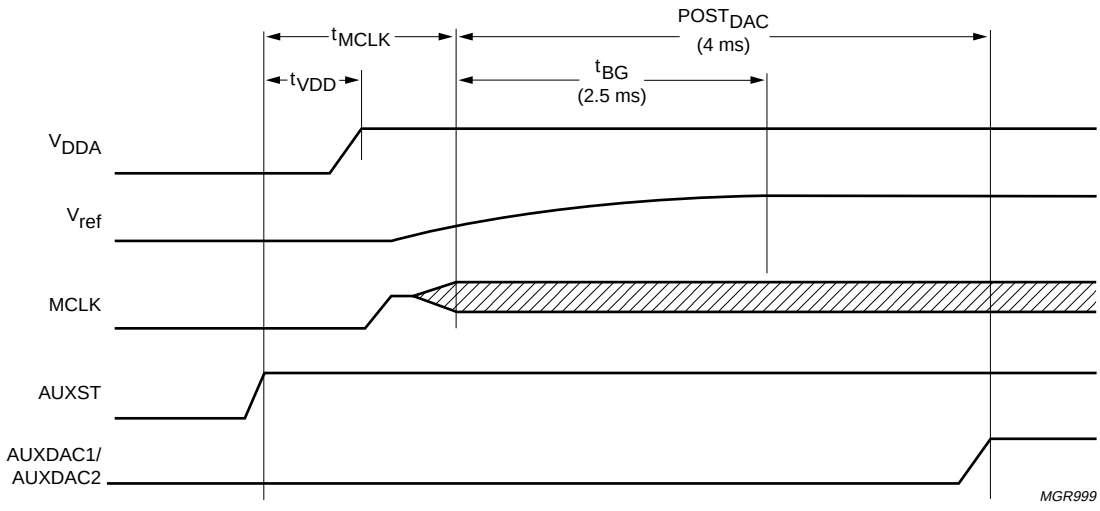
Program every block into power-down via CSI except for the band gap, then pull AUXST LOW to switch off the clock internally. This results in a $I_{DD(total)}$ = 60 µA (typical). Since the band gap has not been programmed into power-down, the only active reference is $V_{ref}$. After a rising edge of AUXST, $POST_{DAC}$ is in the order of 1.5 ms.

#### 19.1.2 Possibility 2

If AUXST is also used to switch off the analog supply voltage, all references are shut down. The power-up time in this case is measured from the point where the MCLK clock input has valid levels or $V_{DDA}$ has settled to its final value (the latter of the two signals sets the reference point).

A down-counter increases the band gap output drive capability for 32768 MCLK cycles which equals approximately 2.5 ms. After that time the voltage at $V_{ref}$ has reached ±0.5 mV of its final value. The timing diagram illustrates the situation (see Fig.15). Other points to note for this possibility:

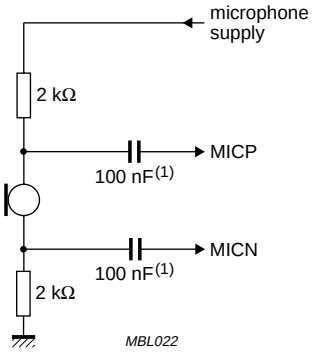
- As long as $V_{DDD}$ is not switched off, all registers keep their values
- As long as $V_{DDA(bb)}$ is not stable, the internal master clock is not running, because the first stage of the clock generator is supplied by $V_{DDA}$
- All digital signals **MUST** remain stable for $t_{MCLK}$ after AUXST has gone HIGH. This is necessary to avoid any timing violations in the digital part of the PCF50732 caused by an unstable MCLK clock input
- The previously mentioned 2.5 ms for $t_{BG}$ are only valid for **$C_{Vref}$ = 68 nF ±10%** or less. The maximum value (68 nF) is highly recommended for good noise and power supply rejection figures.

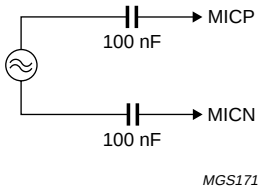



$t_{VDD}$: settling time until $V_{DDA(bb)}$ has reached 95% of its final value. It is assumed that $t_{MCLK} > t_{VDD}$; otherwise $t_{BG}$ and $POST_{DAC}$ are related to $t_{VDD}$.
$t_{MCLK}$: settling time until MCLK clock has reached at least 100 mV (peak-to-peak) level and a frequency of 13 MHz ±10 kHz.
$t_{BG}$: settling time until voltage at $V_{ref}$ has reached ±0.5 mV of its final value for **$C_{Vref}$ = 68 nF ±10%.**
$POST_{DAC}$: settling time until AUXDAC1 and AUXDAC2 have reached their previously programmed value ±2 LSBs.

Fig.15 Possible timing of wake-up sequence.

### 19.2 Microphone input connection and test set-up




(1) 10 nF can be used instead of 100 nF for high-pass filtering.

a. Microphone input connection.

b. Microphone input test set-up.

Fig.16 Microphone input connection and test set-up.

### 19.3 Voice band start-up procedure

Some precautions should be taken to avoid audible clicks at the power-up of the voice band. These are:

1. The firmware should reset the registers of the VSP and reset the noise shaper and FIR blocks
2. The frame clock (AFS) and bit clock (ACLK) signals should be up and running before the audio circuitry is activated
3. The output amplifiers should then only be switched on after sufficient time has elapsed for the firmware to settle; this is of course dependant on the firmware itself but should be at least 300 μs.

An assembler/emulator for the VSP has been written in order to facilitate the development of new firmware. It is strongly suggested to study the existing firmware since it contributes heavily to the performance of the device.

### 19.4 Instruction RAM read out

Due to the different clock domains used in the chip the readout of the VSP instruction RAM is somewhat complicated. Although this function is not normally needed we suggest the following approach for reading out the IRAM content:

vsp_ps = x: write value x into the program counter

read_data_high: get the content of the VSP IRAM high byte

read_data_low: get the content of the VSP IRAM low byte.

Procedure:

```
---------------------------------
vsp_pc = 0
for (i=1; i<512;i=i+1) do
              begin
              vsp_pc = i;
              result[i-1]=read_data_high*256 + read_data_low;
              end
vsp_pc=0;
result[511]=read_data_high*256 + read_data_low;
---------------------------------
```

### 19.5 Power consumption diagrams

The following diagrams show some power consumption figures for the different modes the device typically encounters in a GSM phone. The Idle mode graph shows the dependency between consumption and temperature, while all other graphs also show the dependence between consumption and supply voltage.

It should be noted that the auxiliary DACs have internal pull-down resistors of 10 kΩ each. This means that the current consumption is dependant on the average code at the DACs inputs. The diagrams were measured with the default values for DAC1 and DAC2 and with code 511 on DAC3.

External interfaces are not included. For a signal at the differential earpiece output of amplitude A across a load resistance of R, an average current I must be added:

$$I = \frac{\pi}{4} \cdot \frac{A}{R}$$

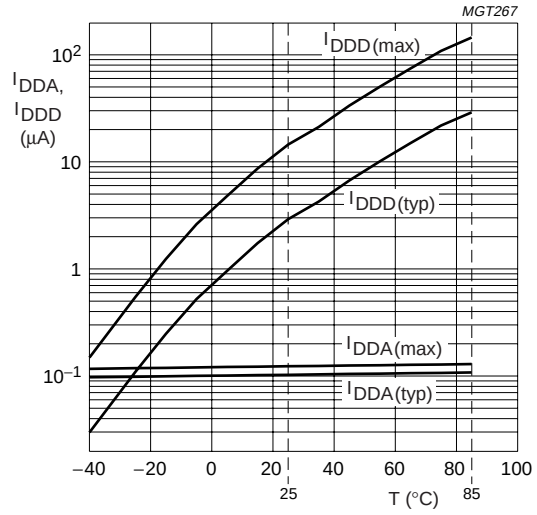
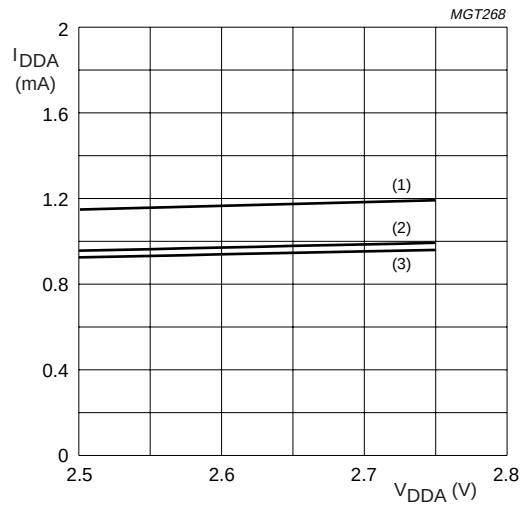
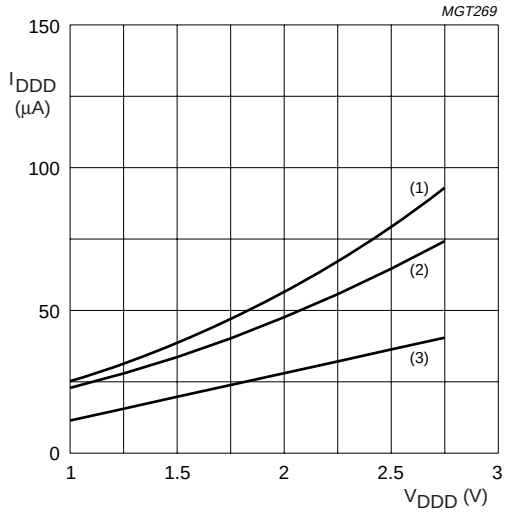



Fig.17 $I_{DDA}$ and $I_{DDD}$ in Idle mode as a function of the temperature.



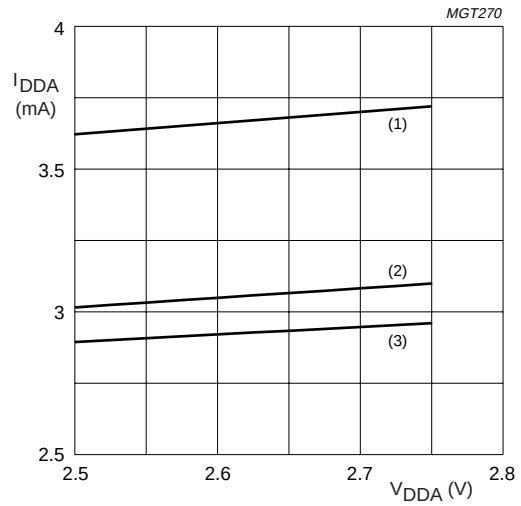

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.18 $I_{DDA}$ in standby mode as a function of $V_{DDA}$.



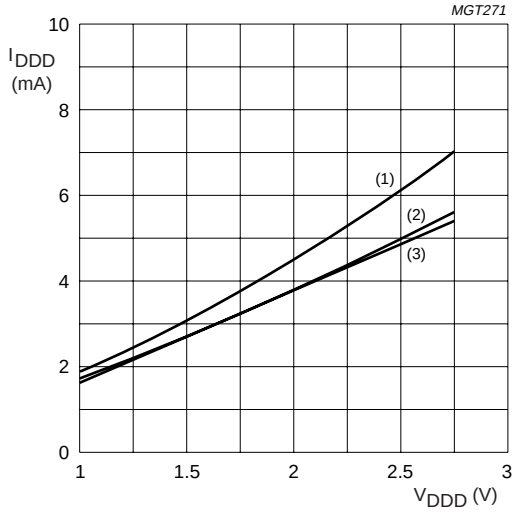

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.19 $I_{DDD}$ in standby mode as a function of $V_{DDD}$.



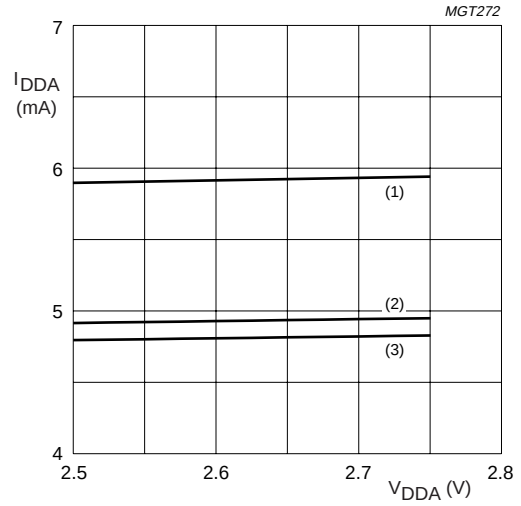

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.20 $I_{DDA}$ in paging mode as a function of $V_{DDA}$.



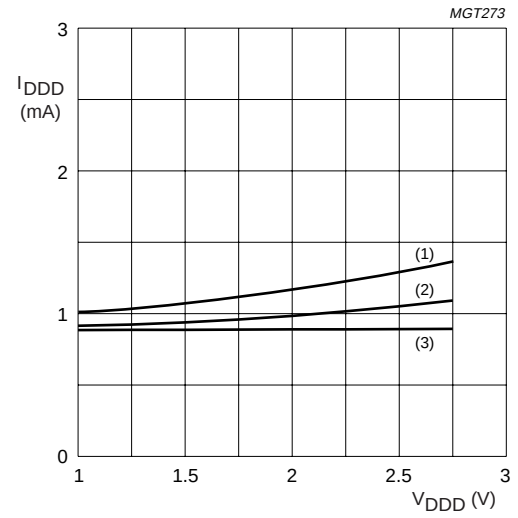

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.21 $I_{DDD}$ in paging mode as a function of $V_{DDD}$.



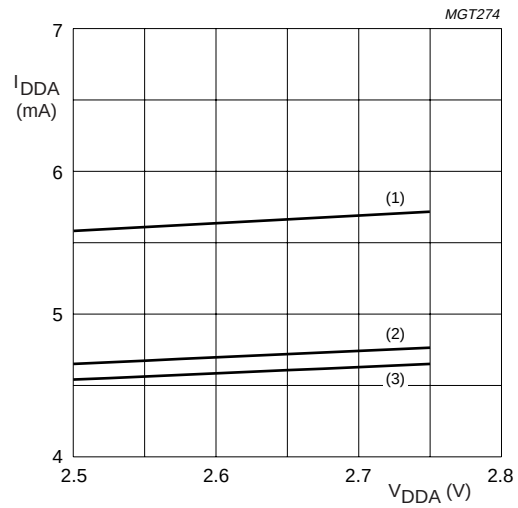

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.22 $I_{DDA}$ during baseband transmit as a function of $V_{DDA}$.



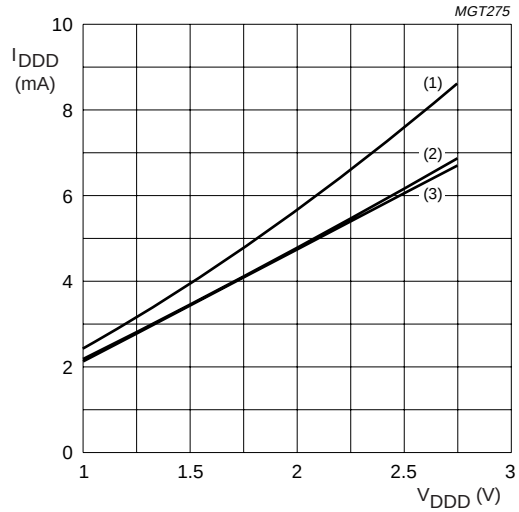

(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

Fig.23 $I_{DDD}$ during baseband transmit as a function of $V_{DDD}$.




(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

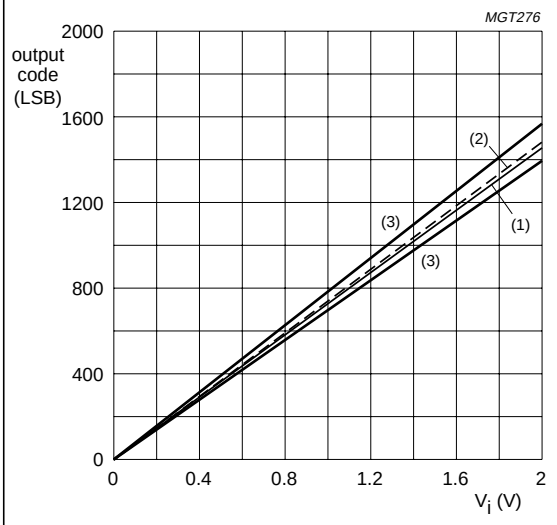
Fig.24 $I_{DDA}$ during full operation as a function of $V_{DDA}$.




(1) $T_{amb(max)}$ = 85 °C.
(2) $T_{amb(typ)}$ = 85 °C.
(3) $T_{amb(typ)}$ = 25 °C.

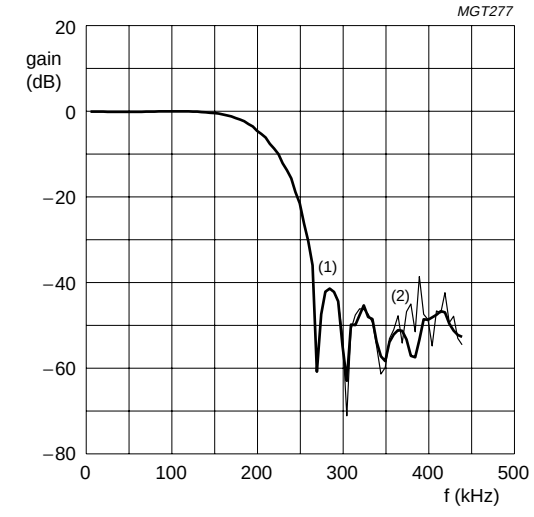
Fig.25 $I_{DDD}$ during full operation as a function of $V_{DDD}$.

### 19.6 Typical performance figures




(1) Measured curve.
(2) Ideal curve.
(3) Specification limits.

Fig.26 AUXADC transfer function.




(1) Differential input voltage 300 mV (p-p).
(2) Differential input voltage 3 V (p-p).

Fig.27 Baseband receive frequency response (NZIF mode).

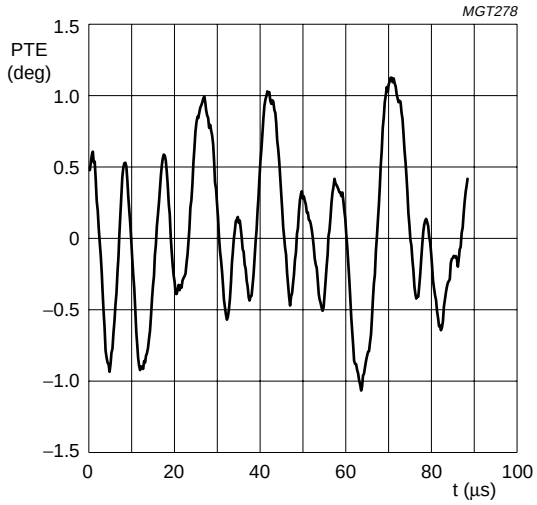
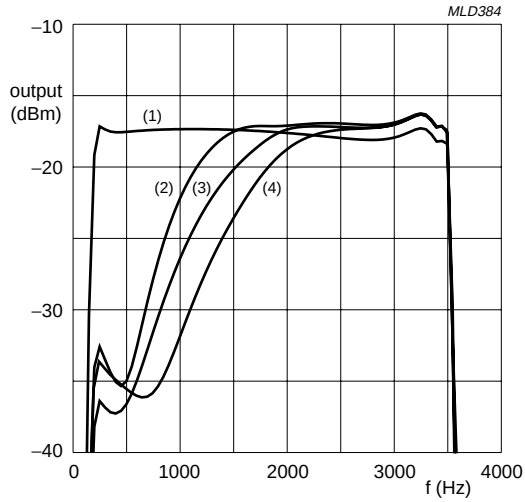
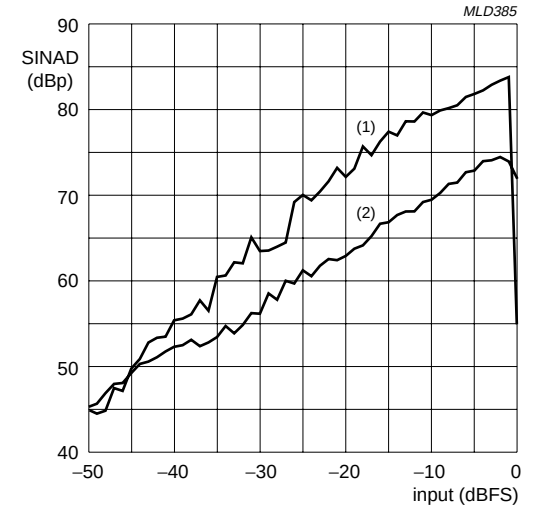



Fig.28 Baseband transmit Phase Trajectory Error (PTE).



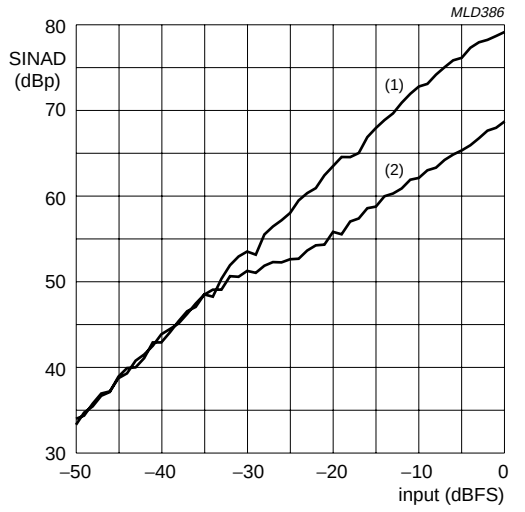

(1) EQ0.
(2) EQ1.
(3) EQ2.
(4) EQ3.

Fig.29 Voice band receive section filter characteristic.



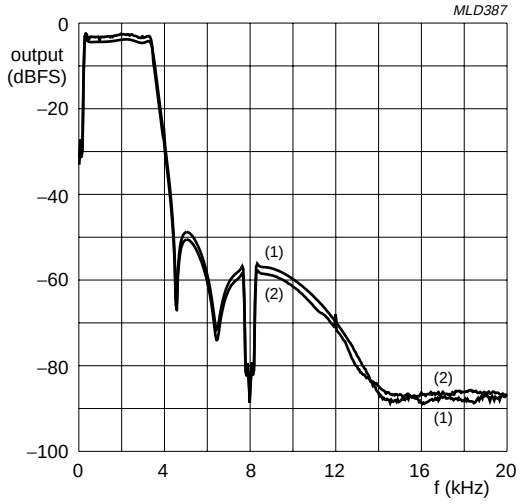

(1) 3000 Hz.
(2) 1000 Hz.

Fig.30 Voice band receive section SINAD (maximum output).



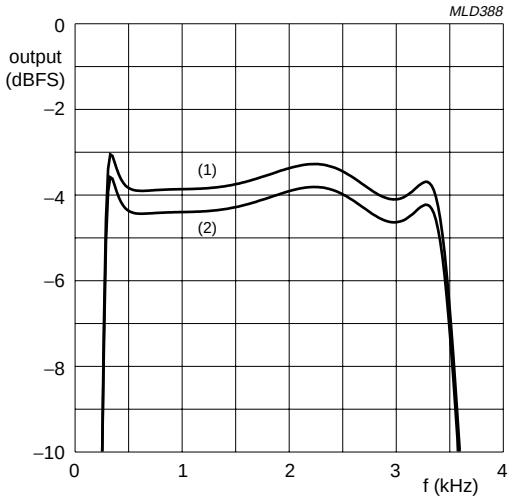

(1) 3000 Hz.
(2) 1000 Hz.

Fig.31 Voice band receive section SINAD (nominal output).



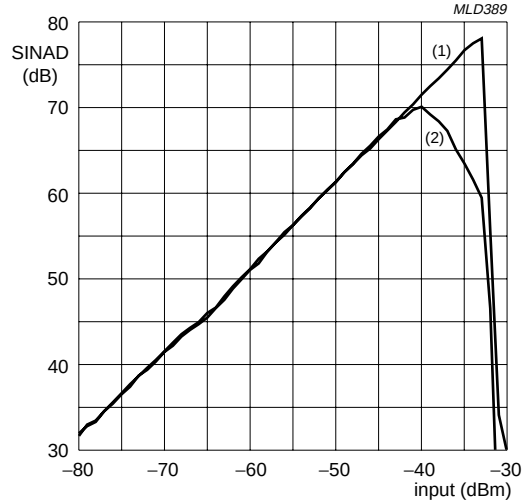

(1) Low gain.
(2) High gain.

Fig.32 Voice band transmit section filter characteristic.



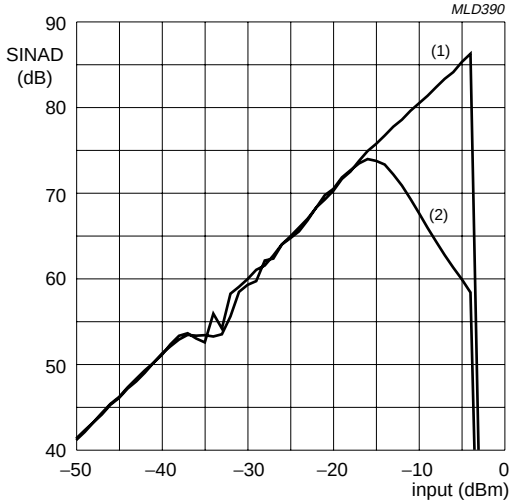

(1) High gain.
(2) Low gain.

Fig.33 Voice band transmit section filter characteristic (pass band detail).




(1) 3000 Hz.
(2) 1000 Hz.

Fig.34 Voice band transmit section SINAD (high gain mode).




(1) 3000 Hz.
(2) 1000 Hz.

Fig.35 Voice band transmit section SINAD (low gain mode).

## 20 GLOSSARY OF ABBREVIATIONS AND TERMS

| | |
|---|---|
| AFC | Automatic frequency control (control of the external system clock oscillator). |
| AGC | Automatic gain control (control of an external gain control part in the RF section of a phone). |
| ASI | The digital audio serial interface. |
| AUXDAC | The auxiliary digital-to-analog converters AUXDAC1 (8-bit), AUXDAC2 (12-bit), AUXDAC3 (10-bit, power ramping). |
| BB | The baseband section. |
| BSI | The baseband digital serial interface. |
| Decimator | A (digital) filter, which performs a signal processing to a lower sampling rate at the output compared to the input. |
| DNL | Difference between individual code width and average code width (1LSB): DNL(i) = [V(i+1)–V(i)–1LSB]/1LSB. Maximum and minimum specified. Min(DNL) > –1 is equivalent to monotonicity [V(i+1) > V(i)]. |
| $DR_{ICN}$ | Dynamic signal range referred to idle channel noise.<br>The signal $S_{in}$ = 0 is applied at the input of the DUT and $N_{out(meas)}$ (note 1) is measured at the output. $S_{out(max)}$ is the output signal level for the maximum allowed input signal level. The measurement is done in two steps: one with maximum input level, one with no input signal:<br>$DR_{ICN} = DR(S_{in} = 0) = \frac{S_{out(max)}}{N_{out(meas)}}$ |
| GMSK modulator | Gaussian minimum shift keying modulator as described in GSM recommendation GSM 05.04. |
| INL | The difference of the output to the best fit line. INL(i) = [(V(i)–(a+i × b)]/1LSB; INL = [max(INL(i)–min(INL(i)]/2. |
| NZIF | A mode into which the BBRX is switched to process data at an intermediate frequency of 100 kHz. |
| Psophometrical weighting | A frequency weighting curve described in CCITT recommendation O.41. |
| PCM | Pulse code modulation, a standardized digital protocol for audio data. |
| QB | Quarterbit, usually referred to the time needed for one quarter of a GSM baseband bit, i.e. a frequency of $1/12 \times 13$ MHz. |
| RX | The receive section of either BB or VB. |
| RXPGA | VB RX programmable gain amplifier. |
| RXVOL | VB RX volume control. |
| SidePGA | VB sidetone programmable gain amplifier. |
| SINAD | Signal-to-noise and distortion. |
| S/N | Signal-to-noise ratio: A signal $S_{in}$ is applied at the input of the DUT and $S_{out(meas)}$ and $N_{out(meas)}$ (note 1) are measured at the output: $S/N = \frac{S_{out(meas)}}{N_{out(meas)}}$ |
| TX | The transmit section of either BB or VB. |
| TXPGA | VB TX programmable gain amplifier. |
| VB | The voice band section. |
| $V_{DDA}$ | Analog circuitry supply voltage with respect to $V_{SS}$. |
| $V_{DDD}$ | Digital circuitry supply voltage with respect to $V_{SS}$. |

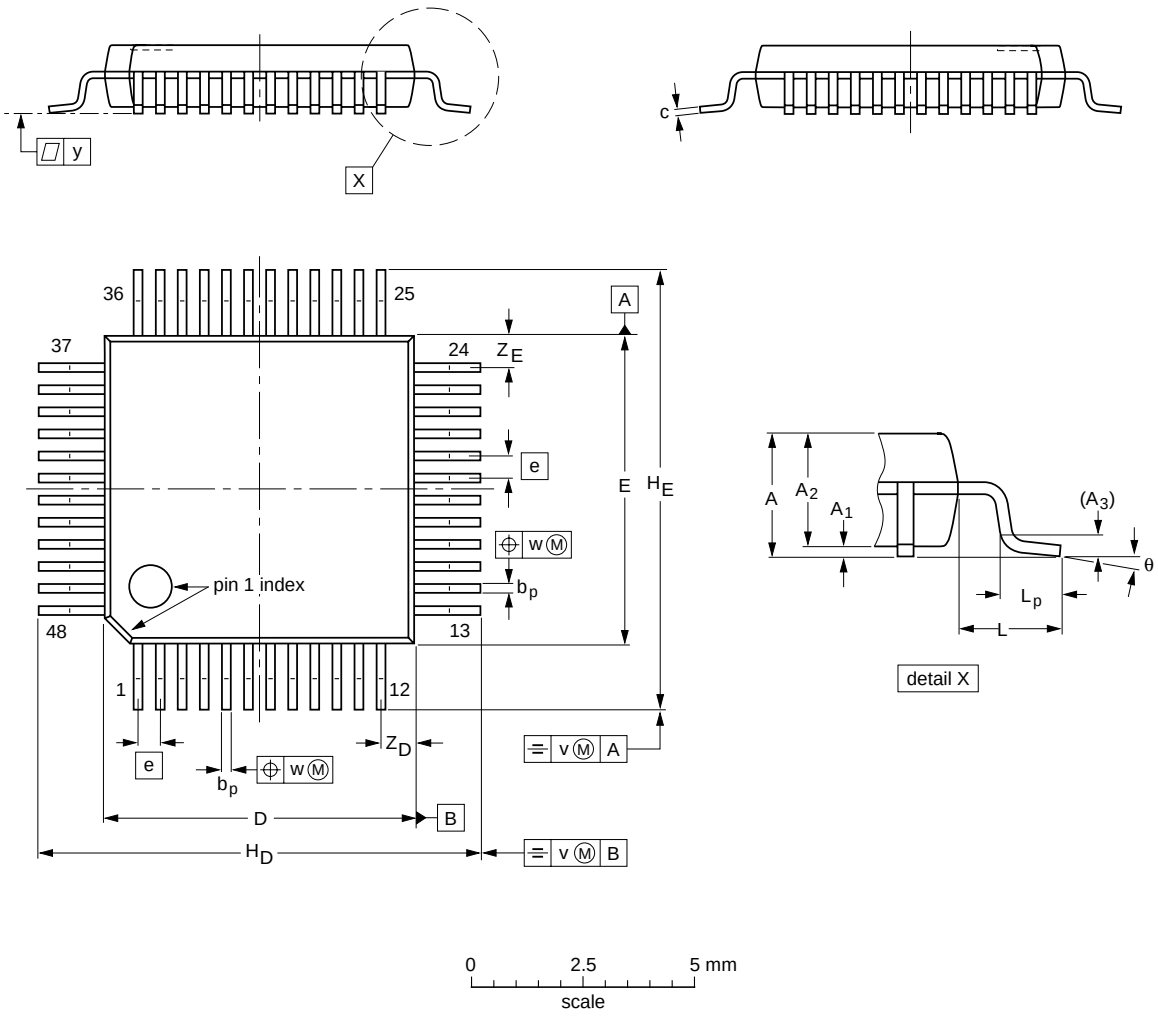
| | |
|---|---|
| VSP | Voice band signal processor, as implemented on the PCF50732. |
| $V_{SS}$ | Reference (ground supply) potential. |
| ZIF | A mode into which the BBRX is switched to process data at an intermediate frequency of zero. |

**Note**

1. If the output signal is a bitstream signal from a sigma-delta ADC, then the $N_{out(meas)}$ is only measured in a reduced bandwidth (e.g. in an audio application: 300 Hz to 3.4 kHz).

## 21 PACKAGE OUTLINE

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

## 22 SOLDERING

### 22.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 22.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

### 22.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 22.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

### 22.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, HBGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 23 DATA SHEET STATUS

| DATA SHEET STATUS | PRODUCT STATUS | DEFINITIONS (1) |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

**Note**

1. Please consult the most recently issued data sheet before initiating or completing a design.

## 24 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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**NOTES**

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