DATA SHEET

SA8025A

Low-voltage 1.8GHz fractional-N
synthesizer

Product specification

1996 Oct 15

IC17 Data Handbook

PHILIPS

PHILIPS

1.8GHz low-voltage Fractional-N synthesizer **SA8025A**

DESCRIPTION

The SA8025A is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. The SA8025A is an improved version of the SA8025, suitable for narrow band systems like the Japan Personal Digital Cellular (PDC) system. The new design improves the performance of the fractional spur compensation circuitry. The new version is pin-for-pin compatible with the previous version. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A four modulus prescaler (divide by 64/65/68/73) is integrated on chip with a maximum input frequency of 1.8GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface. A 1GHz version (SA7025DK) is also available with the same pinout.

FEATURES

- Operation up to 1.8GHz at 3V
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
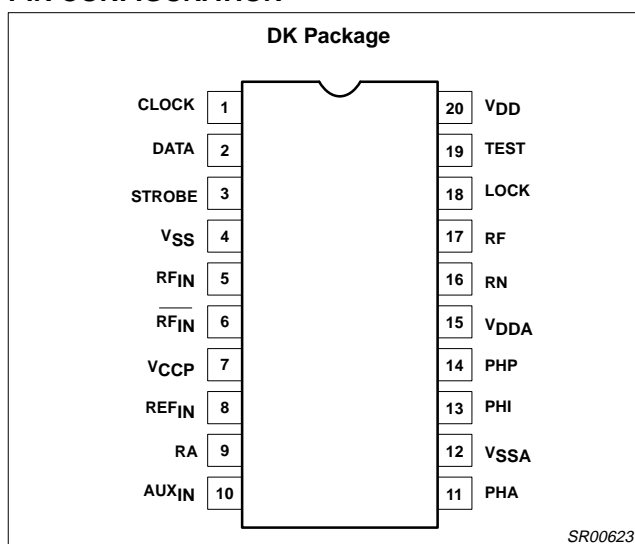- Programmable charge pump currents

PIN CONFIGURATION

DK Package

CLOCK	1	20	V_{DD}
DATA	2	19	TEST
STROBE	3	18	LOCK
V_{SS}	4	17	RF
RF_{IN}	5	16	RN
$\overline{RF_{IN}}$	6	15	V_{DDA}
V_{CCP}	7	14	PHP
REF_{IN}	8	13	PHI
RA	9	12	V_{SSA}
AUX_{IN}	10	11	PHA

SR00623

Figure 1. Pin Configuration

- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: $V_{RF\_IN} = -20dBm$

APPLICATIONS

- PHS (Personal Handy-phone System)
- PDC (Personal Digital Cellular)
- PCS (Personal Communication Service)
- Portable communication systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	−40 to +85°C	SA8025ADK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

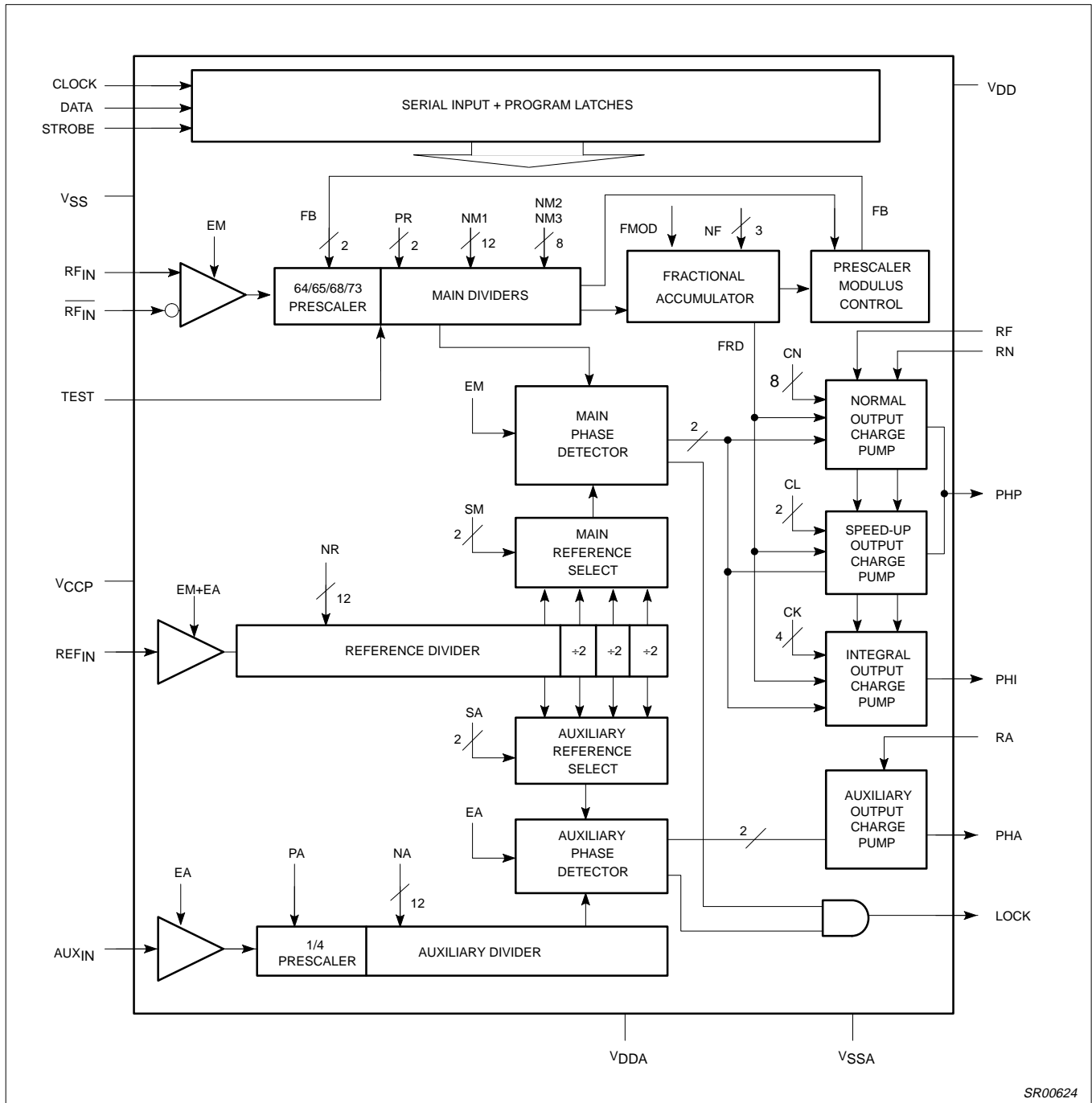## 1.8GHz low-voltage Fractional-N synthesizer

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PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM

Figure 2. Block Diagram

1.8GHz low-voltage Fractional-N synthesizer

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DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{SUPPLY}	Recommended operating conditions	$V_{CCP} = V_{DD}$, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, $I_{RN} = I_{RF} = I_{RA} = 0$		50	500	µA
Operational supply currents: $I = I_{DD} + I_{CCP} + I_{DDA}$; $I_{RN} = 25\mu A$, $I_{RA} = 25\mu A$, (see Note 5)						
I_{AUX}	Operational supply currents	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		11.0		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		13.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3 \times V_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pumps: $V_{DDA} = 3V$ / $I_{RX} = 25\mu A$ or $V_{DDA} = 5V$ / $I_{RX} = 62.5\mu A$, V_{PHX} in range, unless otherwise specified.						
$|I_{RX}|$	Setting current range for any setting resistor	$2.7V < V_{DDA} < 5.5V$		25		µA
		$4.5V < V_{DDA} < 5.5V$		62.5		
V_{PHOUT}	Output voltage range		0.7		$V_{DDA}-0.8$	V
Charge pump PHA						
$|I_{PHA}|$	Output current PHA	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$[13]	400	500	600	µA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{|I_{PHP\_A}|}$	Relative output current variation PHA	$I_{RA} = -62.5\mu A$[2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching PHA pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, normal mode [NO TAG, 4, 6] $V_{RF} = V_{DDA}$						
$|I_{PHP\_N}|$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$[13]	440	550	660	µA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$[2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching PHP normal mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, speed-up mode [NO TAG, 4, 7] $V_{RF} = V_{DDA}$						
$|I_{PHP\_S}|$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$[13]	2.20	2.75	3.30	mA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$[2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching PHP speed-up mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±250	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±300	
Charge pump PHI, speed-up mode [NO TAG, 4, 8] $V_{RF} = V_{DDA}$						
$|I_{PHI}|$	Output current PHI	$I_{RN} = -62.5\mu A$; $V_{PHI} = V_{DDA}/2$[13]	4.4	5.5	6.6	mA
		$I_{RN} = -25\mu A$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5\mu A$[2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching PHI pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±500	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±600	
Fractional compensation PHP, normal mode [NO TAG, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5\mu A$; $F_{RD} = 1$ to 7[13]	−625	−400	−250	nA
		$I_{RF} = -25\mu A$; $F_{RD} = 1$ to 7	−300	−180	−50	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Fractional compensation PHP, speed up mode [NO TAG, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5\mu A$; F_{RD} = 1 to 7[13]	−3.35	−2	−1.1	μA
		$I_{RF} = -25\mu A$; F_{RD} = 1 to 7	−1.35	−1.0	−0.5	
	Pump leakage		−20		20	nA
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[NO TAG]	V_{PHP} = 0.7 to V_{DDA} − 0.8		0.1	20	nA
I_{PHI_L}	Output leakage current PHI; normal mode[NO TAG]	V_{PHI} = 0.7 to V_{DDA} − 0.8		0.1	20	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} − 0.8		0.1	20	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25^{\circ}C$; unless otherwise specified. Test Circuit, Figure 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider guaranteed and tested on an automatic tester. Some performance parameters may be improved by using optimized layout.						
f_{RF_IN}	Input signal frequency	Pin = -20dBm, Direct coupled input[14]	0		1.8	GHz
		Pin = -20dBm, 1000pF input coupling			1.8	
V_{RF_IN}	Input sensitivity	f_{IN} = 1800MHz	−20		0	dBm
Reference divider ($V_{DD} = V_{DDA} = 3V$ or $V_{DD} = 3V / V_{DDA} = 5V$)						
f_{REF_IN}	Input signal frequency	2.7 < V_{DD} and V_{DDA} < 5.5V			25	MHz
		2.7 < V_{DD} and V_{DDA} < 4.5V			30	
V_{REF_IN}	Input signal range, AC coupled	2.7 < V_{DD} and V_{DDA} < 5.5V	500			mV$_{P-P}$
		2.7 < V_{DD} and V_{DDA} < 4.5V	300			
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
				3		pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV$_{P-P}$
Z_{AUX_IN}	Auxiliary divider input impedance[15]			100		kΩ
				3		pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
In-Loop Performance[16] $V_{DDA} = 5V$, $V_{DD} = 2.7V$						
RF_{MM}	Main loop residual FM	F_{VCO} = 1780MHz		600	900	Hz

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AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\dfrac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\dfrac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 68] + t_W$			
		A word, PR = '11'	$\dfrac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$			
		A word, PR = '00'	$\dfrac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$			

NOTES:
1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|} \text{ with } V_1 = 0.7V, V_2 = V_{DDA} - 0.8V \text{ (see Figure 3).}$$

3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with C_N = 0 to 255.
5. Power supply current measured with f_{RF_IN} = 1667.4MHz, NM1 = 0, NM2 = 1, NM3 = 1, NM4 = 4, FMOD = 8, N = 694 6/8, main phase detector frequency = 2.4MHz, $f_{REF\ IN}$ = 19.2MHz, NR = 8, SM = 1, f_{AUX_IN} = 150MHz, NA = 125, SA = 1, PA = 0, auxiliary phase detector frequency = 300kHz, IRN = IRA = IRF = 25μA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, V_{CCP} = V_{DD} = V_{DDA} = 3V. Operational supply current = I_{DDA} + I_{DD} + I_{CCP}.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current | I_{PHI} | = $-I_{RN}$ x CN x $2^{(CL+1)}$ x CK/32:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Any RFD, CL = 1 for speed-up pump. The integral pump is intended for switching only and the fractional compensation is not guaranteed.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
   1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
   2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The matching is defined by the sum of the P and the N pump for a given output voltage.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, low frequency operation requires DC-coupling and a minimum input slew rate of 32V/μs.
15. Guaranteed by design.
16. F_{XTAL} = 14.4MHz, V_{XTAL} = 500mV_{P-P}, comparison Freq. = 200kHz, Loop bandwidth = 5kHz, Audio filter = 300Hz to 15kHz.
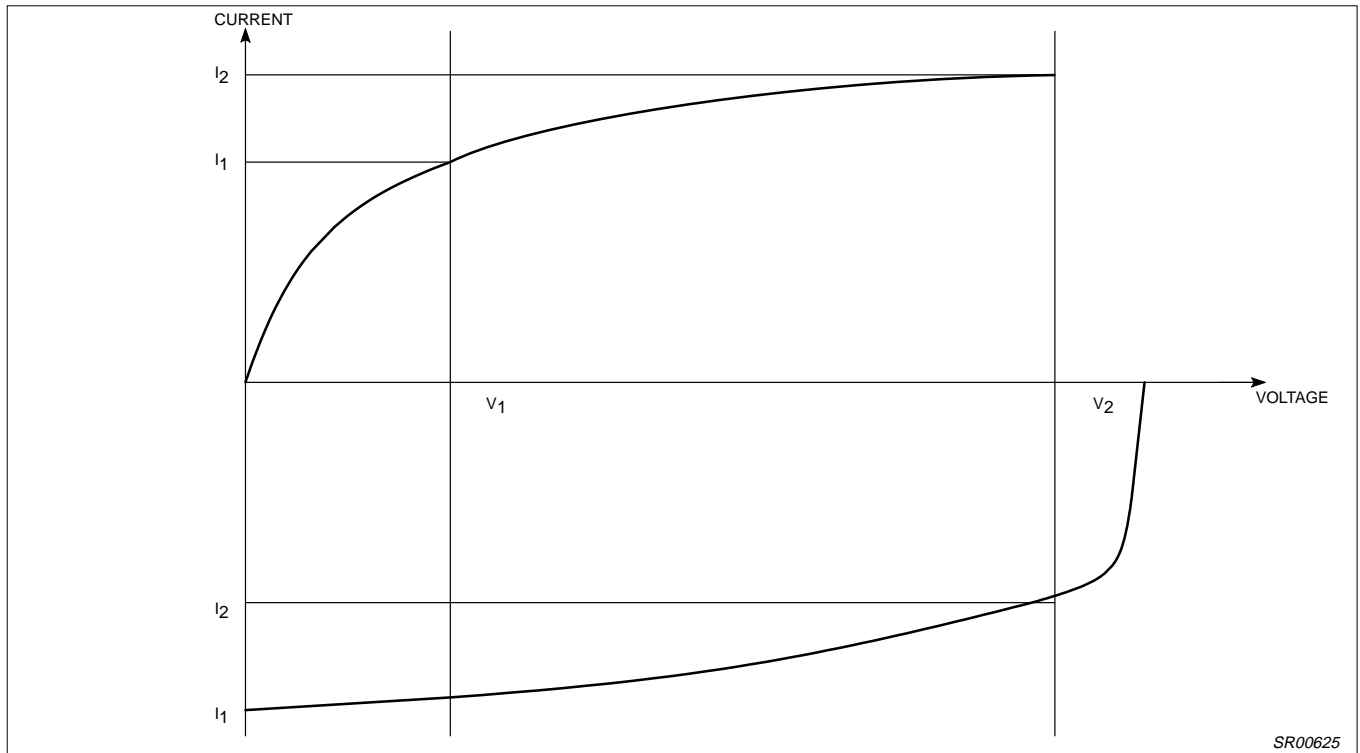
Figure 3. Relative Output Current Variation
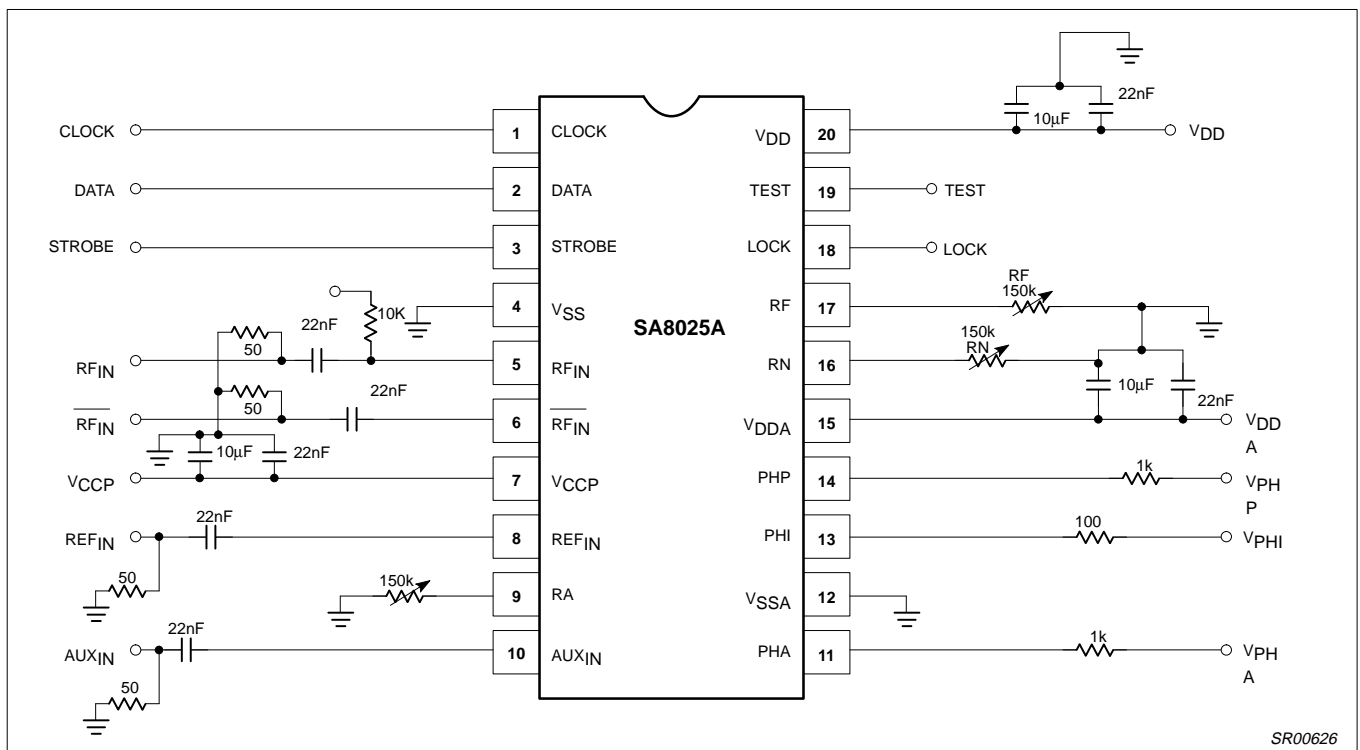
Figure 4. Test Circuit

1.8GHz low-voltage Fractional-N synthesizer

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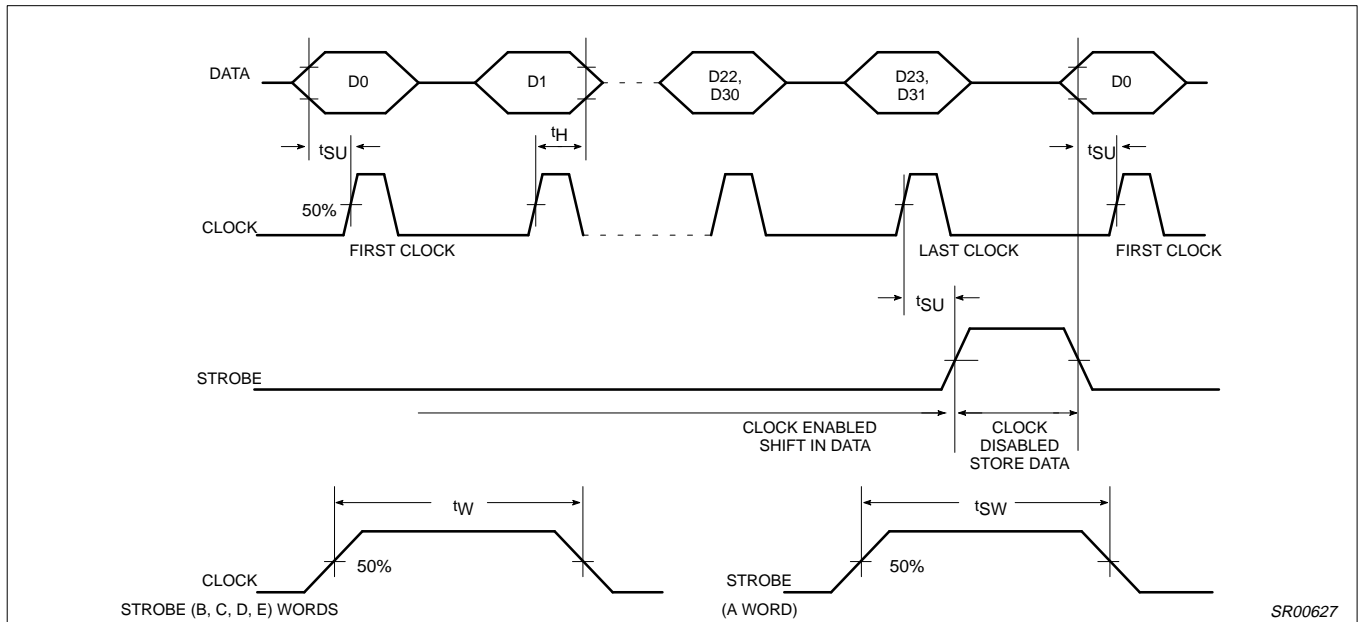
AC TIMING CHARACTERISTICS

Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 5 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 6 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values.

Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

For PR = '01'
$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM2 \cdot 65) + t_W$$

For PR = '10'
$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM2 \cdot 65 + (NM3 + 1) \cdot 68] + t_W$$

For PR = '11'
$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$$

For PR = '00'
$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 7) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1.7GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/68/73, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the

prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ \ = \ N \ + \ \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.
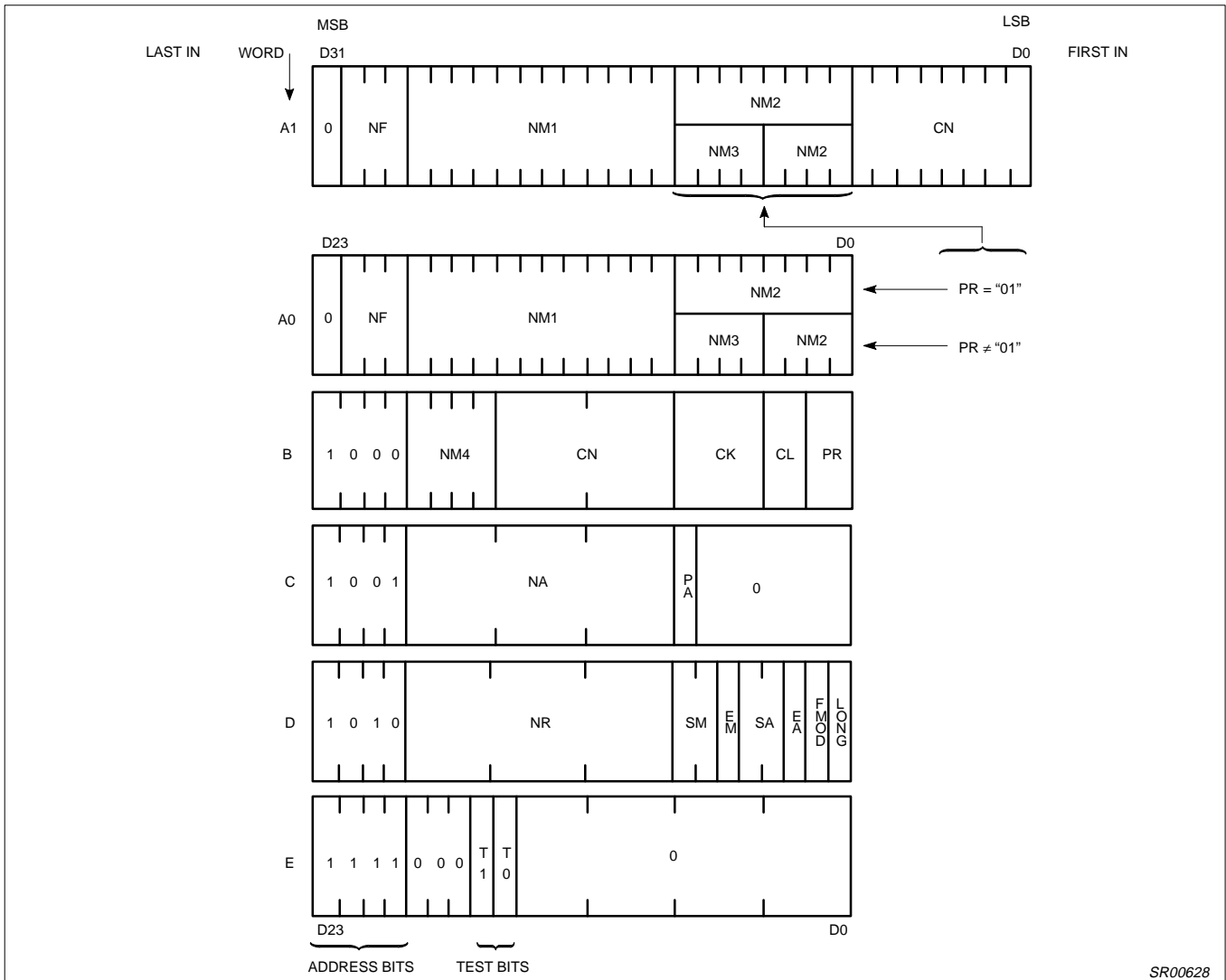
Figure 6. Serial Input Word Format
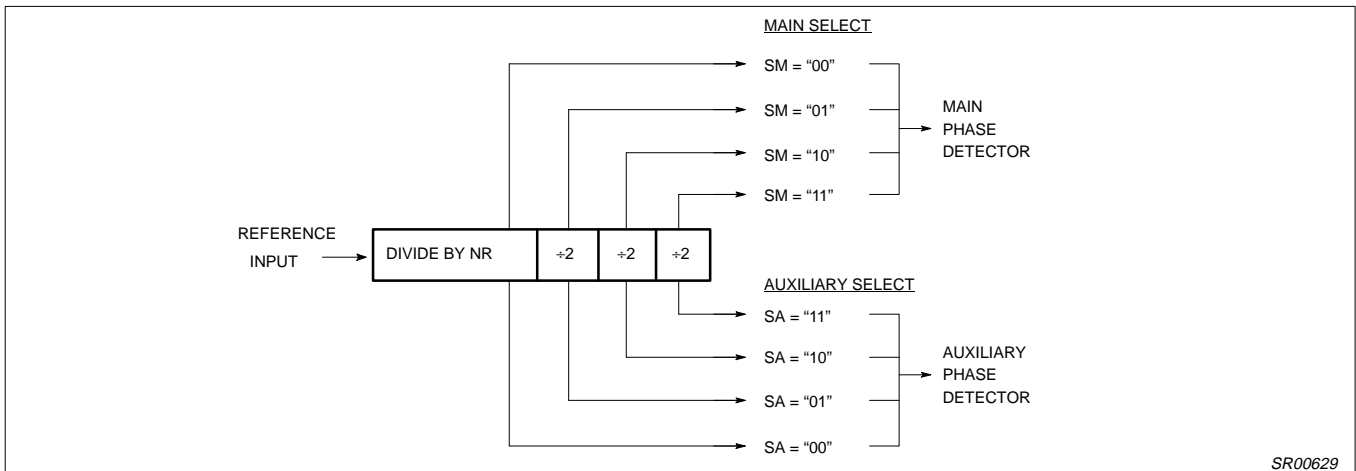
Figure 7. Reference Divider

1.8GHz low-voltage Fractional-N synthesizer

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Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 68*
NM4	4 if PR = "11" or "00"	Number of main divider cycles when prescaler modulus = 73*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/68) PR = "11": modulus 4 prescaler (64/65/68/73) PR = "00": modulus 3 prescaler (64/65/73)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1

*Not including reset cycles and Fractional-N effects.

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 (*)
if PR = "11"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 (*)
if PR = "00"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM4 + 1) x 73
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM4 + 1) x 73 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity			
		NM1	NM2	NM3	NM4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4
00	3	12	8	–	4

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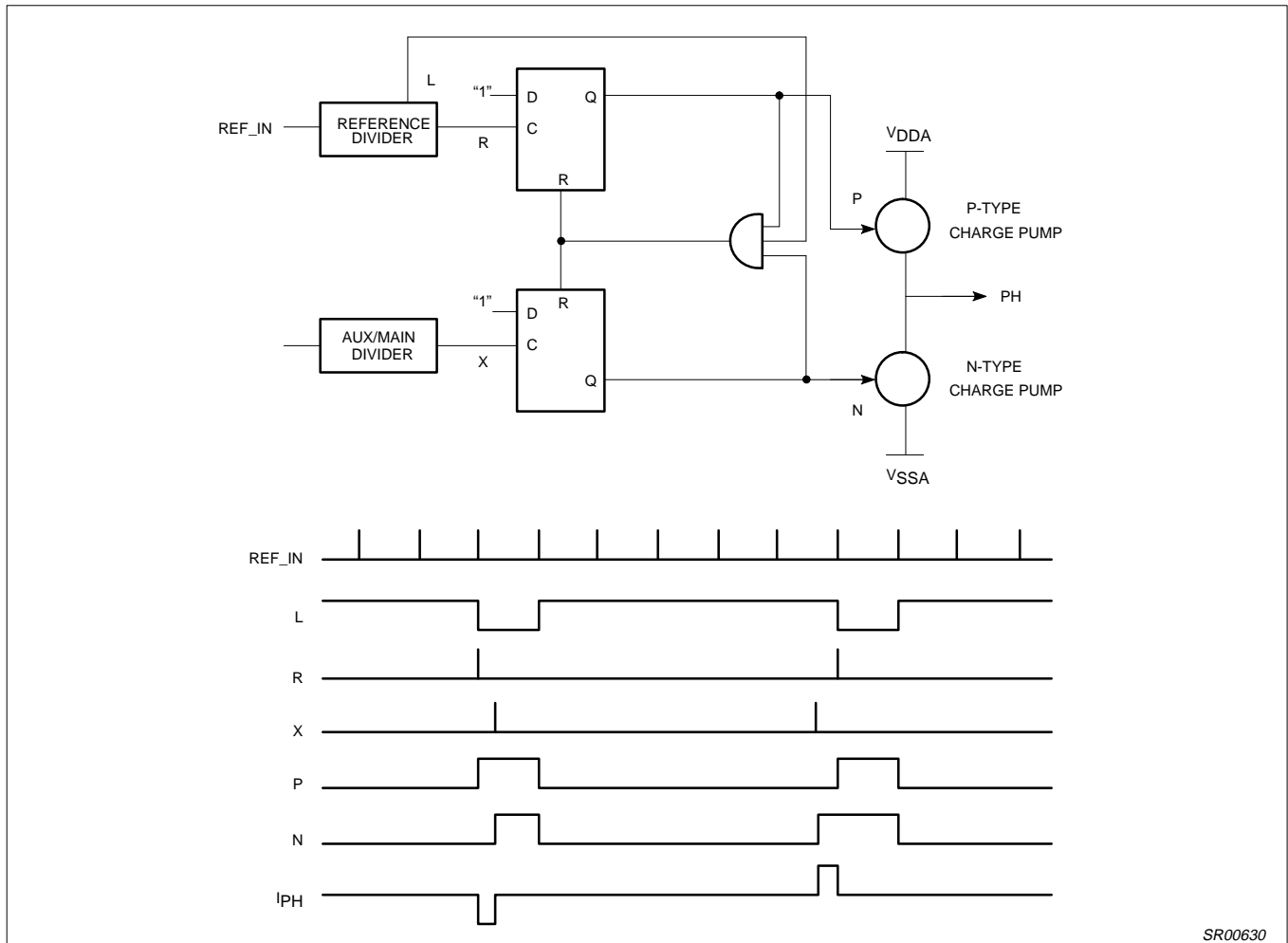
Figure 8. Phase Detector Structure with Timing

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 8. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA8025A has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150 \ \overline{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

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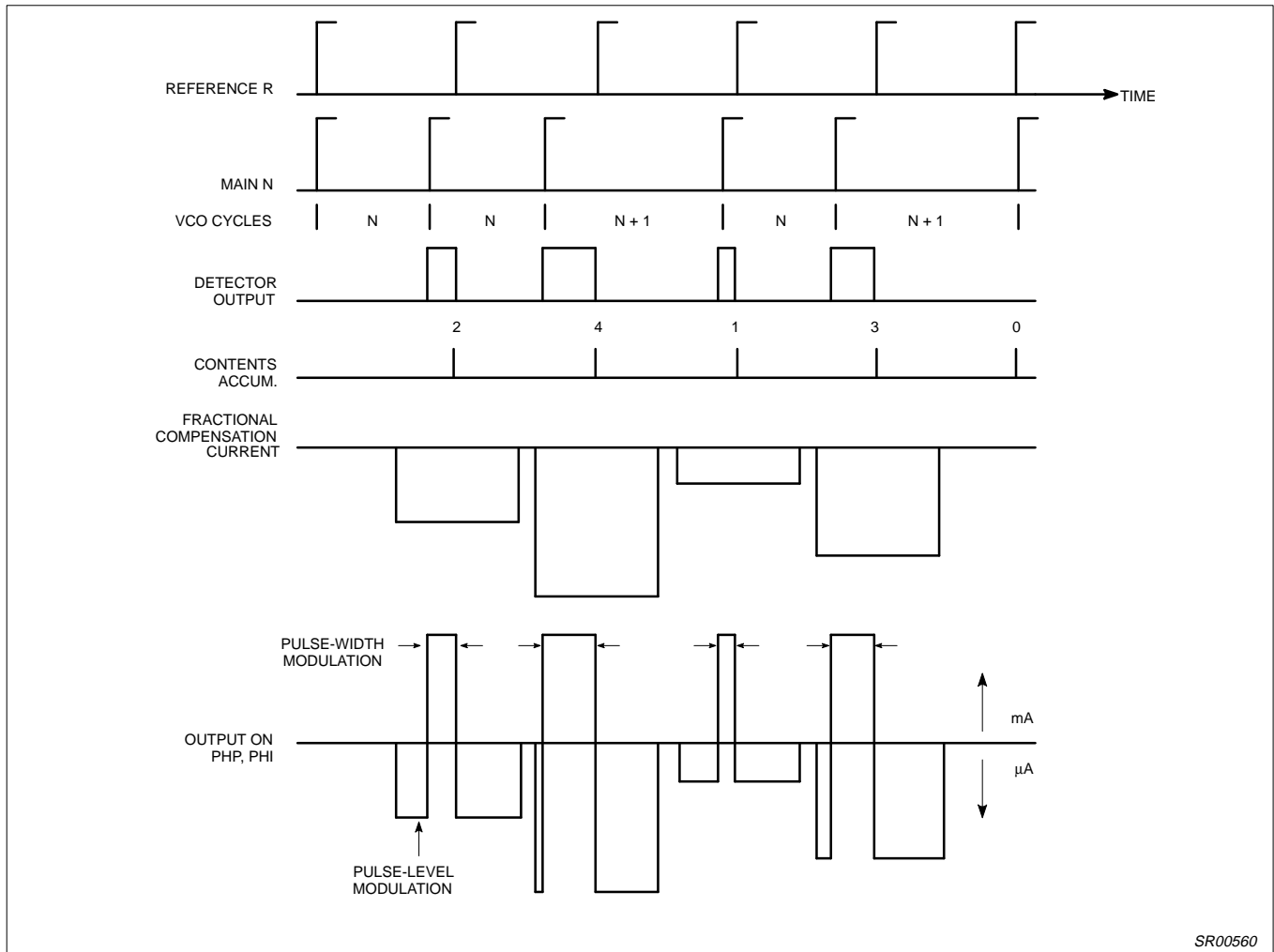
Figure 9. Waveforms for NF = 2, Fraction = 0.4

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 9 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \begin{array}{l}\text{:fractional comp.} \\ \text{current}\end{array}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} (2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \frac{FRD \cdot I_{RF}}{128} (2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \frac{CN \cdot I_{RN}}{32} (2^{CL+1}) \, CK$$

$$|I_{PHI\_comp}| \; = \; \frac{FRD \cdot I_{RN}}{128} \; (2^{CL+1}) \; CK$$

Figure 9 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF is approximately:

$$\frac{I_{RN}}{I_{RF}} \qquad \frac{(Q \cdot f_{VCO})}{(3 \cdot CN \cdot F_{INR})}$$

where:

Q	=	fractional-N modulus
$f_{VCO} = f_{INM} \times N$,		input frequency of the prescaler
$F_{INR} =$		input frequency of the reference divider

PHI pump is meant for switching only. Current and compensation are not as accurate as PHP.

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 6 and 10).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2, NM3 or NM4 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.
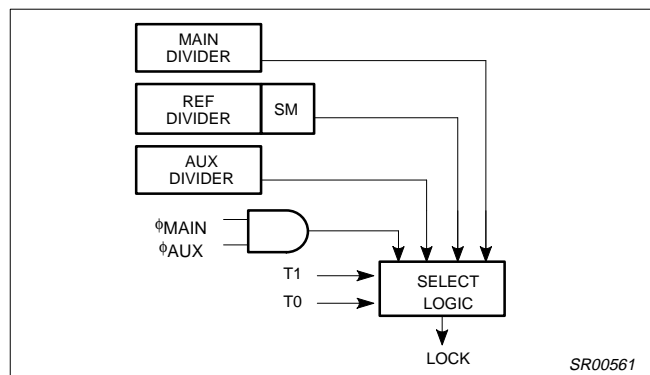
Figure 10. Test Mode Diagram

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PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—		9	RA	1.35	
2	DATA	—		16	RN	1.35	
3	STROBE	—					
19	TEST	—		17	RF	1.35	
5	RF$_{IN}$	2.1		11	PHA	—	
				13	PHI	—	
6	$\overline{RF_{IN}}$	2.1		14	PHP	—	
8	REF$_{IN}$	1.8		18	LOCK	—	
10	AUX$_{IN}$	1.8					

Figure 11. Pin Functions

1.8GHz low-voltage Fractional-N synthesizer

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TYPICAL PERFORMANCE CHARACTERISTICS
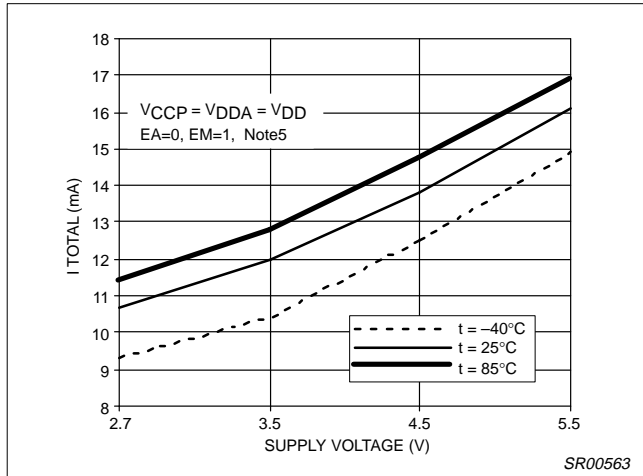
Figure 12. Operational Supply Current vs Supply Voltage and Temperature

Figure 13. Auxiliary Operational Supply Current vs Supply Voltage and Temperature

Figure 14. Main Divider Input Power vs Frequency and Supply
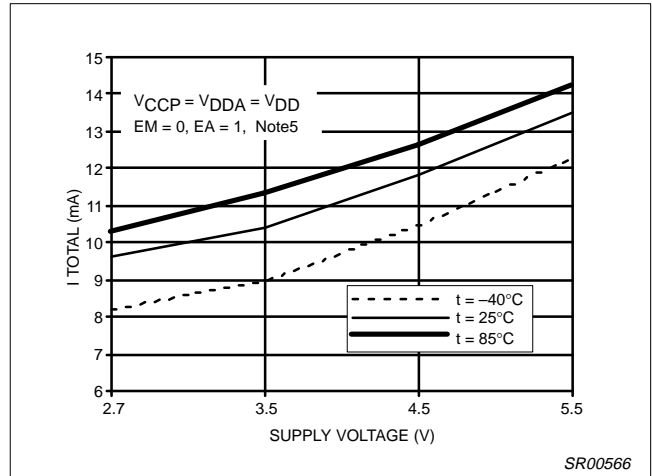
Figure 15. Main Operational Supply Current vs Supply Voltage and Temperature
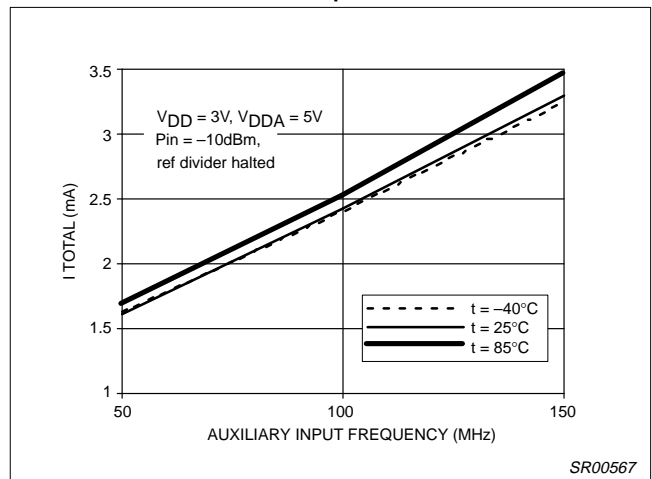
Figure 16. Auxiliary Operational Supply Current vs Frequency and Temperature
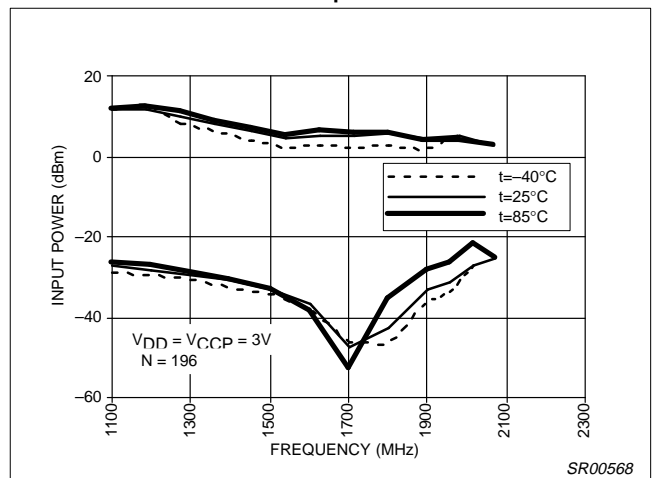
Figure 17. Main Divider Input Power vs Frequency and Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)
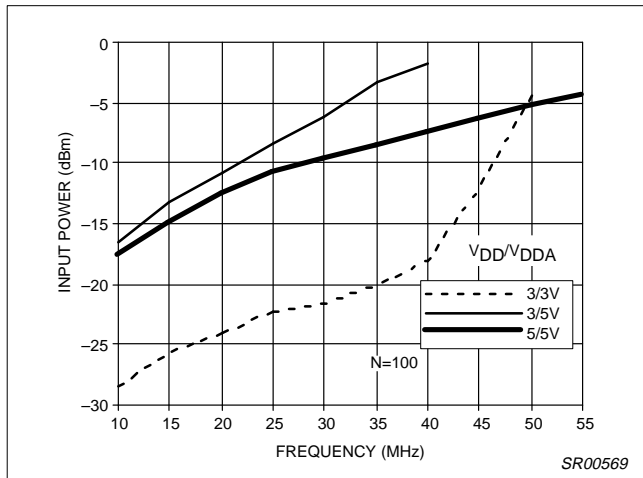
Figure 18. Reference Divider Minimum Input Power vs Frequency and Supply
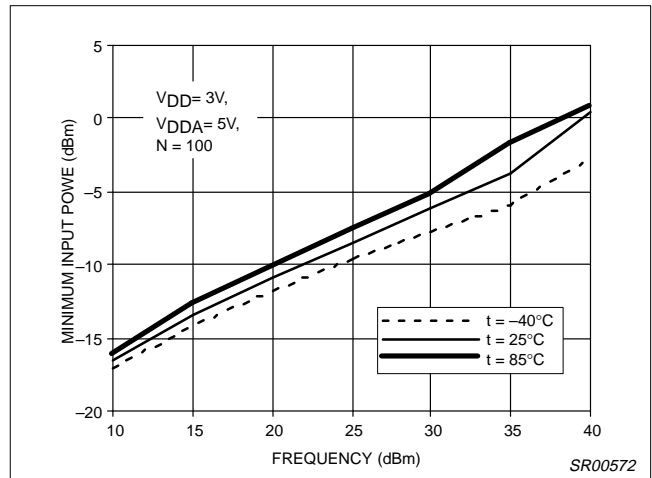
Figure 21. Reference Divider Minimum Input Power vs Frequency and Temperature
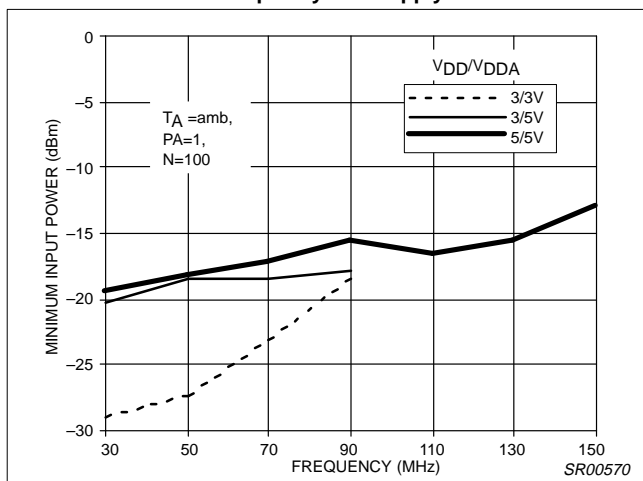
Figure 19. Auxiliary Divider Minimum Input Power vs Frequency and Supply
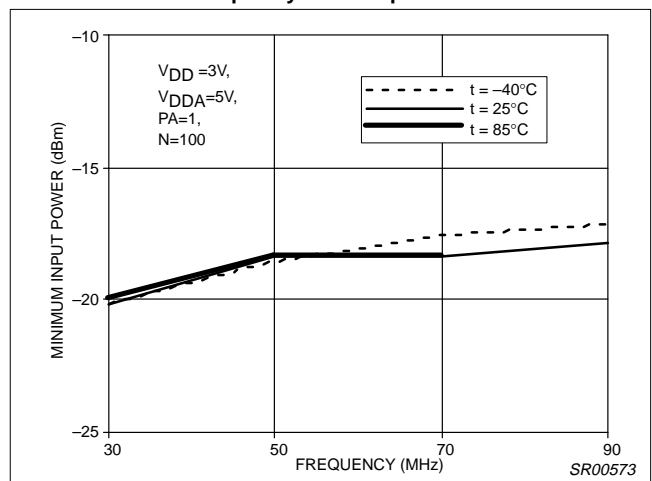
Figure 22. Auxiliary Divider Minimum Input Power vs Frequency and Temperature
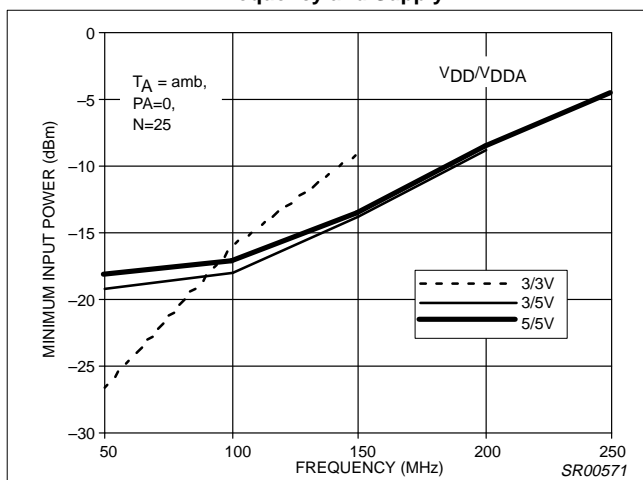
Figure 20. Auxiliary Divider Minimum Input Power vs Frequency and Supply
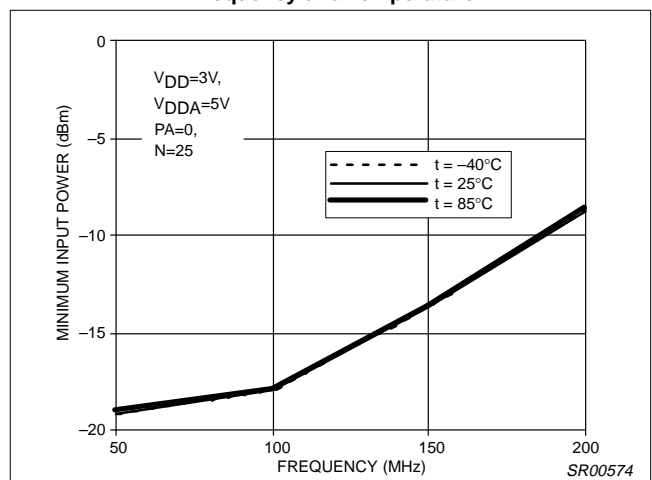
Figure 23. Auxiliary Divider Minumum Input Power vs Frequency and Temperature

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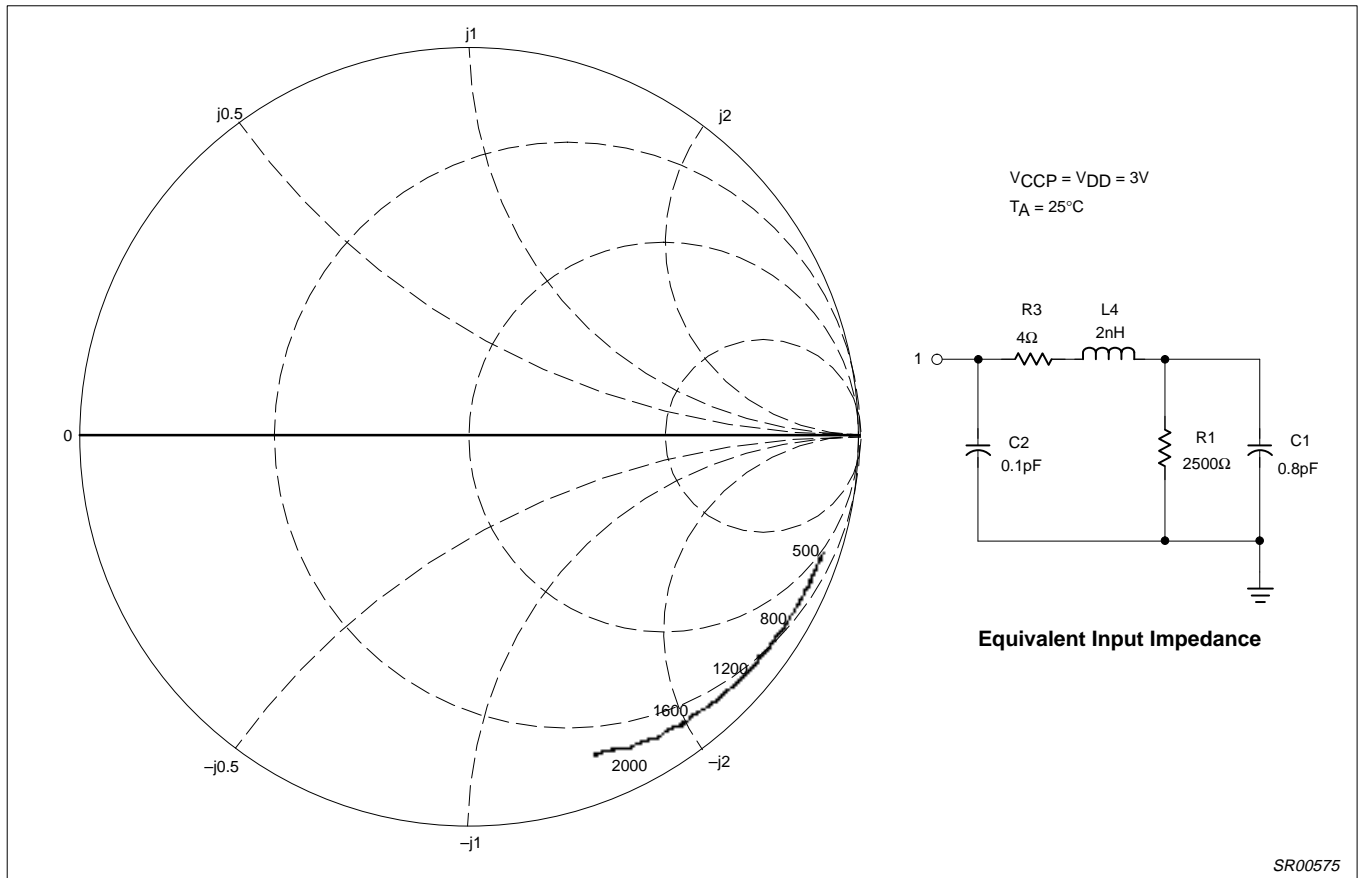
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Figure 24. Typical RF$_{IN}$ Input Impedance
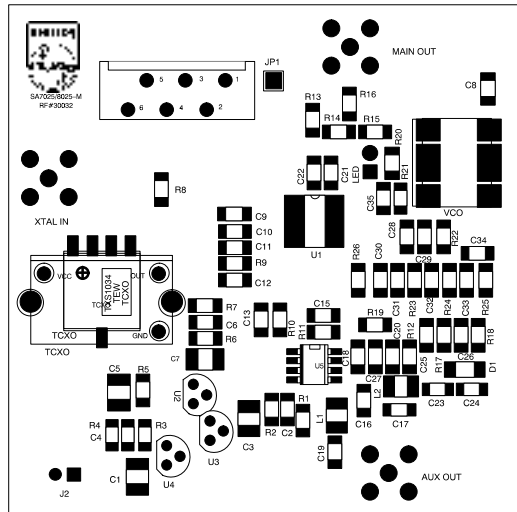
TOP SILK SCREEN
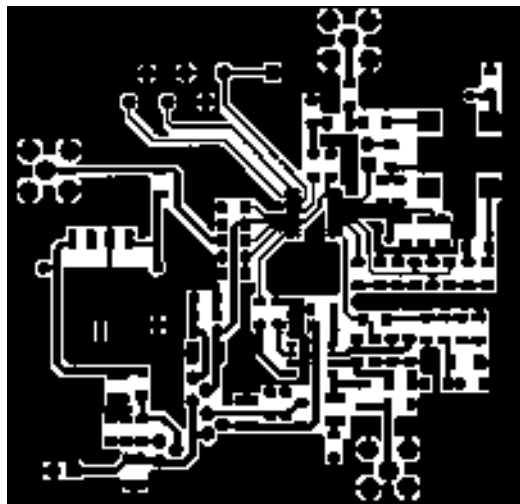
TOP VIEW
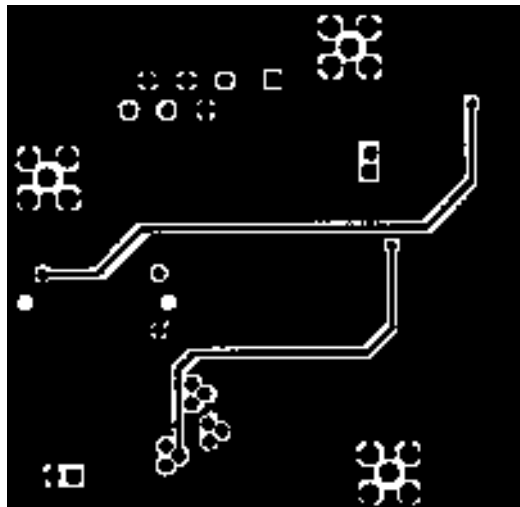
BOTTOM VIEW

SR00576

Figure 25. SA8025ADK Demoboard Layout (NOT ACTUAL SIZE)

1.8GHz low-voltage Fractional-N synthesizer

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Figure 26. SA8025ADK Application Circuit
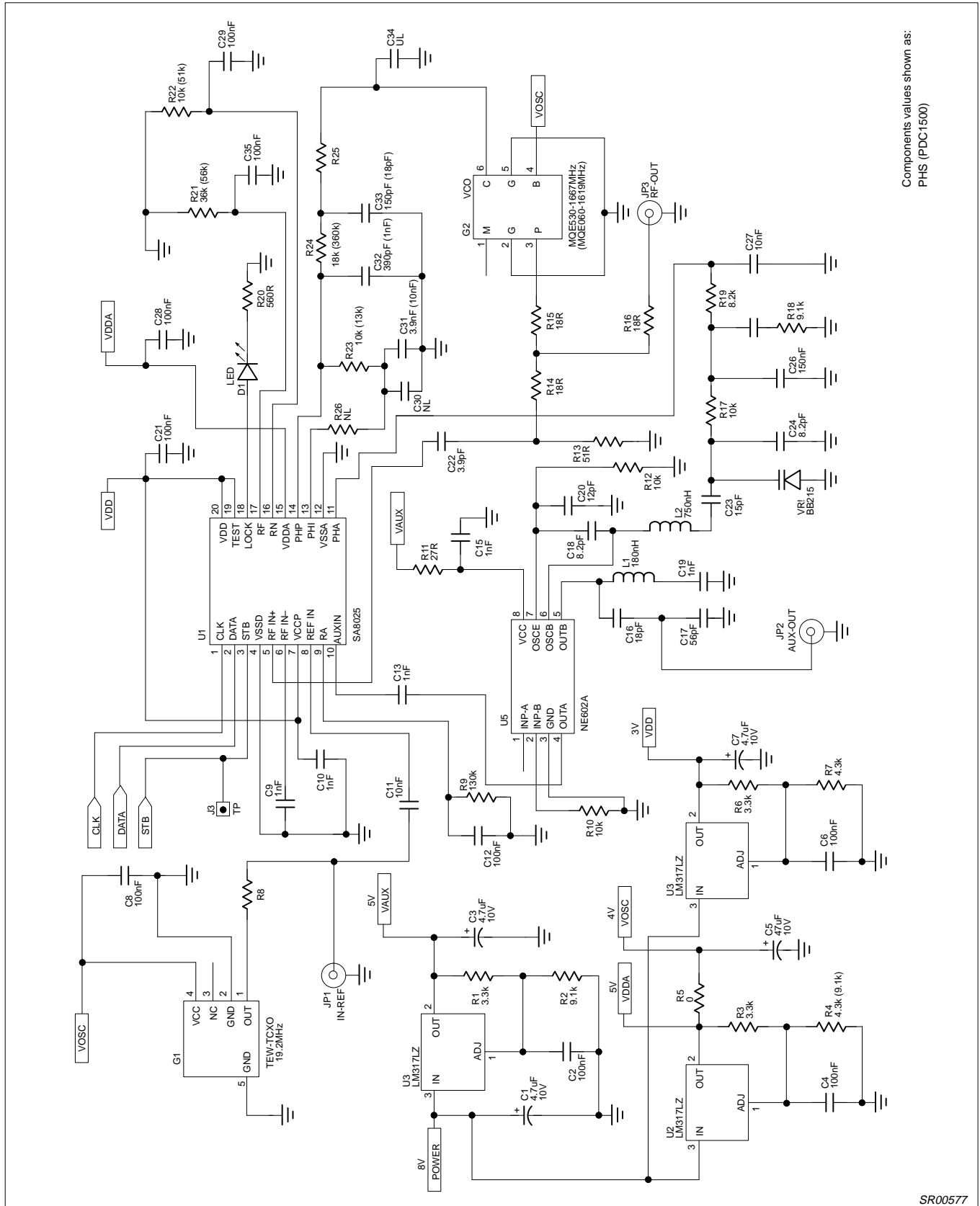
SR00577

Components values shown as:
PHS (PDC1500)

1.8GHz low-voltage Fractional-N synthesizer

SA8025A

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1
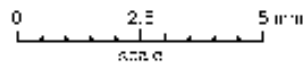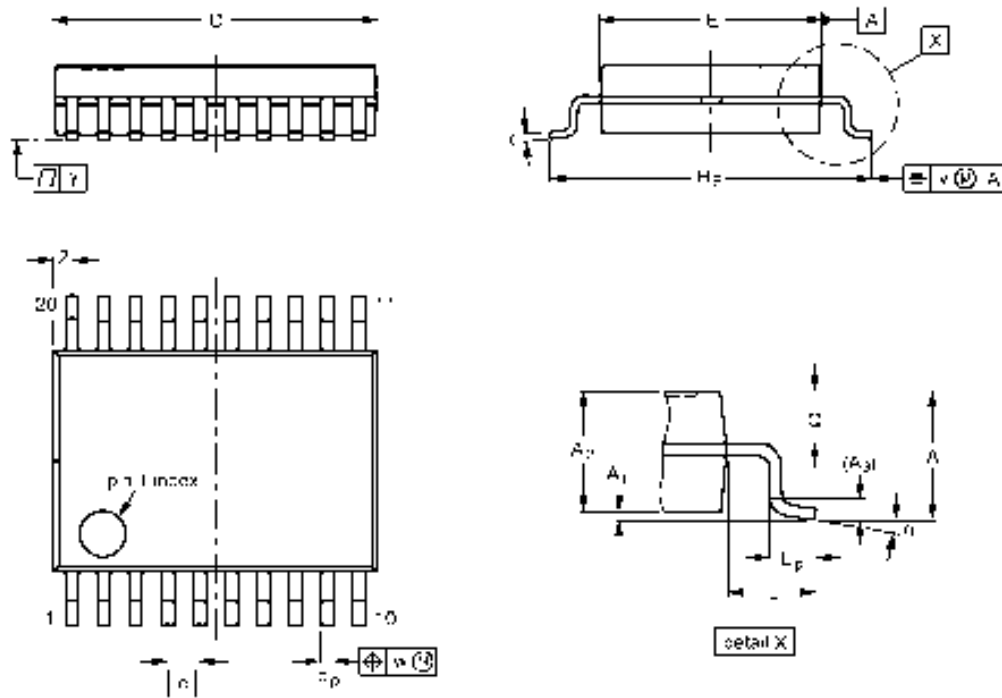
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	Hₑ	L	Lₚ	Q	v	w	y	Z[1]	..
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.63 0.45	0.2	0.10	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						~~99-04-05~~ 95-02-25

1.8GHz low-voltage Fractional-N synthesizer   **SA8025A**

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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