

HM53461 Series

65,536-word x 4-bit Multiport CMOS Video RAM

DESCRIPTION

The HM53461 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

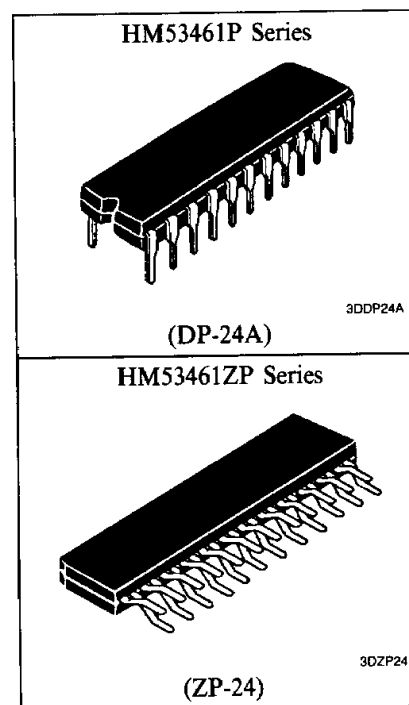
Utilizing the Hitachi 2 μ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

FEATURES

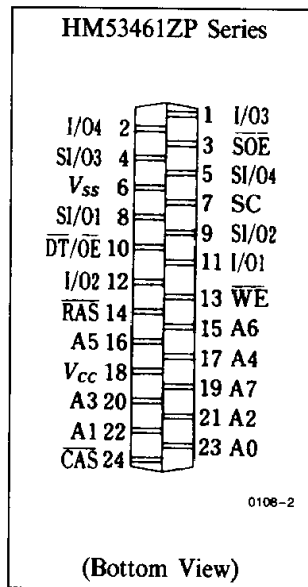
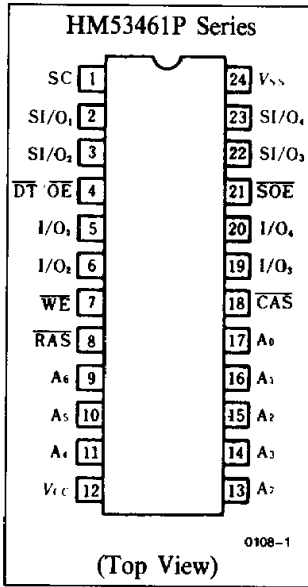
- Multiport Organization
(RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double Layer Polysilicon/Polycide n-Well CMOS Process
- Single 5V ($\pm 10\%$)
- Low Power
 - Active
 - RAM 380 mW (max)
 - SAM 220 mW (max)
 - Standby 40 mW (max)
- Access Time
 - RAM 100 ns/120 ns/150 ns
 - SAM 40 ns/40 ns/60 ns
- Cycle Time Random Read or Write Cycle Time (RAM) 190 ns/220 ns/260 ns
Serial Read or Write Cycle Time (SAM) 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles 4 ms
- Refresh Function
 - $\overline{\text{RAS}}$ Only Refresh
 - $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
 - Hidden Refresh
- Data Transfer Operation (RAM \leftrightarrow SAM)
- Fast Serial Access Operation Asynchronized with RAM Port Except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability

ORDERING INFORMATION

Part No.	Access Time	Package
HM53461P-10	100 ns	400 mil 24-pin
HM53461P-12	120 ns	Plastic DIP
HM53461P-15	150 ns	(DP-24A)
HM53461ZP-10	100 ns	24-pin
HM53461ZP-12	120 ns	Plastic ZIP
HM53461ZP-15	150 ns	(ZP-24)



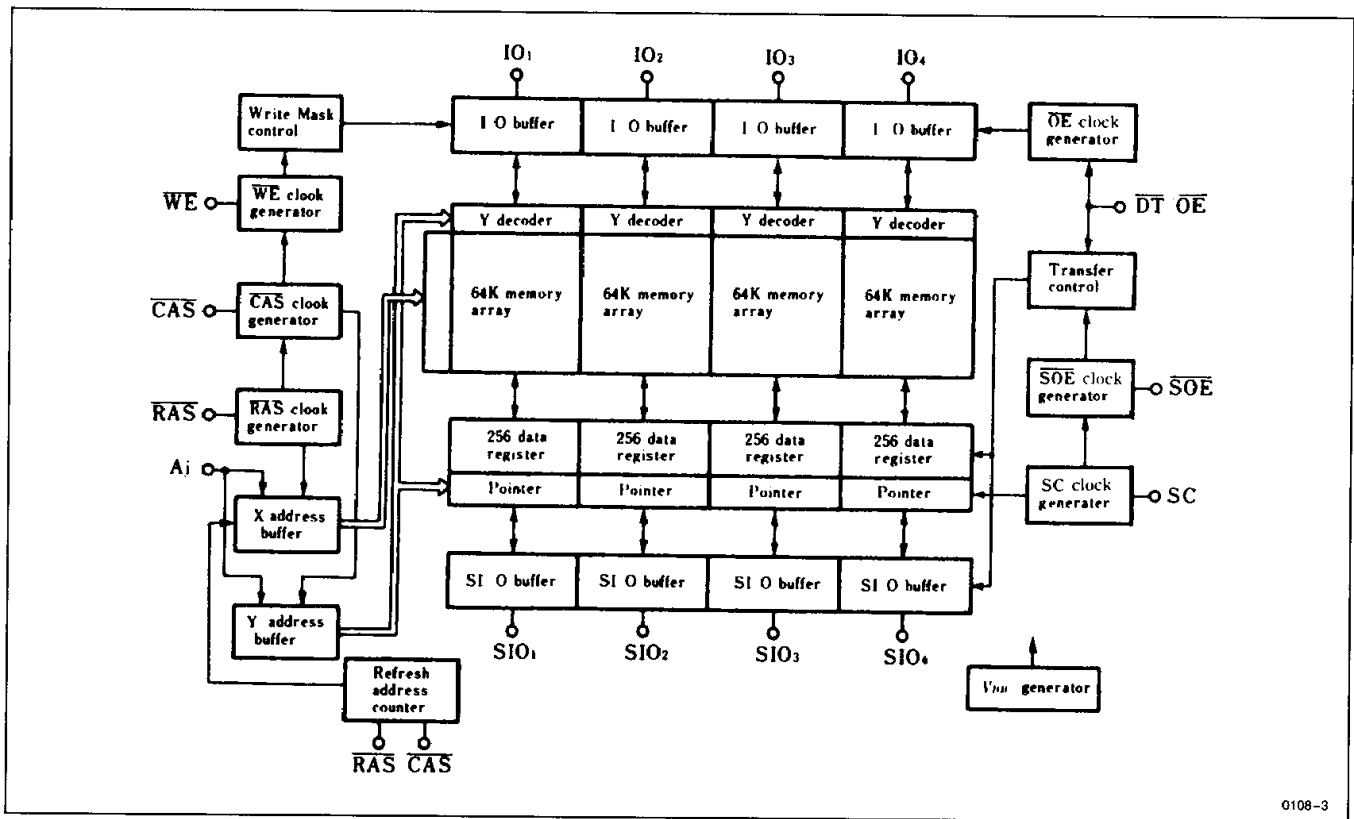
■ PIN OUT



■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₇	Address Inputs
I/O ₁ -I/O ₄	RAM Port Data Input/Output
SI/O ₁ -SI/O ₄	SAM Port Data Input/Output
RAS	Row Address Strobe
CAS	Column Address Strobe
SC	Serial Clock
WE	Write Enable
DT/OE	Data Transfer/Output Enable
SOE	SAM Port Enable
V _{CC}	Power Supply
V _{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Operating Temperature, T_A (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	-0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS} .
2. -3.0V for pulse width \leq 10 ns.

• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	SAM PORT		HM53461-10	HM53461-12	HM53461-15	Unit	RAM PORT	Note
		Standby	Active					Test Conditions	
Operating Current	I_{CC1}	—	×	70	60	50	mA	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = \text{Min}$	
	I_{CC7}	×	—	110	100	80	mA		
Standby Current	I_{CC2}	—	×	7	7	7	mA	$\overline{RAS}, \overline{CAS} = V_{IH}$	
	I_{CC8}	×	—	40	40	30	mA		
\overline{RAS} Only Refresh Current	I_{CC3}	—	×	60	50	40	mA	$\overline{CAS} = V_{IH}$, \overline{RAS} Cycling $t_{RC} = \text{Min}$	
	I_{CC9}	×	—	100	90	70	mA		
Page Mode Current	I_{CC4}	—	×	50	40	35	mA	$\overline{RAS} = V_{IL}$, \overline{CAS} Cycling $t_{PC} = \text{Min}$	
	I_{CC10}	×	—	90	80	65	mA		
CBR Refresh Current	I_{CC5}	—	×	60	50	40	mA	\overline{RAS} Cycling $t_{RC} = \text{Min}$	
	I_{CC11}	×	—	100	90	70	mA		
Data Transfer Current	I_{CC6}	—	×	75	65	55	mA	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = \text{Min}$	
	I_{CC12}	×	—	115	105	85	mA		

Parameter	Symbol	Min	Max	Unit	Test Conditions	Note
Input Leakage	I_{LI}	-10	10	μA		
Output Leakage	I_{LO}	-10	10	μA		
Output High Voltage	V_{OH}	2.4	—	V	$I_{OH} = -2 \text{ mA}$	
Output Low Voltage	V_{OL}	—	0.4	V	$I_{OL} = 4.2 \text{ mA}$	

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	



■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)^{1, 10, 11}

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t _{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t _{PC}	70	—	85	—	105	—	ns	
Access Time from RAS	t _{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t _{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn-off Delay Referenced to CAS	t _{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	6
RAS Precharge Time	t _{RP}	80	—	90	—	100	—	ns	
RAS Pulse Width	t _{RAS}	100	10000	120	10000	150	10000	ns	
CAS Pulse Width	t _{CAS}	50	10000	60	10000	75	10000	ns	
RAS to CAS Delay Time	t _{RCD}	25	50	25	60	30	75	ns	7
RAS Hold Time	t _{RSH}	50	—	60	—	75	—	ns	
CAS Hold Time	t _{CSH}	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t _{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t _{WCP}	15	—	20	—	25	—	ns	
Write Command to RAS Lead Time	t _{RWL}	35	—	40	—	45	—	ns	
Write Command to CAS Lead Time	t _{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t _{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t _{REF}	—	4	—	4	—	4	ms	
RAS Pulse Width (Read-Modify-Write Cycle)	t _{RWS}	170	10000	200	10000	245	10000	ns	
CAS to WE Delay	t _{CWD}	85	—	100	—	125	—	ns	8
CAS Setup Time (CAS Before RAS Refresh)	t _{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh)	t _{CHR}	20	—	25	—	30	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	ns	
CAS Precharge Time	t _{CP}	10	—	15	—	20	—	ns	
Access Time from OE	t _{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay referenced to OE	t _{OFF2}	0	25	0	30	0	40	ns	
OE to Data-in Delay Time	t _{ODD}	25	—	30	—	40	—	ns	
OE Hold Time referenced to WE	t _{OEH}	10	—	15	—	20	—	ns	
Data-in to CAS Delay Time	t _{DZC}	0	—	0	—	0	—	ns	
Data-in to OE Delay Time	t _{DZO}	0	—	0	—	0	—	ns	
OE to RAS Delay Time	t _{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t _{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t _{SCA}	—	40	—	40	—	60	ns	10
Access Time from SOE	t _{SEA}	—	25	—	30	—	40	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

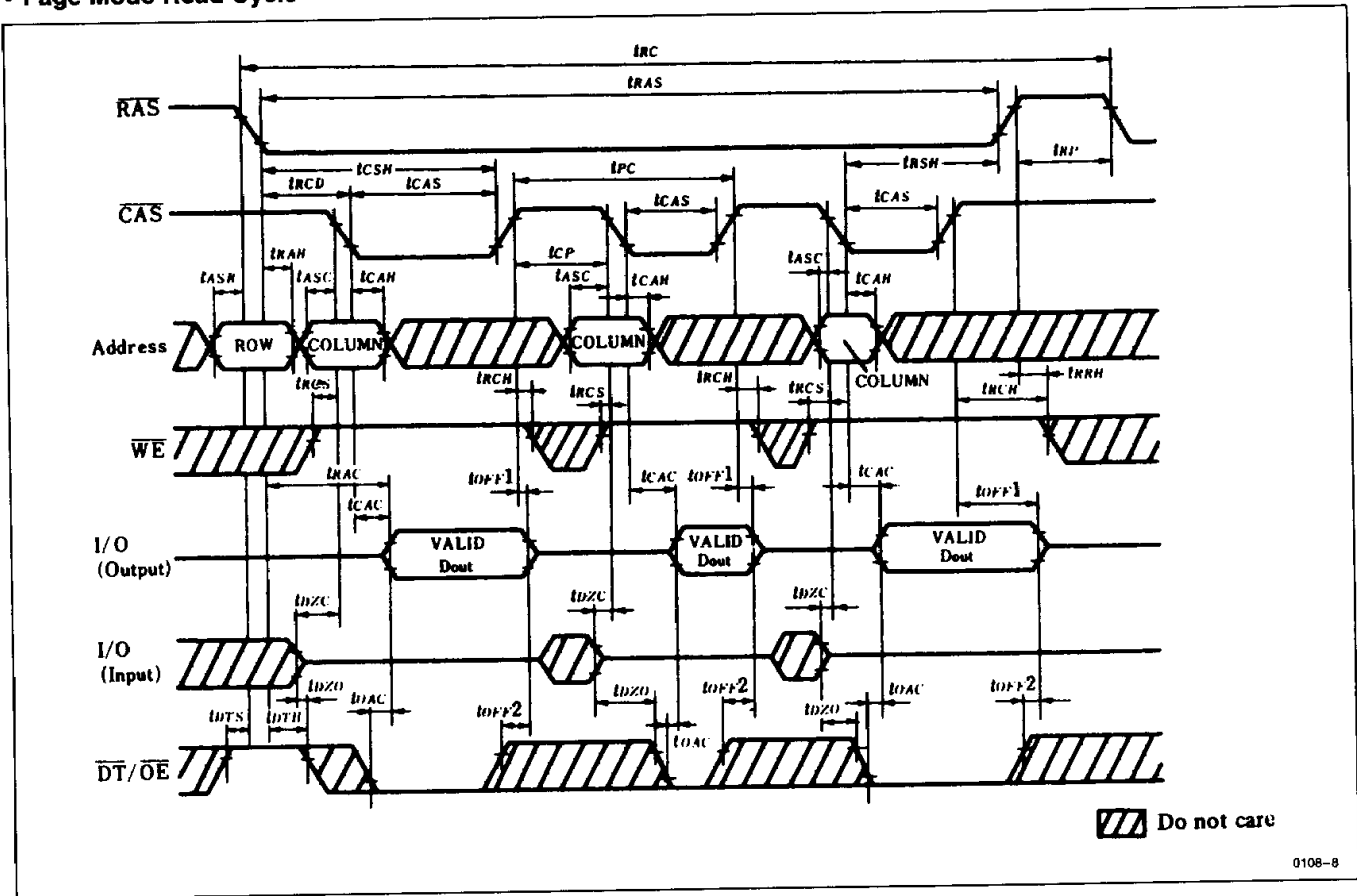
($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)^{1, 10, 11} (continued)

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{\text{SOE}}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{CAS}}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{\text{DT}}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{\text{DT}}$ Hold Time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time	t_{WH}	15	—	15	—	20	—	ms	
I/O to $\overline{\text{RAS}}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{\text{RAS}}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{\text{RAS}}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{\text{SC}}$ to $\overline{\text{RAS}}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{\text{RAS}}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{\text{RAS}}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{\text{DT}}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{\text{SOE}}$ to $\overline{\text{RAS}}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{\text{SOE}}$ to $\overline{\text{RAS}}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{\text{DT}}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

- Notes:
- AC measurements assume $t_T = 5$ ns.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
 - $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 - These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 - Measured with a load circuit equivalent to 2 TTL and 50 pF.
 - An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

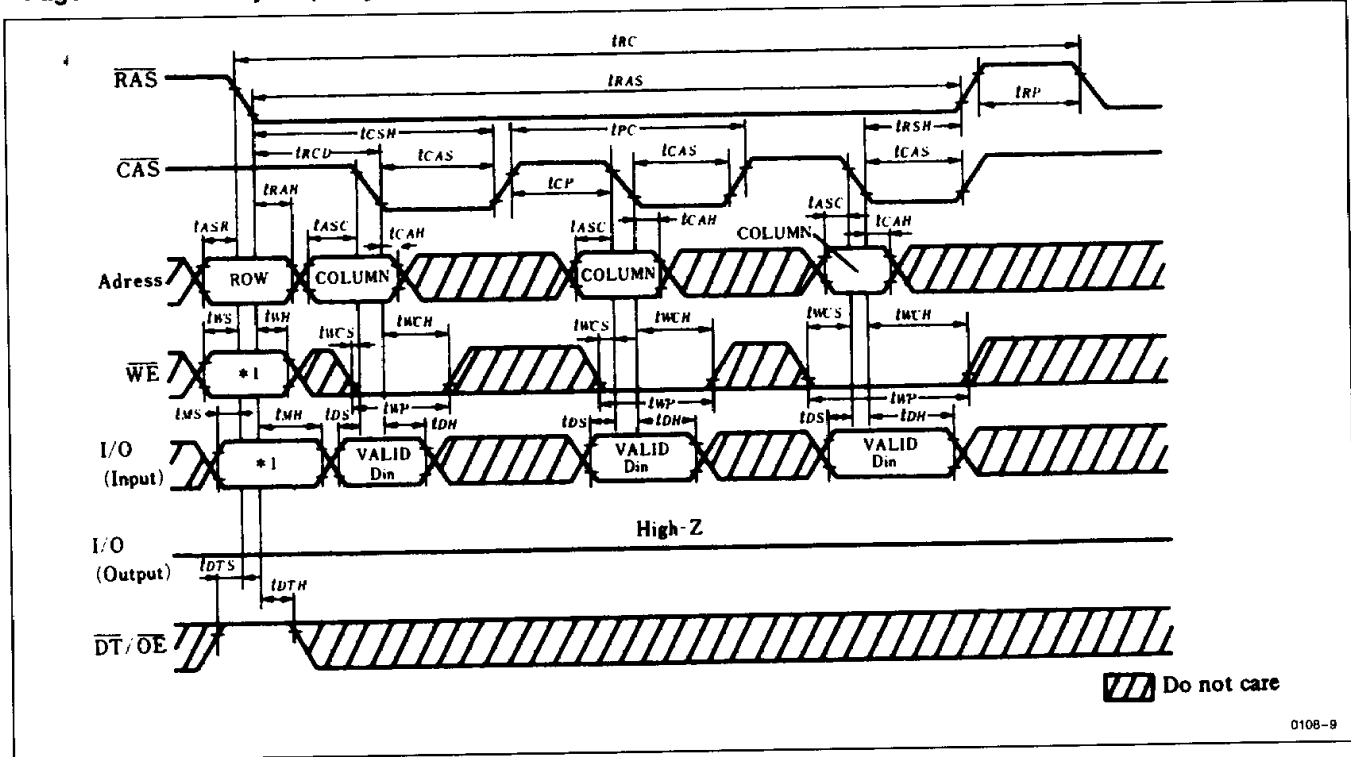


• Page Mode Read Cycle



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• Page Mode Write Cycle (Early Write)

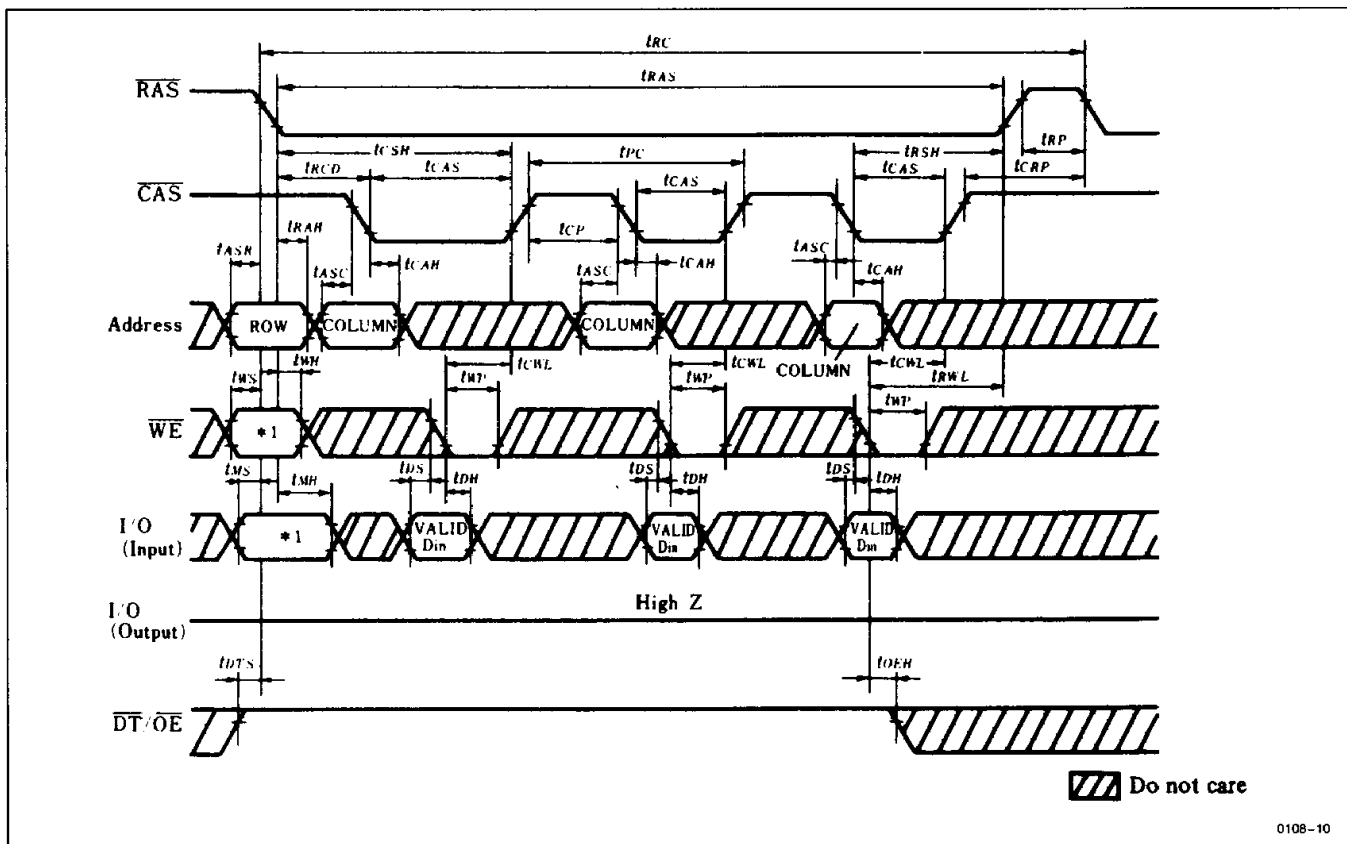


0108-9

Note: *1. When \overline{WE} is "H" level, all the data on I/O₁-I/O₄ can be written into the memory cell.
When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of \overline{RAS} .

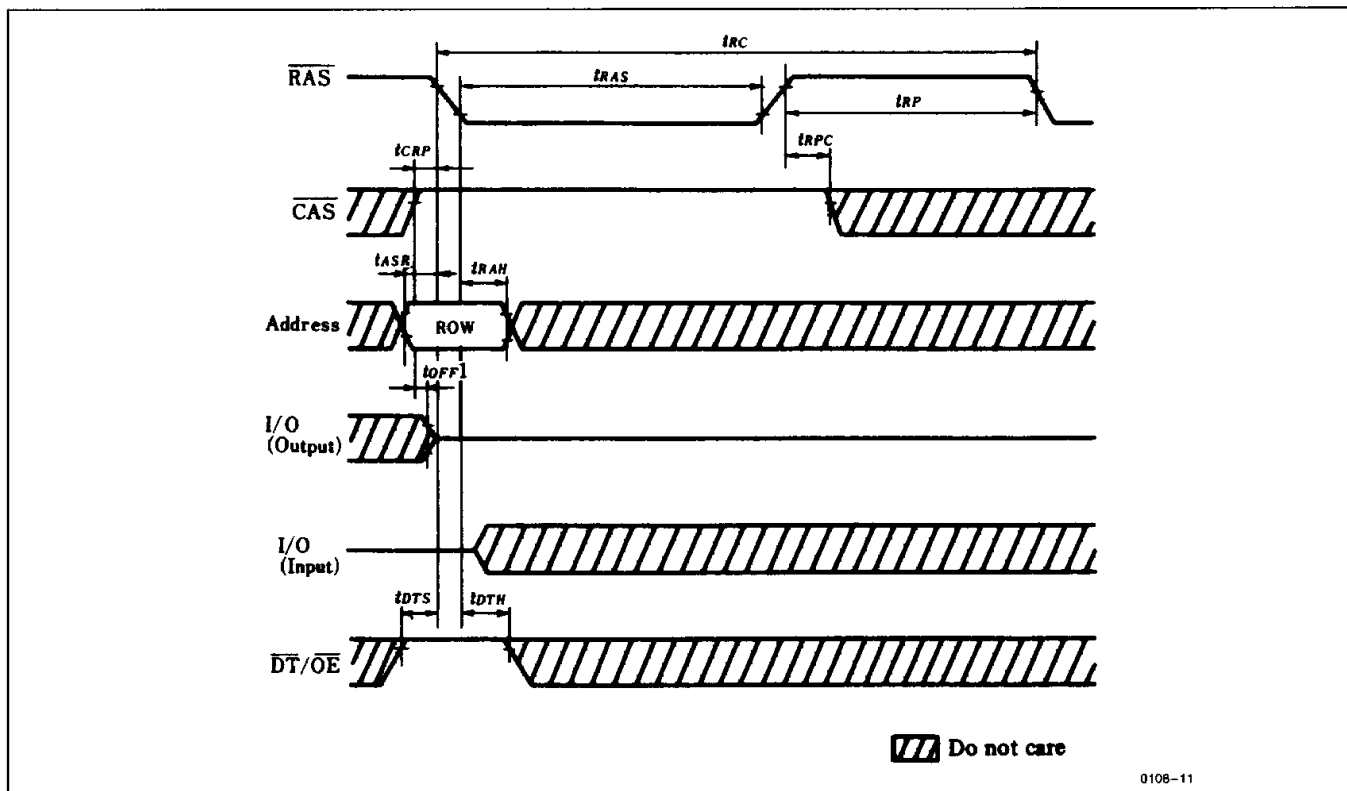


• Page Mode Write Cycle (Delayed Write)

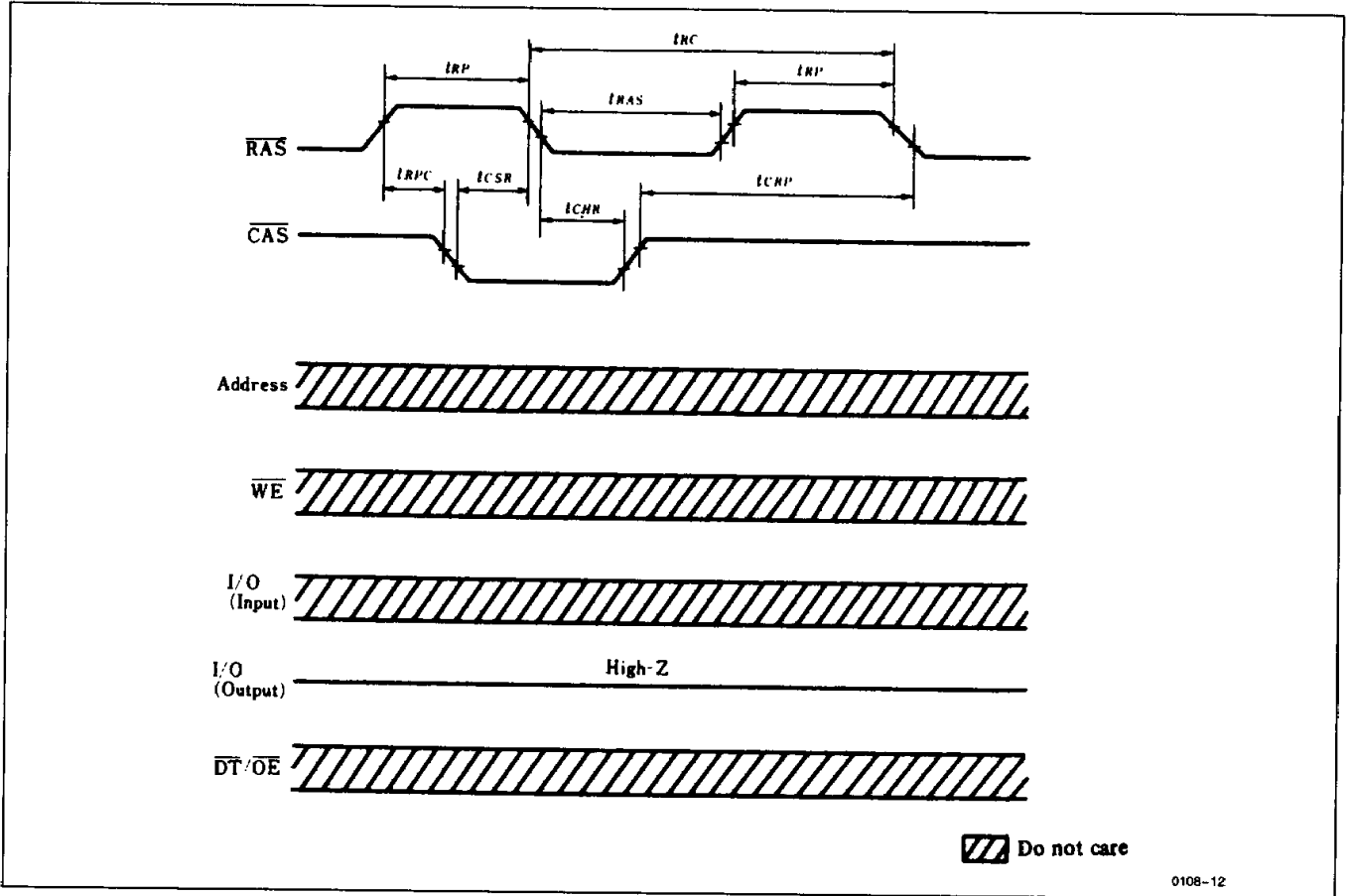


Note: *1. When \overline{WE} is "H" level, all the data on I/O₁-I/O₄ can be written into the memory cell.
When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of \overline{RAS} .

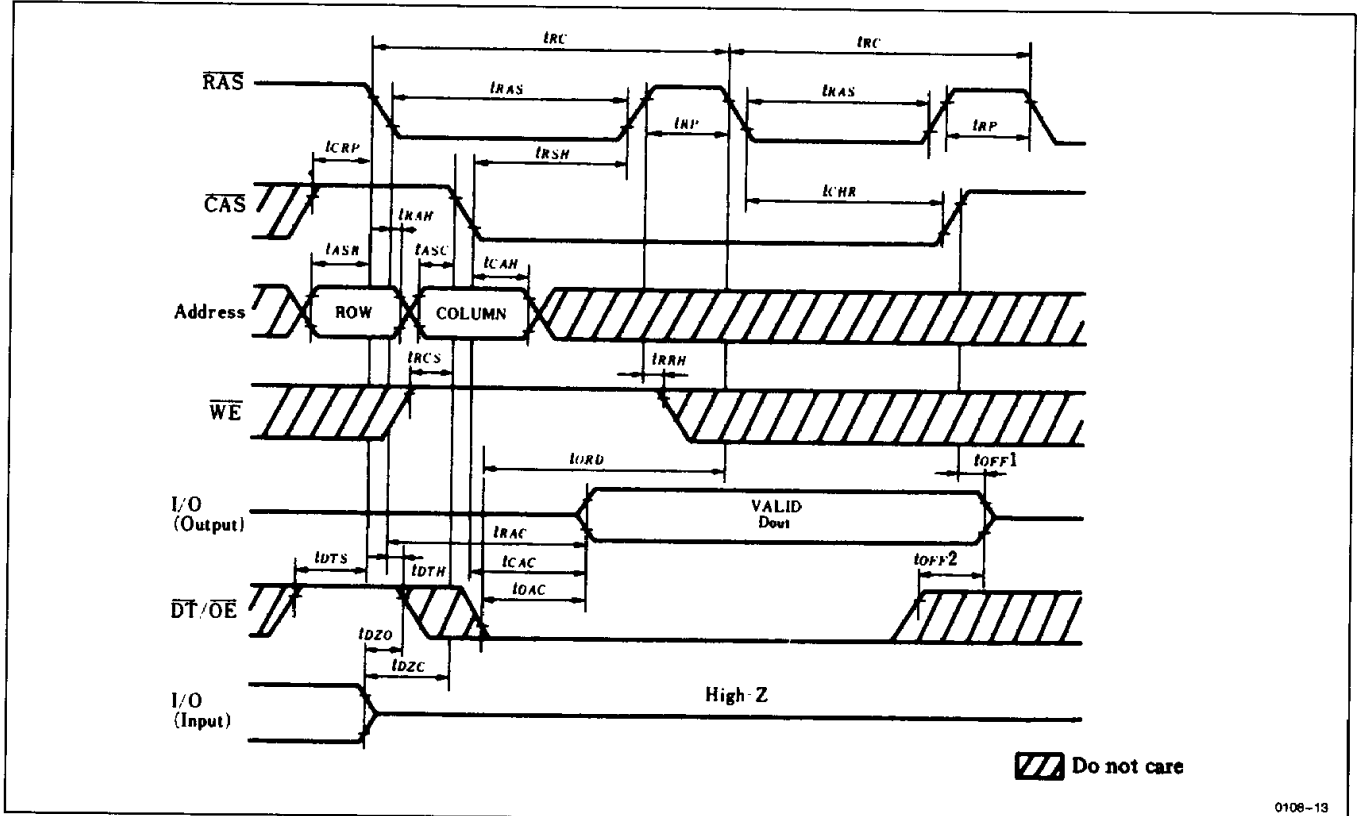
• \overline{RAS} Only Refresh Cycle



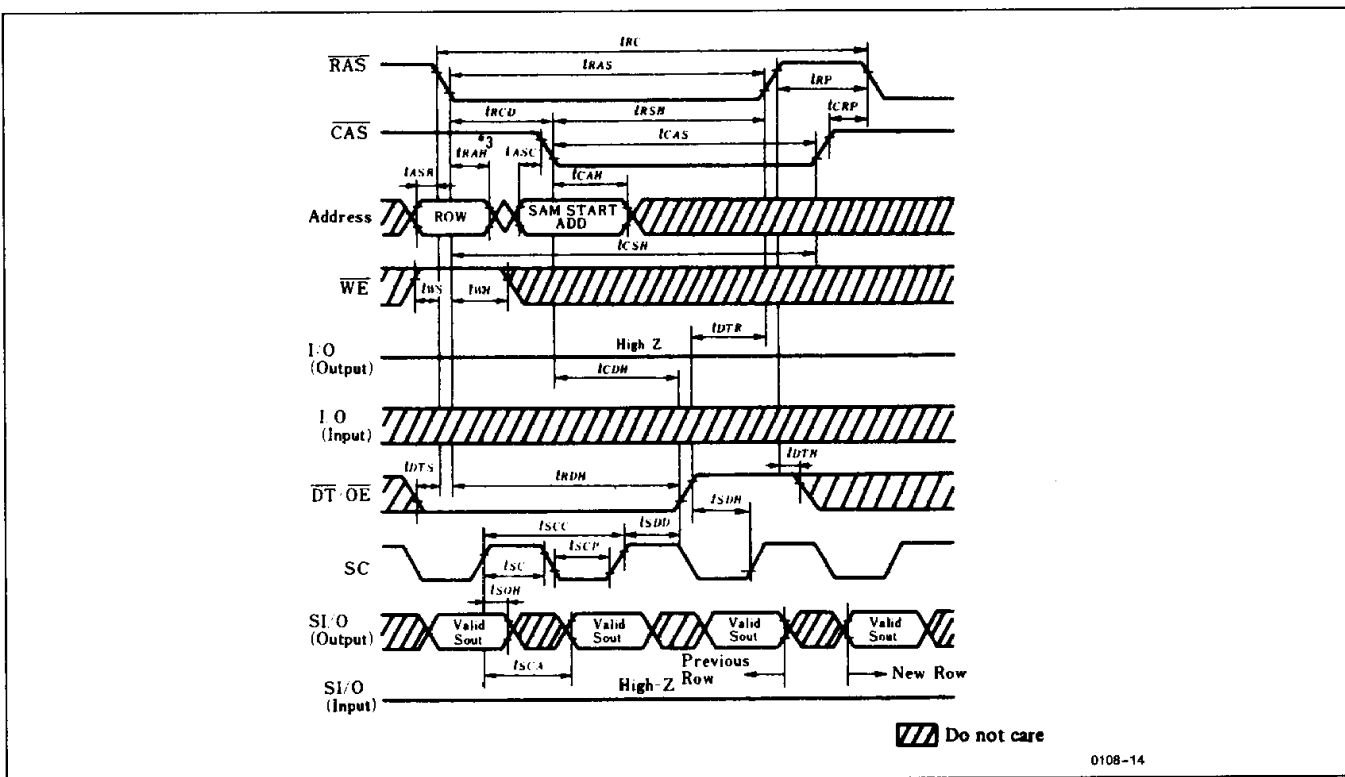
• CAS Before RAS Refresh Cycle



• Hidden Refresh Cycle



• Read Transfer Cycle (1)*1, *2

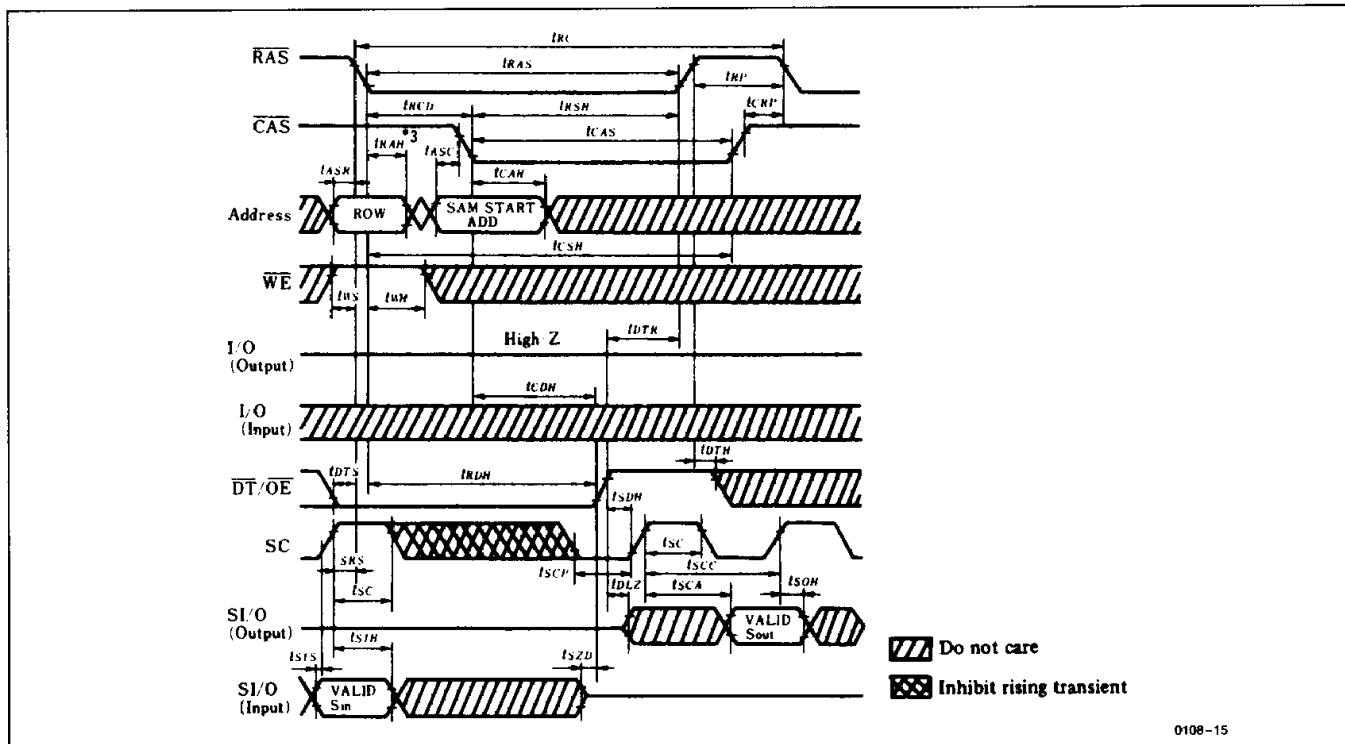


Notes: *1. In the case that the previous data transfer cycle was read transfer.

*2. Assume that SOE is "L" level.

*3. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Read Transfer Cycle (2)*1, *2



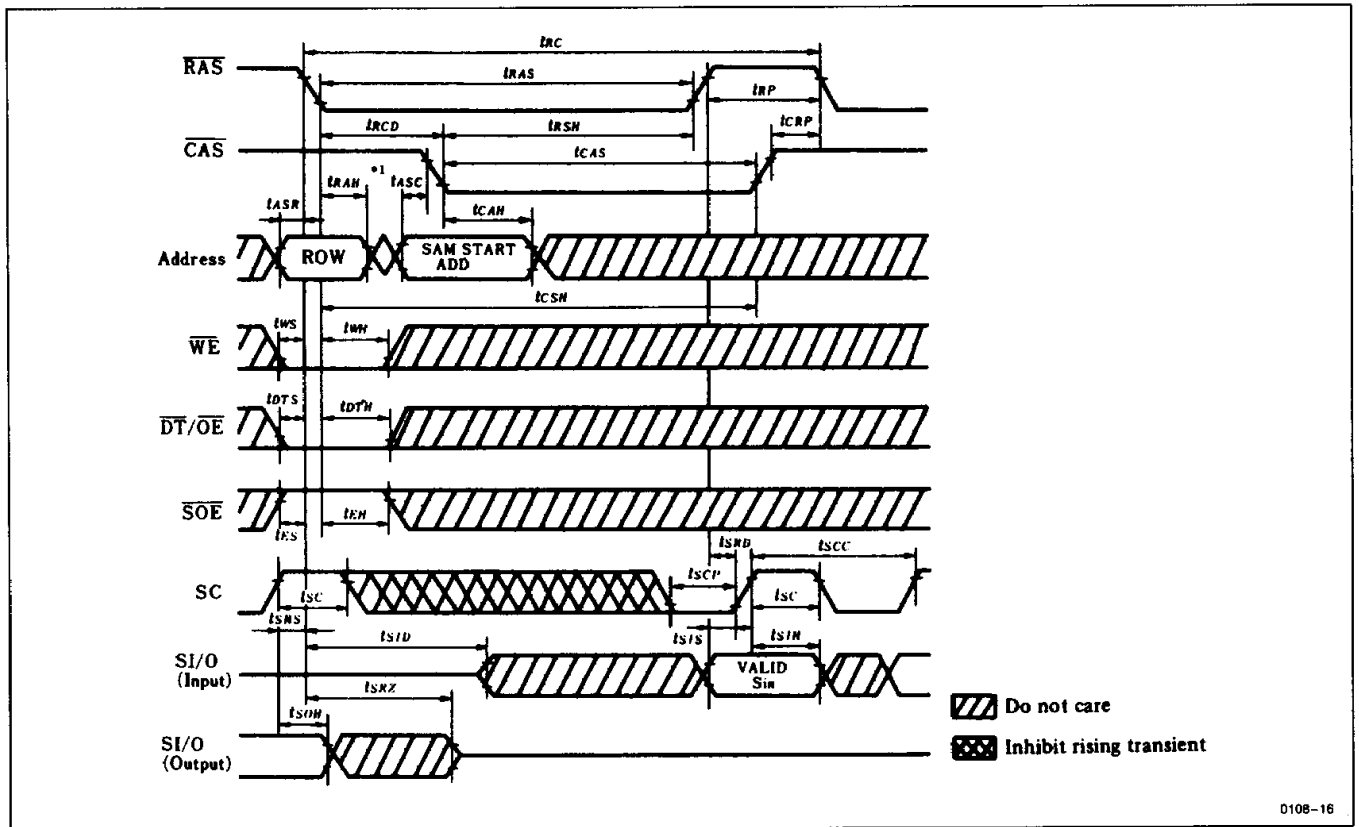
Notes: *1. In the case that the previous data transfer cycle was write transfer or pseudo transfer.

*2. Assume that SOE is "L" level.

*3. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.



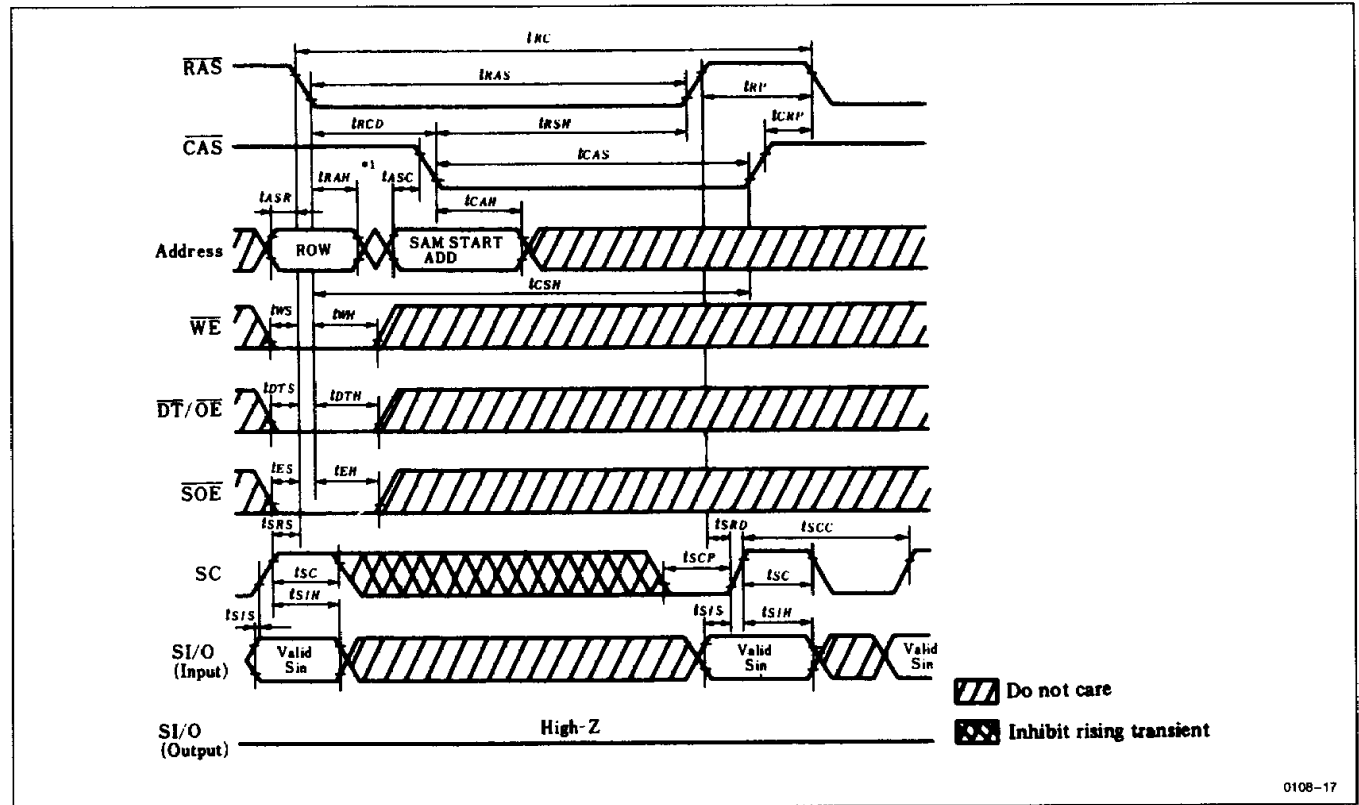
• Pseudo Transfer Cycle



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Note: *1. $\overline{\text{CAS}}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Write Transfer Cycle

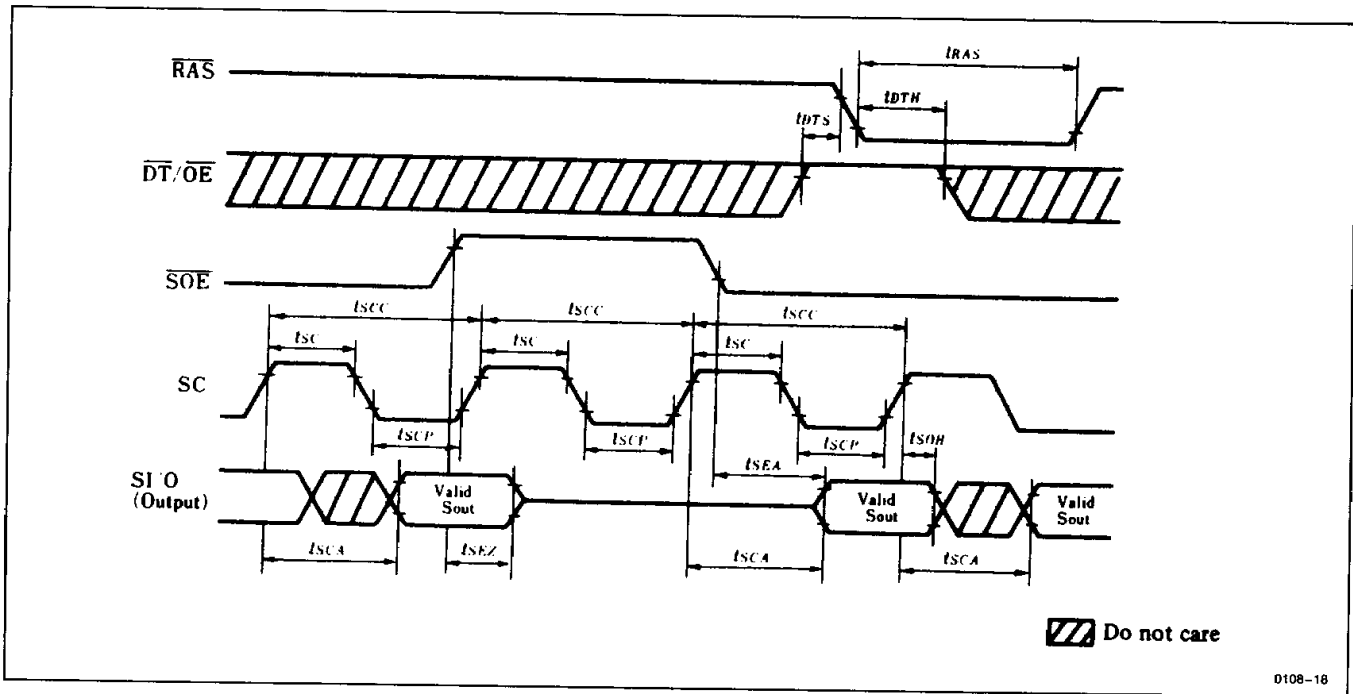


0108-17

Note: *1. $\overline{\text{CAS}}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

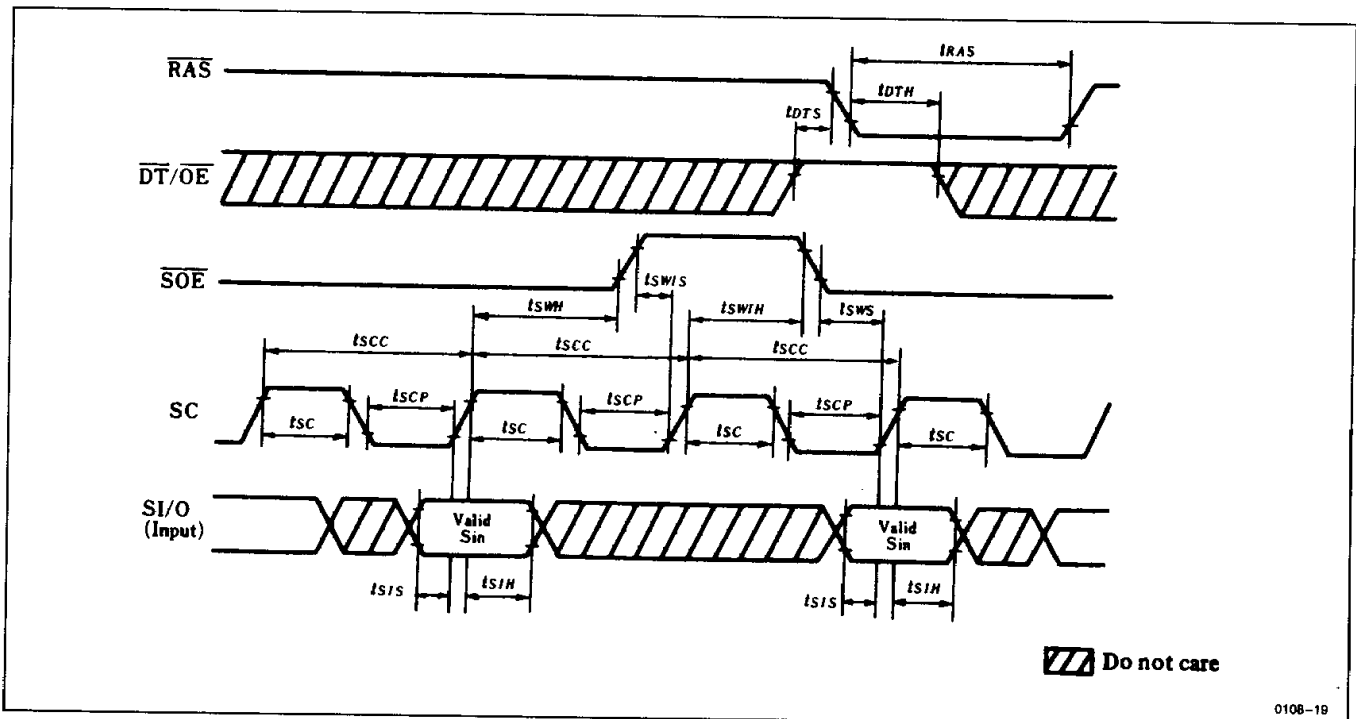


• Serial Read Cycle



0108-18

• Serial Write Cycle



0108-19