

DATA SHEET

PDIUSBP11A Universal Serial Bus Transceiver

Product data
Supersedes data of 1999 Jun 04

2001 Jun 12

Universal Serial Bus transceiver

PDIUSBP11A

FEATURES

- Complies with Universal Serial Bus specification 1.1
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports 12Mbit/s "Full Speed" and 1.5Mbit/s "Low Speed" serial data transmission
- Compatible with the VHDL "Serial Interface Engine" from USB Implementers' Forum
- Supports single-ended data interface
- Single 3.3V supply
- Available in SO-14, SSOP-14 and TSSOP-14 packages

DESCRIPTION

The PDIUSBP11A is a one chip generic USB transceiver. It is designed to allow 5.0V or 3.3V programmable and standard logic to interface with the physical layer of the Universal Serial Bus. It is capable of transmitting and receiving serial data at both full speed (12Mbit/s) and low speed (1.5Mbit/s) data rates.

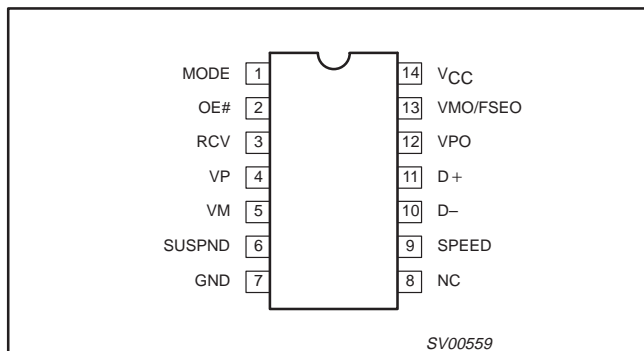
The pinout conforms with the "Serial Interface Engine". Implementation of the Serial Interface Engine along with the USB transceiver allows the designer to make USB compatible devices with off-the-shelf logic and easily modify and update the application.

The PDIUSBP11A is backward compatible to the PDIUSBP11 and allows for single-ended data interfacing.

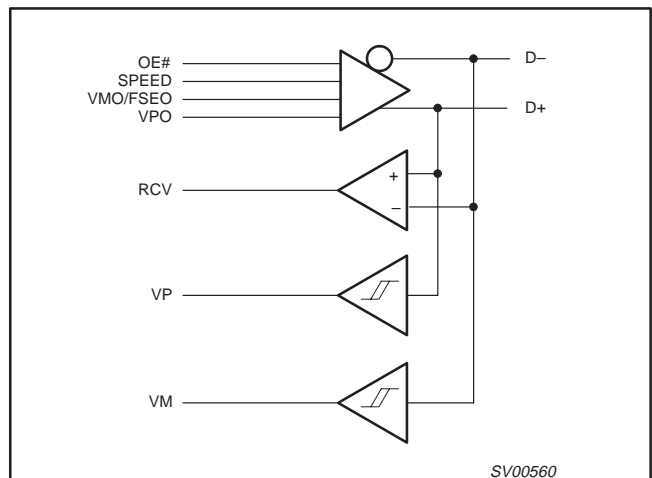
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDIUSBP11AD	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
PDIUSBP11ADB	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
PDIUSBP11APW	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



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PIN DESCRIPTION

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION																											
3	RCV	O	Receive data. CMOS level output for USB differential input																											
2	OE#	I	Output Enable. Active LOW, enables the transceiver to transmit data on the bus. When not active the transceiver is in receive mode																											
1	MODE	I	Mode. When left unconnected, a weak pull-up transistor pulls it to V_{CC} and in this mode, the PDIUSBP11A is backward compatible to PDIUSBP11. When connected to GND, the VMO/FSEO pin takes the function of FSEO (Force SEO).																											
12, 13	VPO, VMO/FSEO	I	Inputs to differential driver. (Outputs from SIE).																											
			<table border="1"> <thead> <tr> <th>MODE</th> <th>VPO</th> <th>VMO/FSEO</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td>0</td> <td>0</td> <td>Logic "0"</td> </tr> <tr> <td>0</td> <td>1</td> <td>SE0#</td> </tr> <tr> <td>1</td> <td>0</td> <td>Logic "1"</td> </tr> <tr> <td>1</td> <td>1</td> <td>SE0#</td> </tr> <tr> <td rowspan="4">1</td> <td>0</td> <td>0</td> <td>SE0#</td> </tr> <tr> <td>0</td> <td>1</td> <td>Logic "0"</td> </tr> <tr> <td>1</td> <td>0</td> <td>Logic "1"</td> </tr> <tr> <td>1</td> <td>1</td> <td>Illegal code</td> </tr> </tbody> </table>	MODE	VPO	VMO/FSEO	RESULT	0	0	0	Logic "0"	0	1	SE0#	1	0	Logic "1"	1	1	SE0#	1	0	0	SE0#	0	1	Logic "0"	1	0	Logic "1"
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	1	0	Logic "1"																											
	1	1	Illegal code																											
4, 5	VP, VM	O	Gated version of D- and D+. Outputs are logic "0" and logic "1". Used to detect single ended zero (SE0#), error conditions, and interconnect speed. (Inputs to SIE).																											
			<table border="1"> <thead> <tr> <th>VP</th> <th>VM</th> <th>RESULT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>SE0#</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low Speed</td> </tr> <tr> <td>1</td> <td>0</td> <td>Full Speed</td> </tr> <tr> <td>1</td> <td>1</td> <td>Error</td> </tr> </tbody> </table>	VP	VM	RESULT	0	0	SE0#	0	1	Low Speed	1	0	Full Speed	1	1	Error												
VP	VM	RESULT																												
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11, 10	D+, D-	AI/O	Data+, Data-. Differential data bus conforming to the Universal Serial Bus standard.																											
6	SUSPND	I	Suspend. Enables a low power state while the USB bus is inactive. While the suspnd pin is active it will drive the RCV pin to a logic "0" state. Both D+ and D- are tri-stated.																											
9	SPEED	I	Edge rate control. Logic "1" operates at edge rates for "full speed". Logic "0" operates edge rates for "low speed".																											
14	VCC		3.0V to 3.6V power supply																											
7	GND		Ground reference																											

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V _{CC}	DC supply voltage		3.0	3.6	V
V _I	DC Input voltage range		0	5.5	V
V _{AI/O}	DC input range for AI/Os		0	V _{CC}	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage		-0.5	+6.5	V
I _{latchup}	Latchup current	V _I < 0 or V _I > V _{CC}	-	200	mA
V _I	DC input voltage	Note 2	-0.5	+5.5	V
V _{I/O}	DC input voltage range for I/Os		-0.5	V _{CC} + 0.5	V
V _O	DC output voltage	Note 2	-0.5	V _{CC} + 0.5	V
I _{CC} , I _{GND}	DC V _{CC} or GND current		-	±100	mA
T _{STO}	Storage temperature range		-60	+150	°C
P _{TOT}	Power dissipation per package				mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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DC CHARACTERISTICS (DIGITAL PINS)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP	MAX	
INPUT LEVELS						
V _{IL}	LOW level input voltage		-	-	0.8	V
V _{IH}	HIGH level input voltage		2.0	-	-	V
OUTPUT LEVELS						
V _{OL}	LOW level output voltage	I _{OL} = 4mA	-	-	0.4	V
		I _{OL} = 20μA	-	-	0.1	
V _{OH}	HIGH level output voltage	I _{OH} = 4mA	2.4	-	-	V
		I _{OH} = 20μA	V _{CC} -0.1	-	-	
LEAKAGE CURRENT						
I _L	Input leakage current		-	-	±5	μA
I _{CCS}	Supply current in Suspend		-	-	5	μA
SUPPLY CURRENT						
I _{CC}	Operating supply current		-	6	15	mA

DC CHARACTERISTICS (A/I/O PINS)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Temp = -40°C to +85°C		
			MIN	MAX	
INPUT LEVELS					
V _{DI}	Differential input sensitivity	(D+) - (D-)	0.2	-	V
V _{CM}	Differential common mode range	Includes V _{DI} range	0.8	2.5	V
V _{SE}	Single ended receiver threshold		0.8	2.0	V
OUTPUT LEVELS					
V _{OL}	Static output LOW voltage	R _L of 1.5 kΩ to 3.6V	-	0.3	V
V _{OH}	Static output HIGH voltage	R _L of 15 kΩ to GND	2.8	3.6	V
LEAKAGE CURRENT					
I _{LO}	Hi-Z State data line leakage current	0V < V _{IN} < 3.3V	-	±10	μA
CAPACITANCE					
C _{IN}	Transceiver capacitance	Pin to GND	-	20	pF
OUTPUT RESISTANCE					
Z _{DRV} ¹	Driver output resistance	Steady state drive	6	18	Ω

NOTE:

- Excludes external resistor. In order to comply with USB Specifications 1.1, external series resistors of 24Ω ±1% each on D+ and D- are recommended.

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AC CHARACTERISTICS (A/I/O PINS. FULL SPEED)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			
			MIN	TYP	MAX	
Driver Characteristics		$C_L = 50\text{pF}$; $R_{pu} = 1.5\text{k}\Omega$ on D+ to V_{CC}				
t_R	Transition Time: Rise time	Between 10% and 90% Waveform 1	41		20	ns
t_F	Fall time	Waveform 1	41		20	ns
t_{RFM}	Rise / Fall time matching	(t_R/t_F)	90		111.1	%
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
Driver Timings						
tp_{LH}	Driver propagation delay	Waveform 2			18	ns
tp_{HL}	(VPO, VMO/FSEO to D+/D-)	Waveform 2			19	ns
tp_{HZ}	Driver disable delay	Waveform 4			13	ns
tp_{LZ}	(OE# to D+/D-)	Waveform 4			13	ns
tp_{ZH}	Driver enable delay	Waveform 4			17	ns
tp_{ZL}	(OE# to D+/D-)	Waveform 4			17	ns
Receiver Timings						
tp_{LH}	Receiver propagation delay	Waveform 3			16	ns
tp_{HL}	(D+, D- to RCV)	Waveform 3			19	ns
tp_{LH}	Single-ended receiver delay	Waveform 3			8	ns
tp_{HL}	(D+, D- to VP, VM)	Waveform 3			8	ns

NOTE:

- The 4ns specification is only for $0^{\circ}\text{C to } +85^{\circ}\text{C}$.

AC CHARACTERISTICS (A/I/O PINS. LOW SPEED)

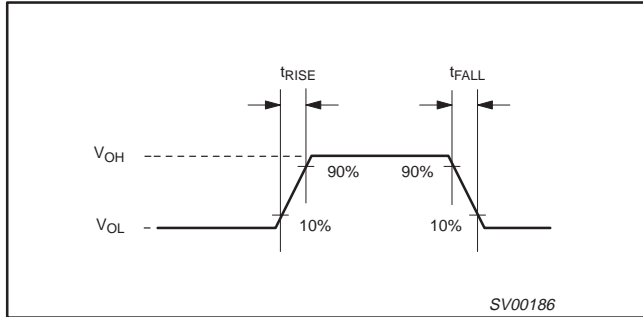
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			
			MIN	TYP	MAX	
Driver Characteristics		$C_L = 200\text{pF}$ and 600pF ; $R_{pu} = 1.5\text{k}\Omega$ on D- to V_{CC}				
t_{LR}	Transition Time: Rise time	Between 10% and 90% $C_L = 200\text{pF}$. Waveform 1	75		300	ns
t_{LF}	Fall time	$C_L = 600\text{pF}$. Waveform 1	75		300	ns
t_{LRFM}	Rise / Fall time matching	(t_{LR}/t_{LF})	80		125	%
V_{LCRS}	Output signal crossover voltage		1.3		2.0	V
Driver Timings						
tp_{LH}	Driver propagation delay	Waveform 2			300	ns
tp_{HL}	(VPO, VMO/FSEO to D+/D-)	Waveform 2			300	ns
tp_{HZ}	Driver disable delay	Waveform 4			13	ns
tp_{LZ}	(OE# to D+/D-)	Waveform 4			13	ns
tp_{ZH}	Driver enable delay	Waveform 4			205	ns
tp_{ZL}	(OE# to D+/D-)	Waveform 4			205	ns
Receiver Timings						
tp_{LH}	Receiver propagation delay	Waveform 3			18	ns
tp_{HL}	(D+, D- to RCV)	Waveform 3			18	ns
tp_{LH}	Single-ended receiver delay	Waveform 3			28	ns
tp_{HL}	(D+, D- to VP, VM)	Waveform 3			28	ns

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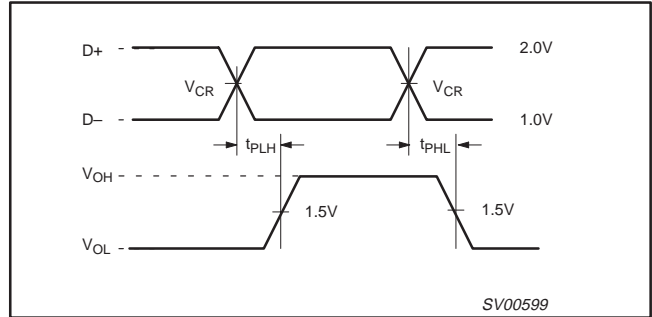
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AC WAVEFORMS

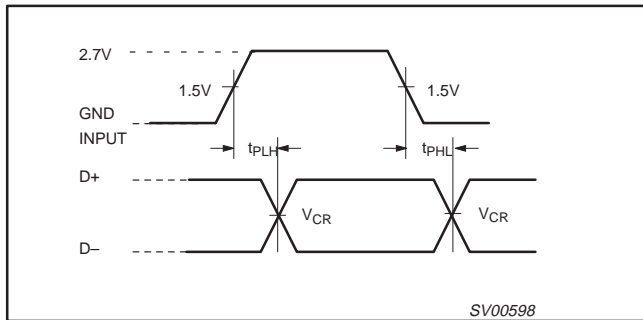
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V).



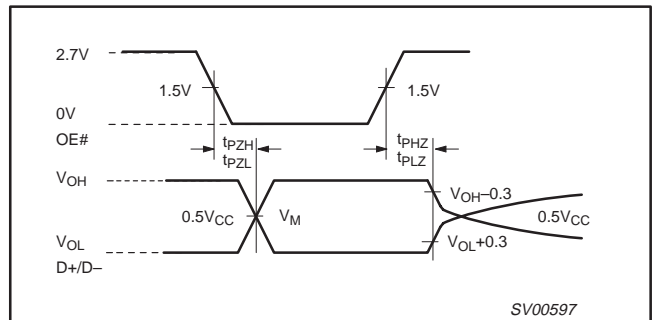
Waveform 1. Rise and Fall Times



Waveform 3. D+/D- to RCV, VP/VM

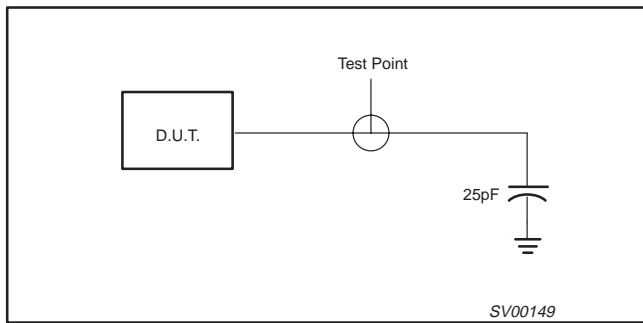


Waveform 2. VPO, VMO/FSEO to D+/D-

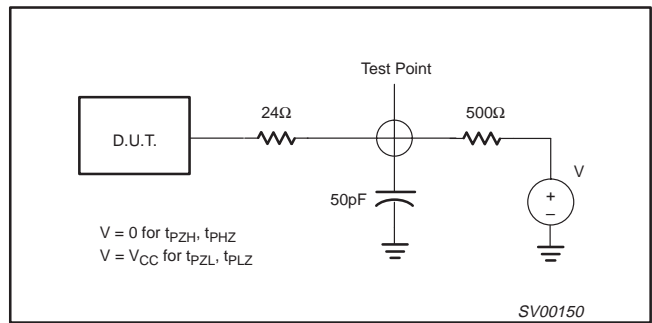


Waveform 4. OE# to D+/D-

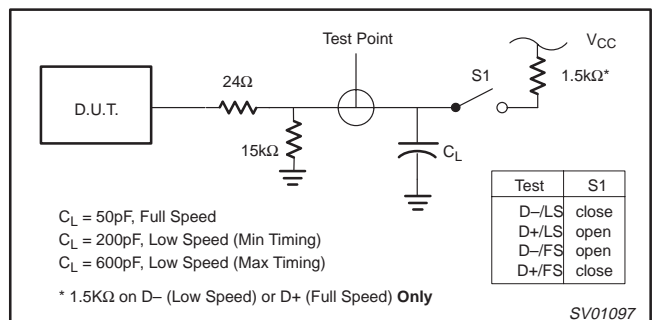
TEST CIRCUITS AND WAVEFORMS



Load for VM/VP and RCV



Load for Enable and Disable Times



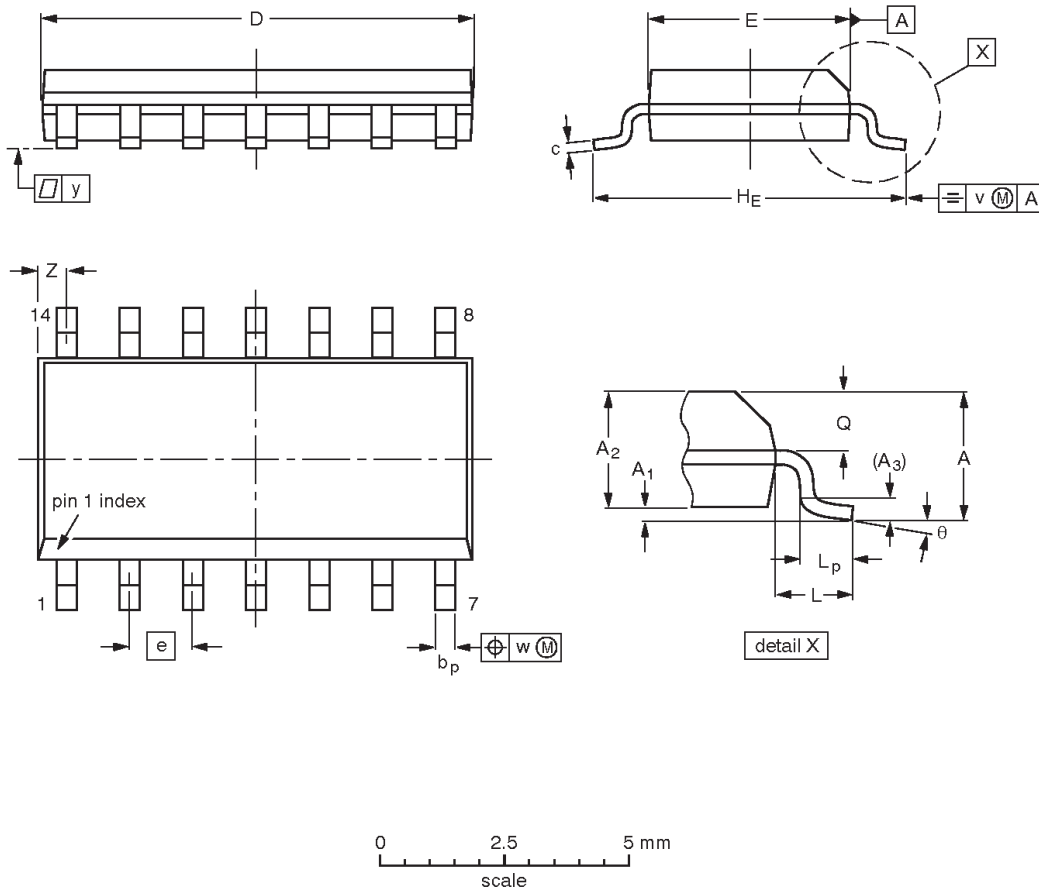
Load for D+/D-

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

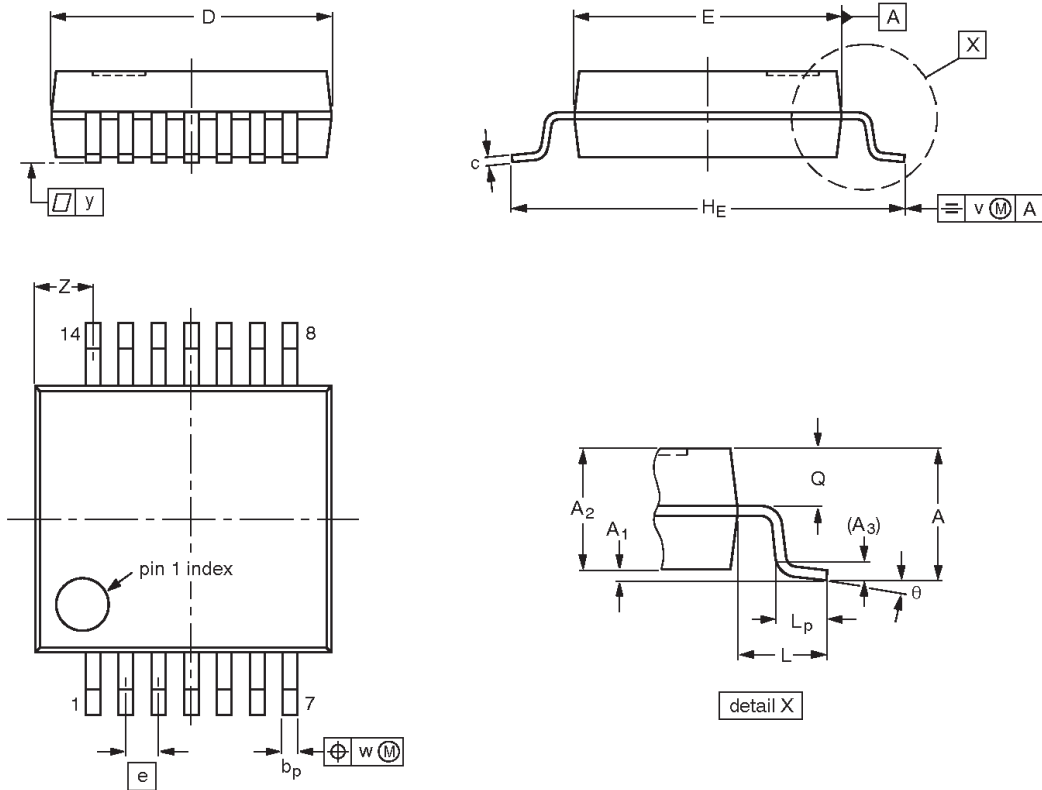
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

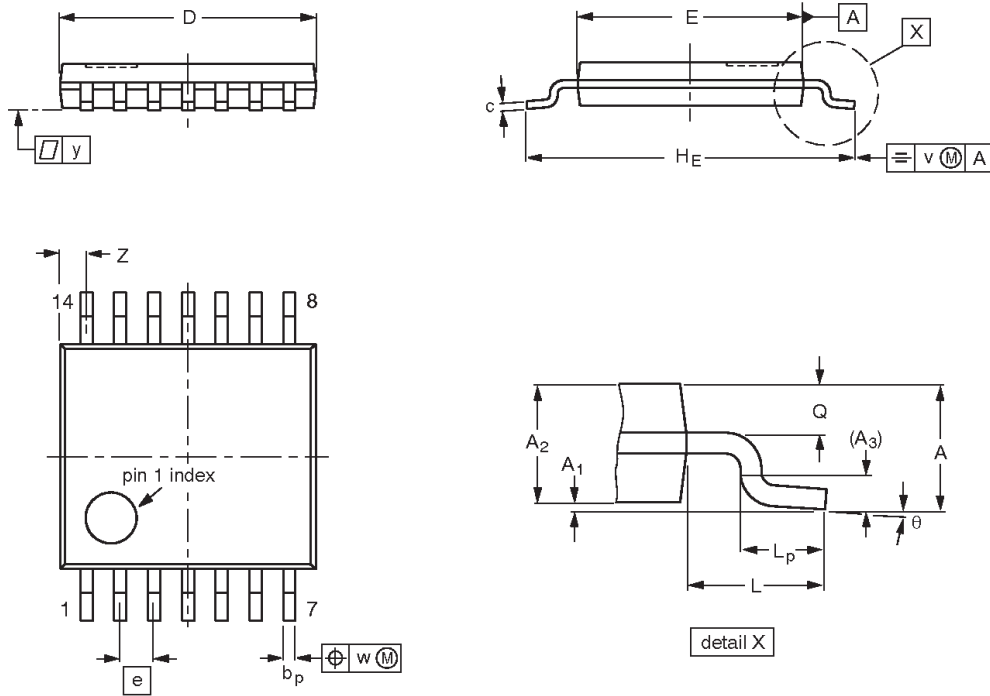
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				96-01-18 99-12-27

Universal Serial Bus transceiver

PDIUSBP11A

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-95-04-04 99-12-27

Universal Serial Bus transceiver

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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