# TFDU6100E/TFDS6500E/TFDT6500E

## 2.7–5.5V Fast Infrared Transceiver Module Family (FIR, 4 Mbit/s)

## Features

- Compliant to IrDA 1.2 (Up to 4 Mbit/s), HP–SIR, Sharp ASK and TV Remote
- Wide Operating Voltage Range (2.7 to 5.5 V )
- Low-Power Consumption (3 mA Supply Current)
- Power Shutdown Mode (1 µA Shutdown Current)
- Long Range (Up to 2.0 m at 4 Mbit/s in Nominal Design)
- High Efficiency Emitter (120 mW/sr min ±15°)
- Three Surface Mount Package Options
  - Universal (9.7 x 4.7 x 4.0 mm)
  - Side View (13.0x5.95x5.3mm)
  - Top View (13.0x7.6x5.95mm)
- BabyFace (Universal) Package Capable of Surface Mount Solderability to Side and Top View Orientation
- Directly Interfaces With Various Super I/O and Controller Devices
- Built–In EMI Protection – No External Shielding Necessary
- Few External Components Required
- Backward Compatible to All TEMIC SIR and FIR Infrared Transceivers

## Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

## Description

The TFDU6100E, TFDS6500E, and TFDT6500E are a family of low-power infrared transceiver modules compliant to the IrDA 1.2 standard for fast infrared (FIR) data communication, supporting IrDA speeds up to 4.0 Mbit/s, HP–SIR, Sharp ASK and carrier based remote control modes up to 2 MHz. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED), and a low-power CMOS control IC to provide a total front–end solution in a single package. TEMIC's FIR transceivers are available in three package options, including our BabyFace package (TFDU6100E), the smallest FIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints.

The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the pulse-width modulation/demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMSC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a current-limiting resistor in series with the infrared emitter and a $V_{CC}$ bypass capacitor are the only external components required to implement a complete solution.

## Package Options

**TFDU6100E**
**Baby Face (Universal)**

**TFDS6500E**
**Side View**

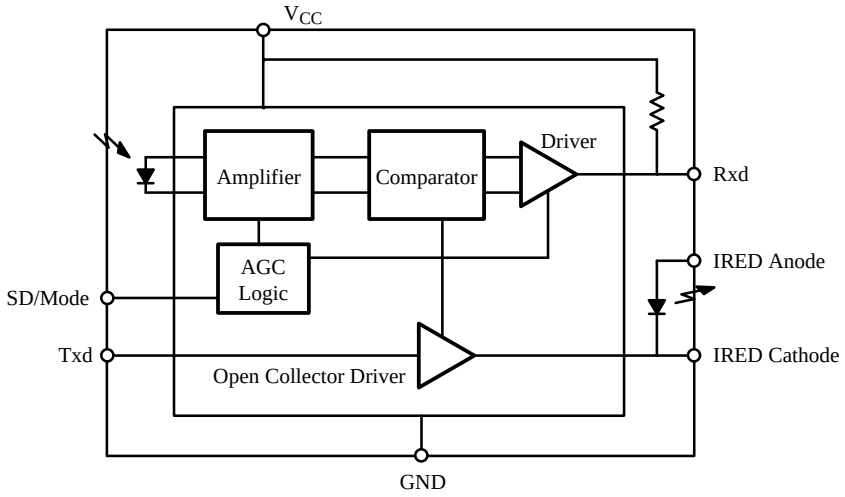
**TFDT6500E**
**Top View**

This product is currently in devleopment. Inquiries regarding the status of this product should be directed to TEMIC Marketing.



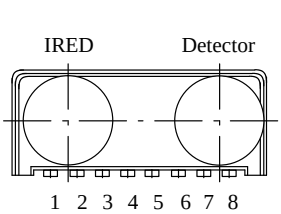
## Pre-Release Information

## Functional Block Diagram

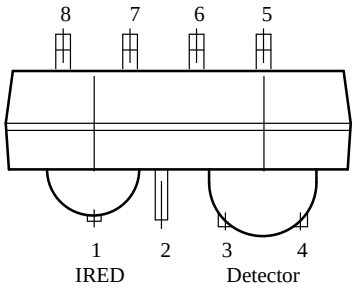



## Pin Assignment and Description

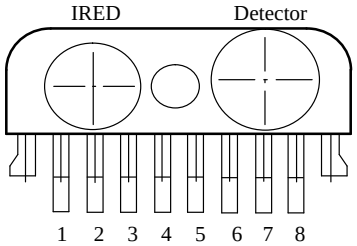
| Pin Number | | Function | Description | I/O | Active |
|---|---|---|---|---|---|
| " U ", " T " Option | " S " Option | | | | |
| 1 | 8 | IRED Anode | IRED anode, should be externally connected to $V_{CC}$ through a current control resistor | | |
| 2 | 1 | IRED Cathode | IRED cathode, internally connected to driver transistor | | |
| 3 | 7 | Txd | Transmit Data Input | I | HIGH |
| 4 | 2 | Rxd | Received Data Output, push–pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull–up or pull–down resistor is required (pin is floating when device is in shutdown mode). | O | LOW |
| 5 | 6 | SD/Mode | Shutdown/Mode | I | HIGH |
| 6 | 3 | $V_{CC}$ | Supply Voltage | | |
| 7 | 5 | NC | Do not connect. | | |
| 8 | 4 | GND | Ground | | |




**"U" Option**
**BabyFace (Universal)**




**"S" Option**
**Side View**




**"T" Option**
**Top View**



# Pre-Release Information

# Ordering Information

| Part Number | Qty/ Reel | Description |
|---|---|---|
| TFDU6100E–TR3 | 1000 pcs | Oriented in carrier tape for side view surface mounting |
| TFDU6100E–TT3 | 1000 pcs | Oriented in carrier tape for top view surface mounting |
| TFDS6500E–TR3 | 750 pcs | |
| TFDT6500E–TR3 | 750 pcs | |

# Absolute Maximum Ratings

| Parameter | Symbol | Test Conditions[a] | Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | | – 0.5 | | 6 | V |
| Supply Voltage Range (Anode) | $V_{anode}$ | | 0 | | $V_{CC}$+1.5 | |
| Input Currents[d] | | | | | 10 | mA |
| Output Sinking Current | | | | | 25 | |
| Power Dissipation[e] | $P_D$ | | | | 350 | mW |
| Junction Temperature | $T_J$ | | | | 125 | °C |
| Ambient Temperature Range (Operating) | $T_{amb}$ | | –25 | | 85 | |
| Storage Temperature Range | $T_{stg}$ | | –25 | | 85 | |
| Soldering Temperature | | See Recommended Solder Profile | | | 240 | |
| Average Output Current | $I_{IRED}$ (DC) | | | | 130 | mA |
| Repetitive Pulsed Output Current | $I_{IRED}$ (RP) | <90 µs, $t_{on}$ <20% | | | 600 | |
| IRED Anode Voltage at Current Output | $V_{IREDA}$ | | – 0.5 | | 6 | V |
| Transmitter Data Input Voltage | $V_{Txd}$ | | – 0.5 | | $V_{CC}$+0.5 | |
| Receiver Data Output Voltage | $V_{Rxd}$ | | – 0.5 | | $V_{CC}$+0.5 | |
| Virtual Source Size[f] | d | | 2.5 | 2.8 | | mm |
| Maximum Intensity for Class 1 Operation of IEC 825 or EN60825[g] | | EN60825, 1997 | | | 320 | mW/sr |

Notes
a. Reference point GND pin unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Maximum input current for all pins (except IRED Anode pin).
e. See Derating Curve.
f. Method: (1-1/e) encircled energy.
g. Worst case IrDA SIR pulse pattern.

# Electrical Characteristics

| Parameter | Symbol | Test Conditions[a] | Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|
| Transceiver | | | | | | |
| Supply Voltage | $V_{CC}$ | | 2.7 | | 5.5 | V |
| Dynamic Supply Current[d] | $I_{CC}$ | SD = Low, $E_e$ = 0 mW/m$^2$ | | 3 | 4 | mA |
| Dynamic Supply Current | $I_{CC}$ | SD = Low, $E_e$ = 1 klx[d] | | 3 | 4 | |
| Standby Supply Current[e] | $I_{SD}$ | SD = High, Mode = floating, 25°C, $E_e$ = 0 klx | | | 1 | µA |
| Standby Supply Current | $I_{SD}$ | SD = High, Mode = floating, T =25°C, $E_e$ = 1 klx[d] | | | 1.5 | |
| Standby Supply Current[e] | $I_{SD}$ | SD = High, Mode = floating, T = 85°C | | | 5 | |
| Operating Temperature Range | $T_A$ | | –25 | | 85 | °C |
| Output Voltage Low | $V_{OL}$ | $R_{load}$ = 2.2 kΩ, $C_{load}$ = 15 pF | | 0.5 | 0.8 | V |
| Output Voltage High | $V_{OH}$ | $R_{load}$ = 2.2 kΩ, $C_{load}$ = 15 pF | $V_{CC}$–0.5 | | | |
| Input Voltage Low | $V_{IL}$ | | 0 | | 0.8 | |
| Input Voltage High[f] | $V_{IH}$ | | 0.9 * $V_{CC}$ | | | |
| Input Voltage High[g] | $V_{IH}$ | $V_{CC} \geq$ 4.5V | 2.4 | | | |
| Input Leakage Current | $I_L$ | | –10 | | +10 | µA |
| Input Capacitance | $C_I$ | | | | 5 | pF |

Notes
a. Tamb = 25°, $V_{CC}$ = 2.7 – 5.5 V unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Receive mode only. In transmit mode, add additional 100 mA (typ) to IRED current.
e. Not ambient light sensitive.
f. CMOS levels.
g. TTL levels.

# Optoelectronic Characteristics

| Parameter | Symbol | Test Conditions[a] | Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|
| **Receiver** | | | | | | |
| Minimum Detection Threshold Irradiance | $E_e$ | 9.6 kbit/s to 115.2 kbit/s | | 20 | 35 | mW/m$^2$ |
| Minimum Detection Threshold Irradiance | $E_e$ | 1.152 Mbit/s to 4 Mbit/s | | 50 | 80 | |
| Maximum Detection Threshold Irradiance | $E_e$ | | 5 | 10 | | kW/m$^2$ |
| Logic LOW Receiver Input Irradiance | $E_e$ | | 4 | | | mW/m$^2$ |
| Rise Time of Output Signal | $t_{RR}$ | 10% to 90%, @2.2 kΩ, 15pF | 10 | | 40 | ns |
| Fall Time of Output Signal | $t_{FR}$ | 90% to 10%, @2.2 kΩ, 15pF | 10 | | 40 | |
| Rx Pulse Width of Output Signal, 50% | $P_w$ | Input pulse length 20 µs, 9.6 kbit/s | 1.2 | 10 | 20 | µs |
| Rx Pulse Width of Output Signal, 50% | $P_w$ | Input pulse length 1.41µs, 115.2 kbit/s mode | 1.2 | | 2.2 | |
| Rx Pulse Width of Output Signal, 50% | $P_w$ | Input pulse length 217 ns, 4.0 Mbit/s mode | 190 | | 260 | ns |
| Rx Pulse Width of Output Signal, 50% | $P_w$ | Input pulse length 125 ns, 4.0 Mbit/s mode | 90 | | 165 | |
| Rx Pulse Width of Output Signal, 50% | $P_w$ | Input pulse length 250 ns, 4.0 Mbit/s mode (double pulse) | 210 | | 290 | |
| Jitter, Leading Edge | | Input Irradiance = 90 mW/m$^2$, 4.0 Mbit/s mode | | | 10 | |
| Latency | $t_L$ | | | | 120 | µs |
| **Transmitter** | | | | | | |
| IRED Operating Current | $I_D$ | $V_{CC}$ = 5 V, $R_1$= 5.6 Ω | | 0.48 | 0.55 | A |
| Output Radiant Intensity[d] | $I_e$ | Txd = High, SD = Low, $R_1$= 5.6 Ω | 120 | 140 | 280 | mW/sr |
| Output Radiant Intensity Half Angle | α | | | ±24 | | ° |
| Output Radiant Intensity[d] | $I_e$ | Txd = Low or SD = High[e], $R_L$=5.6 Ω | | | .04 | mW/sr |
| Peak Wavelength | $\lambda_P$ | | 880 | | 900 | nm |
| Voltage drop at output driver | | $I_F$ = 600 mA, pulse length 2 µs, duty cycle 25% | | 400 | 800 | mV |
| Rise Time, Fall Time | $t_R$, $t_F$ | | 10 | | 40 | ns |
| Optical Overshoot | | | | | 25 | % |

Notes
a. $T_{amb}$ = 25°C, $V_{CC}$ = 2.7 – 5.5 V unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. VCC = 5 V, α = 0°, 15°
e. Receiver is inactive as long as SD = High



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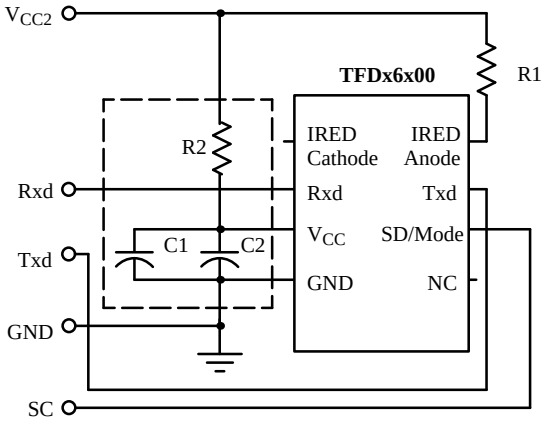
## Recommended Circuit Diagram

The only required components for designing an IrDA 1.2 compatible design using TEMIC FIR transceivers are a current limiting resistor, $R_1$, to the IRED. However, depending on the entire system design and board layout, additional components may be required (see Figure 1).

TEMIC FIR transceivers integrate a sensitive receiver and a built–in power driver. The combination of both needs a careful circuit board layout. The use of thin, long resistive and inductive wiring should be avoided. The inputs (Txd, SD/Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit.




Note: Outlined components are optional depending on quality of power supply.

**Figure 1.** Recommended Application Circuit

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 see Figure 2 . For IrDA compliant operation, a current control resistor of 5.6 Ω is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage $V_{CC}$ and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

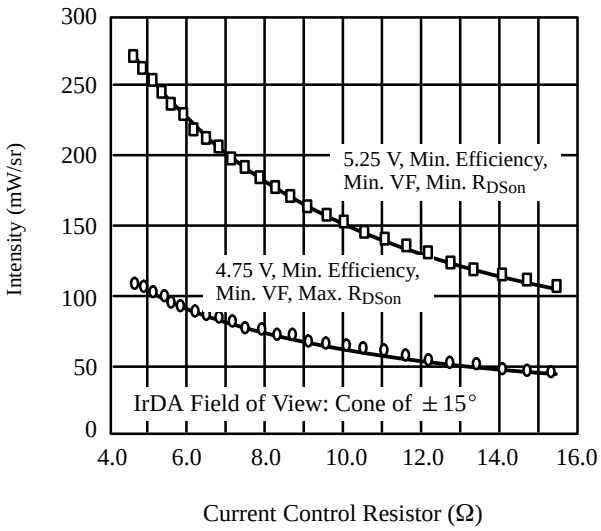



**Figure 2.** $I_e$ vs. $R_l$

The placement of these parts is critical. It is strongly recommended to position C2 as near as possible to the transceiver power supply pins. A tantalum capacitor should be used for C1 while a ceramic capacitor is used for C2. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

**Table 1.** Recommended Application Circuit Components

| Component | Recommended Value |
|---|---|
| C1 | 4.7 µF, Tantalum |
| C2 | 0.1 µF, Ceramic |
| R1 | 5.6 Ω , 0.25 W (recommend using two 0.125 W resistors in parallel) |
| R2 | 47 Ω , 0.125 W |

## Mode Switching

The TFDU6100E, TFDS6500E and TFDT6500E powers on in a no default mode, therefore the data transfer rate has to be set by a programming sequence as described below or selected by setting the mode pin. When using the Mode pin, the standby current might be increased to about 50 to 60 µA. In standby mode, the mode input should float to minimize standby current.

The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower data frequency data can also



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received in high frequency mode with reduced sensitivity. To switch the transceivers from low frequency mode to the 4.0 Mbit/s mode and vice versa, the programming sequences described below are required.

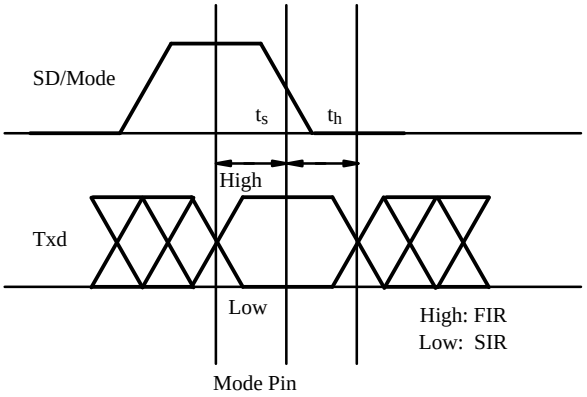



**Figure 3.** Timing Diagram

## Setting to the High Bandwidth Mode (0.576 to 4.0 Mbit/s)

1. Set SD/MODE input to logic ”HIGH”.
2. Set Txd input to logic ”HIGH”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic ”LOW” (this negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd can be set to logic ”LOW”. The hold time of Txd is limited by the maximum allowed pulse length.

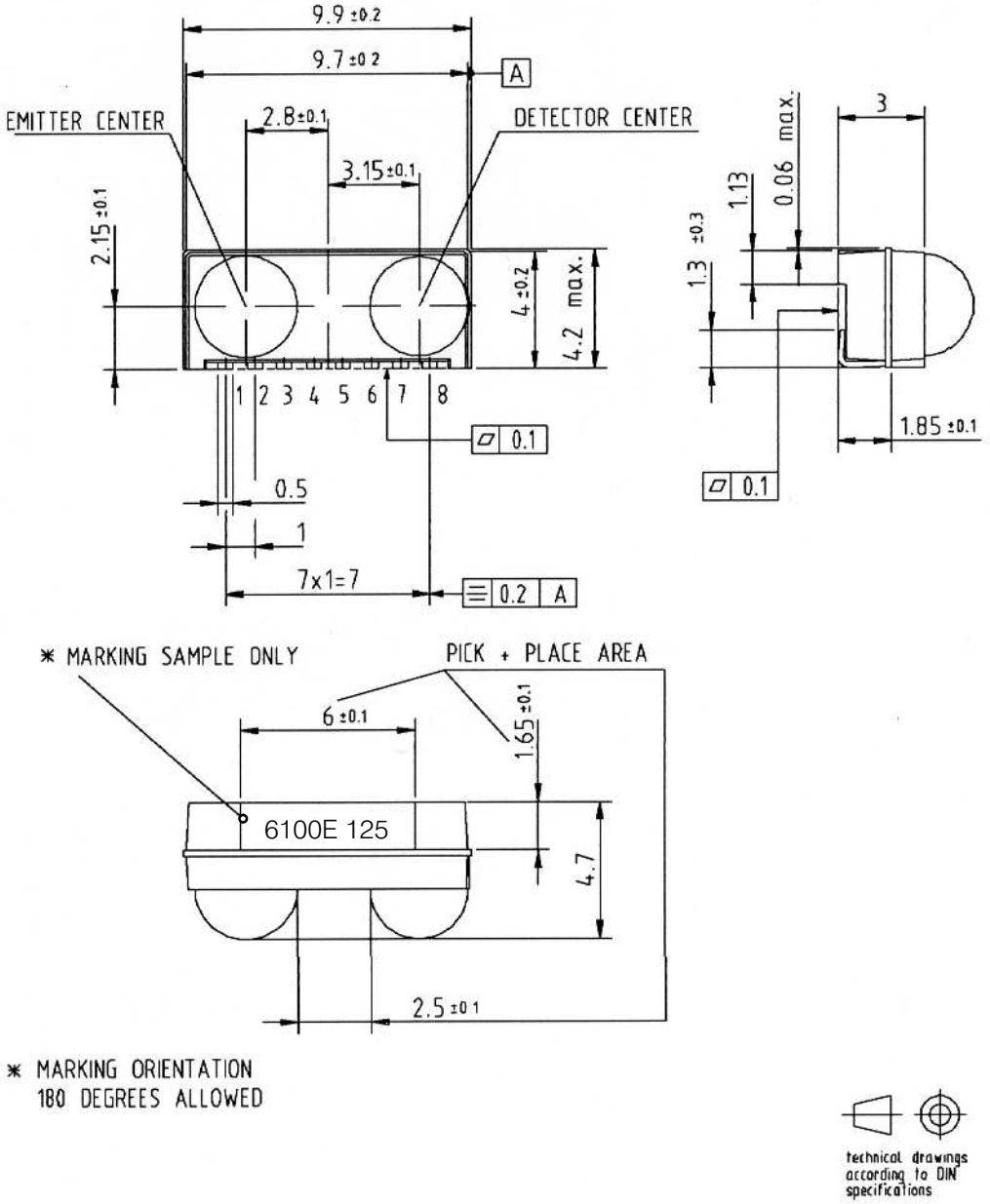
Txd is now enabled as normal Txd input for the high bandwidth mode.

## Setting to the Lower Bandwidth Mode (2.4 to 115.2 kbit/s)

1. Set SD/MODE input to logic ”HIGH”.
2. Set Txd input to logic ”LOW”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic ”LOW” (this negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.

Txd is now enabled as normal Txd input for the lower bandwidth mode.

## TFDU6100E – BabyFace (Universal) Package
## Mechanical Dimensions



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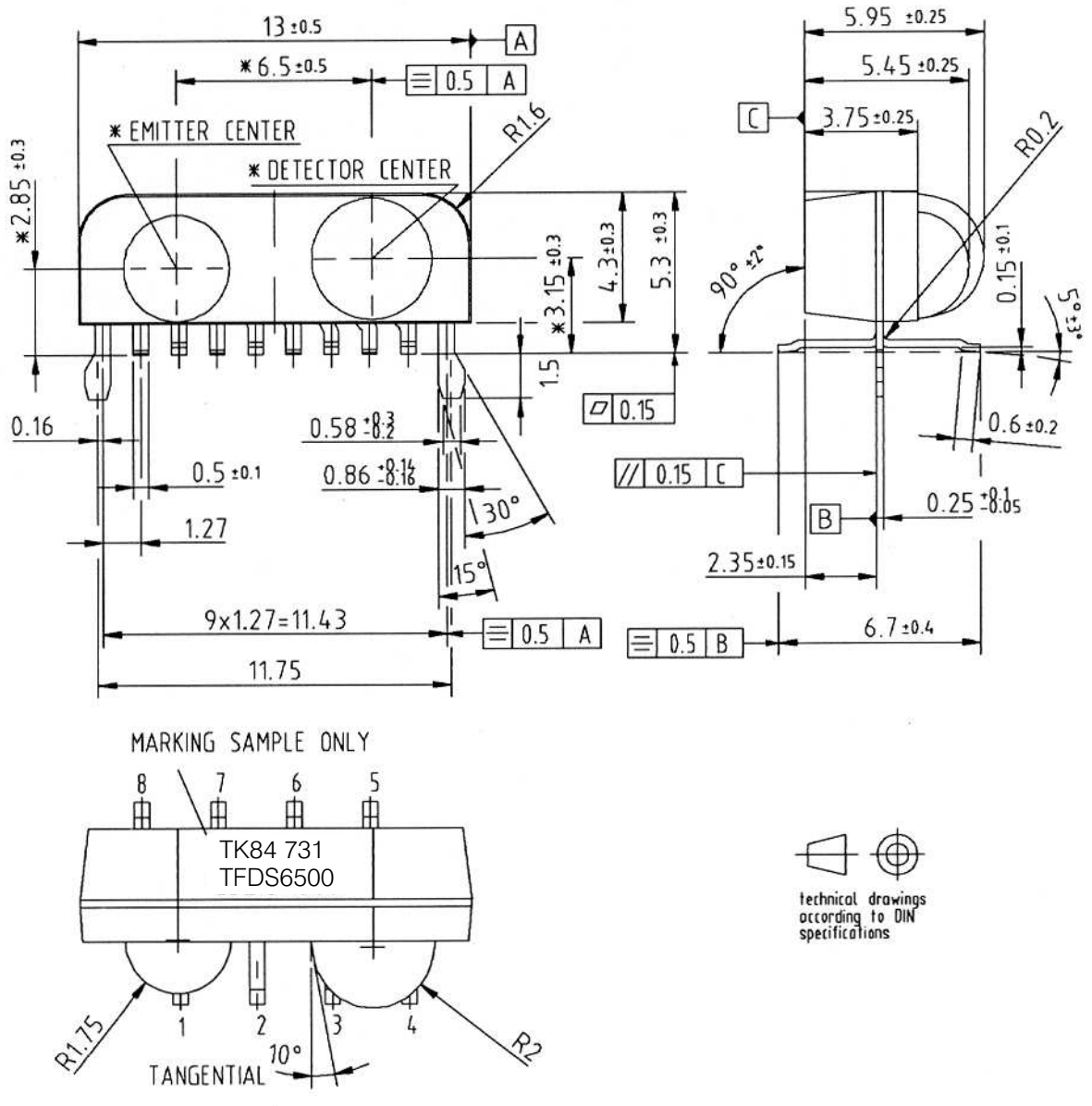
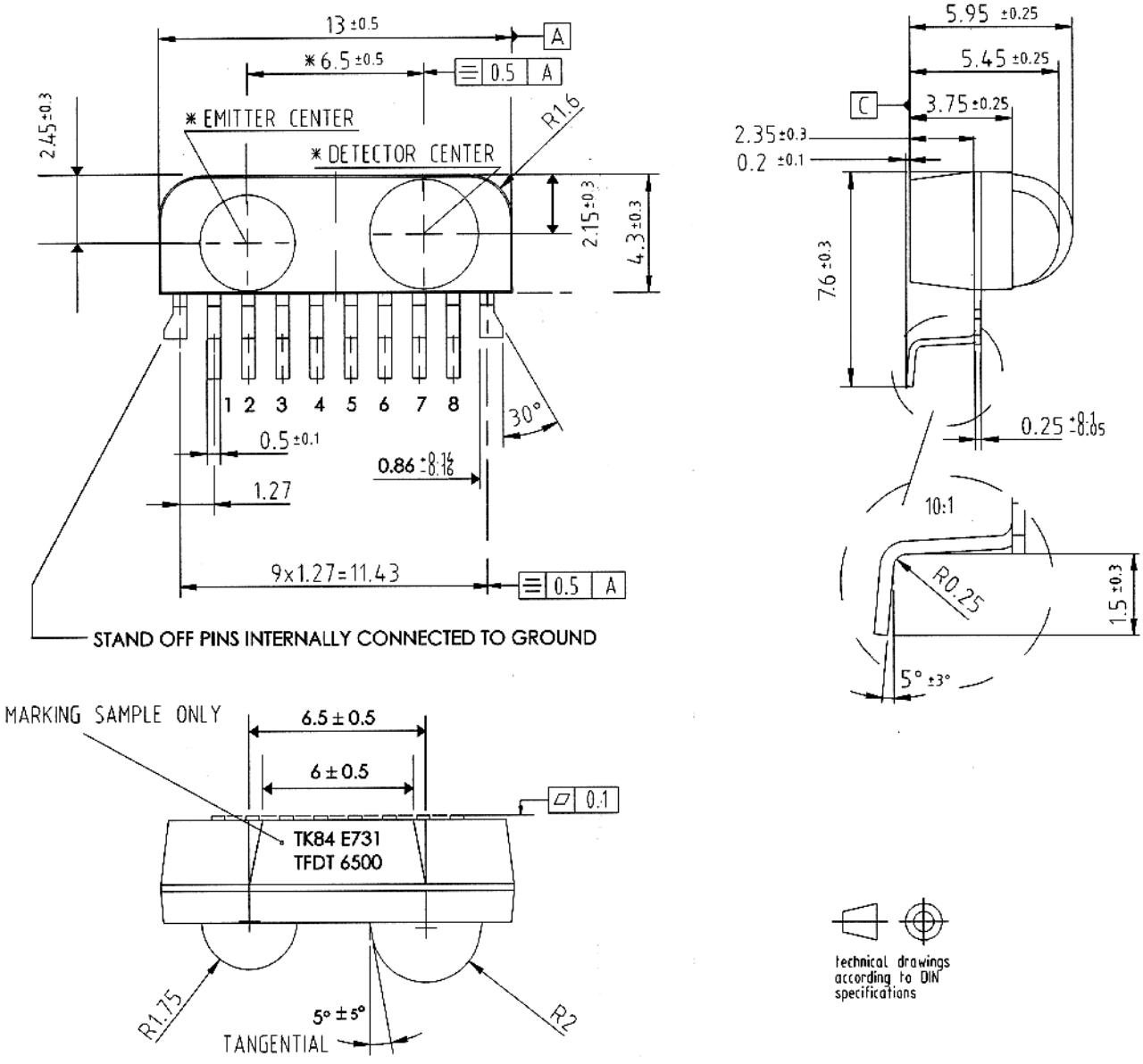
## TFDS6500E – Side View Package
## Mechanical Dimensions



## TFDT6500E – Top View Package
## Mechanical Dimensions



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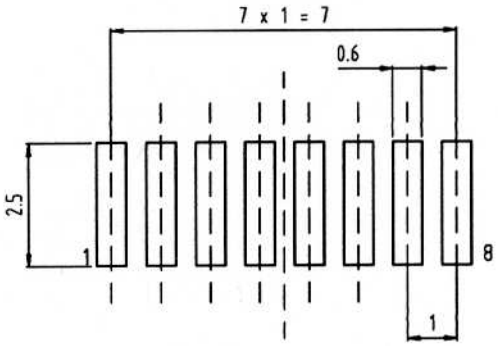
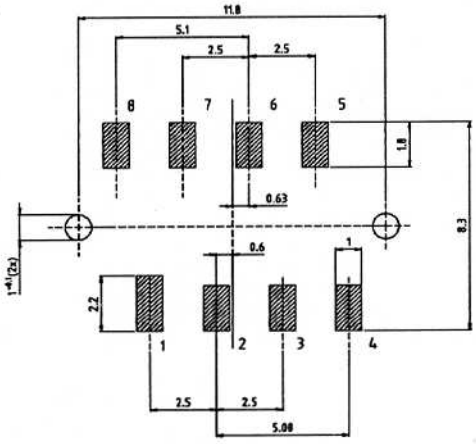
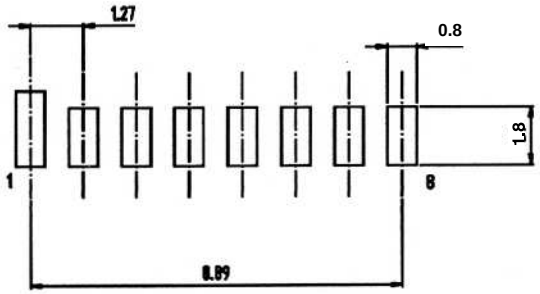
## Recommended SMD Pad Layout[a]




TFDU6100E – BabyFace (Universal) Package




TFDS6500E – Side View Package

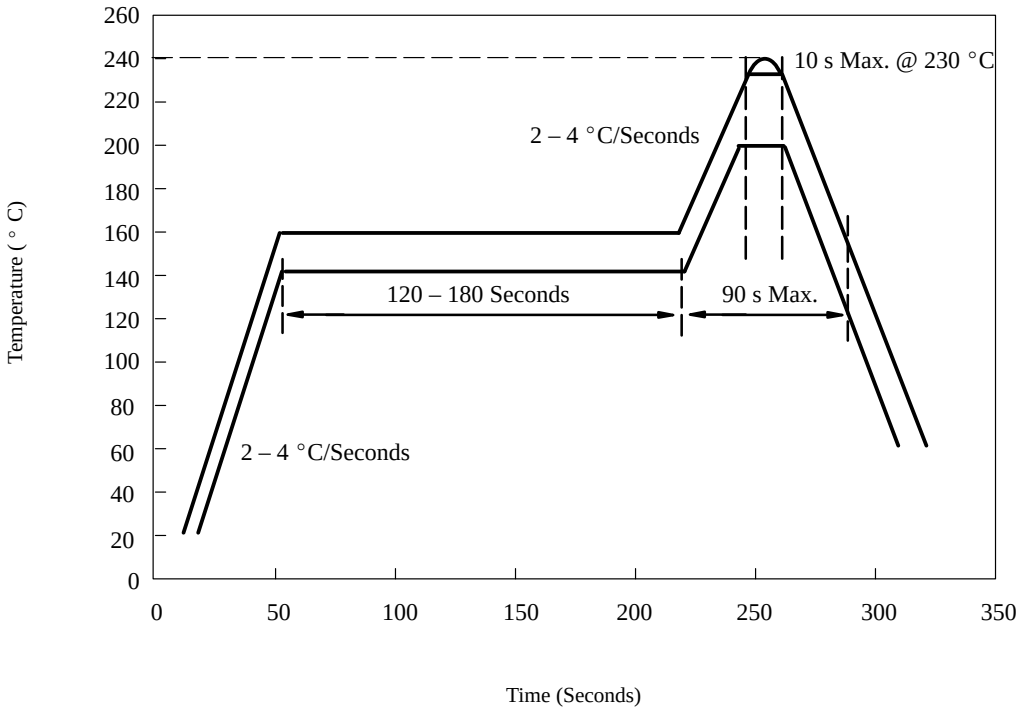



TFDT6500E – Top View Package

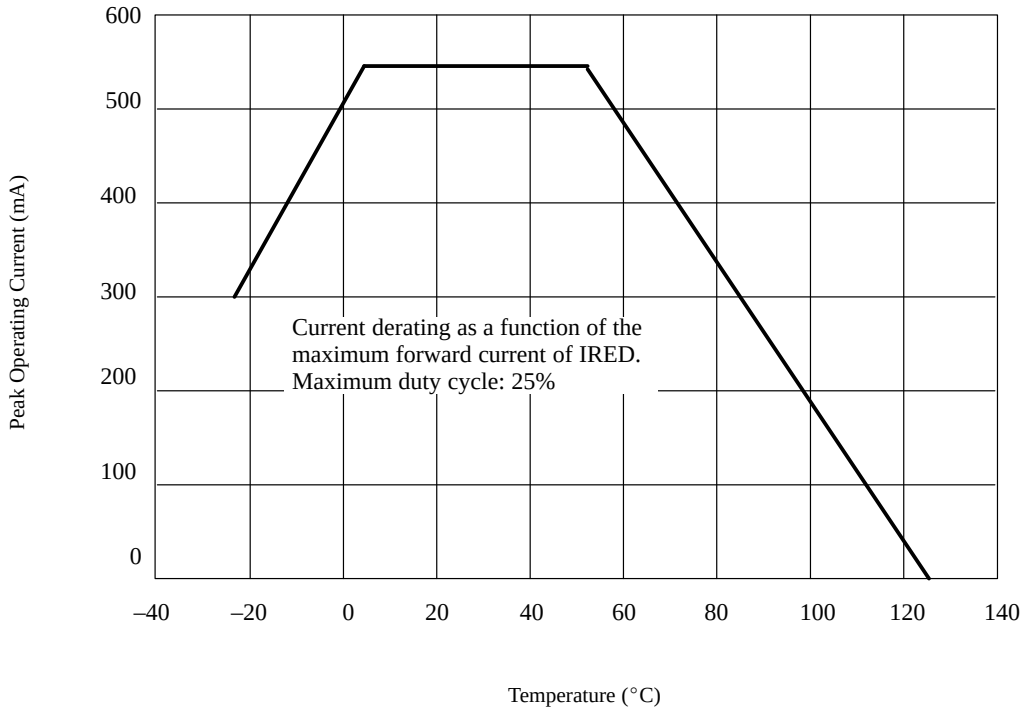
(note: leads of the device should be at least 0.3 mm within the ends of the pads. Pad 1 is longer to designate Pin 1 connection to transceiver.)

a. The leads of the device should be sodered in the center position pads.

## Recommended Solder Profile




## Current Derating Curve



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