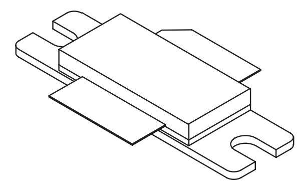
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF187
MRF187R3
MRF187SR3

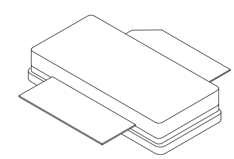
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Guaranteed Performance @ 880 MHz, 26 Volts
  - Output Power — 85 Watts PEP
  - Power Gain — 12 dB
  - Efficiency — 30%
  - Intermodulation Distortion — –28 dBc
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, 880 MHz, 85 Watts CW
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

1.0 GHz, 85 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 465–06, STYLE 1
NI–780
MRF187



CASE 465A–06, STYLE 1
NI–780S
MRF187SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	15	Adc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

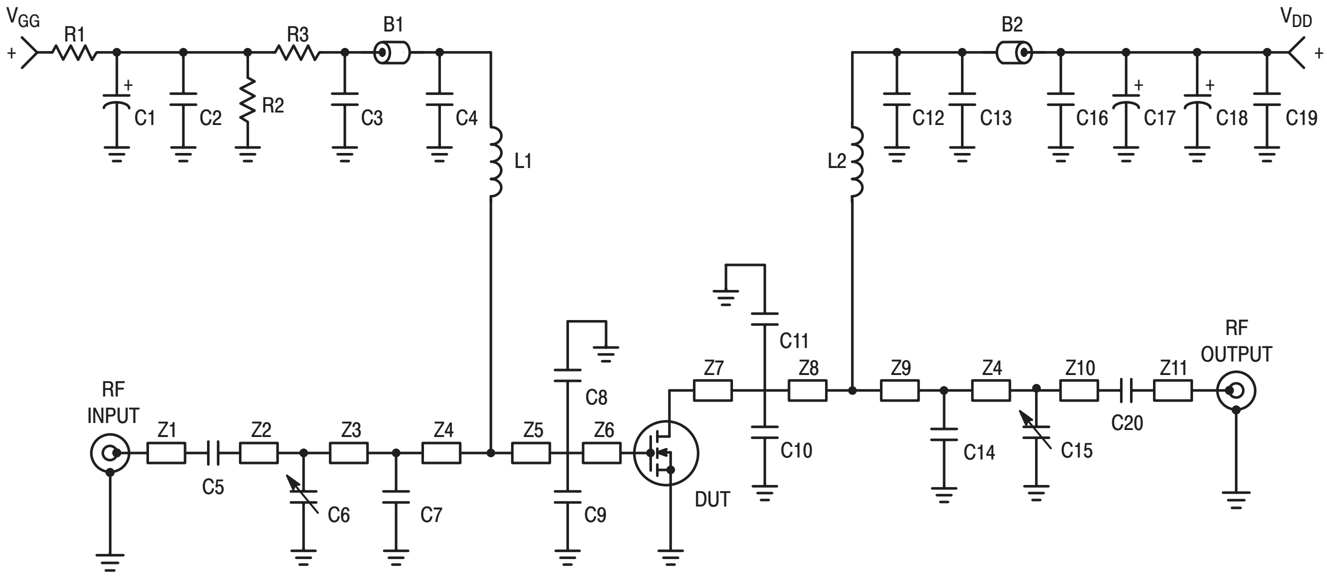
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 550 mAdc)	$V_{GS(Q)}$	3	—	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	0.40	0.55	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Internal Input MOScap) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	295	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	85	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η_D	30	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	9	15	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	η_D	—	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 85 W PEP, I_{DQ} = 550 mA, f1 = 865.0 MHz, f2 = 865.1 MHz and f1 = 895.0 MHz, f2 = 895.1 MHz)	IRL	—	12	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 85 W CW, I_{DQ} = 550 mA, f = 880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			



B1 – B2	Ferrite Bead, Fair Rite, 2743019447	L1, L2	5 Turns, #24 AWG, 0.059″ OD
C1	10 µF, 50 V, Electrolytic Capacitor, ECEV1HV100R Panasonic	R1	12 Ω, 1/4 Watt Carbon
C2, C16	0.10 µF, B Case Chip Capacitors, CDR33BX104AKWS, Kemet	R2	4.7 MΩ, 1/4 Watt Carbon
C3	20000 pF, B Case Chip Capacitor, 200B203MCA50X, ATC	R3	16 kΩ, 1/4 Watt Carbon
C4, C13	100 pF, B Case Chip Capacitors, 100B101JCA500X, ATC	Z1, Z11	0.150″ x 0.220″ Microstrip
C5, C20	47 pF, B Case Chip Capacitors, 100B470JCA500X, ATC	Z2, Z10	0.410″ x 0.220″ Microstrip
C6, C15	0.8 – 8.0 pF, Variable Capacitors, Johanson Gigatrim	Z3	0.160″ x 0.630″ Microstrip
C7	4.7 pF, B Case Chip Capacitor, 100B4R7JCA500X, ATC	Z4	0.160″ x 0.630″ Microstrip
C8, C9	10 pF, B Case Chip Capacitors, 100B100JCA500X, ATC	Z5	0.098″ x 0.630″ Microstrip
C10, C11	16 pF, B Case Chip Capacitors, 100B160JCA500X, ATC	Z6	0.098″ x 0.630″ Microstrip
C12	43 pF, B Case Chip Capacitor, 100B430JCA500X, ATC	Z7	0.210″ x 0.220″ Microstrip
C14	7.5 pF, B Case Chip Capacitor, 100B7R5JCA500X, ATC	Z8	0.050″ x 0.220″ Microstrip
C17, C18, C19	10 µF, 35 V, Electrolytic Capacitors, SMT, Kemet		

Figure 1. MRF187 Schematic

TYPICAL CHARACTERISTICS

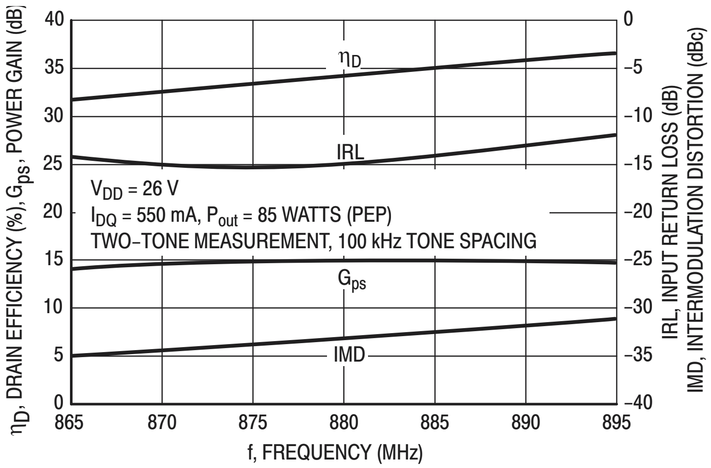


Figure 2. Class AB Broadband Circuit Performance

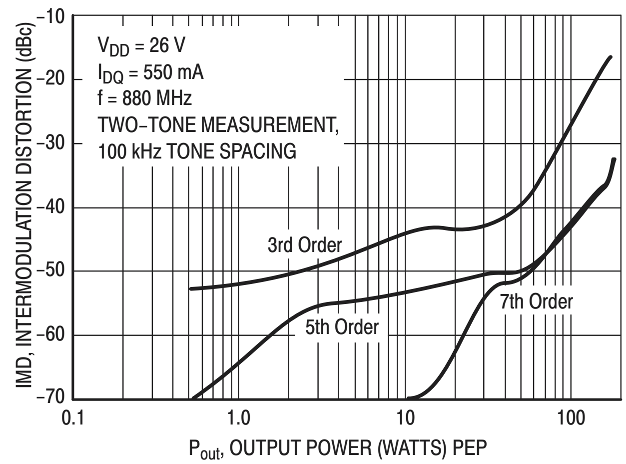


Figure 3. Intermodulation Distortion Products versus Output Power

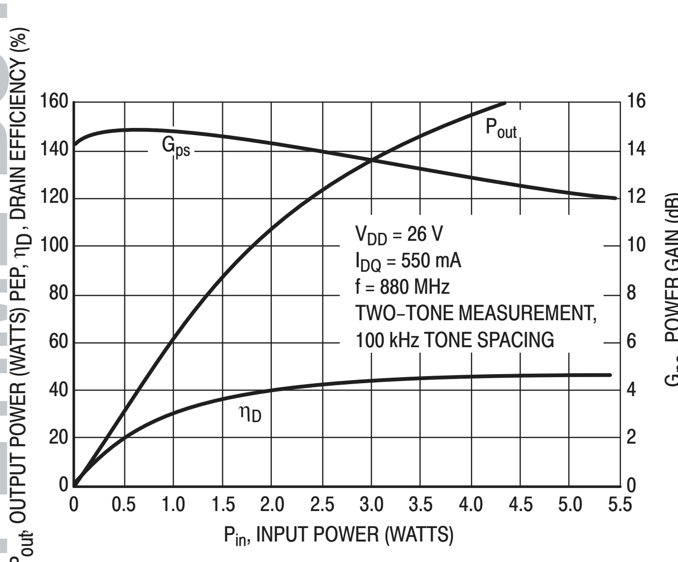


Figure 4. Class AB Parameters versus Input Power

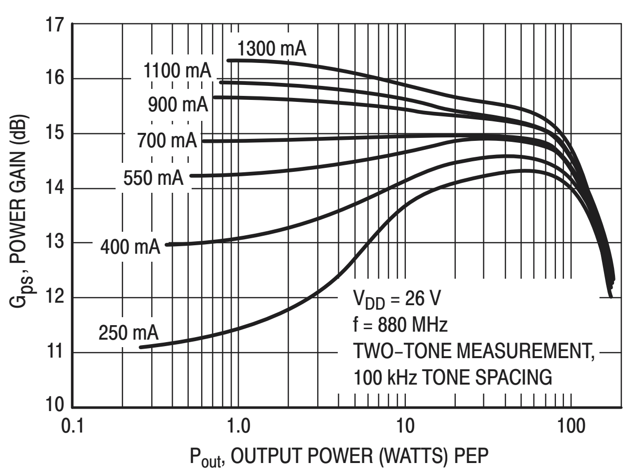


Figure 5. Power Gain versus Output Power

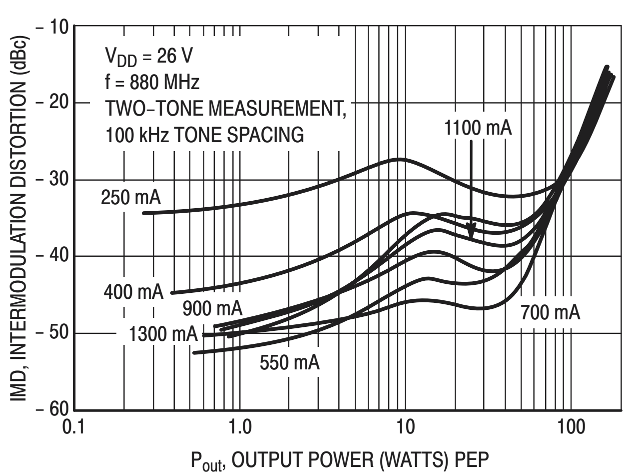
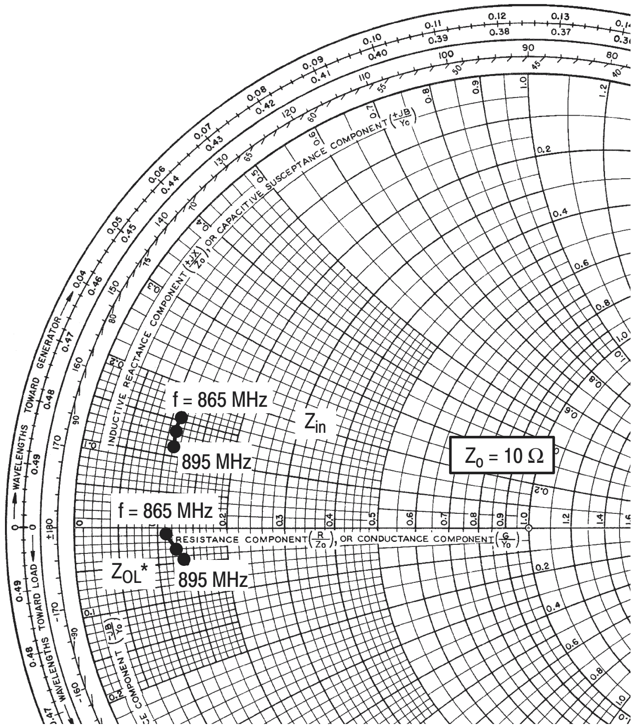


Figure 6. Intermodulation Distortion versus Output Power



V_{CC} = 26 V, I_{DQ} = 550 mA, P_{out} = 85 W PEP

f MHz	Z_{in} Ω	Z_{OL}* Ω
865	1.04 + j1.51	1.13 – j0.091
880	1.03 + j1.39	1.20 – j0.176
895	1.03 + j1.29	1.28 – j0.242

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 7. Series Equivalent Input and Output Impedance

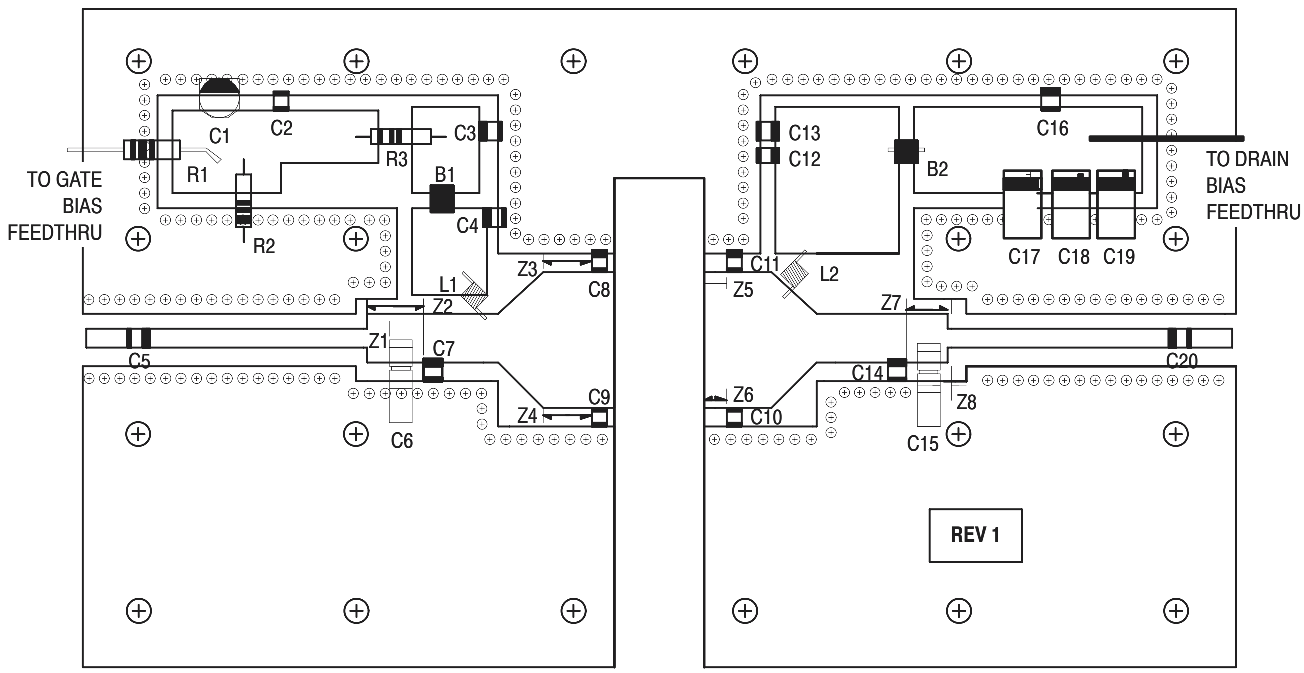
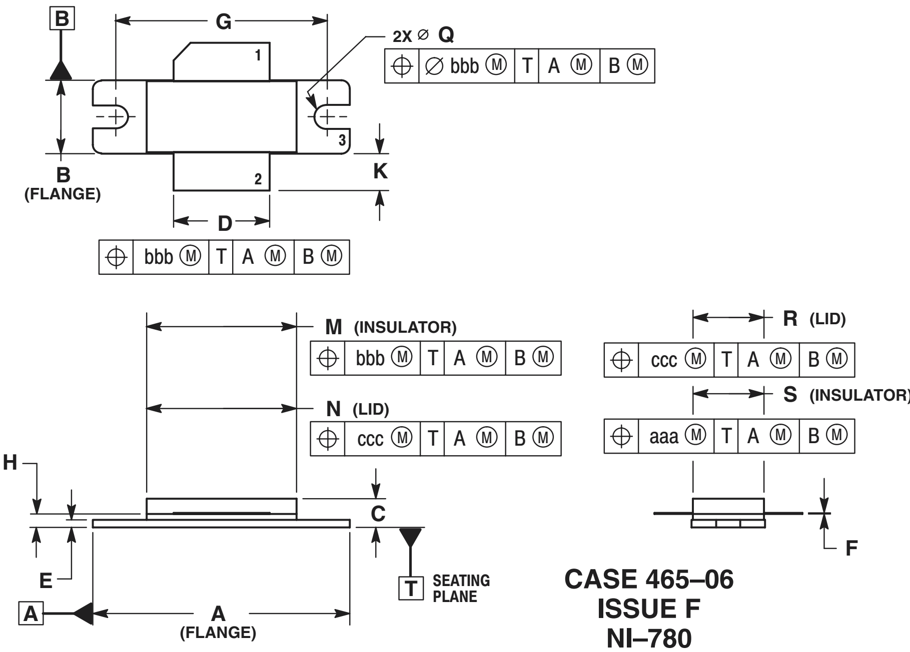


Figure 8. MRF187 Populated PC Board Layout Diagram

PACKAGE DIMENSIONS

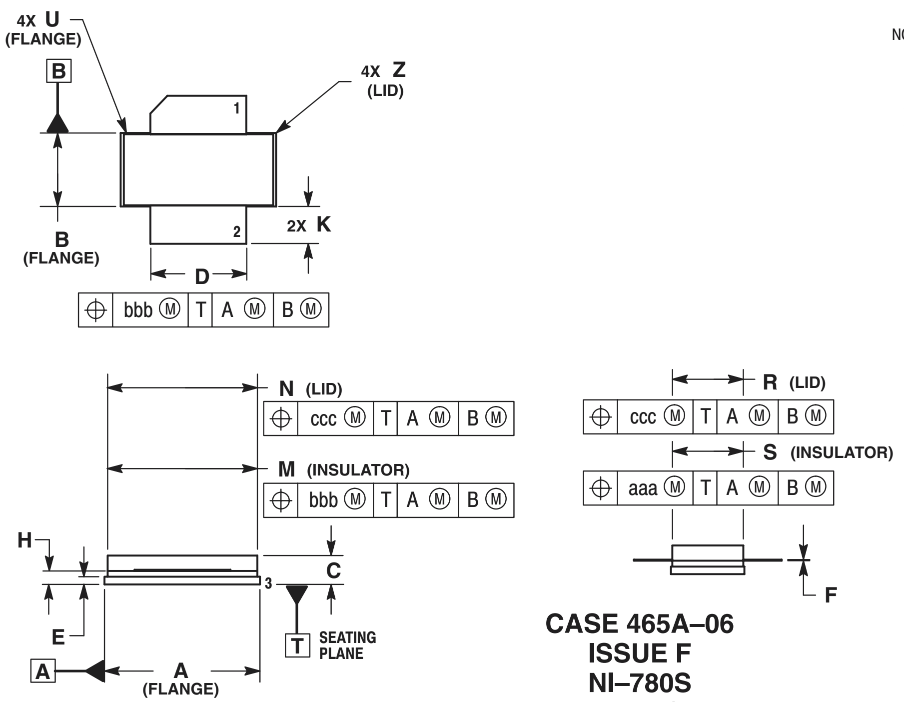


CASE 465–06
ISSUE F
NI–780
MRF187

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



CASE 465A–06
ISSUE F
NI–780S
MRF187SR3

NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

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