DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4517B
LSI
Dual 64-bit static shift register

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

Dual 64-bit static shift register

HEF4517B
LSI

DESCRIPTION

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (CP), data input (D), parallel input-enable/output-enable (PE/$\overline{EO}$) and four 3-state outputs of the 16th, 32nd, 48th and 64th bit positions (O_{16} to O_{64}). Data at the D input is entered into the first bit on the LOW to HIGH transition of the clock, regardless of the state of PE/$\overline{EO}$.

When PE/$\overline{EO}$ is LOW the outputs are enabled and the device is in the 64-bit serial mode.

When PE/$\overline{EO}$ is HIGH the outputs are disabled (high impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with D, O_{16}, O_{32} and O_{48} as data inputs of the 1st, 17th, 33rd, and 49th bit respectively. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

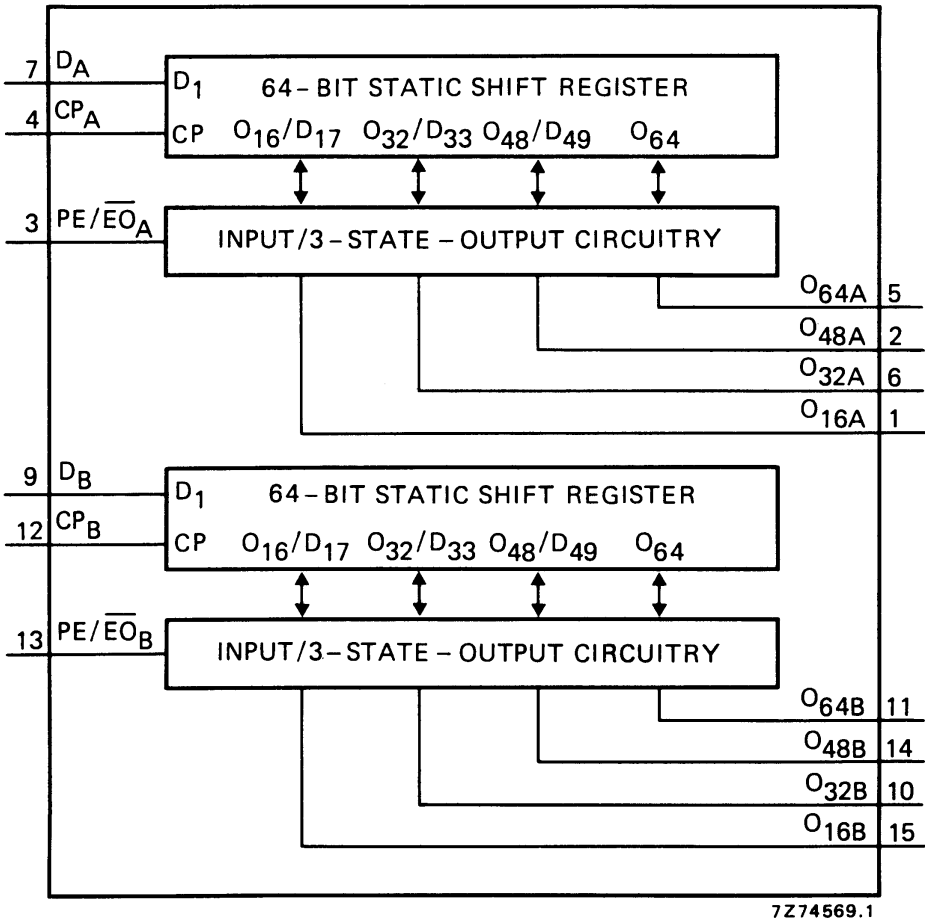

Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

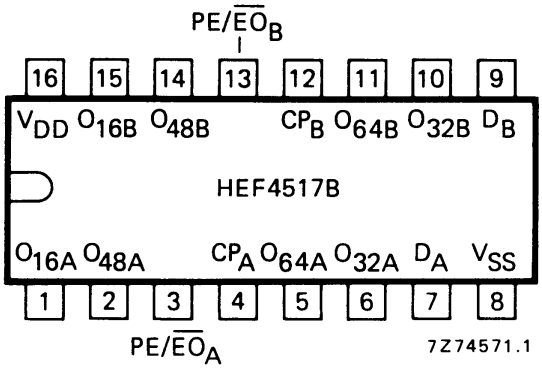

Fig.2 Pinning diagram.

HEF4517BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4517BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4517BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

CP_A, CP_B	clock inputs
PE/$\overline{EO}_A$, PE/$\overline{EO}_B$	parallel input-enable/output-enable inputs
D_A, D_B	data inputs
O_{16A}, O_{32A}, O_{48A}	3-state outputs/inputs
O_{16B}, O_{32B}, O_{48B}	3-state outputs/inputs
O_{64A}, O_{64B}	3-state outputs

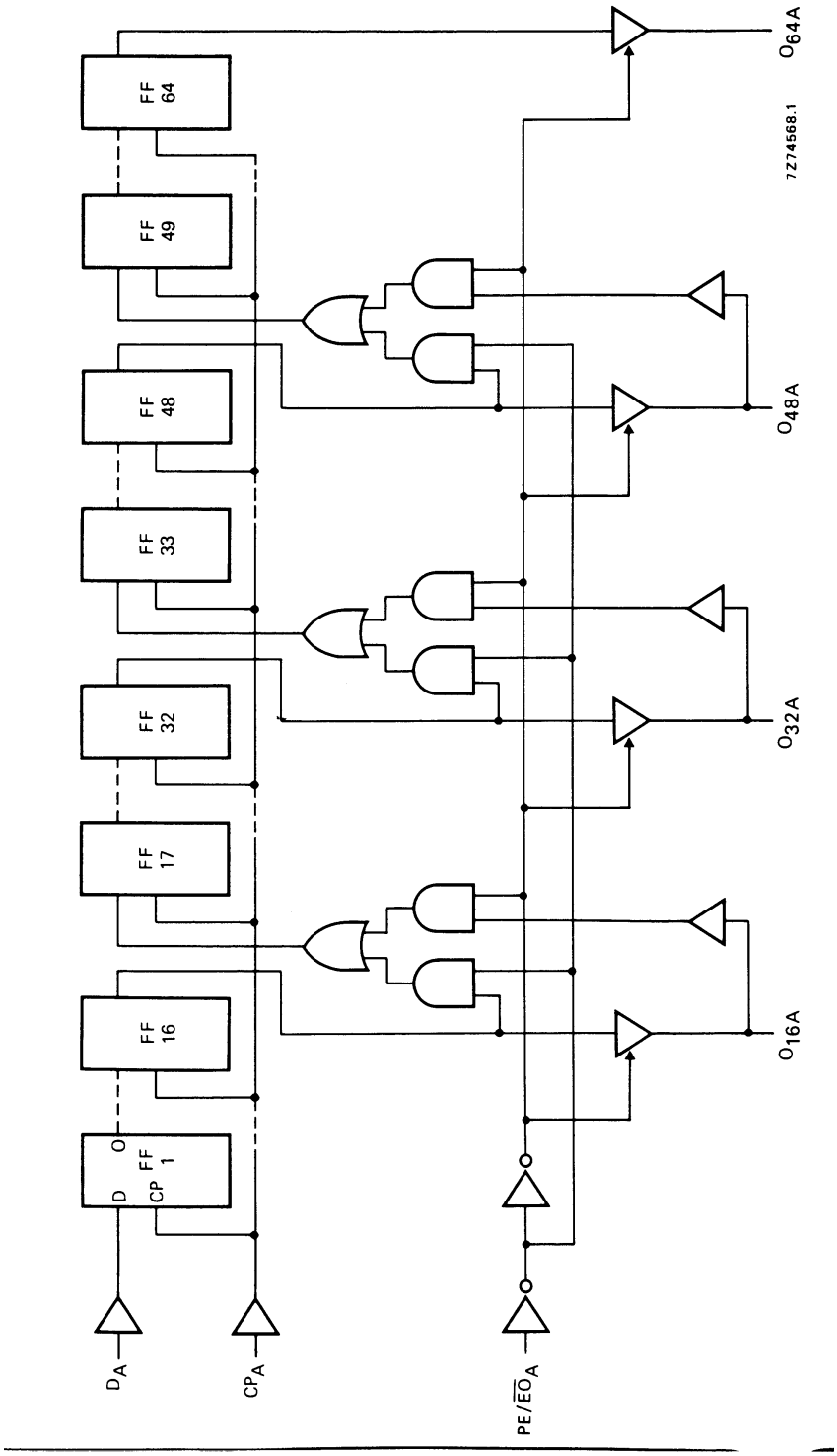

Fig.3 Logic diagram (one shift register).

FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS				MODE
CP	D	PE/$\overline{EO}$	O_{16}	O_{32}	O_{48}	O_{64}	
↗	data entered into 1st bit	L	content of 16th bit displayed	content of 32nd bit displayed	content of 48th bit displayed	content of 64th bit displayed	One 64-bit shift register. The content of the shift register is shifted over one stage
↗	data entered into 1st bit	H	data at O_{16} entered into 17th bit	data at O_{32} entered into 33rd bit	data at O_{48} entered into 49th bit	remains in 'Z' state	Four 16-bit shift register. The content of the shift registers is shifted over one stage.
↘	X	L	no change	no change	no change	no change	no change
↘	X	H	Z	Z	Z	Z	no change

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance state
   ↗ = positive-going transition
   ↘ = negative-going transition

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$7\,000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	where
	10	$28\,000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$70\,000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CP → O_n	5			220	440	ns	193 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Minimum clock pulse width; LOW	5	t_{WCPL}		95	190	ns	see also waveforms Fig.4.
	10			40	80	ns	
	15			30	60	ns	
Set-up times O_n, D → CP	5	t_{su}	30	10		ns	
	10		25	5		ns	
	15		20	5		ns	
Hold time O_n, D → CP	5	t_{hold}	45	15		ns	
	10		30	10		ns	
	15		25	10		ns	
3-state propagation delays							
Output disable times							
PE/$\overline{EO}$ → O_n HIGH	5	t_{PHZ}		40	80	ns	
	10			30	60	ns	
	15			25	50	ns	
LOW	5	t_{PLZ}		50	100	ns	
	10			30	60	ns	
	15			25	50	ns	
Output enable times							
PE/$\overline{EO}$ → O_n HIGH	5	t_{PZH}		45	90	ns	
	10			25	50	ns	
	15			20	40	ns	
LOW	5	t_{PZL}		60	120	ns	
	10			30	60	ns	
	15			25	50	ns	
Maximum clock pulse frequency	5	f_{max}	2	5		MHz	
	10		6	12		MHz	
	15		8	16		MHz	

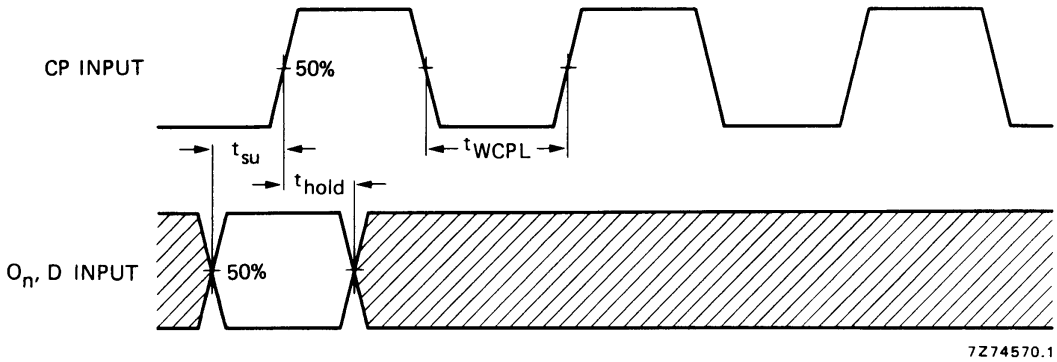

Fig.4 Waveforms showing minimum clock pulse width, set-up and hold times for O_n (as data input) and D to CP.