MOTOROLA

MCVVQ111AFB

Product Preview

VirtuoVue Monochrome Video Display Driver

VirtuoVue Monochrome Video Display

The MCVVQ111AFB VirtuoVue Monochrome Video Display is designed to accept a standard monochrome video signal (525 or 625 lines), and convert it for display on the CyberDisplay320 LCD Display Panel.

The MCVVQ111AFB provides all necessary power supply voltages to the display panel by means of a voltage regulator. The input video signal is converted to appropriate differential video signals required by the LCD display panel. A separate OSD input is provided.

An on-board sync separator, PLL, and logic control section generate the appropriate horizontal and vertical timing signals for the LCD panel. Horizontal and vertical sync outputs are provided.

The MCVVQ111AFB is designed to operate under two input voltages: one is from 2.7 to 5.5 volts ,and the other is 11 volts, A Sleep mode can be set to reduce power consumption.

- •Support 525 and 625 line monochrome systems
- •Separate input pin for OSD signals (OSD overlay).
- •Integrated Voltage regulator provides all necessary voltages for the LCD display panel
- •Internal sync separator, PLL, and logic provide all necessary timing signals to the LCD display panel.
- •Control pins to adjust video black level, gain.
- •Gamma Bias pin to adjust the video output characteristics
- •Supplies required: 2.7 to 5.5 volts DC, 11 volts DC
- •Sleep mode for power conservation.
- •Operating ambient temperature range: -20 to 70^{o}C.
- •Surface mount package.

FB SUFFIX
PLASTIC PACKAGE
CASE 932-02
(LQFP-48)
Package $R\theta_{jA}$=88^{o}C/W (typ)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCVVQ111AFB	-20^{o}C - 70^{o}C	LQFP-48

SIMPLIFIED SYSTEM DIAGRAM

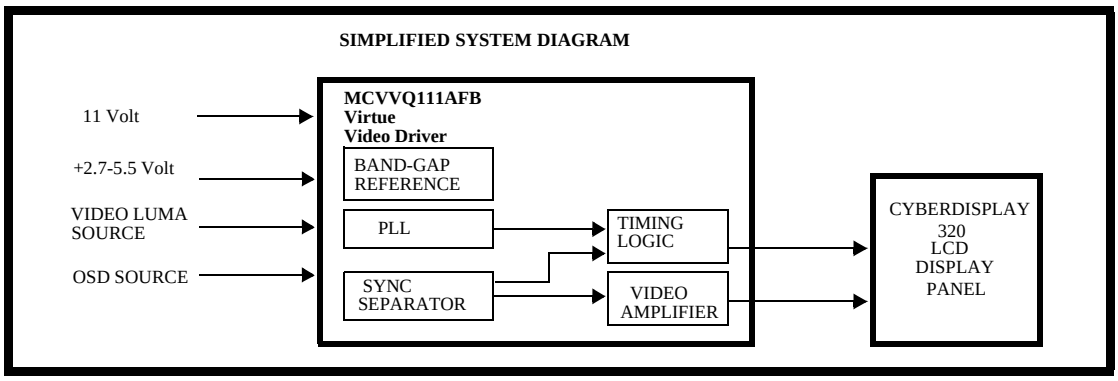
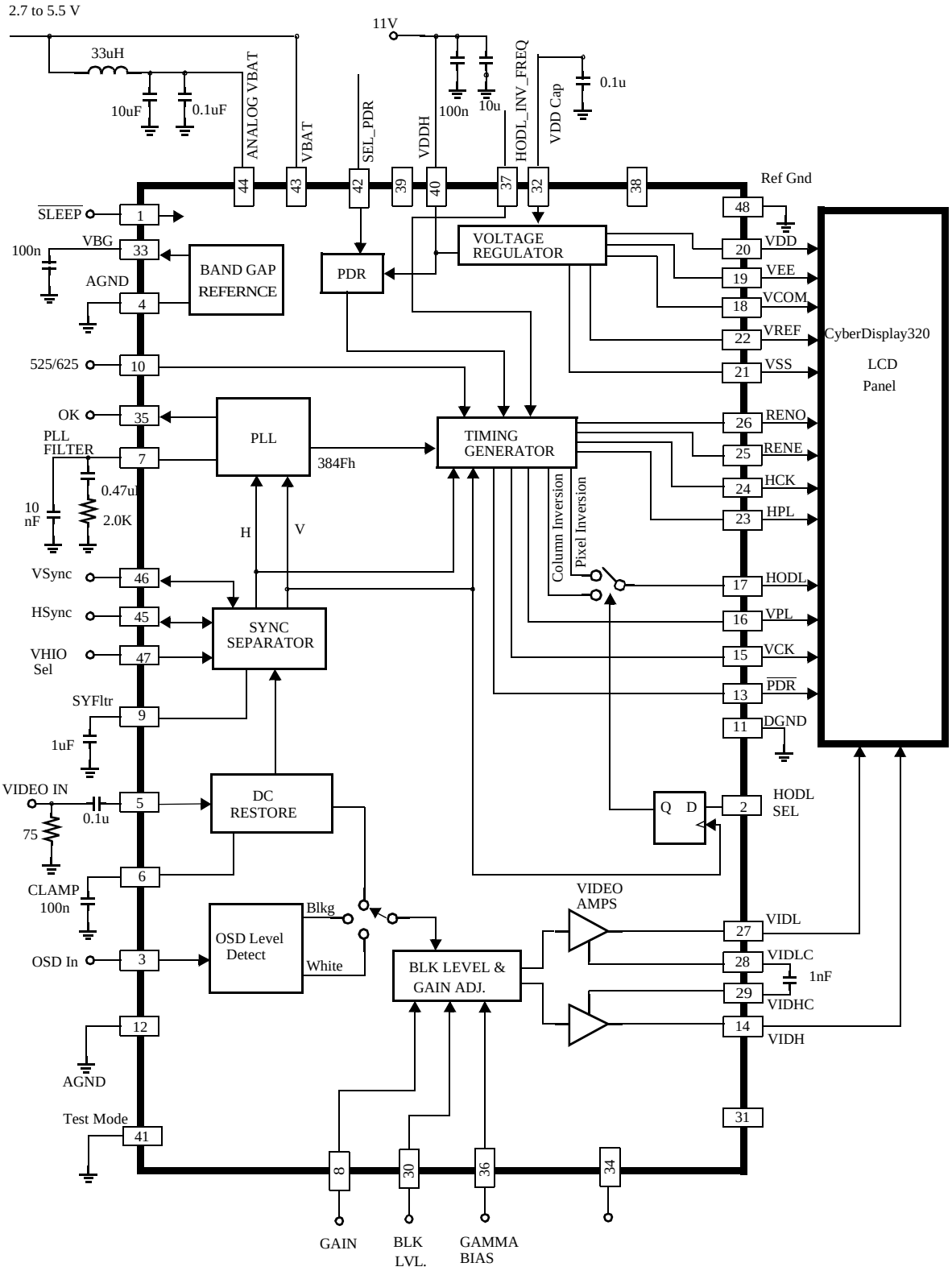


Figure 1 Block Diagram



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage 1	VBat	-0.5,+6.0	Vdc
Power Supply Voltage 2	VDDH	13	Vdc
Maximum Junction Temperature	T_j	+150	^oC
Storage Temperature	Tstg	-65,+150	^oC
Package Thermal Conductivity	$R\theta_{jA}$	88(typ)	$^oC/W$

Devices should not be operated at these limits. The "Recommended Operating Conditions" provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Vbat	2.7	-	5.5	Vdc
Video Signal Input Level (composite video - Luma)	Vvid	-	1.0	-	Vp-p
OSD Input Levels	Vosd	0	-	VBat	Volt
Logic Input Levels (Pins 1, 2, 10,47,37,42)	Vin	0	-	VBat	Volt
Gain Control (Pin 8)	VGC	1.25	-	2.5	Volt
Black Level Control(Pin 30)	VBL	2.0	-	3.0	Volt
Gamma Bias (Pin 36)	VGA	0.5	-	1.5	Volt
External VDDH Supply	VDDH	10.7	11	11.3	Volt
Operating Ambient Temperature	Ta	-20	-	70	^oC

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (All parameters are specified at Ta=25^{o}C, Pin 1 = High unless noted)

Fh stand for line frequency. Fh = 15750Hz in 525/60 system and Fh = 15625Hz in 625/50 system

Parameter	Min	Typ	Max	Unit
POWER SUPPLIES (TO BE UPDATED)				
Supply Current into VBat(Pin 43 and Pin 44) Pins 13-27 open, Pin 1 = High, VBat=5 Volt	-	10	15.5	mA
Supply Current into VBat(Pin 43 and Pin 44), Sleep Mode Pins 13-27 open, Pin 1 = Low, VBat=3.3Volts	-	100	-	uA
Supply Current into VDDH	-	9	18	mA
Power Consumption, VBat=5.0v VDDH= 11.0v	-	149	275.5	mW
DISPLAY OUTPUT VOLTAGES (voltages referenced to VSS)				
VDD (source 1.4mA)	8.5	+9.0	9.5	Volt
VEE (sink 1mA)	1.9	+2.0	2.1	Volt
VCOM (source 2mA)	5.55	+5.8	6.15	Volt

ELECTRICAL CHARACTERISTICS (All parameters are specified at Ta=25°C, Pin 1 = High unless noted)
Fh stand for line frequency. Fh = 15750Hz in 525/60 system and Fh = 15625Hz in 625/50 system

Parameter	Min	Typ	Max	Unit
VREF (source 10uA)	-	VBat/2	-	Volt
VBG Bandgap voltage(Pin 33)	1.185	1.25	1.3	Volt
PLL / SYNC SEPARATOR				
Pixel Clock Oscillator center frequency(Pin 5 = Open)	-	6.0	-	MHz
PLL Lock Range (Horizontal Frequency)	14.175		17.1875	KHz
OSD INPUT				
Black Threshold	-	0.75	1.00	Volt
White Threshold	-	2.25	2.70	Volt
LOGIC INPUT (Pin: 1, 2, 10, 47)				
Maximum logic LOW input level	-	-	0.33xVbat	Volt
Minimum logic HIGH input level	0.66xVbat	-	-	Volt
Input Impedance		600K to AGND		Ohm
HSYNC, VSYNC INPUT/OUTPUT				
Input Impedance (Pin 47 connect to VBat)	-	47K to VBat	-	Ohm
Input Threshold (Pin 47 connect to VBat, -ve sync input)		1.25		Volt
Equivalent Output Impedance (Pin 47 connect to GND)	-	90	-	Ohm
TIMING LOGIC OUTPUT (Pin: 13, 15, 16, 17, 23, 24, 25, 26)				
Equivalent Output Impedance	-	90	-	Ohm
External Capacitive Loading for Logic Timing Signals			20	pF
Logic Output Level High	VBat -0.5	-	-	Volt
Logic Output Level Low	-	-	0.45	Volt
ANALOG VIDEO DRIVER (VIDL, VIDH)				
External Capacitive Loading for VIDL & VIDH			85	pF
VIDEO AMPLIFIER CHARACTERISTIC				
Video Output Amplitude (pin36 open, pin30 connect to pin19<Vee>, pin8 <Gain> set to 2.25V, measured from black level to output peak 80pF capacitive loading.			3.1	V
Gain Control Range (pin36 open, pin30 connect to pin19<Vee>, pin8<Gain> set between 1.25 to 2.5, output attenuation with respect to maximum output amplitude)		-7		dB
Gamma Control Range (pin8 set to 1.5V, pin30 connect to pin19<Vee>, pin36 set to 0.5 - minimum gamma, with 100mV video content or 10% IRE video input level, measure VIDL output amplitude with respect to black level, external VDDH at 11V)	0.2	-	0.4	Volt
Gamma Control Range (pin8 set to 1.5V, pin30 connect to pin19<Vee>, pin36 set to 1.5 - maximum gamma, with 100mV video content or 10% IRE video input level, measure VIDL output amplitude with respect to black level, external VDDH at 11V)	1.3	-	1.7	Volt
Black Level Control Range (pin30<BLK LVL> set at 2 volt measure VIDL output black level voltage.	1.9	-	2.1	Volt

ELECTRICAL CHARACTERISTICS (All parameters are specified at Ta=25°C, Pin 1 = High unless noted)
Fh stand for line frequency. Fh = 15750Hz in 525/60 system and Fh = 15625Hz in 625/50 system

Parameter	Min	Typ	Max	Unit
Black Level Control Range (pin30<BLK LVL> set at 3 volt measure VIDL output black level voltage.	2.9	-	3.1	Volt

Note: Gain, GAMMA-BIAS & BLACK LEVEL are interrelated control, control range may be different at different combination of those setting.

TIMING CHARACTERISTICS (Ta=+25°C)

Note: MCVVQ111AFB is design to work in conjunction with *CyberDisplay* 320 Monochrome Display, all timing output are expected to fulfill the minimum timing requirement stated at *CyberDisplay* 320 Monochrome specification table 2-5, revision "2/13, 1998 " when operate under standard video mode NTSC/PAL.

DISPLAY PANEL TIMING (Fh=15750Hz, 525/60 system, Figure 8-9)

Parameter	Symbol	Min	Typ	Max	Unit
VPL start at	t1	-	line 19	-	-
VPL setup time (VPL start to VCK start)	t2	140	496.5	-	nS
HPL setup time		40	-	-	nS
VCK low time	t3	-	496.5	-	nS
HPL low time	t4	-	165.5	-	nS
HCK Cycle time	t5	-	165.5	-	nS
HPL end to RENE start time	t6	-	827.5	-	nS
RENE low time	t7	-	54.95	-	uS
HPL end to RENO start time	t8	-	827.5	-	nS
RENO low time	t9	-	54.95	-	uS

DISPLAY PANEL TIMING (Fh=15625Hz, 625/50 system, Figure 8-9)

Parameter	Symbol	Min	Typ	Max	Unit
VPL starts at	t1	-	line 23	-	-
VPL setup time (VPL start to VCK start)	t2	140	500	-	nS
HPL setup time		40	-	-	nS
VCK low time	t3	-	500	-	nS
HPL low time	t4	-	166.67	-	nS
HCK Cycle time	t5	-	166.67	-	nS
HPL end to RENE start time	t6	-	833.35	-	nS
RENE low time	t7	-	55.33	-	uS
HPL end to RENO start time	t8	-	833.35	-	nS
RENO low time	t9	-	55.33	-	uS

SYSTEM TIMING

Parameter	Min	Typ	Max	Unit
PDR rising edge after SLEEP rising edge	-	333(NTSC) 400(PAL)	-	mS

SYSTEM TIMING

Parameter	Min	Typ	Max	Unit
PDR falling edge after SLEEP falling edge	-	10	-	nS

PIN DESCRIPTION

Pin No	Pin Name	Description
1	$\overline{\text{SLEEP}}$	Logic level input. A logic low sets the IC into the sleep mode. Internal 500K pull-down provided.
2	HODL Select	Used for HODL selection. Logic 1: column inversion output on HODL for ABNORMAL video (such as cue/review/pause mode) Logic 0: pixel inversion output on HODL for NORMAL video Also refer the description of pin 37
3	OSD In	Input for the OSD signals. See text for required signal levels.
4,12	AGND	Ground for the PLL section.
5	Video Input	Input for standard level monochrome video,525 or 625 lines. Source impedance must be less than 500.
6	Clamp	Clamp capacitor, to ground, for the video black level clamp.
7	PLL Filter	Filter pin for the internal horizontal PLL.
8	Gain	DC control for the gain of the video signal path. Adjustment range is +/- 3.5dB.
9	SYFltr	Filter pin for the sync separator. Capacitor to ground is required.
10	525/625	Set low if the input video is a 525 line system (NTSC). Set high for 625 line systems. Internal 500K pull-down provided.
11	DGND	Ground for the digital sections and signals.
13	$\overline{\text{PDR}}$	Power Down reset output to the LCD panel. Active low.
14	VIDH	Upper video drive signal to the LCD panel.
15	VCK	Vck control signal to the LCD panel.
16	VPL	Vertical start pulse output to the LCD panel.
17	HODL	Inversion control output to the LCD panel.
18	VCOM	Internally generated supply for the LCD panel. Nominally +5.8 volts.
19	VEE	Internally generated supply for the LCD panel. Nominally +2.0 volts.
20	VDD	Internally generated supply for the LCD panel. Nominally +9.0 volts.
21	VSS	Reference ground for the LCD panel.
22	VREF	Internally generated supply for the LCD panel. Nominally VBat/2.
23	HPL	Horizontal start pulse output to the LCD panel.
24	HCK	Horizontal clock output to the LCD panel.
25	RENE	Even Row Enable output to the LCD panel.
26	RENO	Odd Row Enable output to the LCD panel.
27	VIDL	Lower video drive signal to the LCD panel.
28	VIDLC	Connect to VIDHC through a compensation capacitor.
29	VIDHC	Connect to VIDLC through a compensation capacitor,
30	Black Level	DC Control to adjust the video output black level for normal video and OSD signals.
31	N/C	Not connected

PIN DESCRIPTION

Pin No	Pin Name	Description
32	VDD Cap	Connect the decoupling capacitor (0.1uF) for VDD
33	VBG	Output of the bandgap reference. External capacitor may be required.
34	N/C	Not connected
35	OK	For test only. Output indicating the video horizontal freq is within the PLL pull-in range. If PLL is not locked, OK will be set to HIGH.
36	Gamma-bias	Adjust the characteristics of the video output.
37	HODL_INV_FREQ	Select the switching frequency of HODL polarity to either VF/4 (when the pin is set to high) or VF/2(when the pin is set to low. It is the default state). VF is the vertical frequency. This setting applies to both pixel inversion mode and column inversion mode. Refer the description of HODL section for the switching frequencies under NTSC and PAL modes.
38	N/C	Not connected
39	N/C	Not connected
40	VDDH	Power supply input. Voltage range is from 10.7V to 11.3V
41	Test Mode	Used in test mode. It must be connected to ground during normal operation.
42	SEL_PDR	During normal operation, select either scheme 1 or scheme 2. Logic high: scheme 1 is selected. When PDR is asserted during VBlanking, no RENE/RENO pulses will be generated. Logic low: scheme 2 is selected. When PDR is asserted during VBlanking, 3 RENE/RENO pulses will be generated. The default state is logic low.
43	VBat	Power Supply Input. Voltage range is +2.7 to +5.5 volts, and must be within 0.5 volt of pin 44.
44	Analog VBat	Power Supply Input. Voltage range is +2.7 to +5.5 volts, and must be within 0.5 volt of pin 43. This pin powers the PLL,and other noise sensitive sections.
45	HSync	H Sync output of the Sync Separator, or an H Sync input from an external source. Internal 50K pull-up provided.
46	VSync	V Sync output of the Sync Separator, or a V Sync input from an external source. Internal 50K pull-up provided.
47	VH IO Sel	Input. When low, pins 45 & 46 are outputs. When high, pins 45 & 46 are inputs.
48	Ref Gnd.	Ground for the analog sections and signals except for PLL section

Figure 2-Black Level Adjustment

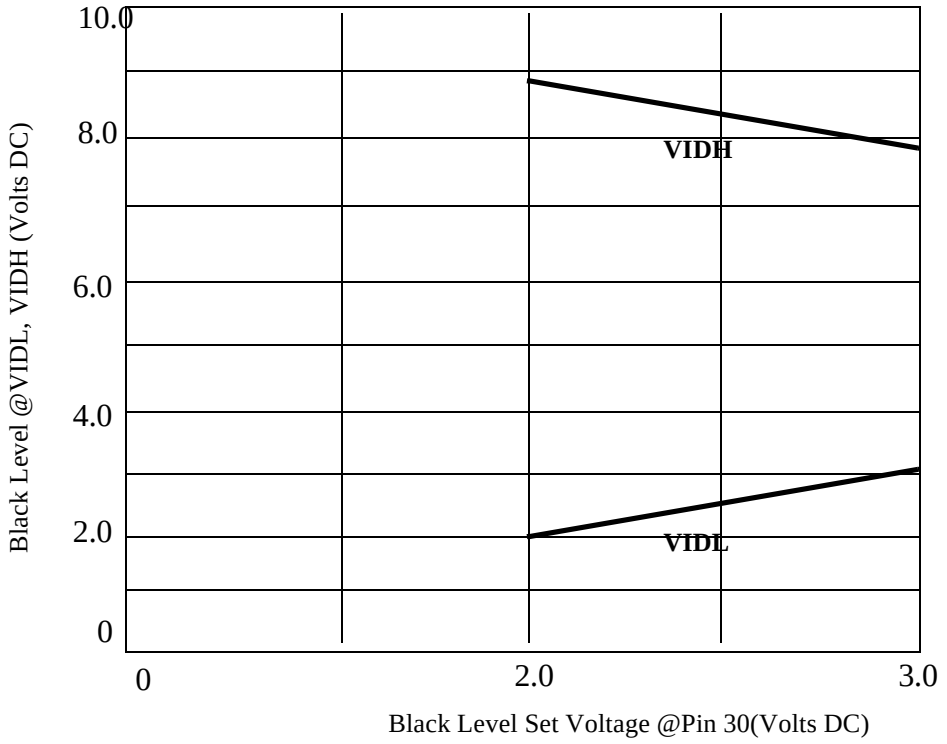


Figure 3 - Gain Adjustment (For 1 Volt video input, Gamma bias was adjusted for a linear characteristic)

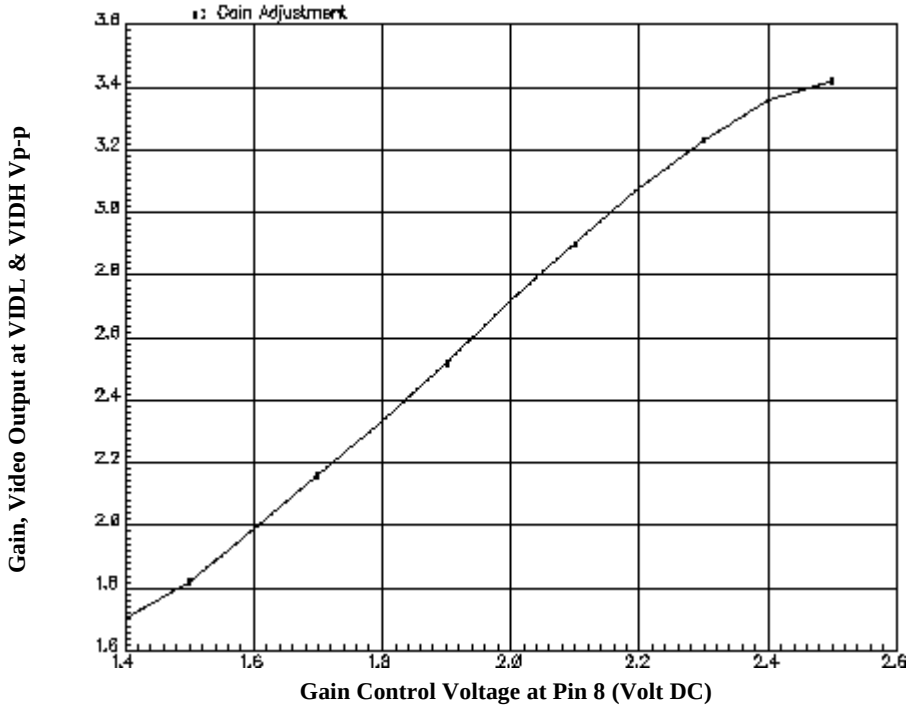


Figure 4 - Horizontal Sync Timing

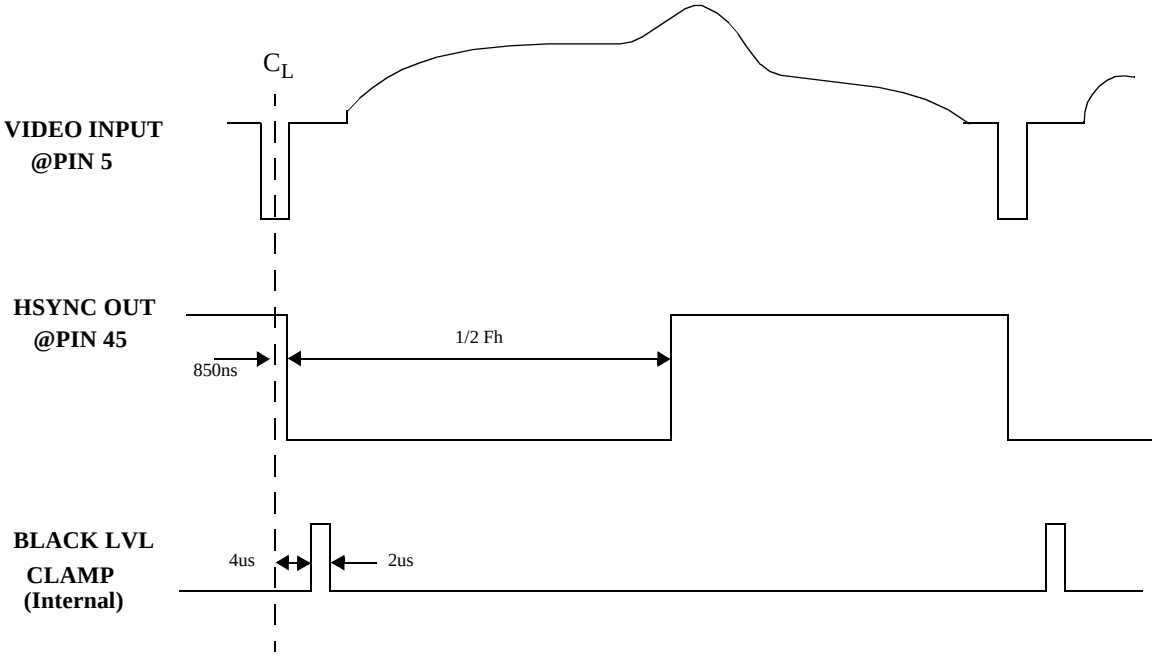


Figure 5 - VSync Output

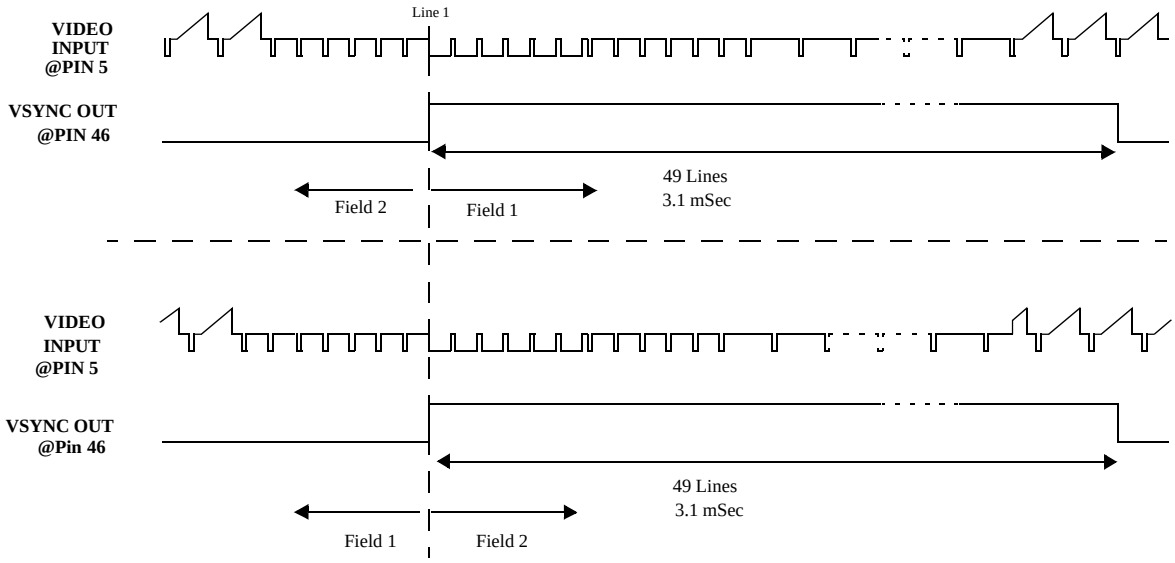


Figure 6 - LCD Panel Supply Voltages

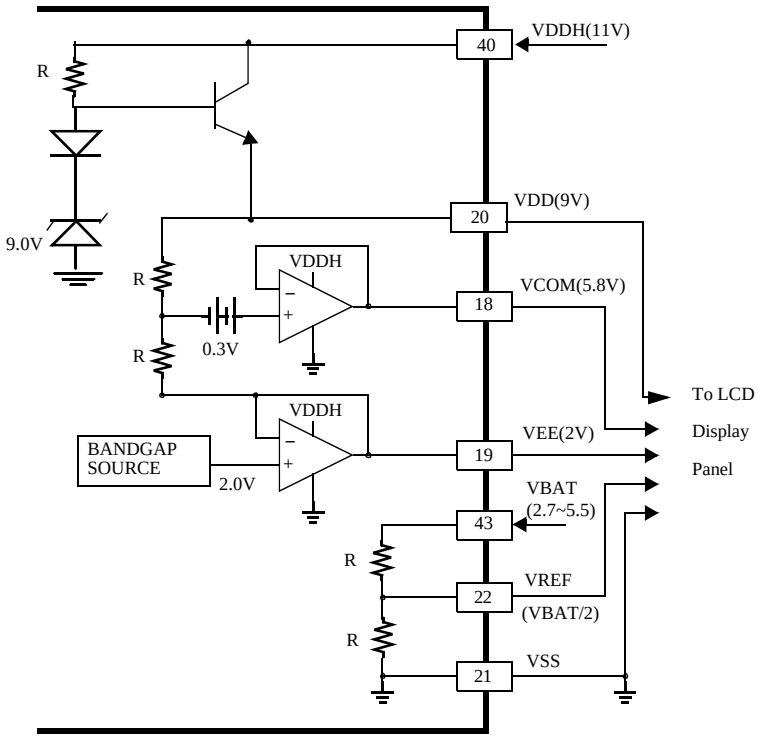
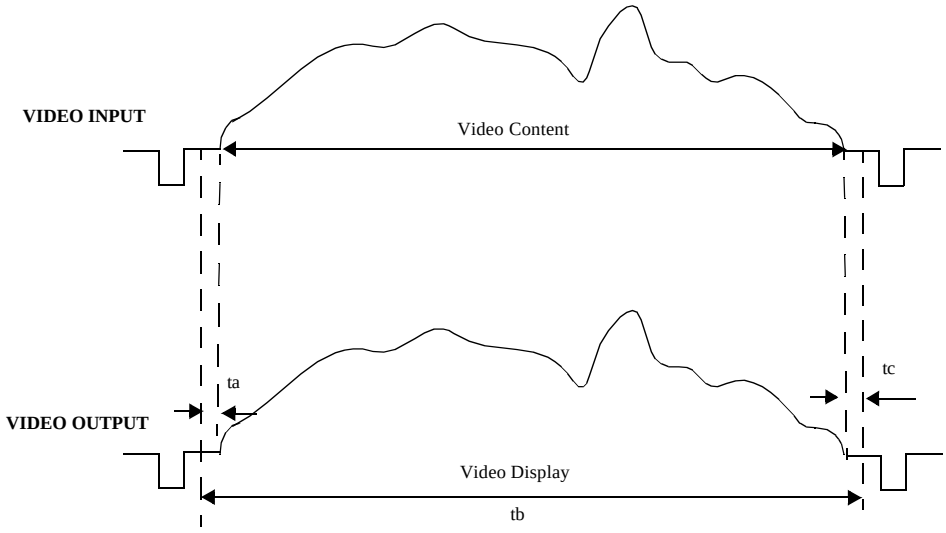


Figure 7 - Video Display vs. Video Input



VIDEO INPUT	1/Fh	HCK	ta	tb	tc	% of video Displayed
525/60	63.5uS	6.05 MHz	0.367uS	53.27uS	0.367uS	101.4%
625/50	64uS	6 MHz	0.364uS	52.73uS	0.364uS	101.4%

Figure 8 - LCD Panel Vertical & Horizontal Timing

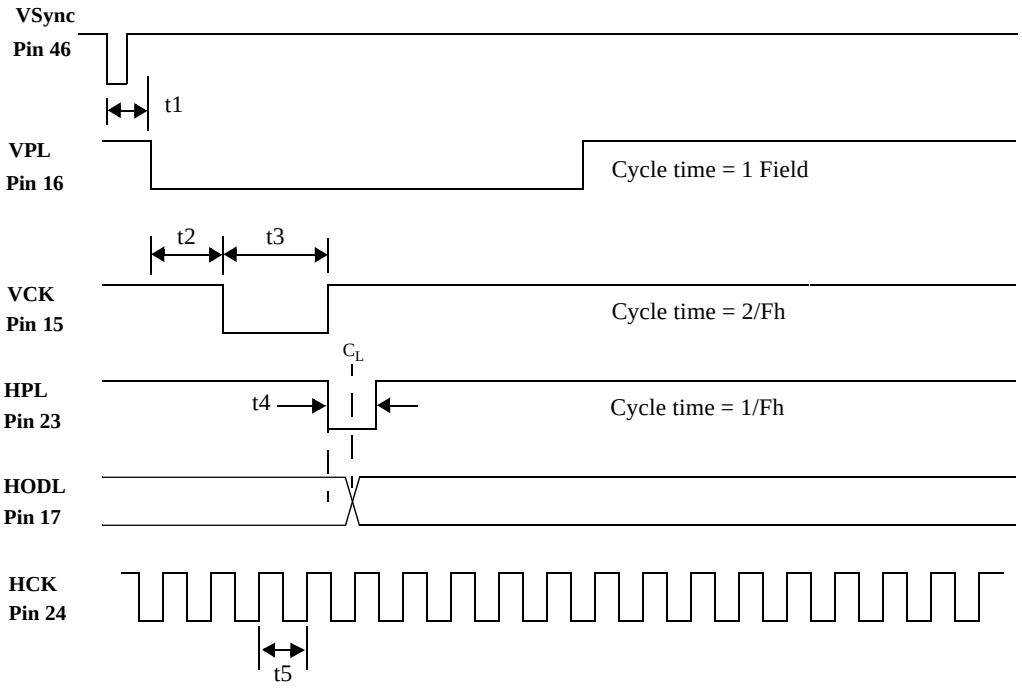


Figure 9 - LCD Panel Active Video Timing

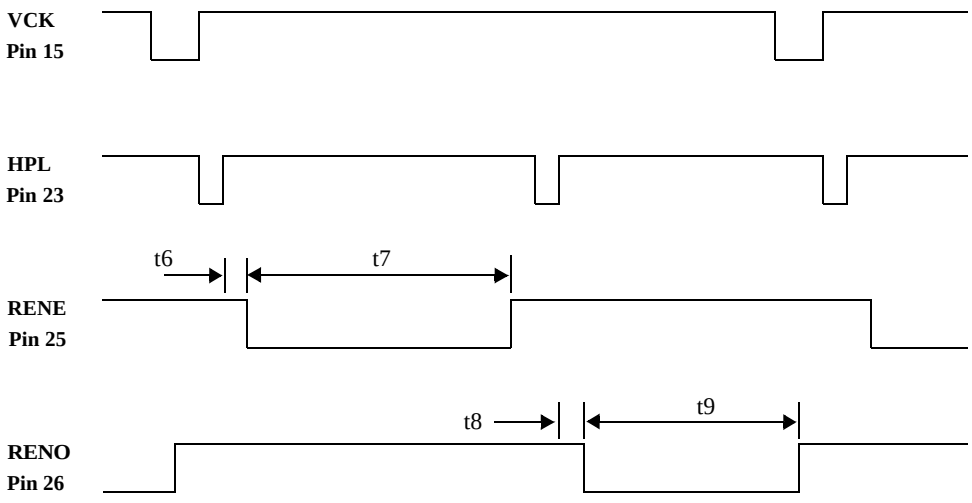


Figure 10 - LCD Timing Signals vs. Fields (NTSC)

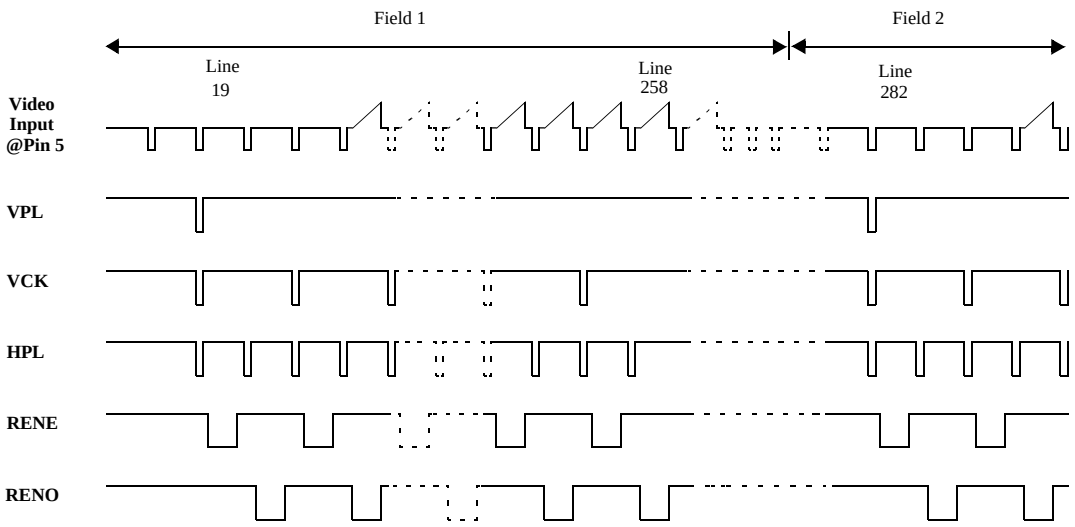


Figure 11 - OSD Input Signal Waveform

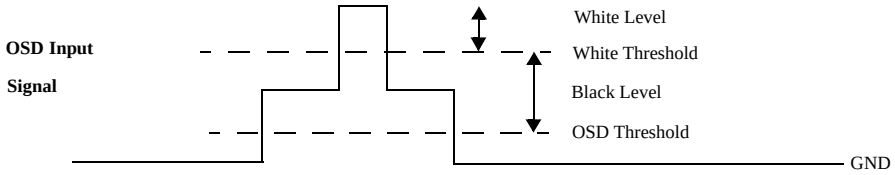
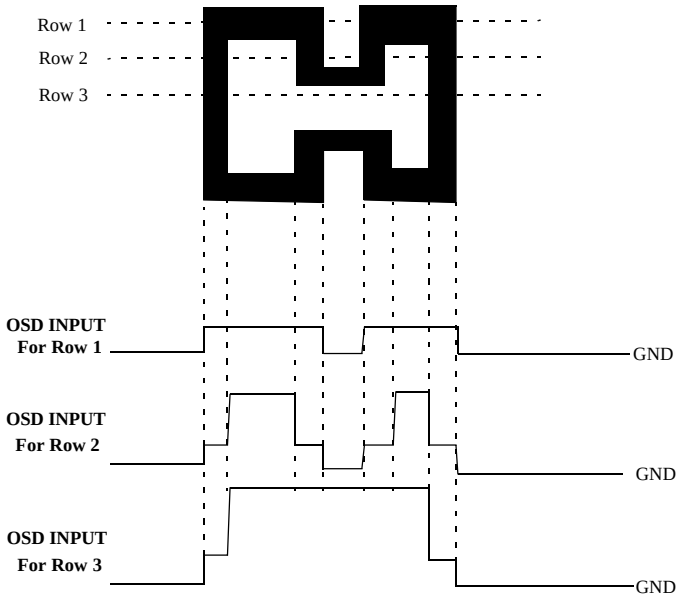


Figure 12 - OSD Display Example



FUNCTIONAL DESCRIPTION (Refer to Figure 1)

The MCVVQ111AFB is designed to receive a standard monochrome video signal (525 or 625 lines) at Pin 5, and drive the *CyberDisplay320* LCD display panel. The IC contains the following sections:

PLL - The PLL will normally lock to the horizontal frequency of the incoming video (via the sync separator) so as to synchronize the timing generator with the video amplifiers. The component values shown at pin 7 are suitable for both 525/60 and 625/50 signals. The PLL output frequency is 384xFh, or 6.05MHz for a standard 525 line/60Hz signal (NTSC), and 6MHz for a standard 625 line/50 Hz signal (PAL/SECAM). The timing generator provides all the timing signals to the LCD panel.

Pins 45 and 46 (HSync and VSync) can be configured as inputs or outputs, controlled by pin 47(VHIO Sel). When Pin 47 is low, pins 45 and 46 are outputs. HSync out is a square wave at the horizontal frequency as shown in Figure 4. VSync out is an active high pulse as shown in Figure 5.

When pin 47 is high, pins 45 and 46 are inputs, require negative sync input pulses. This permits synchronizing the MCVVQ111AFB to an external signal.

When there is no video present, the PLL will continue to provide horizontal and vertical timing signals to the timing generator so as to keep the LCD display active. The PLL frequency will decrease slightly in the absence of video, but will lock up once a valid video signal is applied.

Voltage Regulator- The section will provide all the necessary regulated supply voltages to the LCD display panel from an external 11V supply(VDDH).

Figure 6 shows the various voltages required by the *CyberDisplay320* LCD panel.

Video Processor - The video input is a standard 1.0 volt p-p composite monochrome video signal, either 525 or 625 lines. If only color composite video is available, it is recommended that the chroma frequencies be filtered out prior to this IC.

The DC Restore section provides black level clamping. For this portion to function correctly, the source impedance of the video signal must be <500. The clamp timing is shown in Figure 4 .

The sync separator will separate the horizontal and vertical timing signals from the incoming video, and provide them to the timing generator, and to the PLL. The remaining luma information passes to the two output video amplifiers, via the OSD switch, and the video adjust block.

The Black Level Adjust (pin 30) is a DC input, with an input range of 2.0 to 3.0 volts, setting the black level at VIDH and VIDL according to Figure 2. The black level does not change if the voltage at pin 30 is increased past 3.0 volts, and it is not affected by the Gain adjust(Pin 8).

The Gain Adjust(pin 8) input is a DC input, with a range of 1.25 to +2.5 volts, resulting in a 7 dB change at VIDL and VIDH, as shown in Figure 3 . The gain of Figure 3 is from the Video Input(Pin 5) to VIDL & VIDH, measured from black level to white level, excluding sync. Since VIDL's upper limit (and VIDH's lower limit) are clamped at 5.5 volts, the gain curve is valid as long as the signals are not clamped.

Timing Generator - This section provides the horizontal and vertical scaling, and the eight timing signals required by the *CyberDisplay320* LCD display panel. All fields of the incoming interlaced signal are provided to the display panel sequentially. This section is synchronized by signals from the sync separator and PLL. The HCK frequency is same as PLL output frequency (6.05 MHz or 6.0 MHz).

The vertical scaling algorithm depends on the setting of the 525/625 pin (pin 10). When set low (for 525/60 signals) no vertical scaling occurs. When set high (for 625/50 signals) lines are skipped according to the following algorithms:

- Odd field, line number 22+(12N+6) and 22+(12N+12) where N=0,1,2,3.... were skipped, or, the first skipped line is line 28,
- Even field, line number 334+(12N+3) and 334+(12N+9) where N=0,1,2,3.... were skipped, or, the first skipped line is line 337,

Horizontally, a small portion of the left and right edges of the video content line is expanded. Figure 7 indicates the horizontal timing.

All timing values are multiples of the HCK period. The eight timing signals to the *CyberDisplay320* LCD display panel are (refer Figures 8-10):

- PDR (pin 13) - Power Down Reset is high for normal operation. It is set low when the MCVVQ111AFB is set to the Sleep mode.
- VCK (pin 15) - Vertical Clock. The active low output appears every other line, indicating the beginning of an even numbered row. It is present for video lines 22 through 260 only.
- VPL (pin 16) - Vertical Start Pulse. This active low output appears once per field at line 22, to indicate the start of a field.
- HODL (pin 17) - This output changes polarity to satisfy the HODL inversion requirement of the *CyberDisplay320* LCD display panel. The changes occur during the back porch time of video lines 22 through 261 of each field, with an addition change at line 4 of either Field 1 or 2, depending on the initial lock-up condition.
- HPL (pin 23) - Horizontal Start Pulse. This active output indicates the beginning of each line. It is present for video lines 22 through 261 only.

•HCK (pin 24) - Horizontal Clock. This square wave output has a frequency of 384x the video horizontal frequency. This output is present continuously in both fields.
•RENE (pin 25) - Row Enable (Even) - This active low output occurs during the active video time of each even numbered line. It is present for video lines 22 through 260.
•RENO (pin 26) - Row Enable (Odd) - This active low output occurs during the active video time of each odd numbered line. It is present for video lines 23 through 261.

HODL Selection - During cue/review/pause mode of the camcorder operation or under noisy environment, which defined as Abnormal Video Mode, the HODL should be under Column Inversion Output. HODL Selection(pin 2) is set to HIGH (Column Inversion) for abnormal video mode and LOW (Pixel Inversion) for normal mode. The switching frequency of HODL polarity can be either VF/2 Hz or VF/4 Hz depending on the setting of the HODL_INV_FREQ(pin 37). VF is defined as vertical frequency.

The minimum voltage level for logic HIGH of HODL SEL is 0.66xVBAT volts and the maximum voltage level for logic LOW is 0.33xVBAT volts.

Switching frequency of HODL polarity:

HODL_INV_FREQ	PAL	NTSC
0	25 Hz	30 Hz
1	12.5 Hz	15 Hz

OSD Input - If the OSD display information is not contained in the composite video signal, then OSD information can be applied to pin 3. The signal levels at this pin must conform to that shown in Figure 11, and must be externally generated and synchronized with the video. The sync outputs at pins 45 and 46 can be used for synchronization.

Normally, pin 3 is to be at ground to display the video applied at pin 5. When the OSD input signal at pin 3 exceeds the OSD threshold (0.75 volt), the internal switch transfers the video amplifiers' outputs to the black level, causing a black display at the LCD panel. This black time can be, e.g., a border. The OSD Black level is the same as that set for the normal video black level, and is set by the voltage at pin 30 (see Figure 2).

When the OSD input signal is increased past the White threshold (2.25 volts), the video amplifiers' outputs go to the White Level.

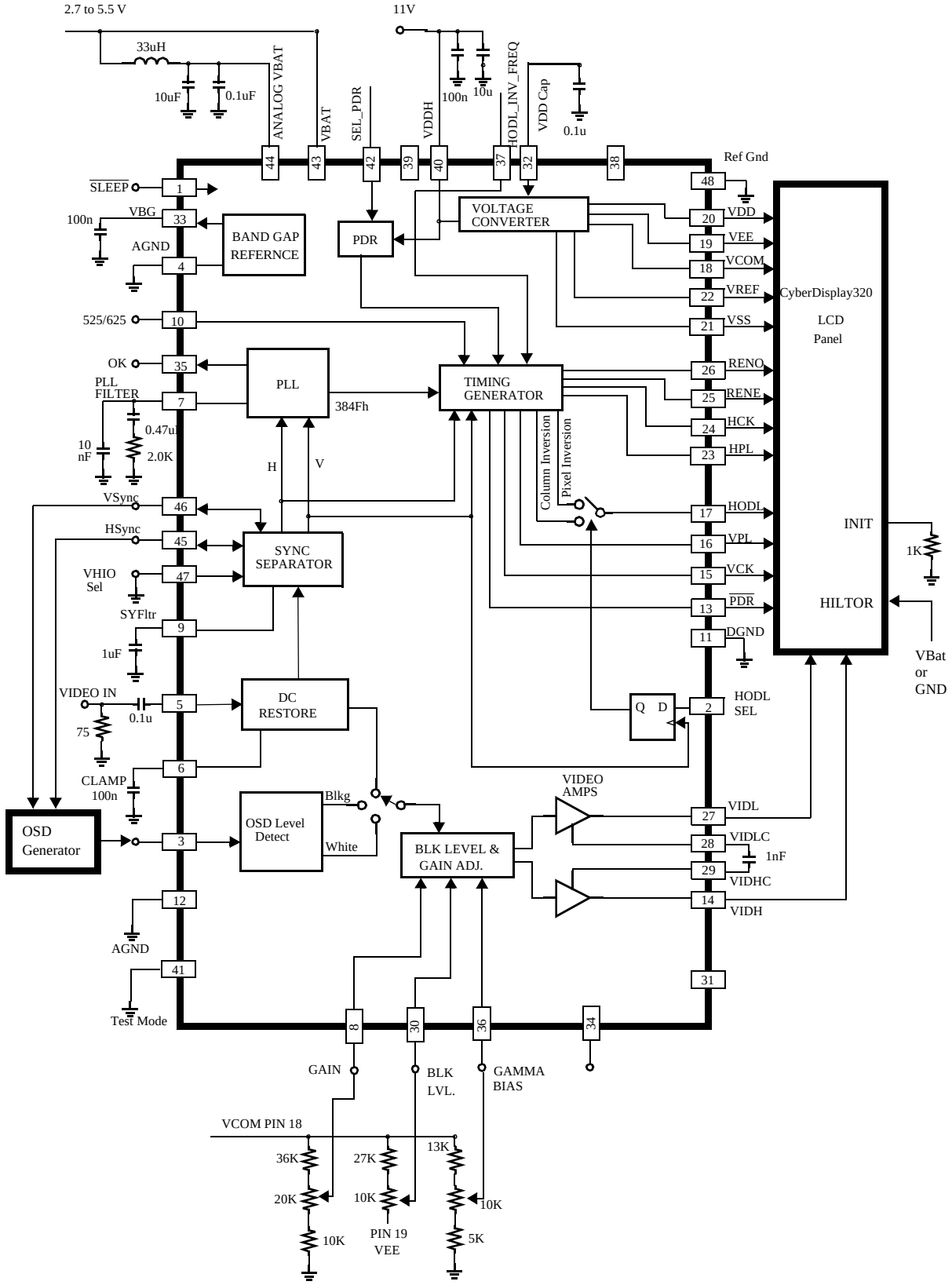
Formation of the on-screen characters is accomplished by appropriate timing of the signal at pin 3, as shown in the example in Figure 12. The OSD input signal must be returned to ground to resume displaying the video signal at pin 5. If the OSD input pin is not used, it must be connected to ground.

The default OSD contrast is 92.5%(1.475V).

Sleep Mode - The Sleep mode, activated by setting SLEEP pin low, will shut off the entire IC by removing all power supply voltages and the driving signals from the LCD display panel. This mode results in power consumption by the IC of less than 1 mW.

PDR - The PDR section prevents invalid video display during the power up or when VDDH drops below 10 volts.
The $\overline{\text{PDR}}$ will be released if following two conditions are met:
. 333 - 400 ms elapses after power up
. VDDH is no less than 10 volts.
Only if both of the above conditions meet, the display panel will be enabled.
The PDR scheme can be either scheme 1 or scheme 2 depending on the setting of SEL_PDR(pin 42). The difference between these two schemes is: When PDR is asserted during VBlanking, 3 RENE/RENO pulses will be generated under scheme 2 but no RENE/RENO pulse will be generated under scheme 1.

Figure 13 Application Circuit



APPLICATION INFORMATION

Figure 13 shows the basic application circuit using MCVVQ111AFB along with CyberDisplay320 LCD Panel. Applicable points are:

- **The components at pins 6, 7, and 9 must be in a neat, tight arrangement connected directly to the ground at pin 4**.
- It is recommended that a socket NOT be used for the MCVVQ111AFB.
- Pins10 can be hard wired to VBat or to Ground, or controlled by a logic circuit (microprocessor), depending on the application.
- The connections to the CyberDisplay320 LCD panel (pins 13 - 27) should be short and direct. The pinout sequence on the MCVVQ111AFB matches that of the LCD panel.
- A ground plane is recommended.
- The components of the loop filter on Pin 7 may be depending on the customer PCB layout.

Gamma Correction

The gamma bias pin and the gain pin control the shape and amplitude of the video output so as to match the panel non-linear transmittance characteristics. The Gain parameter controls the slope from black to white region, whereas the Gamma parameter sets the turning point of the black region. Figure 14, Figure 15 and Figure 16 show how different gamma and gain settings can affect the characteristic of video output. (The detailed plots of characteristic of video output under different gain and gamma settings will be provided in another document: Application note.)

Figure 14 Gain = 1.5V, Gamma=1.25V

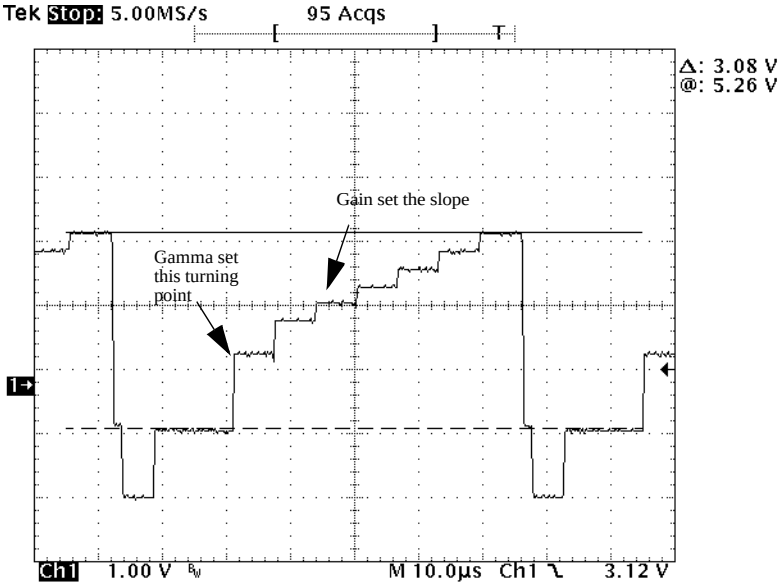
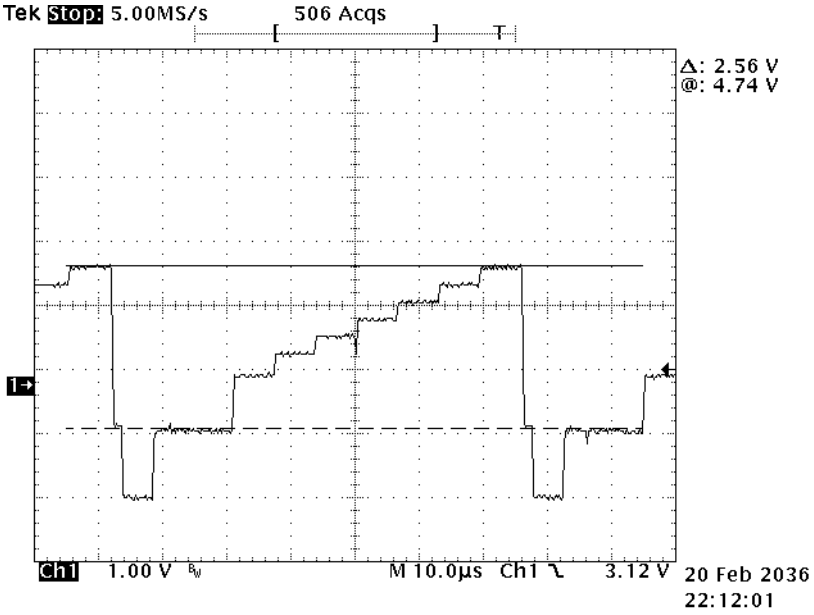
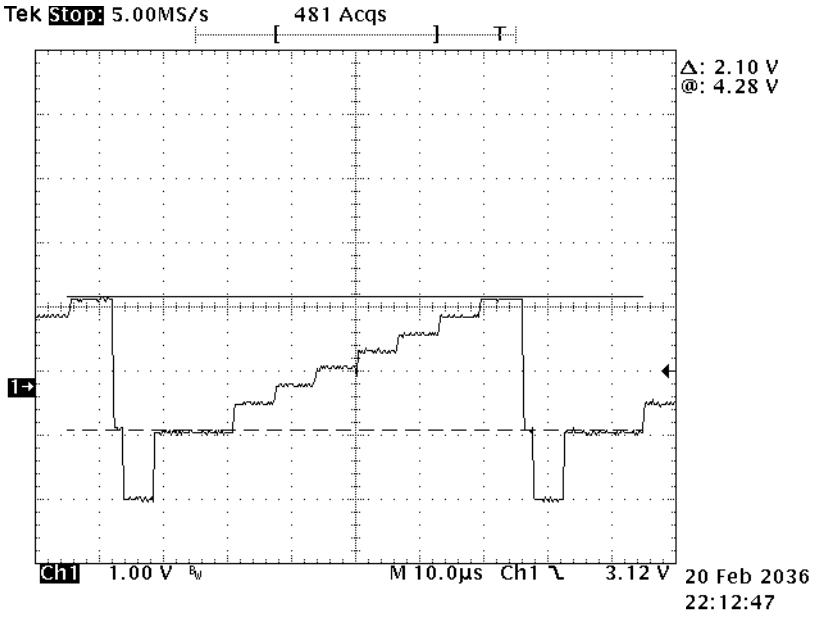


Figure 15 Gain = 1.5V, Gamma=1V



With a smaller gain, the slope in Figure 15 is less steeper than the one in Figure 14

Figure 16 Gain = 1.5V, Gamma = 0.75V



With a smaller gamma, the black region turning point in Figure 16 is lower than the one in Figure 14

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

Mfax‰: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609
INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center,
2 Dai King Street, Taipo Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668333