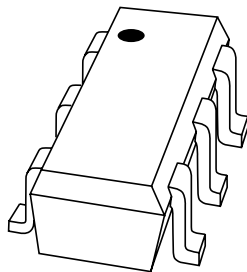


# DATA SHEET



## **PUMD10** NPN/PNP resistor-equipped transistors

Product specification  
Supersedes data of 1998 Dec 04

1999 May 20

# NPN/PNP resistor-equipped transistors

# PUMD10

### FEATURES

- Transistors with different polarity and built-in bias resistors R1 and R2 (typ. 2.2 kΩ and 47 kΩ respectively)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

### APPLICATIONS

- Especially suitable for space reduction in portable equipment
- Inverter circuit configurations without use of external resistors.

### DESCRIPTION

NPN/PNP resistor-equipped transistors in an SC-88 (SOT363) plastic package.

### PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

### MARKING

TYPE NUMBER	MARKING CODE
PUMD10	Dt0

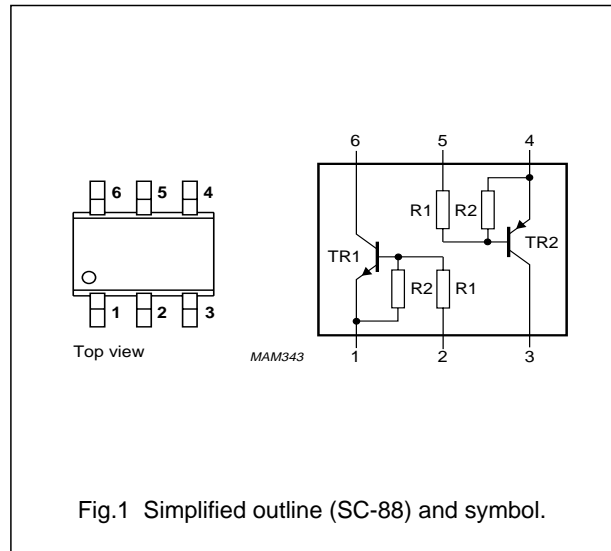


Fig.1 Simplified outline (SC-88) and symbol.

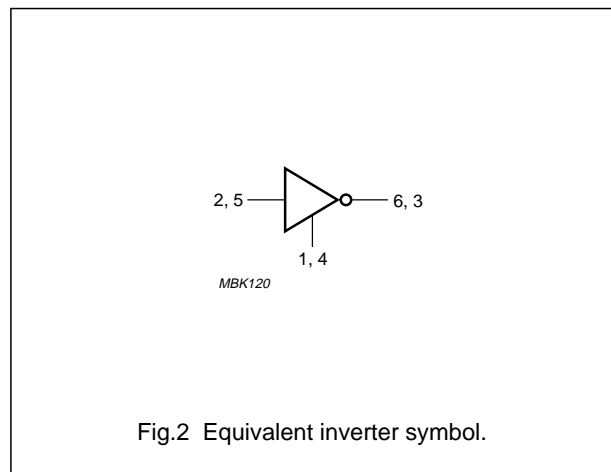


Fig.2 Equivalent inverter symbol.

## NPN/PNP resistor-equipped transistors

## PUMD10

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage positive negative		–	+12	V
			–	–5	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Refer to SC-88 standard mounting conditions.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	416	K/W

**Note**

1. Refer to SC-88 standard mounting conditions.

## NPN/PNP resistor-equipped transistors

## PUMD10

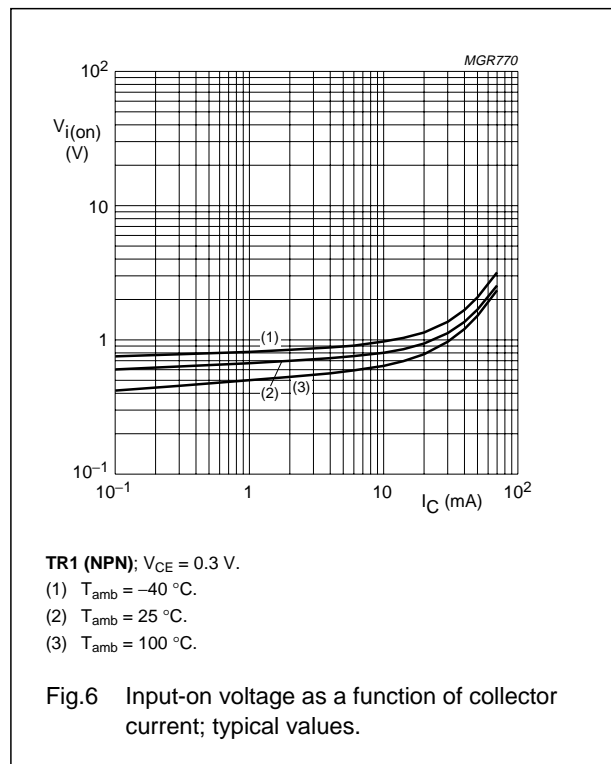
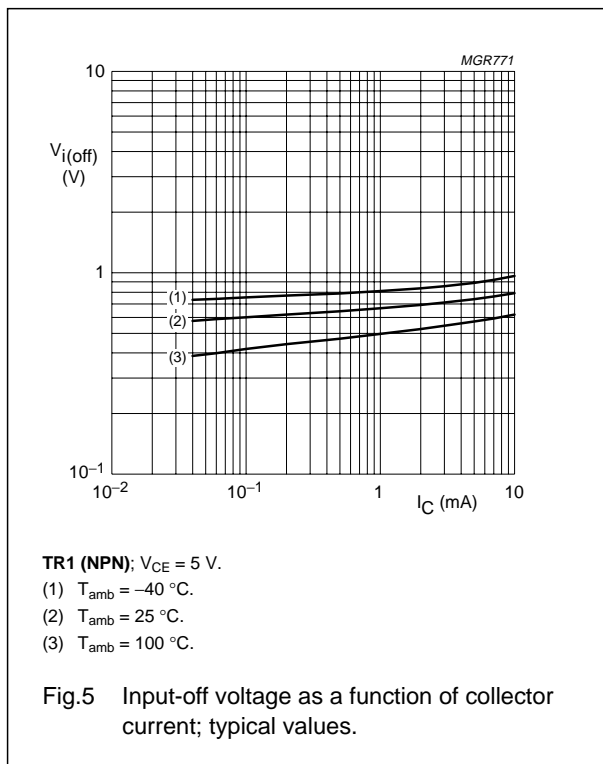
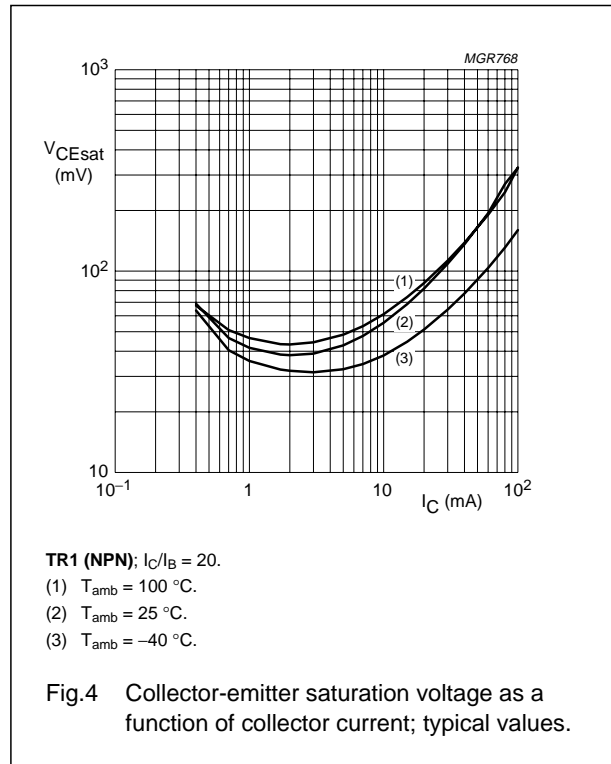
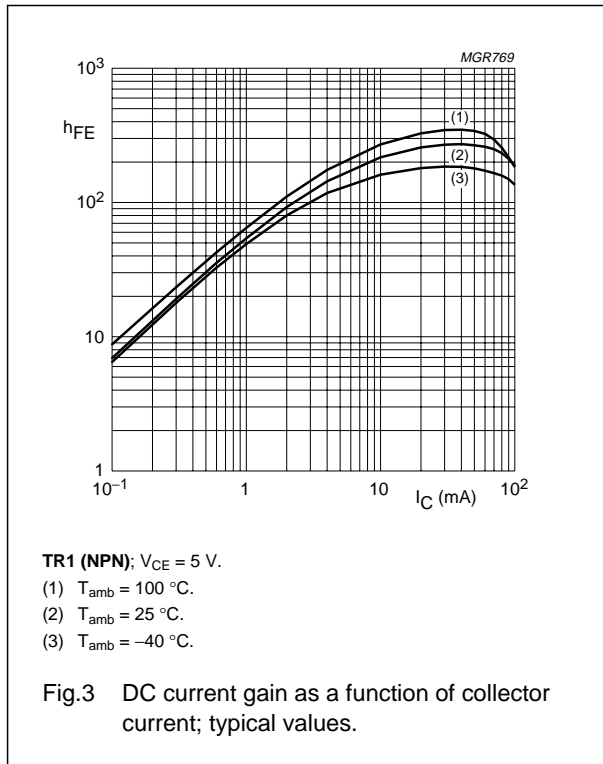
**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector cut-off current	$I_C = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
$I_{CEO}$	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	$\mu\text{A}$
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	180	$\mu\text{A}$
$h_{FE}$	DC current gain	$I_C = 10\text{ mA}; V_{CE} = 5\text{ V}$	100	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	–	–	100	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	0.6	0.5	V
$V_{i(on)}$	input-on voltage	$I_C = 5\text{ mA}; V_{CE} = 0.3\text{ V}$	1.1	0.75	–	V
R1	input resistor		1.54	2.2	2.86	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		17	21	26	
$C_c$	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)	–	–	3	pF	

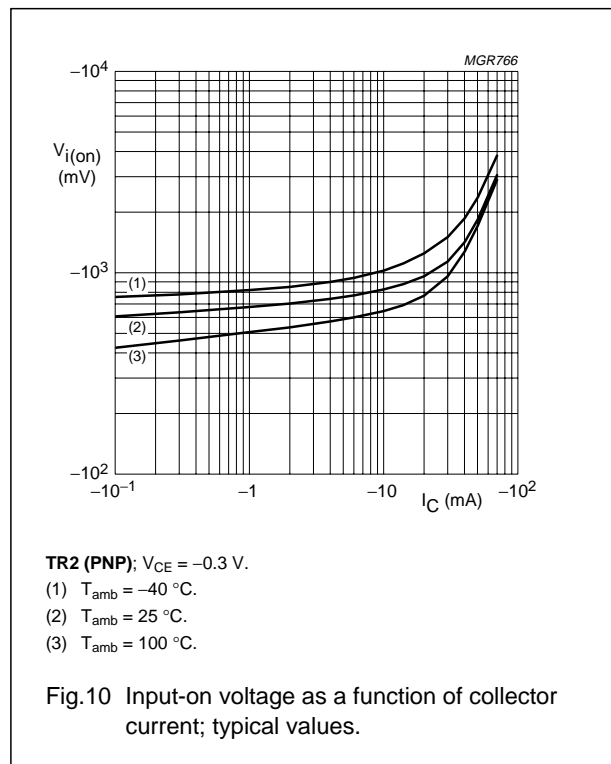
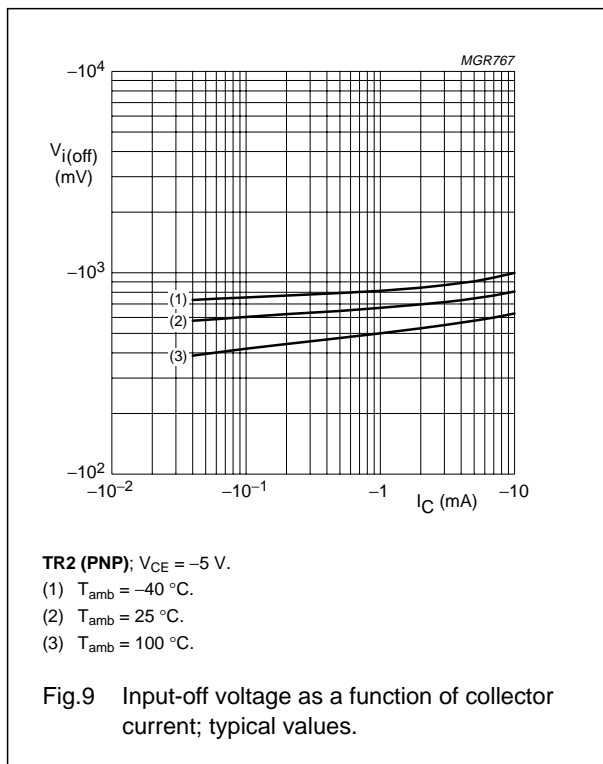
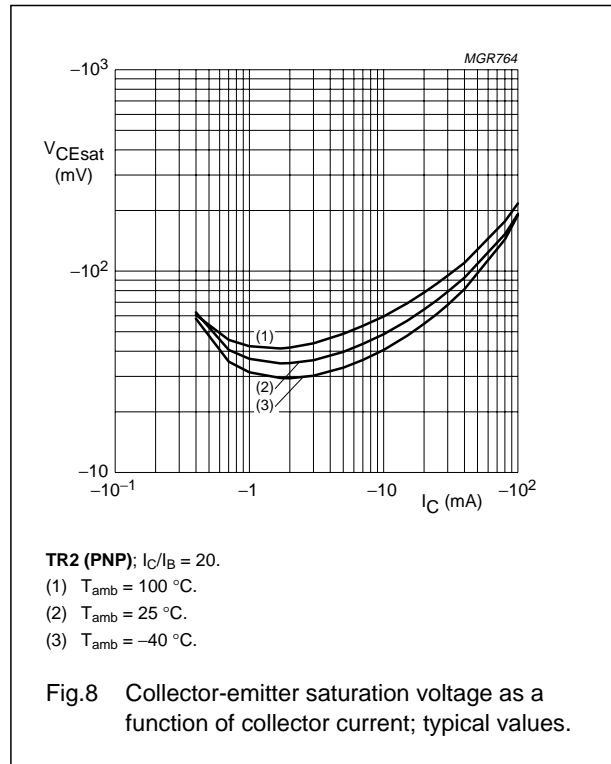
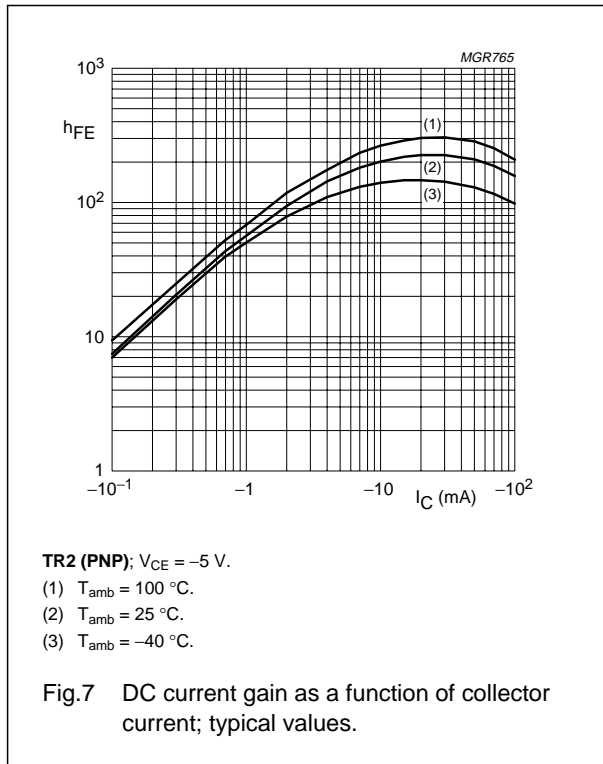
NPN/PNP resistor-equipped transistors

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NPN/PNP resistor-equipped transistors

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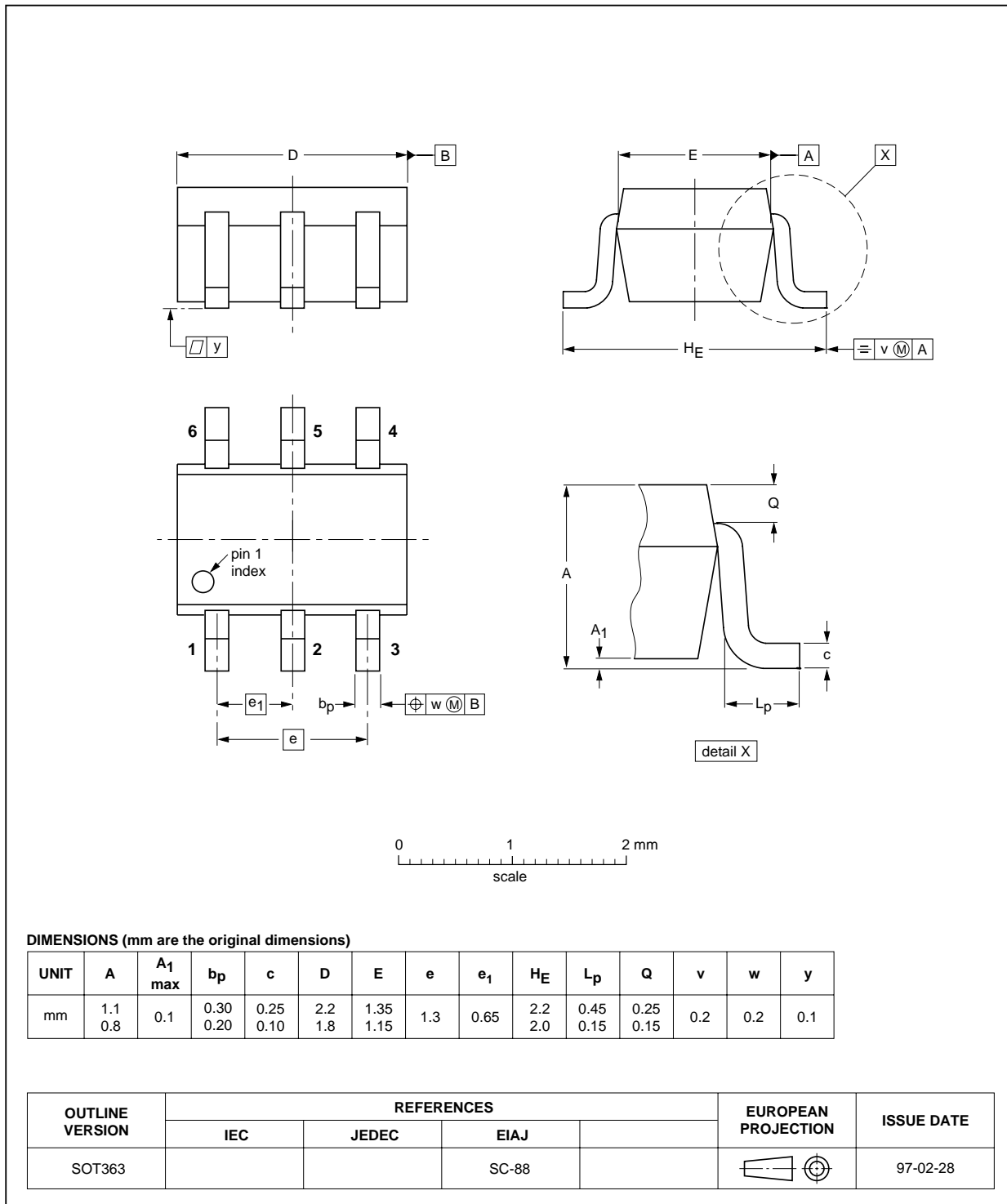
NPN/PNP resistor-equipped transistors

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



## NPN/PNP resistor-equipped transistors

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN/PNP resistor-equipped transistors

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**NOTES**

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**NOTES**

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**NOTES**

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