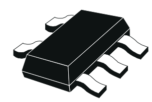
LK112Sxx

Low noise low drop voltage regulator with shutdown function

Features

- Output current up to 200 mA
- Low dropout voltage (500 mV max at I_{OUT} = 200 mA)
- Very low quiescent current: 0.1 µA in OFF mode and max 250 µA in ON mode at I_{OUT} = 0 mA
- Low output noise: typ. 30 µV at I_{OUT} = 60 mA and 10 Hz < f < 80 kHz
- Wide range of output voltages
- Internal current and thermal limit
- V_{OUT} tolerance ± 2% (at 25 °C)
- Operative input voltage from: V_{OUT} + 0.5 to 14 V (for V_{OUT} > 2 V) or from 2.5 V to 14 V (for V_{OUT} < 2 V)



SOT23-5L

Description

The LK112Sxx is a low dropout linear regulator with a built in electronic switch. The internal switch can be controlled by TTL or CMOS logic levels. The device is ON state when the control pin is pulled to a logic high level. An external capacitor can be used connected to the noise bypass pin to lower the output noise level to 30 µVrms. An internal PNP pass transistor is used to achieve a low dropout voltage.

The LK112Sxx has a very low quiescent current in ON MODE while in OFF MODE the Iq is reduced down to 100 nA max. The internal thermal shutdown circuitry limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shutdown in the presence of a short circuit or overcurrent condition at the output.

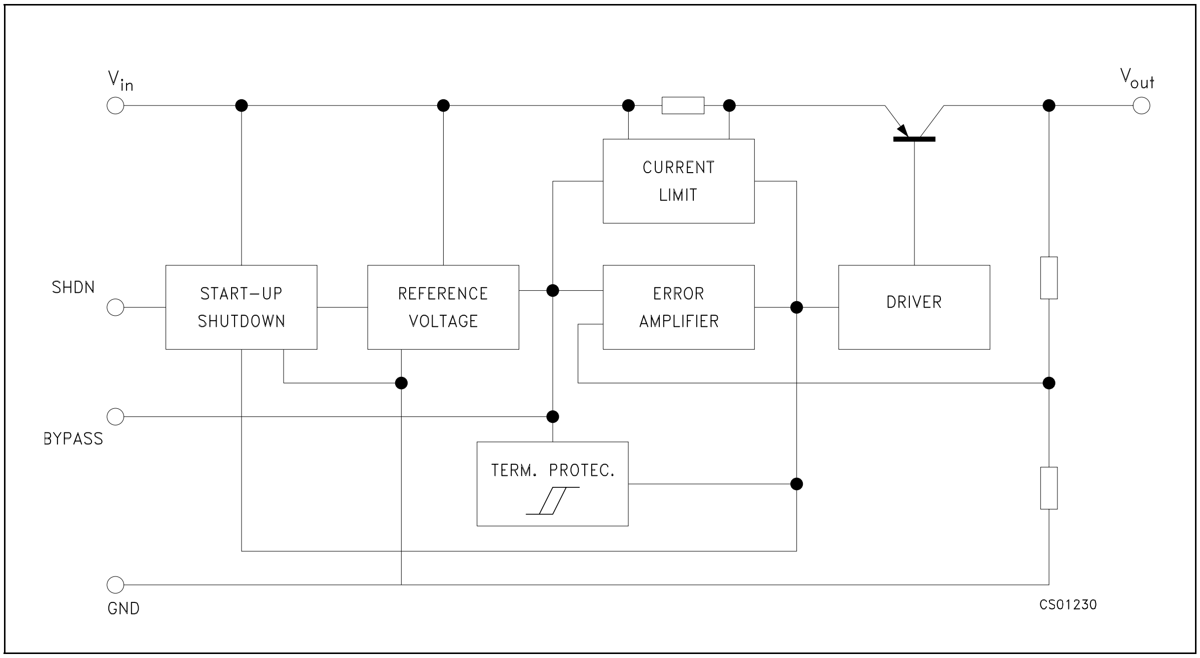
Table 1. Device summary

Part numbers			
LK112SXX13	LK112SXX24	LK112SXX36	LK112SXX45
LK112SXX14	LK112SXX26	LK112SXX37	LK112SXX46
LK112SXX18	LK112SXX28	LK112SXX38	LK112SXX47
LK112SXX19	LK112SXX29	LK112SXX39	LK112SXX48
LK112SXX20	LK112SXX31	LK112SXX41	LK112SXX49
LK112SXX21	LK112SXX33	LK112SXX42	LK112SXX50
LK112SXX22	LK112SXX34	LK112SXX43	
LK112SXX23	LK112SXX35	LK112SXX44	

Contents

1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connection (top view)

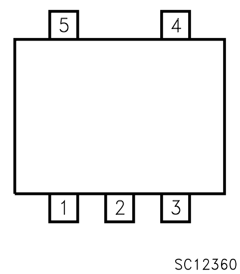


Table 2. Pin description

Pin n°	Symbol	Note
1	SHDN	Shutdown Input: Disables the regulator when is connected to GND or to positive voltage less than 0.6 V
2	GND	Ground Pin: Internally connected to the die attach flag to decrease the total thermal resistance and increase the package ability to dissipate power.
3	Bypass	Bypass Pin: Bypass with 0.1 µF to improve the V_{REF} thermal noise performances.
4	OUT	Output port
5	IN	Input port

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	16	V
V_{SHDN}	DC input voltage	16	V
I_O	Output current	Internally limited	
T_{STG}	Storage temperature range	-55 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Table 4. Thermal data

Symbol	Parameter	SOT23-5L	Unit
R_{thJC}	Thermal resistance junction-case	81	°C/W
R_{thJA}	Thermal resistance junction-ambient	255	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics for LK112S (T_J = 25 °C, V_{IN}=V_{OUT}+1 V (1), I_{OUT} = 0mA, V_{SHDN} = 1.8 V, C_I = 1 µF, C_O = 2.2 µF, C_{BYPASS} = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_d	Quiescent current	ON MODE (except I_{SHDN})		175	250	µA
		OFF MODE, V_I = 8V, V_{SHDN} = 0V		0	0.1	µA
V_O	Output voltage	I_O = 30mA		(see table)		
ΔV_O	Line regulation	$V_I = V_O$+1V to V_O+6V, $V_O \leq 5.6$V		0.7	20	mV
		$V_I = V_O$+1V to V_O+6V, $V_O > 5.6$V		0.8	40	mV
ΔV_O	Load regulation	I_O = 1 to 60mA		15	30	mV
		I_O = 1 to 200mA		30	90	mV
V_d	Dropout voltage	I_O = 60 mA (2)		0.17	0.24	V
		I_O = 200 mA (2)		0.35	0.5	V
I_{SC}	Short circuit current		200			mA
SVR	Supply voltage rejection	$V_I = V_O$+1.5V, C_{BYP} = 0.1µF C_O = 10µF, f = 400Hz, I_O = 30mA		55		dB
eN	Output noise voltage	B= 10Hz to 80kHz, C_{BYP} = 0.1µF C_O = 10µF, $V_I = V_O$+1.5V, I_O = 60mA		30		µVrms
I_{SHDN}	Shutdown input current	V_{SHDN} = 1.8V, Output ON		12	35	µA
V_{SHDN}	Shutdown input logic	Output ON	1.8			V
		Output OFF			0.6	
$\Delta V_O/T_J$	Output voltage temperature coefficient	I_O = 10mA		0.09		mV/°C

1. For version with output voltage less than 2V V_{IN}=2.4V
2. Only for version with output voltage more than 2.1V

5 Typical characteristics

(Unless otherwise specified, T_J = 25 °C, C_I = 1 µF, C_O = 2.2 µF, C_{BYP} = 100 nF)

Figure 3. Output voltage vs temperature

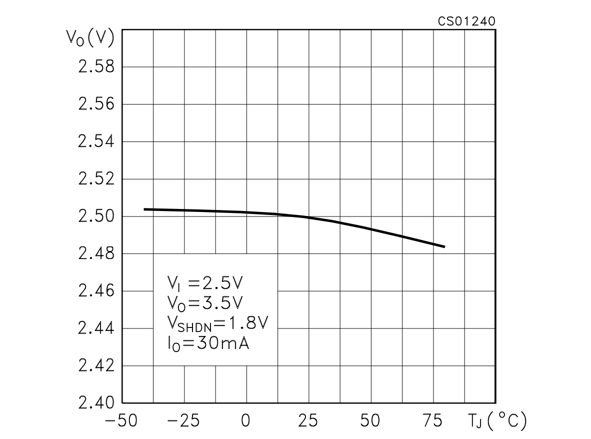


Figure 4. Output voltage vs temperature

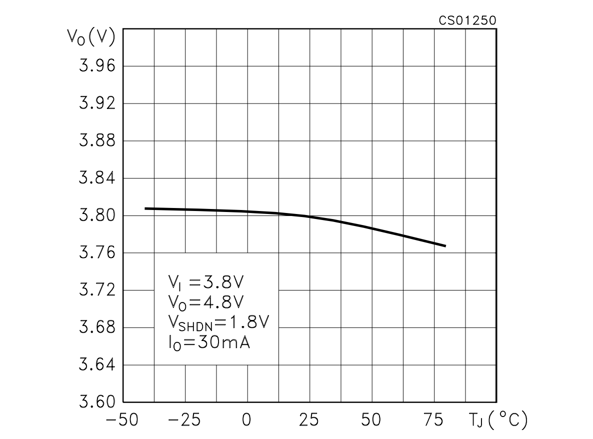


Figure 5. Line regulation vs temperature

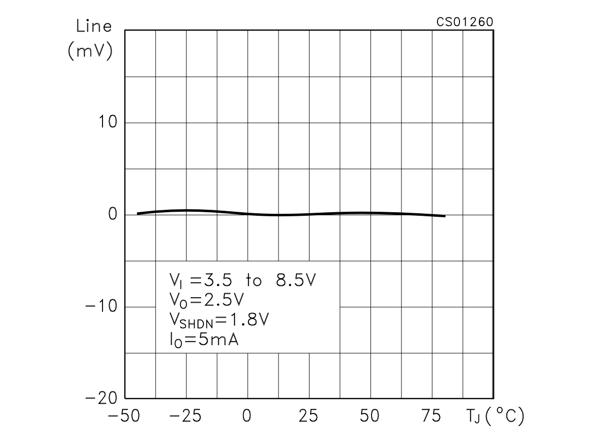


Figure 6. Load regulation vs temperature

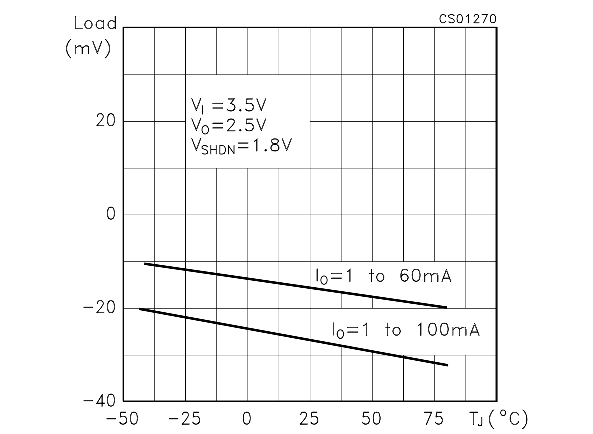


Figure 7. Dropout voltage vs temperature

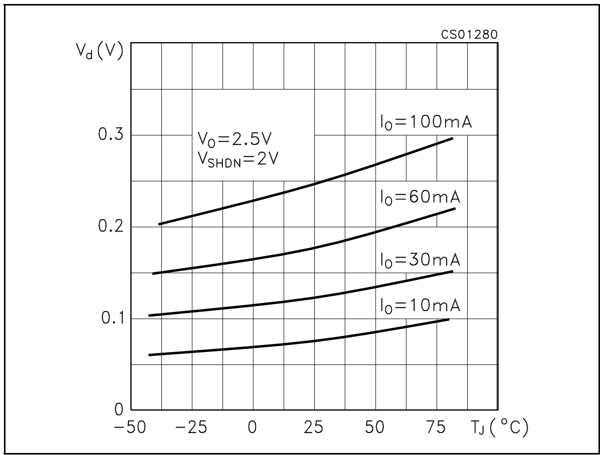


Figure 8. Short circuit current vs dropout voltage

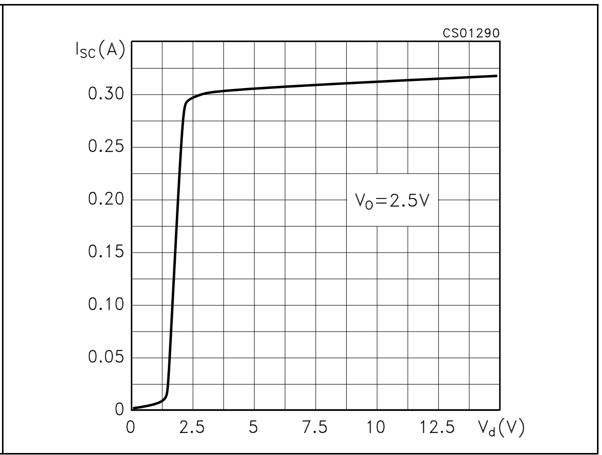


Figure 9. Output voltage vs input voltage

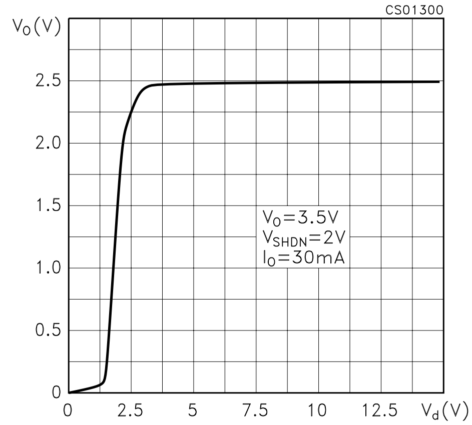


Figure 10. Shutdown voltage vs temperature

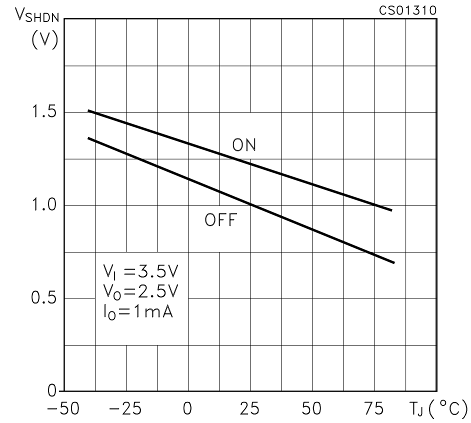


Figure 11. Shutdown current vs shutdown voltage

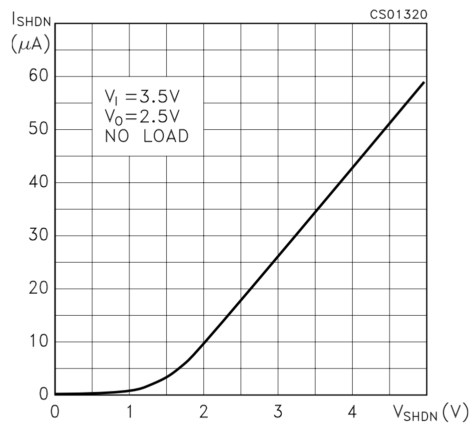


Figure 12. Supply voltage rejection vs temperature

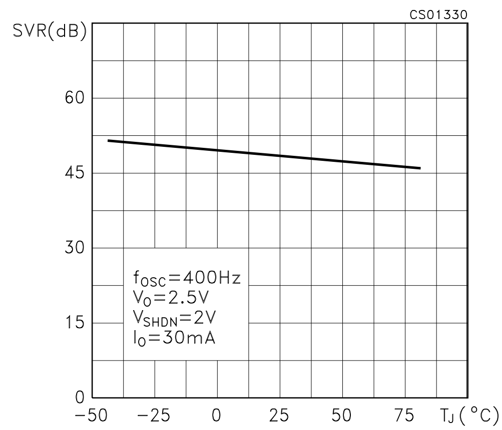


Figure 13. Supply voltage rejection vs output current

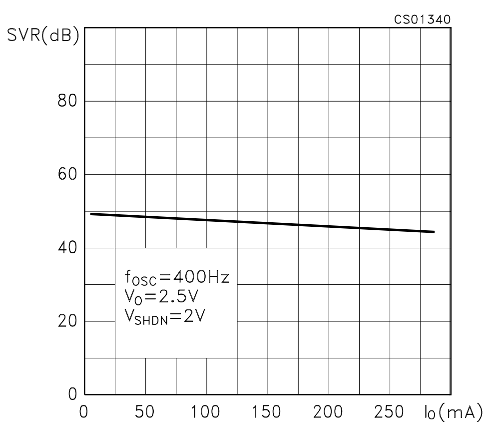


Figure 14. Supply voltage rejection vs frequency

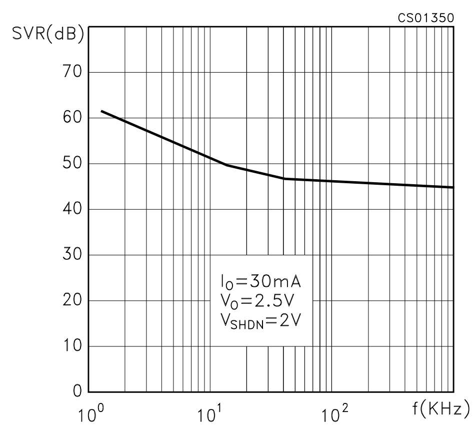


Figure 15. Supply voltage rejection vs temperature

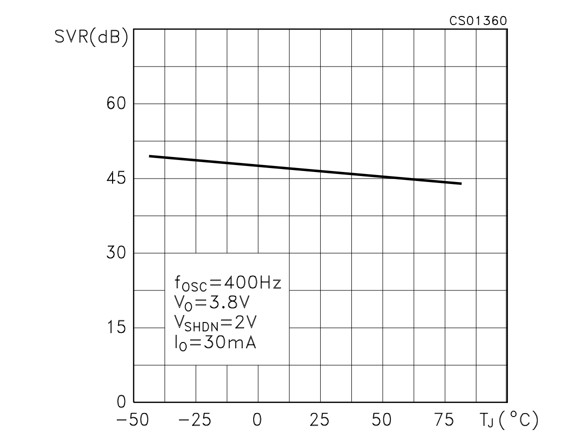


Figure 16. Quiescent current vs temperature

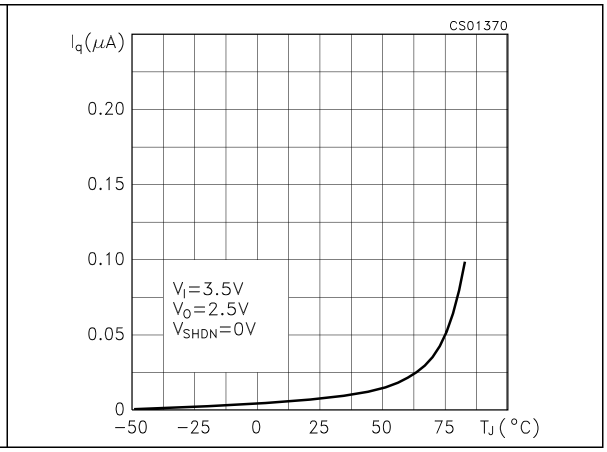


Figure 17. Quiescent current vs input voltage

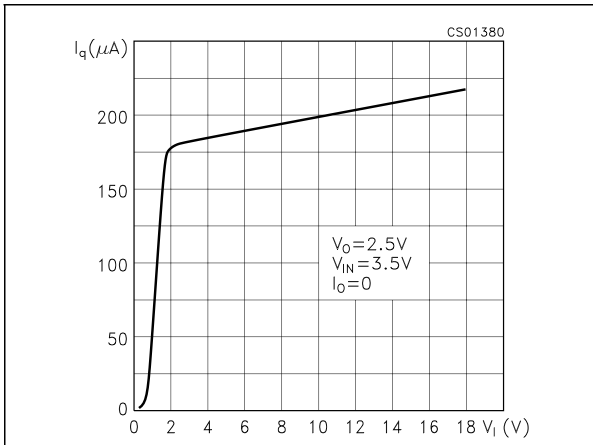


Figure 18. Quiescent current vs shutdown voltage

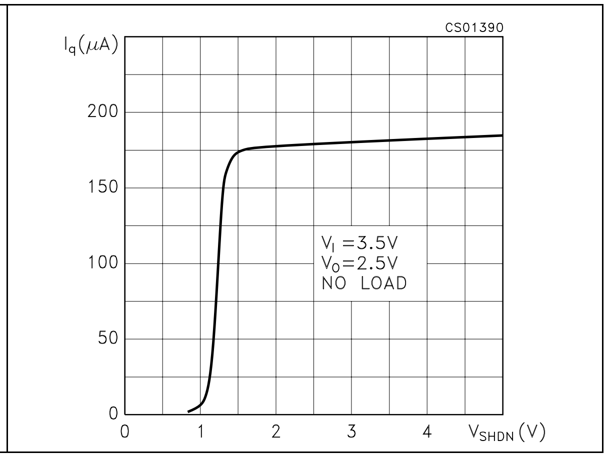


Figure 19. Quiescent current vs temperature

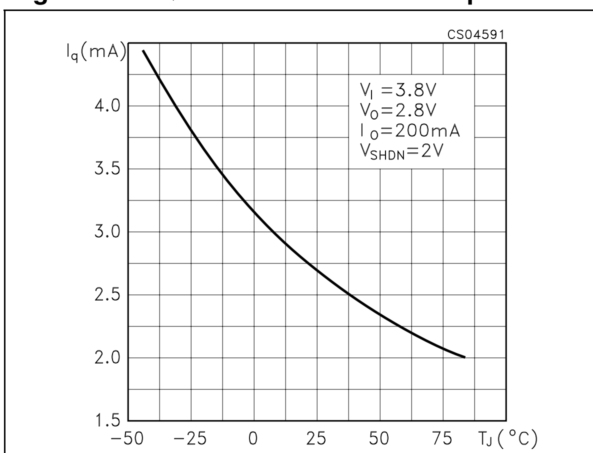


Figure 20. Reverse current vs reverse voltage

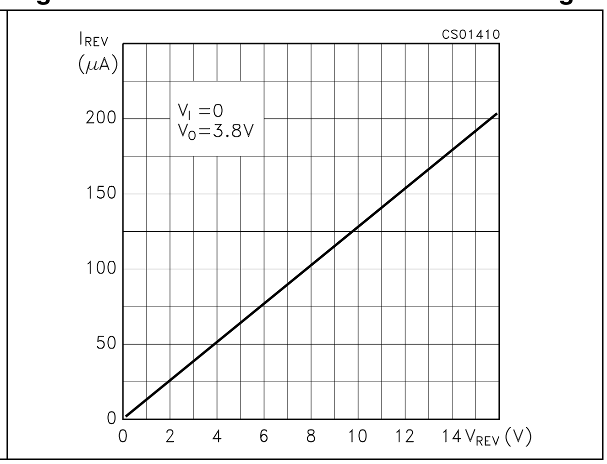


Figure 21. Stability

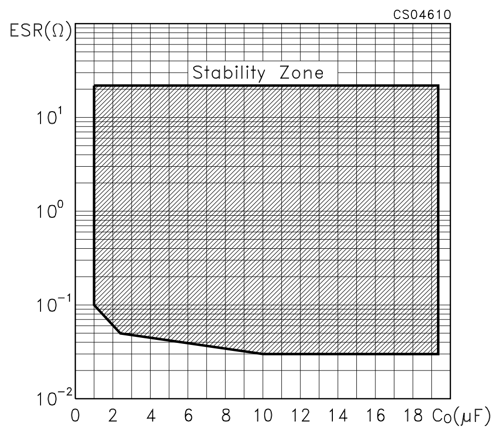


Figure 22. Spectrum noise

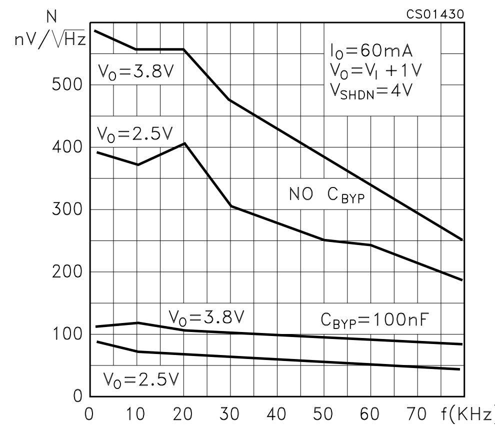
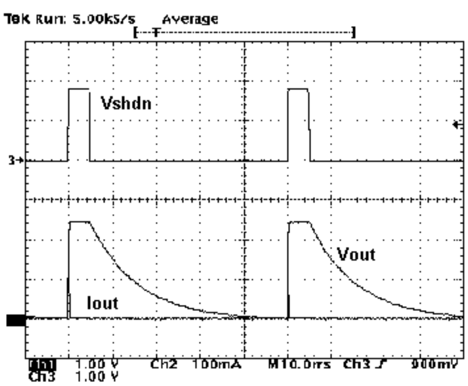
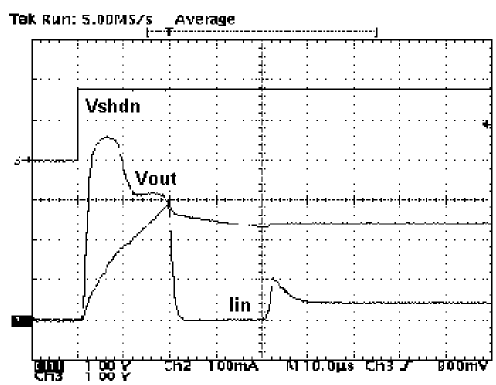


Figure 23. Start-up transient



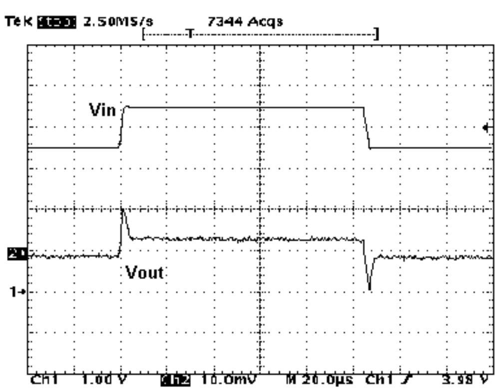
V_I=3.5V, V_O=2.5V, V_{SHDN}= 0 to 1.8V, R_L=2.5kΩ, C_I=1µF, C_O=4.7µF, C_{BYP}=10nF

Figure 24. Start-up transient



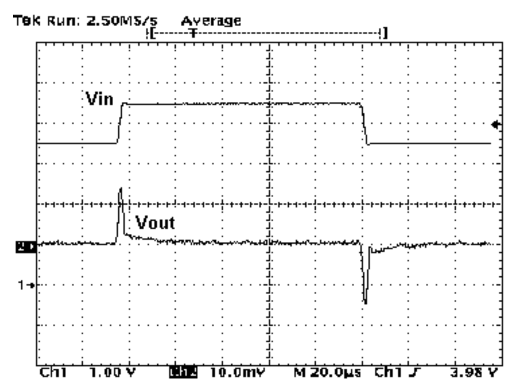
V_I=3.5V, V_O=2.5V, V_{SHDN}= 0 to 1.8V, R_L=68Ω, C_I=1µF, C_O=4.7µF, C_{BYP}=100nF

Figure 25. Line transient



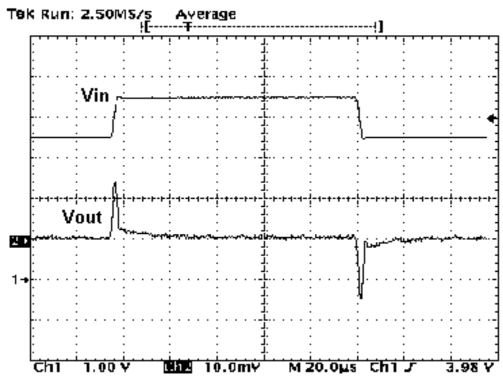
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}= 1.8V, I_O=30mA, no C_I, C_O=100µF, C_{BYP}=10nF, t_s=t_f=2µs

Figure 26. Line transient



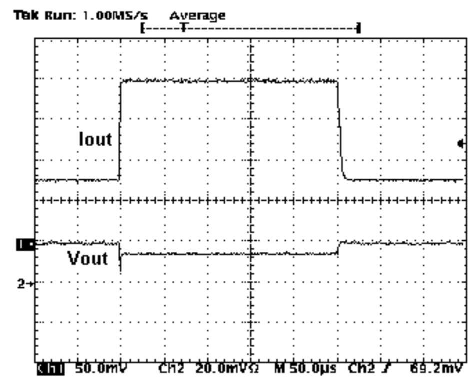
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}= 1.8V, I_O=30mA, no C_I, C_O=10µF, C_{BYP}=10nF, t_s=t_f=2µs

Figure 27. Line transient



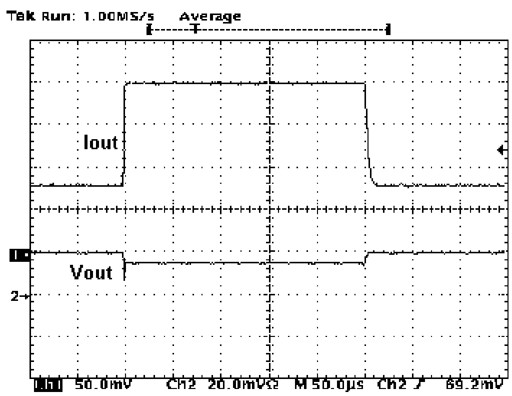
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}= 1.8V, I_O=30mA, no C_I, C_O=1µF, C_{BYP}=1nF, t_s=t_f=2µs

Figure 28. Load transient



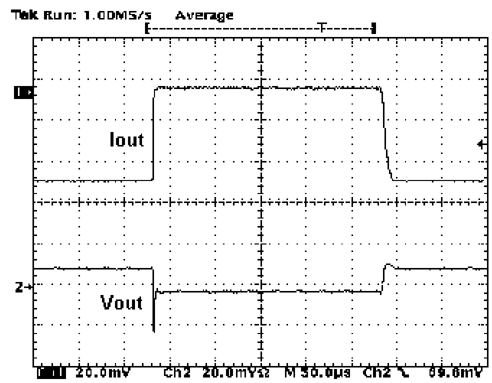
V_I=3.5V, V_O=2.5V, V_{SHDN}= 1.8V, I_O=50 to 100mA, C_I=1µF, C_O=2.2µF, C_{BYP}=10nF, t_s=t_f=250ns

Figure 29. Load transient



V_I=3.5V, V_O=2.5V, V_{SHDN}= 1.8V, I_O=50 to 100mA, C_I=1µF, C_O=10µF, C_{BYP}=100nF, t_s=t_f=250ns

Figure 30. Load transient



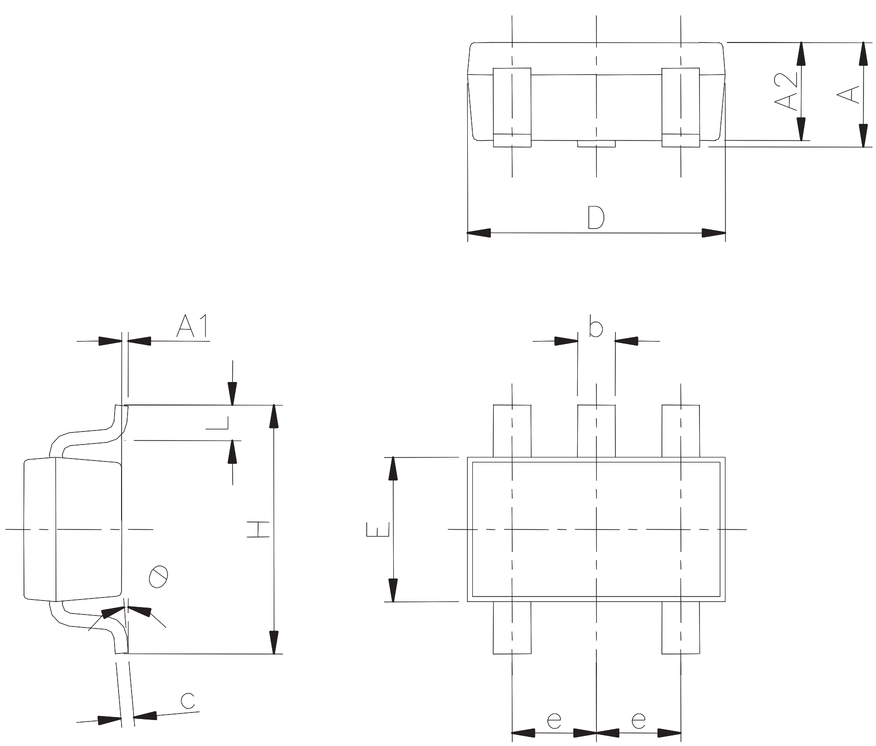
V_I=4.8V, V_O=3.8V, V_{SHDN}= 1.8V, I_O=50 to 100mA, C_I=1µF, C_O=2.2µF, C_{BYP}=10nF, t_s=t_f=250ns

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

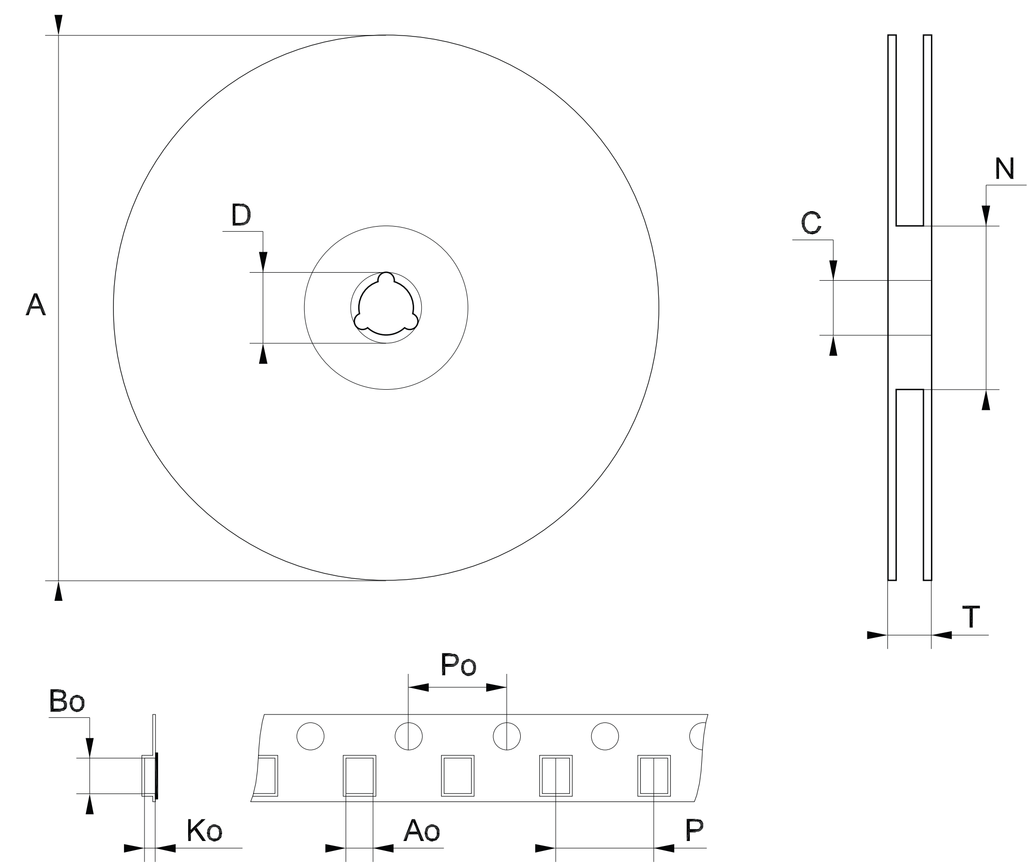
SOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



Tape & reel SOT23-xL mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Note: Drawing not in scale

7 Order codes

Table 6. Order codes

Part number	Output voltage	V_{OUT} Min.	V_{OUT} Max.	Test voltage
LK112SM13TR [1]	1.3V	1.24V	1.36V	2.4V
LK112SM14TR [1]	1.4V	1.34V	1.46V	2.4V
LK112SM18TR	1.8V	1.74V	1.86V	2.4V
LK112SM19TR [1]	1.9V	1.84V	1.96V	2.4V
LK112SM20TR [1]	2.0V	1.94V	2.06V	3.0V
LK112SM21TR [1]	2.1V	2.04V	2.16V	3.1V
LK112SM22TR [1]	2.2V	2.14V	2.26V	3.2V
LK112SM23TR [1]	2.3V	2.24V	2.36V	3.3V
LK112SM24TR [1]	2.4V	2.34V	2.46V	3.4V
LK112SM26TR [1]	2.6V	2.54V	2.66V	3.6V
LK112SM28TR	2.8V	2.74V	2.86V	3.8V
LK112SM29TR [1]	2.9V	2.84V	2.96V	3.9V
LK112SM31TR [1]	3.1V	3.04V	3.16V	4.1V
LK112SM33TR	3.3V	3.24V	3.36V	4.3V
LK112SM34TR [1]	3.4V	3.335V	3.465V	4.4V
LK112SM35TR [1]	3.5V	3.435V	3.565V	4.5V
LK112SM36TR [1]	3.6V	3.535V	3.655V	4.6V
LK112SM37TR [1]	3.7V	3.630V	3.770V	4.7V
LK112SM38TR [1]	3.8V	3.725V	3.875V	4.8V
LK112SM39TR [1]	3.9V	3.825V	3.975V	4.9V
LK112SM41TR [1]	4.1V	4.020V	4.180V	5.1V
LK112SM42TR [1]	4.2V	4.120V	4.280V	5.2V
LK112SM43TR [1]	4.3V	4.215V	4.385V	5.3V
LK112SM44TR [1]	4.4V	4.315V	4.485V	5.4V
LK112SM45TR [1]	4.5V	4.410V	4.590V	5.5V
LK112SM46TR [1]	4.6V	4.510V	4.690V	5.6V
LK112SM47TR [1]	4.7V	4.605V	4.795V	5.7V
LK112SM48TR [1]	4.8V	4.705V	4.895V	5.8V
LK112SM49TR [1]	4.9V	4.800V	5.000V	5.9V
LK112SM50TR	5.0V	4.900V	5.100V	6.0V

1. Available on request.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
31-Aug-2004	3	Mistake on fig. 19.
31-Jan-2005	4	Change maturity code.
12-Jun-2006	5	Order codes updated.
17-Oct-2006	6	The T_{OP} value on table 2 updated.
20-Jul-2007	7	Add *Table 1* in cover page.
21-Sep-2007	8	Features updated.
11-Dec-2007	9	Modified: *Table 6*.
12-Feb-2008	10	Modified: *Table 6 on page 15*.
10-Jul-2008	11	Modified: *Table 1 on page 1* and *Table 6 on page 15*.

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