



# *AMD Geode™ SC3200 Processor Data Book*

---

*March 2004*

Publication ID: Revision 5.1

---

© 2004 Advanced Micro Devices, Inc. All rights reserved.

The contents of this document are provided in connection with Advanced Micro Devices, Inc. ("AMD") products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD's Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD's product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

## **Contacts**

www.amd.com pcs.support@amd.com

## **Trademarks**

AMD, the AMD Arrow logo, and combinations thereof, and Geode, Virtual System Architecture, and WebPAD are trademarks of Advanced Micro Devices, Inc.

Microsoft and Windows are registered trademarks of Microsoft Corporation in the United States and other jurisdictions.

MMX is trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

# Contents

|   |            |
|---|------------|
| <b>List of Figures</b> .....  | <b>5</b>   |
| <b>List of Tables</b> .....   | <b>9</b>   |
| <b>1.0 AMD Geode™ SC3200 Processor</b> .....                            | <b>13</b>  |
| 1.1 General Description .....   | 13         |
| 1.2 Features .....  | 14         |
| <b>2.0 Architecture Overview</b> .....                                  | <b>17</b>  |
| 2.1 GX1 Module .....  | 17         |
| 2.2 Video Processor Module .....  | 22         |
| 2.3 Core Logic Module .....   | 22         |
| 2.4 Super I/O Module .....  | 23         |
| 2.5 Clock, Timers, and Reset Logic .....                                | 23         |
| <b>3.0 Signal Definitions</b> .....                                     | <b>25</b>  |
| 3.1 Ball Assignments .....  | 27         |
| 3.2 Strap Options .....   | 58         |
| 3.3 Multiplexing Configuration .....                                    | 59         |
| 3.4 Signal Descriptions .....   | 63         |
| <b>4.0 General Configuration Block</b> .....                            | <b>87</b>  |
| 4.1 Configuration Block Addresses .....                                 | 87         |
| 4.2 Multiplexing, Interrupt Selection, and Base Address Registers ..... | 88         |
| 4.3 WATCHDOG .....  | 95         |
| 4.4 High-Resolution Timer .....   | 97         |
| 4.5 Clock Generators and PLLs .....                                     | 99         |
| <b>5.0 SuperI/O Module</b> .....  | <b>105</b> |
| 5.1 Features .....  | 106        |
| 5.2 Module Architecture .....   | 107        |
| 5.3 Configuration Structure / Access .....                              | 108        |
| 5.4 Standard Configuration Registers .....                              | 110        |
| 5.5 Real-Time Clock (RTC) .....   | 121        |
| 5.6 System Wakeup Control (SWC) .....                                   | 132        |
| 5.7 ACCESS.bus Interface .....  | 137        |
| 5.8 Legacy Functional Blocks .....                                      | 145        |

|                   |  |            |
|-------------------|--|------------|
| <b>6.0</b>        | <b>Core Logic Module</b> .....         | <b>157</b> |
| 6.1               | Feature List .....                     | 157        |
| 6.2               | Module Architecture .....              | 158        |
| 6.3               | Register Descriptions .....            | 191        |
| 6.4               | Chipset Register Space .....           | 206        |
| <b>7.0</b>        | <b>Video Processor Module</b> .....    | <b>327</b> |
| 7.1               | Module Architecture .....              | 328        |
| 7.2               | Functional Description .....           | 329        |
| 7.3               | Register Descriptions .....            | 345        |
| <b>8.0</b>        | <b>Debugging and Monitoring</b> .....  | <b>367</b> |
| 8.1               | Testability (JTAG) .....               | 367        |
| <b>9.0</b>        | <b>Electrical Specifications</b> ..... | <b>369</b> |
| 9.1               | General Specifications .....           | 369        |
| 9.2               | DC Characteristics .....               | 375        |
| 9.3               | AC Characteristics .....               | 380        |
| <b>10.0</b>       | <b>Package Specifications</b> .....    | <b>439</b> |
| 10.1              | Thermal Characteristics .....          | 439        |
| 10.2              | Physical Dimensions .....              | 441        |
| <b>Appendix A</b> | <b>Support Documentation</b> .....     | <b>443</b> |
| A.1               | Order Information .....                | 443        |
| A.2               | Data Book Revision History .....       | 443        |

# List of Figures

|              |   |     |
|--------------|---|-----|
| Figure 1-1.  | Block Diagram   | 13  |
| Figure 3-1.  | Signal Groups   | 25  |
| Figure 3-2.  | 432-EBGA Ball Assignment Diagram  | 28  |
| Figure 3-3.  | 481-TEPBGA Ball Assignment Diagram  | 42  |
| Figure 4-1.  | WATCHDOG Block Diagram  | 95  |
| Figure 4-2.  | Clock Generation Block Diagram  | 99  |
| Figure 4-3.  | Recommended Oscillator External Circuitry                                     | 100 |
| Figure 5-1.  | SIO Block Diagram   | 105 |
| Figure 5-2.  | Detailed SIO Block Diagram  | 107 |
| Figure 5-3.  | Structure of the Standard Configuration Register File                         | 108 |
| Figure 5-4.  | Standard Configuration Registers Map  | 110 |
| Figure 5-5.  | Recommended Oscillator External Circuitry                                     | 121 |
| Figure 5-6.  | External Oscillator Connections   | 122 |
| Figure 5-7.  | Divider Chain Control   | 122 |
| Figure 5-8.  | Power Supply Connections  | 124 |
| Figure 5-9.  | Typical Battery Configuration   | 124 |
| Figure 5-10. | Typical Battery Current: Battery Backed Power Mode @ $T_C = 25^\circ\text{C}$ | 124 |
| Figure 5-11. | Typical Battery Current: Normal Operation Mode                                | 124 |
| Figure 5-12. | Interrupt/Status Timing   | 126 |
| Figure 5-13. | Bit Transfer  | 137 |
| Figure 5-14. | Start and Stop Conditions   | 137 |
| Figure 5-15. | ACCESS.bus Data Transaction   | 138 |
| Figure 5-16. | ACCESS.bus Acknowledge Cycle  | 138 |
| Figure 5-17. | A Complete ACCESS.bus Data Transaction  | 139 |
| Figure 5-18. | UART Mode Register Bank Architecture  | 147 |
| Figure 5-19. | IRCP/SP3 Register Bank Architecture   | 151 |
| Figure 6-1.  | Core Logic Module Block Diagram   | 158 |
| Figure 6-2.  | Non-Posted Fast-PCI to ISA Access   | 164 |
| Figure 6-3.  | PCI to ISA Cycles with Delayed Transaction Enabled                            | 165 |
| Figure 6-4.  | ISA DMA Read from PCI Memory  | 166 |
| Figure 6-5.  | ISA DMA Write to PCI Memory   | 166 |
| Figure 6-6.  | PCI Change to Sub-ISA and Back  | 168 |
| Figure 6-7.  | PIT Timer   | 170 |
| Figure 6-8.  | PIC Interrupt Controllers   | 171 |
| Figure 6-9.  | PCI and IRQ Interrupt Mapping   | 172 |
| Figure 6-10. | SMI Generation for NMI  | 173 |
| Figure 6-11. | General Purpose Timer and UDEF Trap SMI Tree Example                          | 181 |
| Figure 6-12. | PRD Table Example   | 185 |
| Figure 6-13. | AC97 V2.0 Codec Signal Connections  | 186 |
| Figure 6-14. | Audio SMI Tree Example  | 188 |
| Figure 6-15. | Typical Setup   | 189 |
| Figure 7-1.  | Video Processor Block Diagram   | 328 |
| Figure 7-2.  | NTSC 525 Lines, 60 Hz, Odd Field  | 330 |
| Figure 7-3.  | NTSC 525 Lines, 60 Hz, Even Field   | 330 |
| Figure 7-4.  | VIP Block Diagram   | 331 |

|              |   |     |
|--------------|---|-----|
| Figure 7-5.  | Capture Video Mode Bob Example Using One Video Frame Buffer     | 333 |
| Figure 7-6.  | Capture Video Mode Weave Example Using Two Video Frame Buffers  | 334 |
| Figure 7-7.  | Video Block Diagram   | 335 |
| Figure 7-8.  | Horizontal Downscaler Block Diagram                             | 336 |
| Figure 7-9.  | Linear Interpolation Calculation                                | 337 |
| Figure 7-10. | Mixer/Blender Block Diagram                                     | 338 |
| Figure 7-11. | Graphics/Video Frame with Alpha Windows                         | 340 |
| Figure 7-12. | Color Key and Alpha Blending Logic                              | 342 |
| Figure 7-13. | TFT Power Sequence  | 343 |
| Figure 7-14. | PLL Block Diagram   | 344 |
| Figure 9-1.  | Differential Input Sensitivity for Common Mode Range            | 378 |
| Figure 9-2.  | Drive level and Measurement Points                              | 380 |
| Figure 9-3.  | Memory Controller Drive Level and Measurement Points            | 381 |
| Figure 9-4.  | Memory Controller Output Valid Timing Diagram                   | 383 |
| Figure 9-5.  | Read Data In Setup and Hold Timing Diagram                      | 383 |
| Figure 9-6.  | Video Input Port Timing Diagram                                 | 384 |
| Figure 9-7.  | TFT Timing Diagram  | 385 |
| Figure 9-8.  | ACB Signals: Rising Time and Falling Timing Diagram             | 387 |
| Figure 9-9.  | ACB Start and Stop Condition Timing Diagram                     | 387 |
| Figure 9-10. | ACB Start Condition Timing Diagram                              | 388 |
| Figure 9-11. | ACB Data Bit Timing Diagram                                     | 388 |
| Figure 9-12. | Testing Setup for Slew Rate and Minimum Timing                  | 389 |
| Figure 9-13. | V/I Curves for PCI Output Signals                               | 390 |
| Figure 9-14. | PCICLK Timing and Measurement Points                            | 391 |
| Figure 9-15. | Load Circuits for Maximum Time Measurements                     | 392 |
| Figure 9-16. | Output Timing Measurement Conditions                            | 393 |
| Figure 9-17. | Input Timing Measurement Conditions                             | 394 |
| Figure 9-18. | PCI Reset Timing  | 394 |
| Figure 9-19. | Sub-ISA Read Operation Timing Diagram                           | 397 |
| Figure 9-20. | Sub-ISA Write Operation Timing Diagram                          | 398 |
| Figure 9-21. | LPC Output Timing Diagram                                       | 399 |
| Figure 9-22. | LPC Input Timing Diagram  | 399 |
| Figure 9-23. | IDE Reset Timing Diagram  | 400 |
| Figure 9-24. | Register Transfer to/from Device Timing Diagram                 | 402 |
| Figure 9-25. | PIO Data Transfer to/from Device Timing Diagram                 | 404 |
| Figure 9-26. | Multiword DMA Data Transfer Timing Diagram                      | 406 |
| Figure 9-27. | Initiating an UltraDMA Data in Burst Timing Diagram             | 408 |
| Figure 9-28. | Sustained UltraDMA Data In Burst Timing Diagram                 | 409 |
| Figure 9-29. | Host Pausing an UltraDMA Data In Burst Timing Diagram           | 410 |
| Figure 9-30. | Device Terminating an UltraDMA Data In Burst Timing Diagram     | 411 |
| Figure 9-31. | Host Terminating an UltraDMA Data In Burst Timing Diagram       | 412 |
| Figure 9-32. | Initiating an UltraDMA Data Out Burst Timing Diagram            | 413 |
| Figure 9-33. | Sustained UltraDMA Data Out Burst Timing Diagram                | 414 |
| Figure 9-34. | Device Pausing an UltraDMA Data Out Burst Timing Diagram        | 415 |
| Figure 9-35. | Host Terminating an UltraDMA Data Out Burst Timing Diagram      | 416 |
| Figure 9-36. | Device Terminating an UltraDMA Data Out Burst Timing Diagram    | 417 |
| Figure 9-37. | Data Signal Rise and Fall Timing Diagram                        | 420 |
| Figure 9-38. | Source Differential Data Jitter Timing Diagram                  | 420 |
| Figure 9-39. | EOP Width Timing Diagram  | 421 |
| Figure 9-40. | Receiver Jitter Tolerance Timing Diagram                        | 421 |
| Figure 9-41. | UART, Sharp-IR, SIR, and Consumer Remote Control Timing Diagram | 422 |
| Figure 9-42. | Fast IR (MIR and FIR) Timing Diagram                            | 423 |
| Figure 9-43. | Standard Parallel Port Typical Data Exchange Timing Diagram     | 424 |
| Figure 9-44. | Enhanced Parallel Port Timing Diagram                           | 425 |
| Figure 9-45. | ECP Forward Mode Timing Diagram                                 | 426 |

|              |  |     |
|--------------|--|-----|
| Figure 9-46. | ECP Reverse Mode Timing Diagram . . . . .  | 427 |
| Figure 9-47. | AC97 Reset Timing Diagram . . . . .  | 428 |
| Figure 9-48. | AC97 Sync Timing Diagram . . . . .   | 428 |
| Figure 9-49. | AC97 Clocks Diagram . . . . .  | 429 |
| Figure 9-50. | AC97 Data Timing Diagram . . . . .   | 430 |
| Figure 9-51. | AC97 Rise and Fall Timing Diagram . . . . .                                      | 431 |
| Figure 9-52. | AC97 Low Power Mode Timing Diagram . . . . .                                     | 432 |
| Figure 9-53. | PWRBTN# Trigger and ONCTL# Timing Diagram . . . . .                              | 433 |
| Figure 9-54. | GPWIO and ONCTL# Timing Diagram . . . . .  | 433 |
| Figure 9-55. | Power-Up Sequencing With PWRBTN# Timing Diagram . . . . .                        | 434 |
| Figure 9-56. | Power-Up Sequencing Without PWRBTN# Timing Diagram . . . . .                     | 435 |
| Figure 9-57. | TCK Measurement Points and Timing Diagram . . . . .                              | 436 |
| Figure 9-58. | JTAG Test Timing Diagram . . . . .   | 437 |
| Figure 10-1. | Heatsink Example . . . . .   | 440 |
| Figure 10-2. | 432-Terminal EBGA Package (Body Size: 40x40x1.72 mm; Pitch: 1.27 mm) . . . . .   | 441 |
| Figure 10-3. | 481-Terminal TEPBGA Package (Body Size: 40x40x2.38 mm; Pitch: 1.27 mm) . . . . . | 442 |





# List of Tables

|             |   |     |
|-------------|---|-----|
| Table 2-1.  | SC3200 Memory Controller Register Summary .....                         | 18  |
| Table 2-2.  | SC3200 Memory Controller Registers .....                                | 18  |
| Table 3-1.  | Signal Definitions Legend .....   | 27  |
| Table 3-2.  | 432-EBGA Ball Assignment - Sorted by Ball Number .....                  | 29  |
| Table 3-3.  | 432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name .....   | 38  |
| Table 3-4.  | 481-TEPBGA Ball Assignment - Sorted by Ball Number .....                | 43  |
| Table 3-5.  | 481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name ..... | 54  |
| Table 3-6.  | Strap Options .....   | 58  |
| Table 3-7.  | Two-Signal/Group Multiplexing .....                                     | 59  |
| Table 3-8.  | Three-Signal/Group Multiplexing .....                                   | 60  |
| Table 3-9.  | Four-Signal/Group Multiplexing .....                                    | 62  |
| Table 4-1.  | General Configuration Block Register Summary .....                      | 87  |
| Table 4-2.  | Multiplexing, Interrupt Selection, and Base Address Registers .....     | 88  |
| Table 4-3.  | WATCHDOG Registers .....  | 96  |
| Table 4-4.  | High-Resolution Timer Registers .....                                   | 98  |
| Table 4-5.  | Crystal Oscillator Circuit Components .....                             | 100 |
| Table 4-6.  | Core Clock Frequency .....  | 101 |
| Table 4-7.  | Strapped Core Clock Frequency .....                                     | 101 |
| Table 4-8.  | Clock Generator Configuration .....                                     | 103 |
| Table 5-1.  | SIO Configuration Options .....   | 108 |
| Table 5-2.  | LDN Assignments .....   | 108 |
| Table 5-3.  | Standard Configuration Registers .....                                  | 111 |
| Table 5-4.  | SIO Control and Configuration Register Map .....                        | 113 |
| Table 5-5.  | SIO Control and Configuration Registers .....                           | 113 |
| Table 5-6.  | Relevant RTC Configuration Registers .....                              | 114 |
| Table 5-7.  | RTC Configuration Registers .....                                       | 115 |
| Table 5-8.  | Relevant SWC Registers .....  | 116 |
| Table 5-9.  | Relevant IRCP/SP3 Registers .....                                       | 117 |
| Table 5-10. | IRCP/SP3 Configuration Register .....                                   | 117 |
| Table 5-11. | Relevant Serial Ports 1 and 2 Registers .....                           | 118 |
| Table 5-12. | Serial Ports 1 and 2 Configuration Register .....                       | 118 |
| Table 5-13. | Relevant ACB1 and ACB2 Registers .....                                  | 119 |
| Table 5-14. | ACB1 and ACB2 Configuration Register .....                              | 119 |
| Table 5-15. | Relevant Parallel Port Registers .....                                  | 120 |
| Table 5-16. | Parallel Port Configuration Register .....                              | 120 |
| Table 5-17. | Crystal Oscillator Circuit Components .....                             | 121 |
| Table 5-18. | System Power States .....   | 125 |
| Table 5-19. | RTC Register Map .....  | 127 |
| Table 5-20. | RTC Registers .....   | 127 |
| Table 5-21. | Divider Chain Control / Test Selection .....                            | 130 |
| Table 5-22. | Periodic Interrupt Rate Encoding .....                                  | 130 |
| Table 5-23. | BCD and Binary Formats .....  | 130 |
| Table 5-24. | Standard RAM Map .....  | 131 |
| Table 5-25. | Extended RAM Map .....  | 131 |
| Table 5-26. | Time Range Limits for CEIR Protocols .....                              | 132 |

|             |  |     |
|-------------|--|-----|
| Table 5-27. | Banks 0 and 1 - Common Control and Status Register Map . . . . .                         | 133 |
| Table 5-28. | Bank 1 - CEIR Wakeup Configuration and Control Register Map . . . . .                    | 133 |
| Table 5-29. | Banks 0 and 1 - Common Control and Status Registers . . . . .                            | 134 |
| Table 5-30. | Bank 1 - CEIR Wakeup Configuration and Control Registers . . . . .                       | 135 |
| Table 5-31. | ACB Register Map . . . . .   | 142 |
| Table 5-32. | ACB Registers . . . . .  | 142 |
| Table 5-33. | Parallel Port Register Map for First Level Offset . . . . .                              | 145 |
| Table 5-34. | Parallel Port Register Map for Second Level Offset . . . . .                             | 145 |
| Table 5-35. | Parallel Port Bit Map for First Level Offset . . . . .                                   | 146 |
| Table 5-36. | Parallel Port Bit Map for Second Level Offset . . . . .                                  | 146 |
| Table 5-37. | Bank 0 Register Map . . . . .  | 147 |
| Table 5-38. | Bank Selection Encoding . . . . .  | 148 |
| Table 5-39. | Bank 1 Register Map . . . . .  | 148 |
| Table 5-40. | Bank 2 Register Map . . . . .  | 148 |
| Table 5-41. | Bank 3 Register Map . . . . .  | 148 |
| Table 5-42. | Bank 0 Bit Map . . . . .   | 149 |
| Table 5-43. | Bank 1 Bit Map . . . . .   | 149 |
| Table 5-44. | Bank 2 Bit Map . . . . .   | 150 |
| Table 5-45. | Bank 3 Bit Map . . . . .   | 150 |
| Table 5-46. | Bank 0 Register Map . . . . .  | 151 |
| Table 5-47. | Bank Selection Encoding . . . . .  | 152 |
| Table 5-48. | Bank 1 Register Map . . . . .  | 152 |
| Table 5-49. | Bank 2 Register Map . . . . .  | 152 |
| Table 5-50. | Bank 3 Register Map . . . . .  | 153 |
| Table 5-51. | Bank 4 Register Map . . . . .  | 153 |
| Table 5-52. | Bank 5 Register Map . . . . .  | 153 |
| Table 5-53. | Bank 6 Register Map . . . . .  | 154 |
| Table 5-54. | Bank 7 Register Map . . . . .  | 154 |
| Table 5-55. | Bank 0 Bit Map . . . . .   | 154 |
| Table 5-56. | Bank 1 Bit Map . . . . .   | 155 |
| Table 5-57. | Bank 2 Bit Map . . . . .   | 155 |
| Table 5-58. | Bank 3 Bit Map . . . . .   | 155 |
| Table 5-59. | Bank 4 Bit Map . . . . .   | 155 |
| Table 5-60. | Bank 5 Bit Map . . . . .   | 156 |
| Table 5-61. | Bank 6 Bit Map . . . . .   | 156 |
| Table 5-62. | Bank 7 Bit Map . . . . .   | 156 |
| Table 6-1.  | Physical Region Descriptor Format . . . . .  | 161 |
| Table 6-2.  | UltraDMA/33 Signal Definitions . . . . .   | 162 |
| Table 6-3.  | Cycle Multiplexed PCI / Sub-ISA Balls . . . . .  | 167 |
| Table 6-4.  | PIC Interrupt Mapping . . . . .  | 171 |
| Table 6-5.  | Wakeup Events Capability . . . . .   | 175 |
| Table 6-6.  | Power Planes Control Signals vs. Sleep States . . . . .                                  | 176 |
| Table 6-7.  | Power Planes vs. Sleep/Global States . . . . .   | 176 |
| Table 6-8.  | Power Management Events . . . . .  | 176 |
| Table 6-9.  | Device Power Management Programming Summary . . . . .                                    | 182 |
| Table 6-10. | Bus Masters That Drive Specific Slots of the AC97 Interface . . . . .                    | 183 |
| Table 6-11. | Physical Region Descriptor Format . . . . .  | 184 |
| Table 6-12. | Cycle Types . . . . .  | 190 |
| Table 6-13. | PCI Configuration Address Register (0CF8h) . . . . .                                     | 191 |
| Table 6-14. | F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support Summary . . . . . | 192 |
| Table 6-15. | F0BAR0: GPIO Support Registers Summary . . . . .   | 195 |
| Table 6-16. | F0BAR1: LPC Support Registers Summary . . . . .  | 195 |
| Table 6-17. | F1: PCI Header Registers for SMI Status and ACPI Support Summary . . . . .               | 196 |
| Table 6-18. | F1BAR0: SMI Status Registers Summary . . . . .   | 196 |
| Table 6-19. | F1BAR1: ACPI Support Registers Summary . . . . .   | 197 |

|             |  |     |
|-------------|--|-----|
| Table 6-20. | F2: PCI Header Registers for IDE Controller Support Summary . . . . .                | 198 |
| Table 6-21. | F2BAR4: IDE Controller Support Registers Summary . . . . .                           | 199 |
| Table 6-22. | F3: PCI Header Registers for Audio Support Summary . . . . .                         | 199 |
| Table 6-23. | F3BAR0: Audio Support Registers Summary . . . . .                                    | 200 |
| Table 6-24. | F5: PCI Header Registers for X-Bus Expansion Support Summary . . . . .               | 201 |
| Table 6-25. | F5BAR0: I/O Control Support Registers Summary . . . . .                              | 201 |
| Table 6-26. | PCIUSB: USB PCI Configuration Register Summary . . . . .                             | 202 |
| Table 6-27. | USB_BAR: USB Controller Registers Summary . . . . .                                  | 203 |
| Table 6-28. | ISA Legacy I/O Register Summary . . . . .  | 204 |
| Table 6-29. | F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support . . . . .     | 206 |
| Table 6-30. | F0BAR0+I/O Offset: GPIO Configuration Registers . . . . .                            | 240 |
| Table 6-31. | F0BAR1+I/O Offset: LPC Interface Configuration Registers . . . . .                   | 244 |
| Table 6-32. | F1: PCI Header Registers for SMI Status and ACPI Support . . . . .                   | 252 |
| Table 6-33. | F1BAR0+I/O Offset: SMI Status Registers . . . . .                                    | 253 |
| Table 6-34. | F1BAR1+I/O Offset: ACPI Support Registers . . . . .                                  | 263 |
| Table 6-35. | F2: PCI Header/Channels 0 and 1 Registers for IDE Controller Configuration . . . . . | 273 |
| Table 6-36. | F2BAR4+I/O Offset: IDE Controller Configuration Registers . . . . .                  | 277 |
| Table 6-37. | F3: PCI Header Registers for Audio Configuration . . . . .                           | 279 |
| Table 6-38. | F3BAR0+Memory Offset: Audio Configuration Registers . . . . .                        | 280 |
| Table 6-39. | F5: PCI Header Registers for X-Bus Expansion . . . . .                               | 294 |
| Table 6-40. | F5BAR0+I/O Offset: X-Bus Expansion Registers . . . . .                               | 298 |
| Table 6-41. | PCIUSB: USB PCI Configuration Registers . . . . .                                    | 300 |
| Table 6-42. | USB_BAR+Memory Offset: USB Controller Registers . . . . .                            | 303 |
| Table 6-43. | DMA Channel Control Registers . . . . .  | 313 |
| Table 6-44. | DMA Page Registers . . . . .   | 318 |
| Table 6-45. | Programmable Interval Timer Registers . . . . .                                      | 319 |
| Table 6-46. | Programmable Interrupt Controller Registers . . . . .                                | 321 |
| Table 6-47. | Keyboard Controller Registers . . . . .  | 324 |
| Table 6-48. | Real-Time Clock Registers . . . . .  | 325 |
| Table 6-49. | Miscellaneous Registers . . . . .  | 325 |
| Table 7-1.  | Valid Mixing/Blending Configurations . . . . .                                       | 339 |
| Table 7-2.  | Truth Table for Alpha Blending . . . . .   | 341 |
| Table 7-3.  | F4: PCI Header Registers for Video Processor Support Summary . . . . .               | 345 |
| Table 7-4.  | F4BAR0: Video Processor Configuration Registers Summary . . . . .                    | 345 |
| Table 7-5.  | F4BAR2: VIP Support Registers Summary . . . . .                                      | 347 |
| Table 7-6.  | F4: PCI Header Registers for Video Processor Support Registers . . . . .             | 348 |
| Table 7-7.  | F4BAR0+Memory Offset: Video Processor Configuration Registers . . . . .              | 350 |
| Table 7-8.  | F4BAR2+Memory Offset: VIP Configuration Registers . . . . .                          | 363 |
| Table 8-1.  | JTAG Mode Instruction Support . . . . .  | 367 |
| Table 9-1.  | Electro Static Discharge (ESD) . . . . .   | 369 |
| Table 9-2.  | Absolute Maximum Ratings . . . . .   | 369 |
| Table 9-3.  | Operating Conditions . . . . .   | 370 |
| Table 9-4.  | Power Planes of External Interface Signals . . . . .                                 | 371 |
| Table 9-5.  | System Conditions Used to Measure SC3200 Current During On State . . . . .           | 372 |
| Table 9-6.  | DC Characteristics for On State . . . . .  | 372 |
| Table 9-7.  | DC Characteristics for Active Idle, Sleep, and Off States . . . . .                  | 373 |
| Table 9-8.  | Ball Capacitance and Inductance . . . . .  | 373 |
| Table 9-9.  | Balls with PU/PD Resistors . . . . .   | 374 |
| Table 9-10. | Buffer Types . . . . .   | 375 |
| Table 9-11. | Default Levels for Measurement of Switching Parameters . . . . .                     | 380 |
| Table 9-12. | Memory Controller Timing Parameters . . . . .  | 382 |
| Table 9-13. | Video Input Port Timing Parameters . . . . .   | 384 |
| Table 9-14. | TFT Timing Parameters . . . . .  | 385 |
| Table 9-15. | ACCESS.bus Input Timing Parameters . . . . .   | 386 |
| Table 9-16. | ACCESS.bus Output Timing Parameters . . . . .  | 386 |

|             |  |     |
|-------------|--|-----|
| Table 9-17. | PCI AC Specifications . . . . .  | 389 |
| Table 9-18. | PCI Clock Parameters . . . . .   | 391 |
| Table 9-19. | PCI Timing Parameters . . . . .  | 392 |
| Table 9-20. | Measurement Condition Parameters . . . . .                                   | 393 |
| Table 9-21. | Sub-ISA Timing Parameters . . . . .  | 395 |
| Table 9-22. | LPC and SERIRQ Timing Parameters . . . . .                                   | 399 |
| Table 9-23. | IDE General Timing Parameters . . . . .                                      | 400 |
| Table 9-24. | IDE Register Transfer to/from Device Timing Parameters . . . . .             | 401 |
| Table 9-25. | IDE PIO Data Transfer to/from Device Timing Parameters . . . . .             | 403 |
| Table 9-26. | IDE Multiword DMA Data Transfer Timing Parameters . . . . .                  | 405 |
| Table 9-27. | IDE UltraDMA Data Burst Timing Parameters . . . . .                          | 407 |
| Table 9-28. | USB Timing Parameters . . . . .  | 418 |
| Table 9-29. | UART, Sharp-IR, SIR, and Consumer Remote Control Timing Parameters . . . . . | 422 |
| Table 9-30. | Fast IR Port Timing Parameters . . . . .                                     | 423 |
| Table 9-31. | Standard Parallel Port Timing Parameters . . . . .                           | 424 |
| Table 9-33. | ECP Forward Mode Timing Parameters . . . . .                                 | 426 |
| Table 9-34. | ECP Reverse Mode Timing Parameters . . . . .                                 | 427 |
| Table 9-35. | AC Reset Timing Parameters . . . . .   | 428 |
| Table 9-36. | AC97 Sync Timing Parameters . . . . .  | 428 |
| Table 9-37. | AC97 Clocks Parameters . . . . .   | 429 |
| Table 9-38. | AC97 I/O Timing Parameters . . . . .   | 430 |
| Table 9-39. | AC97 Signal Rise and Fall Timing Parameters . . . . .                        | 431 |
| Table 9-40. | AC97 Low Power Mode Timing Parameters . . . . .                              | 432 |
| Table 9-41. | PWRBTN# Timing Parameters . . . . .  | 433 |
| Table 9-42. | Power Management Event (GPWIO) and ONCTL# Timing Parameters . . . . .        | 433 |
| Table 9-43. | Power-Up Sequence Using the Power Button Timing Parameters . . . . .         | 434 |
| Table 9-44. | Power-Up Sequence Not Using the Power Button Timing Parameters . . . . .     | 435 |
| Table 9-45. | JTAG Timing Parameters . . . . .   | 436 |
| Table 10-1. | $q_{JC}$ (x°C/W) . . . . .   | 439 |
| Table 10-2. | Case-to-Ambient Thermal Resistance Example @ 85°C . . . . .                  | 439 |
| Table A-1.  | Revision History . . . . .   | 443 |
| Table A-2.  | Edits to Current Revision . . . . .  | 445 |

# 1 AMD Geode™ SC3200 Processor

## 1.1 General Description

The AMD Geode™ SC3200 processor is a member of the AMD Geode family of fully integrated x86 system chips. The SC3200 processor includes:

- The Geode GX1 processor module combines advanced CPU performance with MMX™ support, fully accelerated 2D graphics, a 64-bit synchronous DRAM (SDRAM) interface, a PCI bus controller, and a display controller.
- A low-power TFT Video Processor module with a Video Input Port (VIP), and a hardware video accelerator for scaling, filtering, and color space conversion.

- The Core Logic module includes: PC/AT functionality, a USB interface, an IDE interface, a PCI bus interface, an LPC bus interface, Advanced Configuration Power Interface (ACPI) version 1.0 compliant power management, and an audio codec interface.
- The SuperI/O module has: three serial ports (UART1, UART2, and UART3 with fast infrared), a parallel port, two ACCESS.bus (ACB) interfaces, and a real-time clock (RTC).

These features, combined with the device's low power consumption, enable a small form factor design making it ideal as the core for a WebPAD™ system application.

Figure 1-1 shows the relationships between the modules.

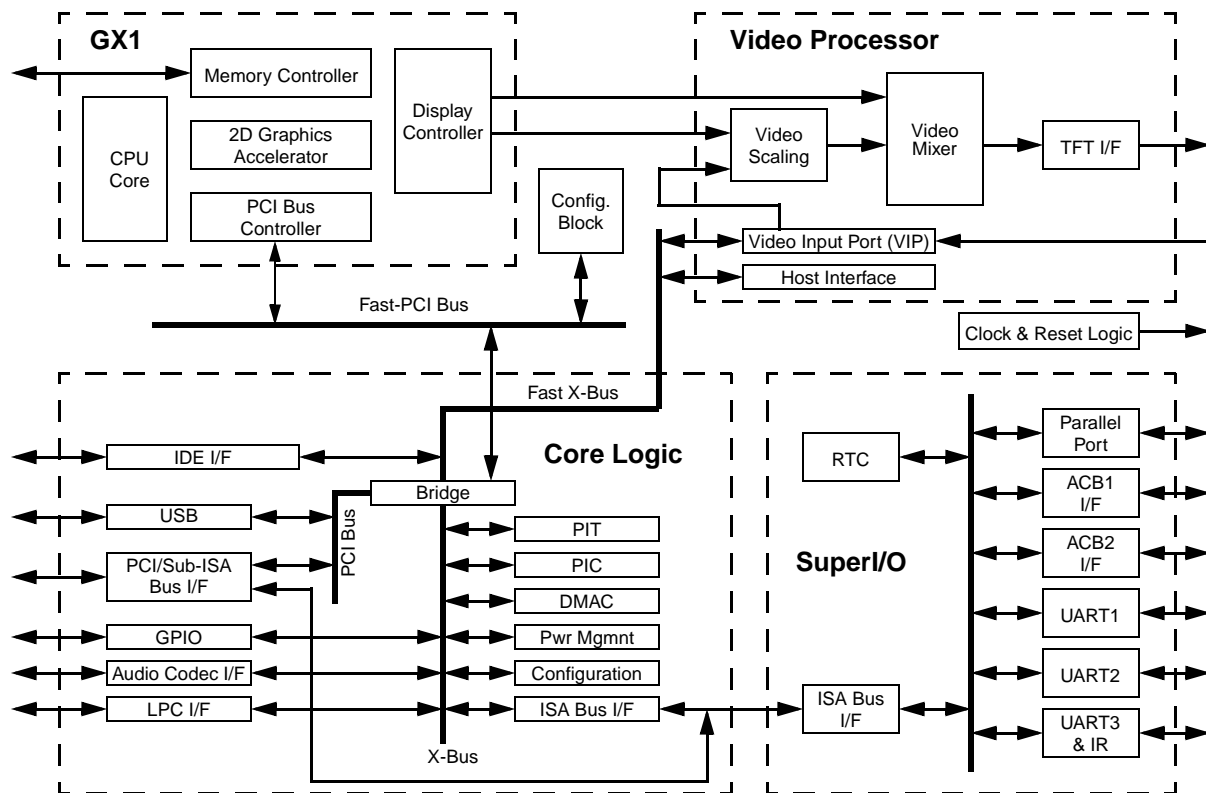


Figure 1-1. Block Diagram

## 1.2 Features

### General Features

- 32-Bit x86 processor, up to 266 MHz, with MMX instruction set support
- Memory controller with 64-bit SDRAM interface
- 2D graphics accelerator
- CCIR-656 video input port with direct video for full screen display
- PC/AT functionality
- PCI bus controller
- IDE interface, two channels
- USB, three ports, OHCI (OpenHost Controller Interface) version 1.0 compliant
- Audio, AC97/AMC97 version 2.0 compliant
- Virtual System Architecture™ (VSA) technology support
- Power management, ACPI (Advanced Configuration Power Interface) version 1.0 compliant
- Package:
  - 432-Terminal EBGA (Enhanced Ball Grid Array)
  - 481-Terminal TEPBGA (Thermally Enhanced Plastic Ball Grid Array)

### GX1 Processor Module

- CPU Core:
  - 32-Bit x86, 266 MHz, with MMX compatible instruction set support
  - 16 KB unified L1 cache
  - Integrated FPU (Floating Point Unit)
  - Re-entrant SMM (System Management Mode) enhanced for VSA
- 2D Graphics Accelerator:
  - Accelerates BitBLTs, line draw and text
  - Supports all 256 raster operations
  - Supports transparent BLTs
  - Runs at core clock frequency
- Memory Controller:
  - 64-Bit SDRAM interface
  - 66 MHz to 100 MHz frequency range
  - Direct interface with CPU/cache, display controller and 2D graphic accelerator
  - Supports clock suspend and power-down/self-refresh
  - Up to two banks of SDRAM (8 devices total) or one SODIMM
- Display Controller:
  - Hardware graphics frame buffer compress/decompress
  - Hardware cursor, 32x32 pixels

### Video Processor Module

- Video Accelerator:
  - Flexible video scaling support of up to 800% (horizontally and vertically)
  - Bilinear interpolation filters (with two taps, and eight phases) to smooth output video
- Video/Graphics Mixer:
  - 8-bit value alpha blending
  - Three blending windows with constant alpha value
  - Color key
- Video Input Port (VIP):
  - Video capture or display
  - CCIR-656 and VESA Video Interface Port v1.1 compliant
  - Lock display timing to video input timing (GenLock)
  - Able to transfer video data into main memory
  - Direct video transfer for full screen display
  - Separate memory location for VBI
- TFT Interface:
  - Direct connection to TFT panels
  - 800x600 non-interlaced TFT @ 16 bpp graphics, up to 85 Hz
  - 1024x768 non-interlaced TFT @ 16 bpp graphics, up to 75 Hz
  - TFT on IDE: FPCLK max is 40 MHz
  - TFT on Parallel Port: FPCLK max is 80 MHz

### Core Logic Module

- Audio Codec Interface:
  - AC97/AMC97 (Rev. 2.0) codec interface
  - Six DMA channels
- PC/AT Functionality:
  - Programmable Interrupt Controller (PIC), 8259A-equivalent
  - Programmable Interval Timer (PIT), 8254-equivalent
  - DMA Controller (DMAC), 8237-equivalent
- Power Management:
  - ACPI v1.0 compliant
  - Sx state control of three power planes
  - Cx/Sx state control of clocks and PLLs
  - Thermal event input
  - Wakeup event support:
    - Three general-purpose events
    - AC97 codec event
    - UART2 RI# signal
    - Infrared (IR) event
- General Purpose I/Os (GPIOs):
  - 27 multiplexed GPIO signals
- Low Pin Count (LPC) Bus Interface:
  - Specification v1.0 compatible

- PCI Bus Interface:
  - PCI v2.1 compliant with wakeup capability
  - 32-Bit data path, up to 33 MHz
  - Glueless interface for an external PCI device
  - Fixed priority
  - 3.3V signal support only
- Sub-ISA Bus Interface:
  - Up to 16 MB addressing
  - Supports a chip select for ROM or Flash EPROM boot device
  - Supports either:
    - M-Systems DiskOnChip DOC2000 Flash file system
    - NAND EEPROM
  - Supports up to two chip selects for external I/O devices
  - 8-Bit (optional 16-bit) data bus width
  - Shares balls with PCI signals
  - Is not a subtractive agent
- IDE Interface:
  - Two IDE channels for up to four external IDE devices
  - Supports ATA-33 synchronous DMA mode transfers, up to 33 MB/s
- Universal Serial Bus (USB):
  - USB OpenHCI v1.0 compliant
  - Three ports

### SuperI/O Module

- Real-Time Clock (RTC):
  - DS1287, MC146818 and PC87911 compatible
  - Multi-century calendar
- ACCESS.bus (ACB) Interface:
  - Two ACB interface ports
- Parallel Port:
  - EPP 1.9 compliant
  - IEEE 1284 ECP compliant, including level 2
- Serial Port (UART):
  - UART1, 16550A compatible (SIN, SOUT, BOUT pins), used for SmartCard interface
  - UART2, 16550A compatible
  - Enhanced UART with fast Infrared (IR)

### Other Features

- High-Resolution Timer:
  - 32-Bit counter with 1  $\mu$ s count interval
- WATCHDOG Timer:
  - Interfaces to INTR, SMI, Reset
- Clocks:
  - Input (external crystals):
    - 32.768 KHz (internal clock oscillator)
    - 27 MHz (internal clock oscillator)
  - Output:
    - AC97 clock (24.576 MHz)
    - Memory controller clock (66 MHz to 100 MHz)
    - PCI clock (33 MHz)
- JTAG Testability:
  - Bypass, Extest, Sample/Preload, IDcode, Clamp, HiZ
- Voltages
  - Internal logic: 266 or 233 MHz @ 1.8V
  - Standby logic: 266 or 233 MHz @ 1.8V
  - I/O: 3.3V
  - Standby I/O: 3.3V
  - Battery (if used): 3.0V





# Architecture Overview

# 2

As illustrated in Figure 1-1 on page 13, the SC3200 processor contains the following modules in one integrated device:

- **GX1 Module:**
  - Combines advanced CPU performance with MMX support, fully accelerated 2D graphics, a 64-bit synchronous DRAM (SDRAM) interface and a PCI bus controller. Integrates GX1 silicon revision 8.1.1.
- **Video Processor Module:**
  - A low-power TFT support module with a video input port, and a hardware video accelerator for scaling, filtering and color space conversion.
- **Core Logic Module:**
  - Includes PC/AT functionality, an IDE interface, a Universal Serial Bus (USB) interface, ACPI v1.0 compliant power management, and an audio codec interface.
- **SuperI/O Module:**
  - Includes two Serial Ports, an Infrared (IR) Port, a Parallel Port, two ACCESS.bus interfaces, and a Real-Time Clock (RTC).

## 2.1 GX1 Module

The GX1 processor (silicon revision 8.1.1) is the central module of the SC3200. For detailed information regarding the GX1 module, refer to the *AMD Geode™ GX1 Processor Data Book* and the *AMD Geode™ GX1 Processor Silicon Revision 8.1.1 Specification Update* documents.

The SC3200 processor's device ID is contained in the GX1 module. Software can detect the revision by reading the DIR0 and DIR1 Configuration registers (see Configuration registers in the *AMD Geode™ GX1 Processor Data Book*). The *AMD Geode™ SC3200 Specification Update* document contains the specific values.

### 2.1.1 Memory Controller

The GX1 module is connected to external SDRAM devices. For more information see Section 3.4.2 "Memory Interface Signals" on page 65, and the "Memory Controller" chapter in the *AMD Geode™ GX1 Processor Data Book*.

There are some differences in the SC3200 processor's memory controller and the stand-alone GX1 processor's memory controller:

- 1) There is drive strength/slew control in the SC3200 that is not in the GX1. The bits that control this function are in the MC\_MEM\_CNTRL1 and MC\_MEM\_CNTRL2 registers. In the GX1 processor, these bits are marked as reserved.
- 2) The SC3200 supports two banks of memory. The GX1 supports four banks of memory. In addition, the SC3200 supports a maximum of eight devices and the GX1 supports up to 32 devices. With this difference, the MC\_BANK\_CFG register is different.

Table 2-1 summarizes the 32-bit registers contained in the SC3200 processor's memory controller. Table 2-2 gives detailed register/bit formats.

Table 2-1. SC3200 Memory Controller Register Summary

| GX_BASE+ Memory Offset | Width (Bits) | Type | Name/Function   | Reset Value |
|------------------------|--------------|------|---|-------------|
| 8400h-8403h            | 32           | R/W  | <b>MC_MEM_CNTRL1.</b> Memory Controller Control Register 1            | 248C0040h   |
| 8404h-8407h            | 32           | R/W  | <b>MC_MEM_CNTRL2.</b> Memory Controller Control Register 2            | 00000801h   |
| 8408h-840Bh            | 32           | R/W  | <b>MC_BANK_CFG.</b> Memory Controller Bank Configuration              | 41104110h   |
| 840Ch-840Fh            | 32           | R/W  | <b>MC_SYNC_TIM1.</b> Memory Controller Synchronous Timing Register 1  | 2A733225h   |
| 8414h-8417h            | 32           | R/W  | <b>MC_GBASE_ADD.</b> Memory Controller Graphics Base Address Register | 00000000h   |
| 8418h-841Bh            | 32           | R/W  | <b>MC_DR_ADD.</b> Memory Controller Dirty RAM Address Register        | 00000000h   |
| 841Ch-841Fh            | 32           | R/W  | <b>MC_DR_ACC.</b> Memory Controller Dirty RAM Access Register         | 0000000xh   |

Table 2-2. SC3200 Memory Controller Registers

| Bit                         | Description   |
|-----------------------------|---|
| <b>GX_BASE+ 8400h-8403h</b> | <b>MC_MEM_CNTRL1 (R/W)</b> <span style="float: right;"><b>Reset Value: 248C0040h</b></span>   |
| 31:30                       | <b>MDCTL</b> (MD[63:0] Drive Strength). 11 is strongest, 00 is weakest.   |
| 29                          | <b>RSVD (Reserved)</b> Write as 0.  |
| 28:27                       | <b>MABACTL</b> (MA[12:0] and BA[1:0] Drive Strength). 11 is strongest, 00 is weakest.   |
| 26                          | <b>RSVD (Reserved)</b> . Write as 0.  |
| 25:24                       | <b>MEMCTL</b> (RASA#, CASA#, WEA#, CS[1:0]#, CKEA, DQM[7:0] Drive Strength). 11 is strongest, 00 is weakest.  |
| 23:22                       | <b>RSVD (Reserved)</b> . Write as 0.  |
| 21                          | <b>RSVD (Reserved)</b> . Must be written as 0. Wait state on the X-Bus x_data during read cycles - for debug only.  |
| 20:18                       | <b>SDCLKRATE (SDRAM Clock Ratio)</b> . Selects SDRAM clock ratio.<br>000: Reserved <span style="margin-left: 100px;">100: ÷ 3.5</span><br>001: ÷ 2 <span style="margin-left: 100px;">101: ÷ 4</span><br>010: ÷ 2.5 <span style="margin-left: 100px;">110: ÷ 4.5</span><br>011: ÷ 3 (Default) <span style="margin-left: 100px;">111: ÷ 5</span><br>Ratio does not take effect until the SDCLKSTRT bit (bit 17 of this register) transitions from 0 to 1. |
| 17                          | <b>SDCLKSTRT (Start SDCLK)</b> . Start operating SDCLK using the new ratio and shift value (selected in bits [20:18] of this register).<br>0: Clear.<br>1: Enable.<br>This bit must transition from zero (written to zero) to one (written to one) in order to start SDCLK or to change the shift value.  |
| 16:8                        | <b>RFSHRATE (Refresh Interval)</b> . This field determines the number of processor core clocks multiplied by 64 between refresh cycles to the DRAM. By default, the refresh interval is 00h. Refresh is turned off by default.  |
| 7:6                         | <b>RFSHSTAG (Refresh Staggering)</b> . This field determines number of clocks between the RFSH commands to each of the four banks during refresh cycles:<br>00: 0 SDRAM clocks<br>01: 1 SDRAM clocks (Default)<br>10: 2 SDRAM clocks<br>11: 4 SDRAM clocks<br>Staggering is used to help reduce power spikes during refresh by refreshing one bank at a time. If only one bank is installed, this field must be written as 00.                          |
| 5                           | <b>2CLKADDR (Two Clock Address Setup)</b> . Assert memory address for one extra clock before CS# is asserted.<br>0: Disable.<br>1: Enable.<br>This can be used to compensate for address setup at high frequencies and/or high loads.   |

Table 2-2. SC3200 Memory Controller Registers (Continued)

| Bit                           | Description   |
|-------------------------------|---|
| 4                             | <b>RFSHTST (Test Refresh).</b> This bit, when set high, generates a refresh request. This bit is only used for testing purposes.  |
| 3                             | <b>XBUSARB (X-Bus Round Robin).</b> When round robin is enabled, processor, graphics pipeline, and low priority display controller requests are arbitrated at the same priority level. When disabled, processor requests are arbitrated at a higher priority level. High priority Display Controller requests always have the highest arbitration priority.<br>0: Disable.<br>1: Enable round robin.  |
| 2                             | <b>SMM_MAP (SMM Region Mapping).</b> Maps the SMM memory region at GX_BASE+400000 to physical address A0000 to BFFFF in SDRAM.<br>0: Disable.<br>1: Enable.   |
| 1                             | <b>RSVD (Reserved).</b> Write as 0.   |
| 0                             | <b>SDRAMPRG (Program SDRAM).</b> When this bit is set, the memory controller will program the SDRAM MRS register using LTMODE in MC_SYNC_TIM1.<br>This bit must transition from zero (written to zero) to one (written to one) in order to program the SDRAM devices.   |
| <b>GX_BASE+8404h-8407h</b>    |   |
| <b>MC_MEM_CNTRL2 (R/W)</b>    |   |
| <b>Reset Value: 00000801h</b> |   |
| 31:14                         | <b>RSVD (Reserved).</b> Write as 0.   |
| 13:12                         | <b>SDCLKCTL (SDCLK High Drive/Slew Control).</b> Controls the high drive and slew rate of SDCLK[3:0] and SDCLK_OUT. 11 is strongest, 00 is weakest.   |
| 11                            | <b>RSVD (Reserved).</b> Write as 0.   |
| 10                            | <b>SDCLK0MSK# (Enable SDCLK_OUT).</b> Turns on the output.<br>0: Enable.<br>1: Disable.   |
| 9                             | <b>SDCLK3MSK# (Enable SDCLK3).</b> Turns on the output.<br>0: Enable.<br>1: Disable.  |
| 8                             | <b>SDCLK2MSK# (Enable SDCLK2).</b> Turns on the output.<br>0: Enable.<br>1: Disable.  |
| 7                             | <b>SDCLK1MSK# (Enable SDCLK1).</b> Turns on the output. 0<br>0: Enable.<br>1: Disable.  |
| 6                             | <b>SDCLK0MSK# (Enable SDCLK0).</b> Turns on the output.<br>0: Enable.<br>1: Disable.  |
| 5:3                           | <b>SHFTSDCLK (Shift SDCLK).</b> This function allows shifting SDCLK to meet SDRAM setup and hold time requirements. The shift function will not take effect until the SDCLKSTRT bit (bit 17 of MC_MEM_CNTRL1) transitions from 0 to 1:<br>000: No shift<br>001: Shift 0.5 core clock<br>010: Shift 1 core clock<br>011: Shift 1.5 core clock<br>100: Shift 2 core clocks<br>101: Shift 2.5 core clocks<br>110: Shift 3 core clocks<br>111: Reserved |
| 2                             | <b>RSVD (Reserved).</b> Write as 0.   |
| 1                             | <b>RD (Read Data Phase).</b> Selects if read data is latched one or two core clock after the rising edge of SDCLK.<br>0: 1 Core clock.<br>1: 2 Core clocks.   |
| 0                             | <b>FSTRDMSK (Fast Read Mask).</b> Do not allow core reads to bypass the request FIFO.<br>0: Disable.<br>1: Enable.  |

Table 2-2. SC3200 Memory Controller Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>GX_BASE+8408h-840Bh</b> <span style="float:right"><b>MC_BANK_CFG (R/W)</b></span> <span style="float:right"><b>Reset Value: 41104110h</b></span>  |  |
| 31:16  | <b>RSVD (Reserved).</b> Write as 0070h   |
| 15   | <b>RSVD (Reserved).</b> Write as 0.  |
| 14   | <b>SODIMM_MOD_BNK (SODIMM Module Banks - Banks 0 and 1).</b> Selects number of module banks installed per SODIMM for SODIMM:<br>0: 1 Module bank (Bank 0 only)<br>1: 2 Module banks (Bank 0 and 1)   |
| 13   | <b>RSVD (Reserved).</b> Write as 0.  |
| 12   | <b>SODIMM_COMP_BNK (SODIMM Component Banks - Banks 0 and 1).</b> Selects the number of component banks per module bank for SODIMM:<br>0: 2 Component banks<br>1: 4 Component banks<br>Banks 0 and 1 must have the same number of component banks.  |
| 11   | <b>RSVD (Reserved).</b> Write as 0.  |
| 10:8   | <b>SODIMM_SZ (SODIMM Size - Banks 0 and 1).</b> Selects the size of SODIMM:<br>000: 4 MB      010: 16 MB      100: 64 MB      110: 256 MB<br>001: 8 MB      011: 32 MB      101: 128 MB      111: 512 MB<br>This size is the total of both banks 0 and 1. Also, banks 0 and 1 must be the same size.   |
| 7  | <b>RSVD (Reserved).</b> Write as 0.  |
| 6:4  | <b>SODIMM_PG_SZ (SODIMM Page Size - Banks 0 and 1).</b> Selects the page size of SODIMM:<br>000: 1 KB      010: 4 KB      1xx: 16 KB<br>001: 2 KB      011: 8 KB      111: SODIMM not installed<br>Both banks 0 and 1 must have the same page size.  |
| 3:0  | <b>RSVD (Reserved).</b> Write as 0.  |
| <b>GX_BASE+840Ch-840Fh</b> <span style="float:right"><b>MC_SYNC_TIM1 (R/W)</b></span> <span style="float:right"><b>Reset Value: 2A733225h</b></span> |  |
| 31   | <b>RSVD (Reserved).</b> Write as 0.  |
| 30:28  | <b>LTMODE (CAS Latency).</b> CAS latency is the delay, in SDRAM clock cycles, between the registration of a read command and the availability of the first piece of output data. This parameter significantly affects system performance. Optimal setting should be used. If an SODIMM is used, BIOS can interrogate EEPROM across the ACCESS.bus interface to determine this value:<br>000: Reserved      010: 2 CLK      100: 4 CLK      110: 6 CLK<br>001: Reserved      011: 3 CLK      101: 5 CLK      111: 7 CLK<br>This field will not take effect until SDRAMPRG (bit 0 of MC_MEM_CNTRL1) transitions from 0 to 1. |
| 27:24  | <b>RC (RFSH to RFSH/ACT Command Period, tRC).</b> Minimum number of SDRAM clock between RFSH and RFSH/ACT commands:<br>0000: Reserved      0100: 5 CLK      1000: 9 CLK      1100: 13 CLK<br>0001: 2 CLK      0101: 6 CLK      1001: 10 CLK      1101: 14 CLK<br>0010: 3 CLK      0110: 7 CLK      1010: 11 CLK      1110: 15 CLK<br>0011: 4 CLK      0111: 8 CLK      1011: 12 CLK      1111: 16 CLK  |
| 23:20  | <b>RAS (ACT to PRE Command Period, tRAS).</b> Minimum number of SDRAM clocks between ACT and PRE commands:<br>0000: Reserved      0100: 5 CLK      1000: 9 CLK      1100: 13 CLK<br>0001: 2 CLK      0101: 6 CLK      1001: 10 CLK      1101: 14 CLK<br>0010: 3 CLK      0110: 7 CLK      1010: 11 CLK      1110: 15 CLK<br>0011: 4 CLK      0111: 8 CLK      1011: 12 CLK      1111: 16 CLK   |
| 19   | <b>RSVD (Reserved).</b> Write as 0.  |
| 18:16  | <b>RP (PRE to ACT Command Period, tRP).</b> Minimum number of SDRAM clocks between PRE and ACT commands:<br>000: Reserved      010: 2 CLK      100: 4 CLK      110: 6 CLK<br>001: 1 CLK      011: 3 CLK      101: 5 CLK      111: 7 CLK  |
| 15   | <b>RSVD (Reserved).</b> Write as 0.  |
| 14:12  | <b>RCD (Delay Time ACT to READ/WRT Command, tRCD).</b> Minimum number of SDRAM clock between ACT and READ/WRT commands. This parameter significantly affects system performance. Optimal setting should be used:<br>000: Reserved      010: 2 CLK      100: 4 CLK      110: 6 CLK<br>001: 1 CLK      011: 3 CLK      101: 5 CLK      111: 7 CLK  |



### 2.1.2 Fast-PCI Bus

The GX1 module communicates with the Core Logic module via a Fast-PCI bus that can work at up to 66 MHz. The Fast-PCI bus is internal for the SC3200 and is connected to the General Configuration Block (see Section 4.0 on page 87 for details on the General Configuration Block).

This bus supports seven bus masters. The requests (REQs) are fixed in priority. The seven bus masters in order of priority are:

- 1) VIP
- 2) IDE Channel 0
- 3) IDE Channel 1
- 4) Audio
- 5) USB
- 6) External REQ0#
- 7) External REQ1#

### 2.1.3 Display

The GX1 module generates display timing, and controls internal VSYNC and HSYNC signals of the Video Processor module.

The GX1 module interfaces with the Video Processor via a video data bus and a graphics data bus.

- **Video data.** The GX1 module uses the core clock, divided by 2 or 4 (typically 100 - 133 MHz). It drives the video data using this clock. Internal signals VID\_VAL and VID\_RDY are used as data-flow handshake signals between the GX1 module and the Video Processor.
- **Graphics data.** The GX1 module uses the internal signal DCLK, supplied by the PLL of the Video Processor, to drive the 18-bit graphics-data bus of the Video Processor. Each six bits of this bus define a different color. Each of these 6-bit color definitions is expanded (by adding two zero LSB lines) to form an 8-bit bus, at the Video Processor.

For more information about the GX1 module's interface to the Video Processor, see the "Display Controller" chapter in the *AMD Geode™ GX1 Processor Data Book*.

## 2.2 Video Processor Module

The Video Processor provides high resolution and graphics for a TFT/DSTN interface. The following subsections provide a summary of how the Video Processor interfaces with the other modules of the SC3200. For detailed information about the Video Processor, see Section 7.0 "Video Processor Module" on page 327.

### 2.2.1 GX1 Module Interface

The Video Processor is connected to the GX1 module in the following way:

- The Video Processor's DOTCLK output signal is used as the GX1 module's DCLK input signal.
- The GX1 module's PCLK output signal is used as the GFXCLK input signal of the Video Processor.

### 2.2.2 Video Input Port

The Video Input Port (VIP) within the Video Processor contains a standard interface that is typically connected to a media processor or TV encoder. The clock is supplied by the externally connected device; typically at 27 MHz.

Video input can be sent to the GX1 module's video frame buffer (Capture Video mode) or can be used directly (Direct Video mode).

### 2.2.3 Core Logic Module Interface

The Video Processor interfaces to the Core Logic module for accessing PCI function configuration registers.

## 2.3 Core Logic Module

The Core Logic module is described in detail in Section 6.0 "Core Logic Module" on page 157.

The Core Logic module is connected to the Fast-PCI bus. It uses signal AD28 as the IDSEL for all PCI configuration functions except for USB which uses AD29.

### 2.3.1 Other Core Logic Module Interfaces

The following interfaces of the Core Logic module are implemented via external balls of the SC3200. Each interface is listed below with a reference to the descriptions of the relevant balls.

- IDE: See Section 3.4.9 "IDE Interface Signals" on page 75.
- AC97: See Section 3.4.14 "AC97 Audio Interface Signals" on page 80.
- PCI: See Section 3.4.6 "PCI Bus Interface Signals" on page 68.
- USB: See Section 3.4.10 "Universal Serial Bus (USB) Interface Signals" on page 76. The USB function uses signal AD29 as the IDSEL for PCI configuration.
- LPC: See Section 3.4.8 "Low Pin Count (LPC) Bus Interface Signals" on page 74.

- Sub-ISA: See Section 3.4.7 "Sub-ISA Interface Signals" on page 73, Section 6.2.5 "Sub-ISA Bus Interface" on page 163, and Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88
- GPIO: See Section 3.4.16 "GPIO Interface Signals" on page 82.
- More detailed information about each of these interfaces is provided in Section 6.2 "Module Architecture" on page 158.
- Super/IO Block Interfaces: See Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88, Section 3.4.5 "ACCESS.bus Interface Signals" on page 67, Section 3.4.13 "Fast Infrared (IR) Port Interface Signals" on page 79, and Section 3.4.12 "Parallel Port Interface Signals" on page 78.

The Core Logic module interface to the GX1 module consists of seven miscellaneous connections, the PCI bus interface signals, plus the display controller connections. Note that the PC/AT legacy signals NMI, WM\_RST, and A20M are all virtual functions executed in SMM (System Management Mode) by the BIOS.

- P SERIAL is a one-way serial bus from the GX1 to the Core Logic module used to communicate power-management states and VSYNC information for VGA emulation.
- IRQ13 is an input from the GX1 module indicating that a floating point error was detected and that INTR should be asserted.
- INTR is the level output from the integrated 8259A PICs and is asserted if an unmasked interrupt request (IRQn) is sampled active.
- SMI# is a level-sensitive interrupt to the GX1 module that can be configured to assert on a number of different system events. After an SMI# assertion, SMM is entered and program execution begins at the base of the SMM address space. Once asserted, SMI# remains active until the SMI source is cleared.
- SUSP# and SUSPA# are handshake signals for implementing CPU Clock Stop and clock throttling.
- CPU\_RST resets the CPU and is asserted for approximately 100  $\mu$ s after the negation of POR#.
- PCI bus interface signals.

## 2.4 Super I/O Module

The SuperI/O (SIO) module is a PC98 and ACPI compliant SIO that offers a single-cell solution to the most commonly used ISA peripherals.

The SIO module incorporates: two Serial Ports, an Infrared Communication Port that supports FIR, MIR, HP-SIR, Sharp-IR, and Consumer Electronics-IR, a full IEEE 1284 Parallel Port, two ACCESS.bus Interface (ACB) ports, System Wakeup Control (SWC), and a Real-Time Clock (RTC) that provides RTC timekeeping.

## 2.5 Clock, Timers, and Reset Logic

In addition to the four main modules (i.e., GX1, Core Logic, Video Processor and SIO) that make up the SC3200, the following blocks of logic have also been integrated into the SC3200:

- Clock Generators as described in Section 4.5 "Clock Generators and PLLs" on page 99.
- Configuration Registers as described in Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88.
- A WATCHDOG timer as described in Section 4.3 "WATCHDOG" on page 95.
- A High-Resolution timer as described in Section 4.4 "High-Resolution Timer" on page 97.

### 2.5.1 Reset Logic

This section provides a description of the reset flow of the SC3200.

#### 2.5.1.1 Power-On Reset

Power-on reset is triggered by assertion of the POR# signal. Upon power-on reset, the following things happen:

- Strap balls are sampled.
- PLL4, PLL5, and PLL6 are reset, disabling their output. When the POR# signal is negated, the clocks lock and then each PLL outputs its clock. PLL6 is the last clock generator to output a clock. See Section 4.5 "Clock Generators and PLLs" on page 99.
- Certain WATCHDOG and High-Resolution Timer register bits are cleared.

#### 2.5.1.2 System Reset

System reset causes signal PCIRST# to be issued, thus triggering a reset of all PCI and LPC agents. A system reset is triggered by any of the following events:

- Power-on, as indicated by POR# signal assertion.
- A WATCHDOG reset event (see Section 4.3.2 "WATCHDOG Registers" on page 96).
- Software initiated system reset.

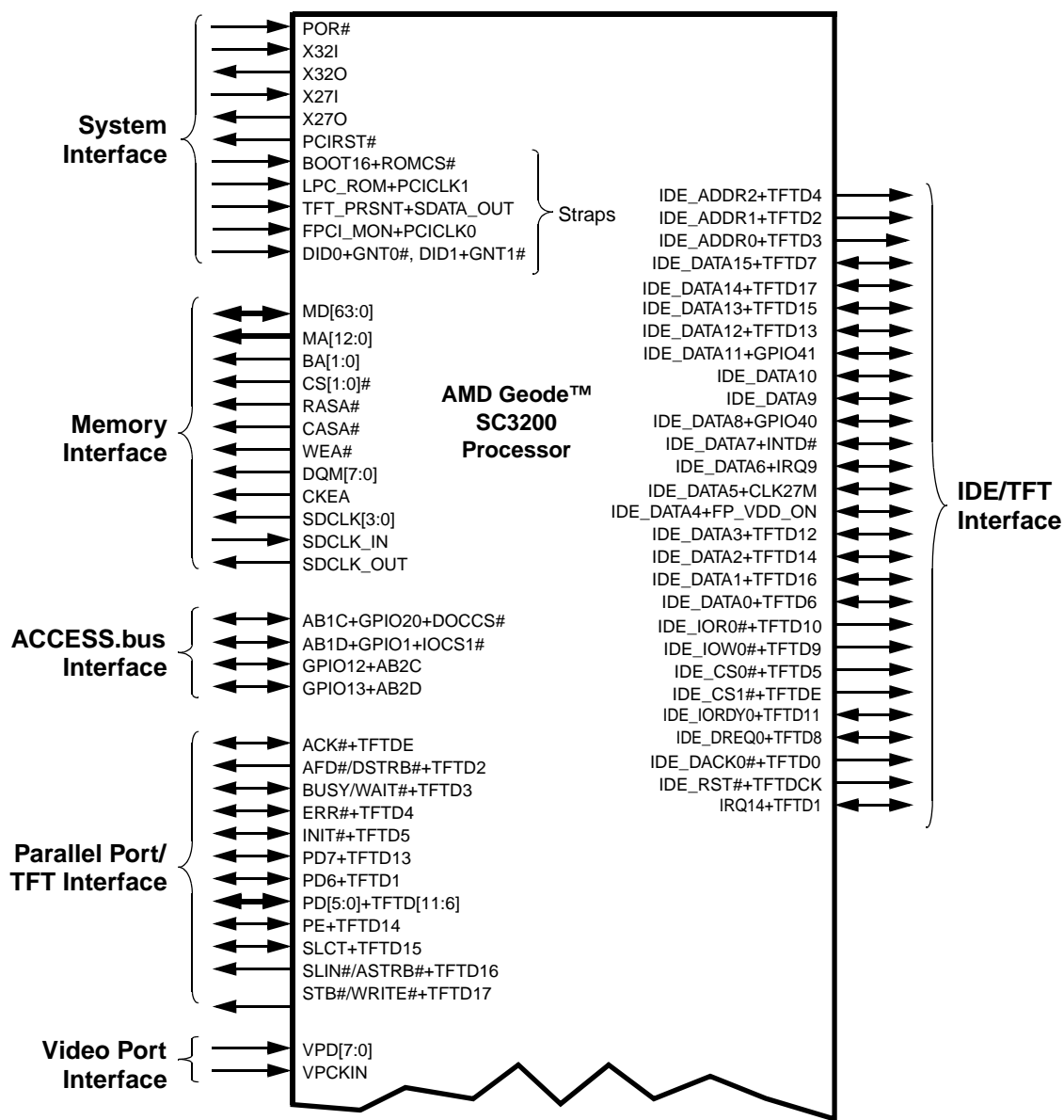




# Signal Definitions 3

This section defines the signals and describes the external interface of the SC3200. Figure 2-1 shows the signals organized by their functional groups. Where signals are multiplexed, the default signal name is listed first and is

separated by a plus sign (+). A slash (/) in a signal name means that the function is always enabled and available (i.e., cycle multiplexed).



**Note:** Straps are not the default signal, shown with system signals for reader convenience. However, also listed in figure with the appropriate functional group.

**Figure 3-1. Signal Groups**

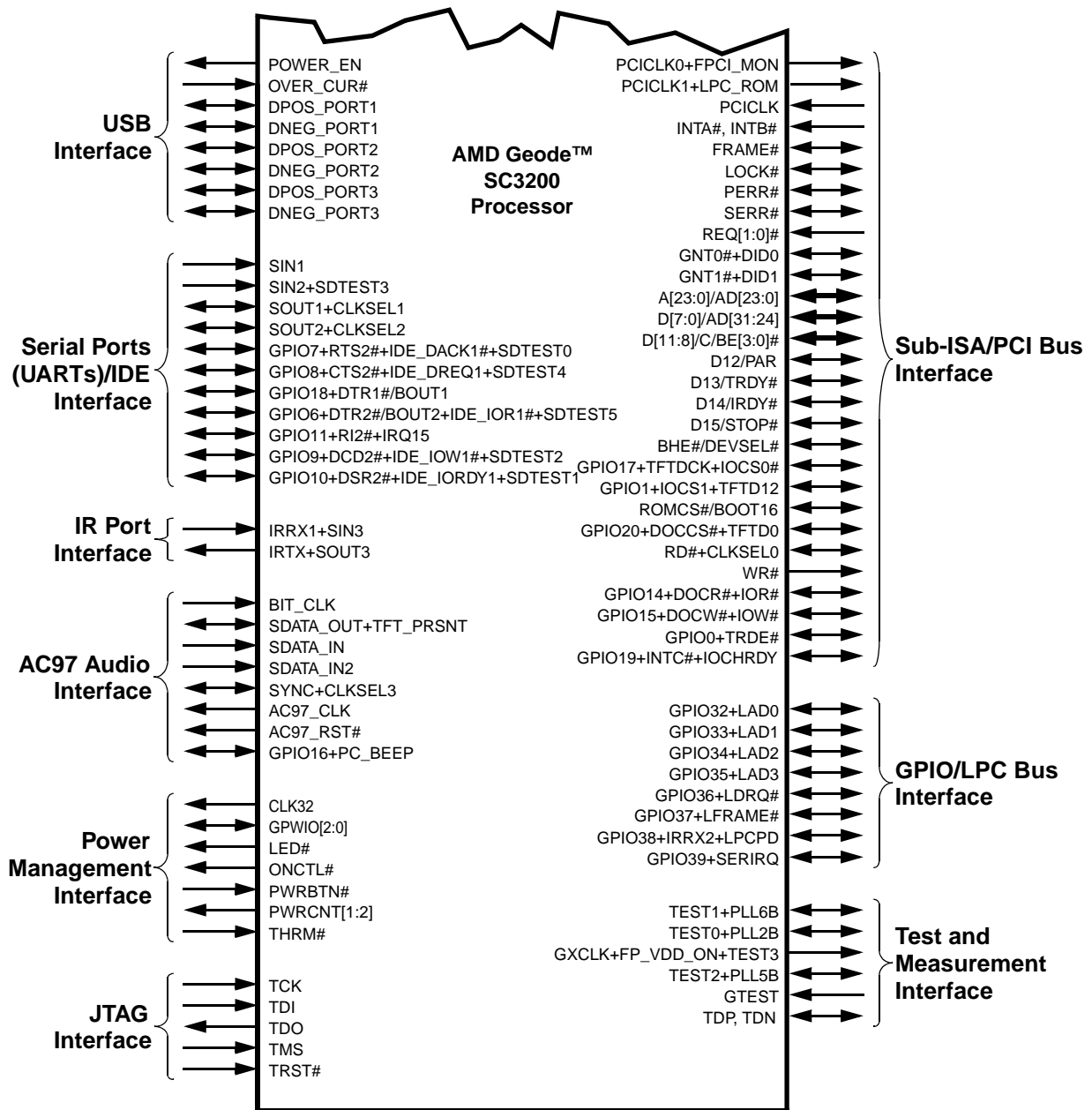


Figure 3-1. Signal Groups (Continued)

The remaining subsections of this chapter describe:

- Section 3.1 "Ball Assignments": Provides a ball assignment diagram and tables listing the signals sorted according to ball number and alphabetically by signal name.
- Section 3.2 "Strap Options": Several balls are read at power-up that set up the state of the SC3200. This section provides details regarding those balls.
- Section 3.3 "Multiplexing Configuration": Lists multiplexing options and their configurations.
- Section 3.4 "Signal Descriptions": Detailed descriptions of each signal according to functional group.

### 3.1 Ball Assignments

The SC3200 is highly configurable as illustrated in Figure 3-1 on page 25. Strap options and register programming are used to set various modes of operation and specific signals on specific balls. This section describes which signals are available on which balls and provides configuration information:

- Figure 3-2 on page 28 and Figure 3-3 on page 42: Illustrations of EBGA and TEPBGA ball assignments.
- Table 3-2 on page 29 and Table 3-4 on page 43: Lists signals according to ball number. Power Rail, Signal Type, Buffer Type and, where relevant, Pull-Up or Pull-Down resistors are indicated for each ball in this table. For multiplexed balls, the necessary configuration for each signal is listed as well.
- Table 3-3 on page 38 and Table 3-5 on page 54: Quick reference signal list sorted alphabetically - listing all signal names and ball numbers. The tables in this chapter use several common abbreviations. Table 3-1 lists the mnemonics and their meanings

#### Notes:

- 1) For each GPIO signal, there is an optional pull-up resistor on the relevant ball. After system reset, the pull-up is present.

This pull-up resistor can be disabled via registers in the Core Logic module. The configuration is without regard to the selected ball function (except for GPIO12, GPIO13, and GPIO16). Alternate functions for GPIO12, GPIO13, and GPIO16 control pull-up resistors.

For more information, see Section 6.4.1 "Bridge, GPIO, and LPC Registers - Function 0" on page 206.

- 2) Configuration settings listed in this table are with regard to the Pin Multiplexing Register (PMR). See Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88 for a detailed description of this register.

**Table 3-1. Signal Definitions Legend**

| Mnemonic          | Definition   |
|-------------------|--|
| A                 | Analog   |
| AV <sub>SS</sub>  | Ground ball: Analog  |
| AV <sub>CC</sub>  | Power ball: Analog   |
| GCB               | General Configuration Block registers. Refer to Section 4.0 "General Configuration Block" on page 87.<br><br>Location of the General Configuration Block cannot be determined by software. See the <i>AMD Geode™ SC3200 Specification Update</i> document. |
| I                 | Input ball   |
| I/O               | Bidirectional ball   |
| MCR[x]            | Miscellaneous Configuration Register Bit x: A register, located in the GCB. Refer to Section 4.1 "Configuration Block Addresses" on page 87 for further details.   |
| O                 | Output ball  |
| OD                | Open-drain   |
| PD                | Pull-down  |
| PMR[x]            | Pin Multiplexing Register Bit x: A register, located in the GCB, used to configure balls with multiple functions. Refer to Section 4.1 "Configuration Block Addresses" on page 87 for further details.   |
| PU                | Pull-up  |
| TS                | TRI-STATE  |
| V <sub>CORE</sub> | Power ball: 1.2V   |
| V <sub>IO</sub>   | Power ball: 3.3V   |
| V <sub>SS</sub>   | Ground ball  |
| #                 | The # symbol in a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. Otherwise, the signal is asserted when at a high voltage level.  |
| /                 | A / in a signal name indicates both functions are always enabled (i.e., cycle multiplexed).  |
| +                 | A + in signal name indicates the function is available on the ball, but that either strapping options or register programming is required to select the desired function.  |

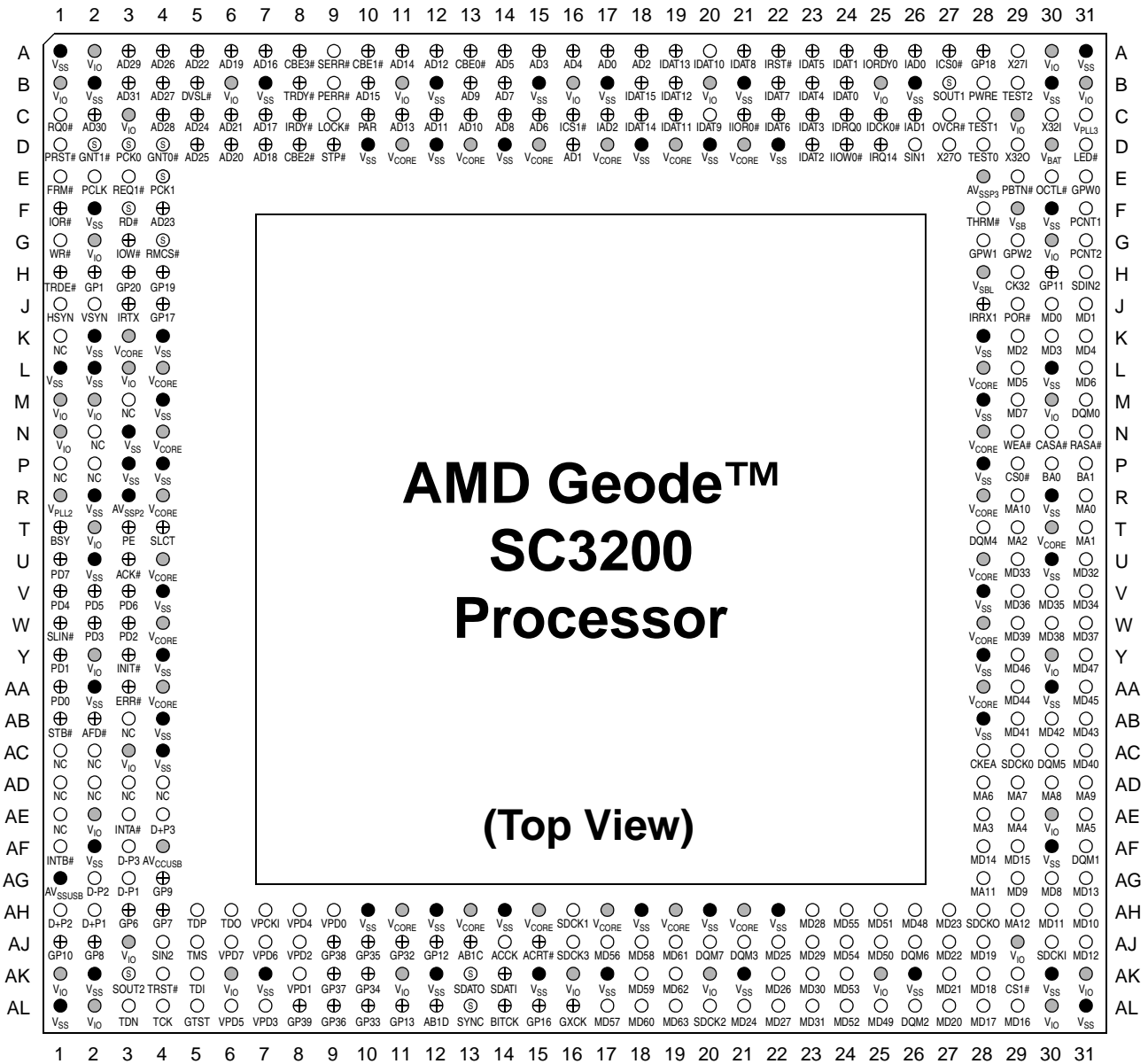


Figure 3-2. 432-EBGA Ball Assignment Diagram

Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number

| Ball No. | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type                 | Power Rail      | Configuration     |
|----------|-----------------|---------------------------|--|-----------------|-------------------|
| A1       | V <sub>SS</sub> | GND                       | ---                                      | ---             | ---               |
| A2       | V <sub>IO</sub> | PWR                       | ---                                      | ---             | ---               |
| A3       | AD29            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D5              | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| A4       | AD26            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D2              | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| A5       | AD22            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A22             | O                         | O <sub>PCI</sub>                         |                 |                   |
| A6       | AD19            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A19             | O                         | O <sub>PCI</sub>                         |                 |                   |
| A7       | AD16            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A16             | O                         | O <sub>PCI</sub>                         |                 |                   |
| A8       | C/BE3#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D11             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| A9       | SERR#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>DPCI</sub> | V <sub>IO</sub> | ---               |
| A10      | C/BE1#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D9              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| A11      | AD14            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A14             | O                         | O <sub>PCI</sub>                         |                 |                   |
| A12      | AD12            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A12             | O                         | O <sub>PCI</sub>                         |                 |                   |
| A13      | C/BE0#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D8              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| A14      | AD5             | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A5              | O                         | O <sub>PCI</sub>                         |                 |                   |
| A15      | AD3             | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A3              | O                         | O <sub>PCI</sub>                         |                 |                   |
| A16      | AD4             | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A4              | O                         | O <sub>PCI</sub>                         |                 |                   |
| A17      | AD0             | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A0              | O                         | O <sub>PCI</sub>                         |                 |                   |

| Ball No. | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type                 | Power Rail      | Configuration     |
|----------|-----------------|---------------------------|--|-----------------|-------------------|
| A18      | AD2             | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A2              | O                         | O <sub>PCI</sub>                         |                 |                   |
| A19      | IDE_DATA13      | I/O                       | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD15          | O                         | O <sub>1/4</sub>                         |                 |                   |
| A20      | IDE_DATA10      | I/O                       | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0       |
| A21      | IDE_DATA8       | I/O                       | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0       |
|          | GPIO40          | I/O                       | IN <sub>TS1</sub> ,<br>O <sub>1/4</sub>  |                 |                   |
| A22      | IDE_RST#        | O                         | O <sub>1/4</sub>                         | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTDCK          | O                         | O <sub>1/4</sub>                         |                 |                   |
| A23      | IDE_DATA5       | I/O                       | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0       |
|          | CLK27M          | O                         | O <sub>1/4</sub>                         |                 |                   |
| A24      | IDE_DATA1       | I/O                       | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD16          | O                         | O <sub>1/4</sub>                         |                 |                   |
| A25      | IDE_IORDY0      | I                         | IN <sub>TS1</sub>                        | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD11          | O                         | O <sub>1/4</sub>                         |                 |                   |
| A26      | IDE_ADDR0       | O                         | O <sub>1/4</sub>                         | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD3           | O                         | O <sub>1/4</sub>                         |                 |                   |
| A27      | IDE_CS0#        | O                         | O <sub>1/4</sub>                         | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD5           | O                         | O <sub>1/4</sub>                         |                 |                   |
| A28      | GPIO18          | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>      | V <sub>IO</sub> | PMR[16] = 0       |
|          | DTR1#/BOUT1     | O (PU <sub>22.5</sub> )   | O <sub>8/8</sub>                         |                 |                   |
| A29      | X27I            | I                         | WIRE                                     | V <sub>IO</sub> | ---               |
| A30      | V <sub>IO</sub> | PWR                       | ---                                      | ---             | ---               |
| A31      | V <sub>SS</sub> | GND                       | ---                                      | ---             | ---               |
| B1       | V <sub>IO</sub> | PWR                       | ---                                      | ---             | ---               |
| B2       | V <sub>SS</sub> | GND                       | ---                                      | ---             | ---               |
| B3       | AD31            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D7              | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| B4       | AD27            | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D3              | I/O                       | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |
| B5       | DEVSEL#         | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | BHE#            | O                         | O <sub>PCI</sub>                         |                 |                   |
| B6       | V <sub>IO</sub> | PWR                       | ---                                      | ---             | ---               |
| B7       | V <sub>SS</sub> | GND                       | ---                                      | ---             | ---               |
| B8       | TRDY#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D13             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub>  |                 |                   |

Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No. | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail      | Configuration                     |
|----------|-----------------|---------------------------|---------------------------------------|-----------------|-----------------------------------|
| B9       | PERR#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | ---                               |
| B10      | AD15            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A15             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| B11      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| B12      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B13      | AD9             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A9              | O                         | O <sub>PCI</sub>                      |                 |                                   |
| B14      | AD7             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A7              | O                         | O <sub>PCI</sub>                      |                 |                                   |
| B15      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B16      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| B17      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B18      | IDE_DATA15      | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTD7           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| B19      | IDE_DATA12      | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTD13          | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| B20      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| B21      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B22      | IDE_DATA7       | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | INTD#           | I                         | IN <sub>TS</sub>                      |                 | PMR[24] = 1                       |
| B23      | IDE_DATA4       | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | FP_VDD_ON       | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| B24      | IDE_DATA0       | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTD6           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| B25      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| B26      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B27      | SOUT1           | O                         | O <sub>8/8</sub>                      | V <sub>IO</sub> | ---                               |
|          | CLKSEL1         | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                 | Strap (See Table 3-6 on page 58.) |
| B28      | POWER_EN        | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub> | ---                               |
|          | TFTDE           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| B29      | TEST2           | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | PMR[29] = 1                       |
|          | PLL5B           | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   |                 | PMR[29] = 0                       |
| B30      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| B31      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| C1       | REQ0#           | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                     | V <sub>IO</sub> | ---                               |
| C2       | AD30            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | D6              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                                   |
| C3       | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| C4       | AD28            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | D4              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                                   |
| C5       | AD24            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | D0              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                                   |
| C6       | AD21            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A21             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C7       | AD17            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A17             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C8       | IRDY#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | D14             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                                   |
| C9       | LOCK#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | ---                               |
| C10      | PAR             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | D12             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                                   |
| C11      | AD13            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A13             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C12      | AD11            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A11             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C13      | AD10            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A10             | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C14      | AD8             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A8              | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C15      | AD6             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                 |
|          | A6              | O                         | O <sub>PCI</sub>                      |                 |                                   |
| C16      | IDE_CS1#        | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTDE           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| C17      | IDE_ADDR2       | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTD4           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| C18      | IDE_DATA14      | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | TFTD17          | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| C19      | IDE_DATA11      | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |
|          | GPIO41          | I/O                       | IN <sub>TS1</sub> , O <sub>1/4</sub>  |                 | PMR[24] = 1                       |
| C20      | IDE_DATA9       | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                       |

Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No. | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail       | Configuration                     |
|----------|-------------------|---------------------------|---------------------------------------|------------------|-----------------------------------|
| C21      | IDE_IOR0#         | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | TFTD10            | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| C22      | IDE_DATA6         | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | IRQ9              | I                         | IN <sub>TS1</sub>                     |                  | PMR[24] = 1                       |
| C23      | IDE_DATA3         | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | TFTD12            | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| C24      | IDE_DREQ0         | I                         | IN <sub>TS1</sub>                     | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | TFTD8             | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| C25      | IDE_DACK0#        | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | TFTD0             | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| C26      | IDE_ADDR1         | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub>  | PMR[24] = 0                       |
|          | TFTD2             | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| C27      | OVER_CUR#         | I                         | IN <sub>TS</sub>                      | V <sub>IO</sub>  | ---                               |
| C28      | TEST1             | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | PMR[29] = 1                       |
|          | PLL6B             | I/O                       | IN <sub>TS</sub> , TS <sub>2/5</sub>  |                  | PMR[29] = 0                       |
| C29      | V <sub>IO</sub>   | PWR                       | ---                                   | ---              | ---                               |
| C30      | X32I              | I                         | WIRE                                  | V <sub>BAT</sub> | ---                               |
| C31      | V <sub>PLL3</sub> | PWR                       | ---                                   | ---              | ---                               |
| D1       | PCIRST#           | O                         | O <sub>PCI</sub>                      | V <sub>IO</sub>  | ---                               |
| D2       | GNT1#             | O                         | O <sub>PCI</sub>                      | V <sub>IO</sub>  | ---                               |
|          | DID1              | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                  | Strap (See Table 3-6 on page 58.) |
| D3       | PCICLK0           | O                         | O <sub>PCI</sub>                      | V <sub>IO</sub>  | ---                               |
|          | FPCI_MON          | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                  | Strap (See Table 3-6 on page 58.) |
| D4       | GNT0#             | O                         | O <sub>PCI</sub>                      | V <sub>IO</sub>  | ---                               |
|          | DID0              | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                  | Strap (See Table 3-6 on page 58.) |
| D5       | AD25              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|          | D1                | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                  |                                   |
| D6       | AD20              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|          | A20               | O                         | O <sub>PCI</sub>                      |                  |                                   |
| D7       | AD18              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|          | A18               | O                         | O <sub>PCI</sub>                      |                  |                                   |
| D8       | C/BE2#            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|          | D10               | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                  |                                   |
| D9       | STOP#             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|          | D15               | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                  |                                   |
| D10      | V <sub>SS</sub>   | GND                       | ---                                   | ---              | ---                               |

| Ball No.           | Signal Name          | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail       | Configuration                     |
|--------------------|----------------------|---------------------------|---------------------------------------|------------------|-----------------------------------|
| D11                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D12                | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |
| D13                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D14                | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |
| D15                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D16                | AD1                  | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | Cycle Multiplexed                 |
|                    | A1                   | O                         | O <sub>PCI</sub>                      |                  |                                   |
| D17                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D18                | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |
| D19                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D20                | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |
| D21                | V <sub>CORE</sub>    | PWR                       | ---                                   | ---              | ---                               |
| D22                | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |
| D23                | IDE_DATA2            | I/O                       | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub>  | PMR[24] = 0                       |
|                    | TFTD14               | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| D24                | IDE_IOW0#            | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub>  | PMR[24] = 0                       |
|                    | TFTD9                | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| D25                | IRQ14                | I                         | IN <sub>TS1</sub>                     | V <sub>IO</sub>  | PMR[24] = 0                       |
|                    | TFTD1                | O                         | O <sub>1/4</sub>                      |                  | PMR[24] = 1                       |
| D26                | SIN1                 | I                         | IN <sub>TS</sub>                      | V <sub>IO</sub>  | ---                               |
| D27                | X27O                 | O                         | WIRE                                  | V <sub>IO</sub>  | ---                               |
| D28                | TEST0                | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | PMR[29] = 1                       |
|                    | PLL2B                | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   |                  | PMR[29] = 0                       |
| D29                | X32O                 | O                         | WIRE                                  | V <sub>BAT</sub> | ---                               |
| D30                | V <sub>BAT</sub>     | PWR                       | ---                                   | ---              | ---                               |
| D31                | LED#                 | O                         | OD <sub>14</sub>                      | V <sub>SB</sub>  | ---                               |
| E1                 | FRAME#               | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub>  | ---                               |
| E2                 | PCICLK               | I                         | IN <sub>T</sub>                       | V <sub>IO</sub>  | ---                               |
| E3                 | REQ1#                | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                     | V <sub>IO</sub>  | ---                               |
| E4                 | PCICLK1              | O                         | O <sub>PCI</sub>                      | V <sub>IO</sub>  | ---                               |
|                    | LPC_ROM              | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                  | Strap (See Table 3-6 on page 58.) |
| E28                | AV <sub>SSPLL3</sub> | GND                       | ---                                   | ---              | ---                               |
| E29                | PWRBTN#              | I (PU <sub>100</sub> )    | IN <sub>BTN</sub>                     | V <sub>SB</sub>  | ---                               |
| E30 <sup>3,4</sup> | ONCTL#               | O                         | OD <sub>14</sub>                      | V <sub>SB</sub>  | ---                               |
| E31                | GPWIO0               | I/O (PU <sub>100</sub> )  | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub>  | ---                               |
| F1                 | IOR#                 | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub>  | PMR[21] = 0 and PMR[2] = 0        |
|                    | DOCR#                | O                         | O <sub>3/5</sub>                      |                  | PMR[21] = 0 and PMR[2] = 1        |
|                    | GPIO14               | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>   |                  | PMR[21] = 1 and PMR[2] = 1        |
| F2                 | V <sub>SS</sub>      | GND                       | ---                                   | ---              | ---                               |

**Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.           | Signal Name      | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail      | Configuration                            |
|--------------------|------------------|---------------------------|---------------------------------------|-----------------|--|
| F3                 | RD#              | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub> | ---                                      |
|                    | CLKSELO          | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                 | Strap (See Table 3-6 on page 58.)        |
| F4                 | AD23             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed                        |
|                    | A23              | O                         | O <sub>PCI</sub>                      |                 |  |
| F28                | THR#             | I                         | IN <sub>TS</sub>                      | V <sub>SB</sub> | ---                                      |
| F29                | V <sub>SB</sub>  | PWR                       | ---                                   | ---             | ---                                      |
| F30                | V <sub>SS</sub>  | GND                       | ---                                   | ---             | ---                                      |
| F31 <sup>3,4</sup> | PWRCNT1          | O                         | OD <sub>14</sub>                      | V <sub>SB</sub> | ---                                      |
| G1                 | WR#              | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub> | ---                                      |
| G2                 | V <sub>IO</sub>  | PWR                       | ---                                   | ---             | ---                                      |
| G3                 | IOW#             | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub> | PMR[21] = 0 and PMR[2] = 0               |
|                    | DOCW#            | O                         | O <sub>3/5</sub>                      |                 | PMR[21] = 0 and PMR[2] = 1               |
|                    | GPIO15           | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>   |                 | PMR[21] = 1 and PMR[2] = 1               |
| G4                 | ROMCS#           | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub> | ---                                      |
|                    | BOOT16           | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                    |                 | Strap (See Table 3-6 on page 58.)        |
| G28                | GPWIO1           | I/O (PU <sub>100</sub> )  | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub> | ---                                      |
| G29                | GPWIO2           | I/O (PU <sub>100</sub> )  | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub> | ---                                      |
| G30                | V <sub>IO</sub>  | PWR                       | ---                                   | ---             | ---                                      |
| G31 <sup>3,4</sup> | PWRCNT2          | O                         | OD <sub>14</sub>                      | V <sub>SB</sub> | ---                                      |
| H1                 | TRDE#            | O                         | O <sub>3/5</sub>                      | V <sub>IO</sub> | PMR[12] = 0                              |
|                    | GPIO0            | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>   |                 | PMR[12] = 1                              |
| H2                 | GPIO1            | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>    | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and PMR[13] = 0 |
|                    | IOCS1#           | O (PU <sub>22.5</sub> )   | O <sub>3/5</sub>                      |                 | PMR[23] <sup>2</sup> = 0 and PMR[13] = 1 |
|                    | TFTD12           | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                      |                 | PMR[23] <sup>2</sup> = 1                 |
| H3                 | GPIO20           | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>    | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and PMR[7] = 0  |
|                    | DOCCS#           | O (PU <sub>22.5</sub> )   | O <sub>3/5</sub>                      |                 | PMR[23] <sup>2</sup> = 0 and PMR[7] = 1  |
|                    | TFTD0            | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                      |                 | PMR[23] <sup>2</sup> = 1                 |
| H4                 | GPIO19           | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>   | V <sub>IO</sub> | PMR[9] = 0 and PMR[4] = 0                |
|                    | INTC#            | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                      |                 | PMR[9] = 0 and PMR[4] = 1                |
|                    | IOCHRDY          | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                     |                 | PMR[9] = 1 and PMR[4] = 1                |
| H28                | V <sub>SBL</sub> | PWR                       | ---                                   | ---             | ---                                      |
| H29                | CLK32            | O                         | O <sub>2/5</sub>                      | V <sub>SB</sub> | ---                                      |

| Ball No.         | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type            | Power Rail      | Configuration                           |
|------------------|-------------------|---------------------------|-------------------------------------|-----------------|---|
| H30              | GPIO11            | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub> | V <sub>IO</sub> | PMR[18] = 0 and PMR[8] = 0              |
|                  | RI2#              | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                    |                 | PMR[18] = 1 and PMR[8] = 0              |
|                  | IRQ15             | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                   |                 | PMR[18] = 0 and PMR[8] = 1              |
| H31              | SDATA_IN2         | I                         | IN <sub>TS</sub>                    | V <sub>SB</sub> | F3BAR0+Memory Offset 08h[21] = 1        |
| J1               | HSYNC             | O                         | O <sub>1/4</sub>                    | V <sub>IO</sub> | ---                                     |
| J2               | VSYSN             | O                         | O <sub>1/4</sub>                    | V <sub>IO</sub> | ---                                     |
| J3               | IRTX              | O                         | O <sub>8/8</sub>                    | V <sub>IO</sub> | PMR[6] = 0                              |
|                  | SOUT3             | O                         | O <sub>8/8</sub>                    |                 | PMR[6] = 1                              |
| J4               | GPIO17            | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and PMR[5] = 0 |
|                  | IOCS0#            | O (PU <sub>22.5</sub> )   | O <sub>3/5</sub>                    |                 | PMR[23] <sup>2</sup> = 0 and PMR[5] = 1 |
|                  | TFTDCK            | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                    |                 | PMR[23] <sup>2</sup> = 1                |
| J28              | IRRX1             | I                         | IN <sub>TS</sub>                    | V <sub>SB</sub> | PMR[6] = 0                              |
|                  | SIN3              | I                         | IN <sub>TS</sub>                    |                 | PMR[6] = 1                              |
| J29              | POR#              | I                         | IN <sub>TS</sub>                    | V <sub>IO</sub> | ---                                     |
| J30 <sup>3</sup> | MD0               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| J31 <sup>3</sup> | MD1               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| K1               | NC                | ---                       | ---                                 | ---             | ---                                     |
| K2               | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| K3               | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                                     |
| K4               | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| K28              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| K29 <sup>3</sup> | MD2               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| K30 <sup>3</sup> | MD3               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| K31 <sup>3</sup> | MD4               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| L1               | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| L2               | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| L3               | V <sub>IO</sub>   | PWR                       | ---                                 | ---             | ---                                     |
| L4               | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                                     |
| L28              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                                     |
| L29 <sup>3</sup> | MD5               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| L30              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| L31 <sup>3</sup> | MD6               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| M1               | V <sub>IO</sub>   | PWR                       | ---                                 | ---             | ---                                     |
| M2               | V <sub>IO</sub>   | PWR                       | ---                                 | ---             | ---                                     |
| M3               | NC                | ---                       | ---                                 | ---             | ---                                     |
| M4               | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| M28              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                                     |
| M29 <sup>3</sup> | MD7               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                                     |
| M30              | V <sub>IO</sub>   | PWR                       | ---                                 | ---             | ---                                     |
| M31              | DQM0              | O                         | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                                     |
| N1               | V <sub>IO</sub>   | PWR                       | ---                                 | ---             | ---                                     |
| N2               | NC                | ---                       | ---                                 | ---             | ---                                     |



Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.          | Signal Name          | I/O (PU/PD)                                | Buffer <sup>1</sup> Type | Power Rail      | Configuration   |
|-------------------|----------------------|--|--------------------------|-----------------|---|
| N3                | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| N4                | V <sub>CORE</sub>    | PWR  | ---                      | ---             | ---   |
| N28               | V <sub>CORE</sub>    | PWR  | ---                      | ---             | ---   |
| N29               | WEA#                 | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| N30               | CASA#                | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| N31               | RASA#                | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| P1                | NC                   | ---  | ---                      | ---             | ---   |
| P2                | NC                   | ---  | ---                      | ---             | ---   |
| P3                | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| P4                | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| P28               | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| P29               | CS0#                 | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| P30               | BA0                  | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| P31               | BA1                  | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| R1                | V <sub>PLL2</sub>    | PWR  | ---                      | ---             | ---   |
| R2                | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| R3                | AV <sub>SSPLL2</sub> | GND  | ---                      | ---             | ---   |
| R4                | V <sub>CORE</sub>    | PWR  | ---                      | ---             | ---   |
| R28               | V <sub>CORE</sub>    | PWR  | ---                      | ---             | ---   |
| R29               | MA10                 | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| R30               | V <sub>SS</sub>      | GND  | ---                      | ---             | ---   |
| R31               | MA0                  | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |
| T1 <sup>3,4</sup> | BUSY/WAIT#           | I  | IN <sub>T</sub>          | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                   | TFTD3                | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                   | F_C/BE1#             | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| T2                | V <sub>IO</sub>      | PWR  | ---                      | ---             | ---   |
| T3 <sup>3,4</sup> | PE                   | I (PU <sub>22.5</sub> PD <sub>22.5</sub> ) | IN <sub>T</sub>          | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) (PU/PD under software control.) |
|                   | TFTD14               | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                   | F_C/BE2#             | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| T4 <sup>3,4</sup> | SLCT                 | I  | IN <sub>T</sub>          | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                   | TFTD15               | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                   | F_C/BE3#             | O  | O <sub>1/4</sub>         |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| T28               | DQM4                 | O  | O <sub>2/5</sub>         | V <sub>IO</sub> | ---   |

| Ball No.          | Signal Name       | I/O (PU/PD) | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|-------------------|-------------------|-------------|--------------------------------------|-----------------|---|
| T29               | MA2               | O           | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| T30               | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| T31               | MA1               | O           | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| U1 <sup>3,4</sup> | PD7               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | TFTD13            | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | F_AD7             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| U2                | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| U3 <sup>3,4</sup> | ACK#              | I           | IN <sub>T</sub>                      | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | TFTDE             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | FPCICLK           | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| U4                | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| U28               | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| U29 <sup>3</sup>  | MD33              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| U30               | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| U31 <sup>3</sup>  | MD32              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| V1 <sup>3,4</sup> | PD4               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | TFTD10            | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | F_AD4             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| V2 <sup>3,4</sup> | PD5               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | TFTD11            | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | F_AD5             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| V3 <sup>3,4</sup> | PD6               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | TFTD1             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                   | F_AD6             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| V4                | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| V28               | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| V29 <sup>3</sup>  | MD36              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |

**Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.           | Signal Name       | I/O (PU/PD) | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|--------------------|-------------------|-------------|--------------------------------------|-----------------|---|
| V30 <sup>3</sup>   | MD35              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| V31 <sup>3</sup>   | MD34              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| W1 <sup>3, 4</sup> | SLIN#/ASTRB#      | O           | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD16            | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_IRDY#           | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| W2 <sup>3, 4</sup> | PD3               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD9             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD3             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| W3 <sup>3, 4</sup> | PD2               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD8             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD2             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| W4                 | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| W28                | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| W29 <sup>3</sup>   | MD39              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| W30 <sup>3</sup>   | MD38              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| W31 <sup>3</sup>   | MD37              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| Y1 <sup>3, 4</sup> | PD1               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD7             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD1             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| Y2                 | V <sub>IO</sub>   | PWR         | ---                                  | ---             | ---   |
| Y3 <sup>3, 4</sup> | INIT#             | O           | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD5             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | SMI_O             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| Y4                 | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| Y28                | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| Y29 <sup>3</sup>   | MD46              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| Y30                | V <sub>IO</sub>   | PWR         | ---                                  | ---             | ---   |
| Y31 <sup>3</sup>   | MD47              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |

| Ball No.            | Signal Name       | I/O (PU/PD) | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|---------------------|-------------------|-------------|--------------------------------------|-----------------|---|
| AA1 <sup>3, 4</sup> | PD0               | I/O         | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | TFTD6             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | F_AD0             | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| AA2                 | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| AA3 <sup>3, 4</sup> | ERR#              | I           | IN <sub>T</sub> , O <sub>1/4</sub>   | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | TFTD4             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | F_C/BE0#          | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| AA4                 | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| AA28                | V <sub>CORE</sub> | PWR         | ---                                  | ---             | ---   |
| AA29 <sup>3</sup>   | MD44              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AA30                | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| AA31 <sup>3</sup>   | MD45              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AB1 <sup>3, 4</sup> | STB#/WRITE#       | O           | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | TFTD17            | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | F_FRAME#          | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| AB2 <sup>3, 4</sup> | AFD#/DSTRB#       | O           | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | TFTD2             | O           | O <sub>1/4</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                     | INTR_O            | O           | O <sub>14/14</sub>                   |                 | PMR[23] <sup>2</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| AB3                 | NC                | ---         | ---                                  | ---             | ---   |
| AB4                 | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| AB28                | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| AB29 <sup>3</sup>   | MD41              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AB30 <sup>3</sup>   | MD42              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AB31 <sup>3</sup>   | MD43              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AC1                 | NC                | ---         | ---                                  | ---             | ---   |
| AC2                 | NC                | ---         | ---                                  | ---             | ---   |
| AC3                 | V <sub>IO</sub>   | PWR         | ---                                  | ---             | ---   |
| AC4                 | V <sub>SS</sub>   | GND         | ---                                  | ---             | ---   |
| AC28                | CKEA              | O           | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AC29                | SDCLK0            | O           | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AC30                | DQM5              | O           | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AC31 <sup>3</sup>   | MD40              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |

Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.          | Signal Name          | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail             | Configuration              |
|-------------------|----------------------|---------------------------|--------------------------------------|------------------------|----------------------------|
| AD1               | NC                   | ---                       | ---                                  | ---                    | ---                        |
| AD2               | NC                   | ---                       | ---                                  | ---                    | ---                        |
| AD3               | NC                   | ---                       | ---                                  | ---                    | ---                        |
| AD4               | NC                   | ---                       | ---                                  | ---                    | ---                        |
| AD28              | MA6                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AD29              | MA7                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AD30              | MA8                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AD31              | MA9                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AE1               | NC                   | ---                       | ---                                  | ---                    | ---                        |
| AE2               | V <sub>IO</sub>      | PWR                       | ---                                  | ---                    | ---                        |
| AE3               | INTA#                | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub>        | ---                        |
| AE4 <sup>3</sup>  | DPOS_PORT3           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| AE28              | MA3                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AE29              | MA4                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AE30              | V <sub>IO</sub>      | PWR                       | ---                                  | ---                    | ---                        |
| AE31              | MA5                  | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AF1               | INTB#                | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub>        | ---                        |
| AF2               | V <sub>SS</sub>      | GND                       | ---                                  | ---                    | ---                        |
| AF3 <sup>3</sup>  | DNEG_PORT3           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| AF4               | AV <sub>CC</sub> USB | PWR                       | ---                                  | ---                    | ---                        |
| AF28 <sup>3</sup> | MD14                 | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub>        | ---                        |
| AF29 <sup>3</sup> | MD15                 | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub>        | ---                        |
| AF30              | V <sub>SS</sub>      | GND                       | ---                                  | ---                    | ---                        |
| AF31              | DQM1                 | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AG1               | AV <sub>SS</sub> USB | GND                       | ---                                  | ---                    | ---                        |
| AG2 <sup>3</sup>  | DNEG_PORT2           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| AG3 <sup>3</sup>  | DNEG_PORT1           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| AG4               | GPIO9                | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>1/4</sub>  | V <sub>IO</sub>        | PMR[18] = 0 and PMR[8] = 0 |
|                   | DCD2#                | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                        | PMR[18] = 1 and PMR[8] = 0 |
|                   | IDE_IOW1#            | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                     |                        | PMR[18] = 0 and PMR[8] = 1 |
|                   | SDTEST2              | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                        | PMR[18] = 1 and PMR[8] = 1 |
| AG28              | MA11                 | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub>        | ---                        |
| AG29 <sup>3</sup> | MD9                  | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub>        | ---                        |
| AG30 <sup>3</sup> | MD8                  | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub>        | ---                        |
| AG31 <sup>3</sup> | MD13                 | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub>        | ---                        |
| AH1 <sup>3</sup>  | DPOS_PORT2           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| AH2 <sup>3</sup>  | DPOS_PORT1           | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |

| Ball No.          | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type            | Power Rail      | Configuration              |
|-------------------|-------------------|---------------------------|-------------------------------------|-----------------|----------------------------|
| AH3               | GPIO6             | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>1/4</sub> | V <sub>IO</sub> | PMR[18] = 0 and PMR[8] = 0 |
|                   | DTR2#/BOUT2       | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                    |                 | PMR[18] = 1 and PMR[8] = 0 |
|                   | IDE_IOR1#         | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                    |                 | PMR[18] = 0 and PMR[8] = 1 |
|                   | SDTEST5           | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                    |                 | PMR[18] = 1 and PMR[8] = 1 |
| AH4               | GPIO7             | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>1/4</sub> | V <sub>IO</sub> | PMR[17] = 0 and PMR[8] = 0 |
|                   | RTS2#             | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                    |                 | PMR[17] = 1 and PMR[8] = 0 |
|                   | IDE_DACK1#        | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                    |                 | PMR[17] = 0 and PMR[8] = 1 |
|                   | SDTEST0           | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                    |                 | PMR[17] = 1 and PMR[8] = 1 |
| AH5               | TDP               | I/O                       | Diode                               | ---             | ---                        |
| AH6               | TDO               | O                         | O <sub>PCI</sub>                    | V <sub>IO</sub> | ---                        |
| AH7               | VPCKIN            | I                         | IN <sub>T</sub>                     | V <sub>IO</sub> | ---                        |
| AH8               | VPD4              | I                         | IN <sub>T</sub>                     | V <sub>IO</sub> | ---                        |
| AH9               | VPD0              | I                         | IN <sub>T</sub>                     | V <sub>IO</sub> | ---                        |
| AH10              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH11              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH12              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH13              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH14              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH15              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH16              | SDCLK1            | O                         | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                        |
| AH17              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH18              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH19              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH20              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH21              | V <sub>CORE</sub> | PWR                       | ---                                 | ---             | ---                        |
| AH22              | V <sub>SS</sub>   | GND                       | ---                                 | ---             | ---                        |
| AH23 <sup>3</sup> | MD28              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH24 <sup>3</sup> | MD55              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH25 <sup>3</sup> | MD51              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH26 <sup>3</sup> | MD48              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH27 <sup>3</sup> | MD23              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH28              | SDCLK_OUT         | O                         | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                        |
| AH29              | MA12              | O                         | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                        |
| AH30 <sup>3</sup> | MD11              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AH31 <sup>3</sup> | MD10              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                        |
| AJ1               | GPIO10            | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub> | V <sub>IO</sub> | PMR[18] = 0 and PMR[8] = 0 |
|                   | DSR2#             | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                    |                 | PMR[18] = 1 and PMR[8] = 0 |
|                   | IDE_IORDY1        | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                   |                 | PMR[18] = 0 and PMR[8] = 1 |
|                   | SDTEST1           | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                    |                 | PMR[18] = 1 and PMR[8] = 1 |

**Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.          | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|-------------------|-----------------|---------------------------|--------------------------------------|-----------------|---|
| AJ2               | GPIO8           | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>  | V <sub>IO</sub> | PMR[17] = 0 and PMR[8] = 0  |
|                   | CTS2#           | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                 | PMR[17] = 1 and PMR[8] = 0  |
|                   | IDE_DREQ1       | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                    |                 | PMR[17] = 0 and PMR[8] = 1  |
|                   | SDTEST4         | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                 | PMR[17] = 1 and PMR[8] = 1  |
| AJ3               | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AJ4               | SIN2            | I                         | IN <sub>TS</sub>                     | V <sub>IO</sub> | PMR[28] = 0   |
|                   | SDTEST3         | O                         | O <sub>2/5</sub>                     |                 | PMR[28] = 1   |
| AJ5               | TMS             | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| AJ6               | VPD7            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AJ7               | VPD6            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AJ8               | VPD2            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AJ9               | GPIO38/IRRX2    | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0. The IRRX2 input is connected to the input path of GPIO38. There is no logic required to enable IRRX2, just a simple connection. Hence, when GPIO38 is the selected function, IRRX2 is also selected. |
|                   | LPCPD#          | O                         | O <sub>PCI</sub>                     |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1   |
| AJ10              | GPIO35          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0   |
|                   | LAD3            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1   |
| AJ11              | GPIO32          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0   |
|                   | LAD0            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1   |
| AJ12              | GPIO12          | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8/8</sub>  | V <sub>IO</sub> | PMR[19] = 0   |
|                   | AB2C            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    |                 | PMR[19] = 1   |
| AJ13              | AB1C            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0  |
|                   | GPIO20          | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>   |                 | PMR[23] <sup>2</sup> = 1 and PMR[7] = 0   |
|                   | DOCCS#          | O                         | O <sub>3/5</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and PMR[7] = 1   |
| AJ14              | AC97_CLK        | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | PMR[25] = 1   |
| AJ15              | AC97_RST#       | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | FPCI_MON = 0  |
|                   | F_STOP#         | O                         | O <sub>2/5</sub>                     |                 | FPCI_MON = 1  |
| AJ16              | SDCLK3          | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AJ17 <sup>3</sup> | MD56            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ18 <sup>3</sup> | MD58            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ19 <sup>3</sup> | MD61            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ20              | DQM7            | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AJ21              | DQM3            | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AJ22 <sup>3</sup> | MD25            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ23 <sup>3</sup> | MD29            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ24 <sup>3</sup> | MD54            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ25 <sup>3</sup> | MD50            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ26              | DQM6            | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AJ27 <sup>3</sup> | MD22            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ28 <sup>3</sup> | MD19            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AJ29              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AJ30              | SDCLK_IN        | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AJ31 <sup>3</sup> | MD12            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK1               | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK2               | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK3               | SOUT2           | O                         | O <sub>8/8</sub>                     | V <sub>IO</sub> | ---   |
|                   | CLKSEL2         | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)   |
| AK4               | TRST#           | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| AK5               | TDI             | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| AK6               | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK7               | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK8               | VPD1            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AK9               | GPIO37          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0   |
|                   | LFRAME#         | O                         | O <sub>PCI</sub>                     |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1   |
| AK10              | GPIO34          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0   |
|                   | LAD2            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1   |
| AK11              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK12              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK13              | SDATA_OUT       | O                         | O <sub>AC97</sub>                    | V <sub>IO</sub> | ---   |
|                   | TFT_PRSN_T      | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)   |
| AK14              | SDATA_IN        | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | FPCI_MON = 0  |
|                   | F_GNT0#         | O                         | O <sub>2/5</sub>                     |                 | FPCI_MON = 1  |
| AK15              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK16              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK17              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK18 <sup>3</sup> | MD59            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK19 <sup>3</sup> | MD62            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK20              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK21              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK22 <sup>3</sup> | MD26            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |

Table 3-2. 432-EBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.          | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|-------------------|-----------------|---------------------------|--------------------------------------|-----------------|---|
| AK23 <sup>3</sup> | MD30            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK24 <sup>3</sup> | MD53            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK25              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AK26              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK27 <sup>3</sup> | MD21            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK28 <sup>3</sup> | MD18            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>  | V <sub>IO</sub> | ---   |
| AK29              | CS1#            | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | ---   |
| AK30              | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AK31              | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AL1               | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---   |
| AL2               | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---   |
| AL3               | TDN             | I/O                       | WIRE                                 | V <sub>IO</sub> | ---   |
| AL4               | TCK             | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| AL5               | GTEST           | I (PD <sub>22.5</sub> )   | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AL6               | VPD5            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AL7               | VPD3            | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | ---   |
| AL8               | GPIO39          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0 |
|                   | SERIRQ          | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1 |
| AL9               | GPIO36          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0 |
|                   | LDRQ#           | I                         | IN <sub>PCI</sub>                    |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1 |
| AL10              | GPIO33          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>5</sup> = 0 and PMR[22] <sup>5</sup> = 0 |
|                   | LAD1            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>5</sup> = 1 and PMR[22] <sup>5</sup> = 1 |
| AL11              | GPIO13          | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[19] = 0   |
|                   | AB2D            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[19] = 1   |
| AL12              | AB1D            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0                              |
|                   | GPIO1           | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>   |                 | PMR[23] <sup>2</sup> = 1 and PMR[13] = 0              |
|                   | IOCS1#          | O                         | O <sub>3/5</sub>                     |                 | PMR[23] <sup>2</sup> = 1 and PMR[13] = 1              |
| AL13              | SYNC            | O                         | O <sub>AC97</sub>                    | V <sub>IO</sub> | ---   |
|                   | CLKSEL3         | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)                     |
| AL14              | BIT_CLK         | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | FPCI_MON = 0  |
|                   | F_TRDY#         | O                         | O <sub>1/4</sub>                     |                 | FPCI_MON = 1  |
| AL15              | GPIO16          | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>2/5</sub>   | V <sub>IO</sub> | PMR[0] = 0 and FPCI_MON = 0                           |
|                   | PC_BEEP         | O                         | O <sub>2/5</sub>                     |                 | PMR[0] = 1 = 0 and FPCI_MON = 0                       |
|                   | F_DEVSEL#       | O                         | O <sub>2/5</sub>                     |                 | FPCI_MON = 1  |

| Ball No.          | Signal Name     | I/O (PU/PD) | Buffer <sup>1</sup> Type            | Power Rail      | Configuration                                |
|-------------------|-----------------|-------------|-------------------------------------|-----------------|--|
| AL16              | GXCLK           | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | PMR[23] <sup>2</sup> = 0 and PMR[29] = 0     |
|                   | FP_VDD_ON       | O           | O <sub>1/4</sub>                    |                 | PMR[23] <sup>2</sup> = 1                     |
|                   | TEST3           | O           | O <sub>2/5</sub>                    |                 | PMR[23] <sup>2</sup> = 0 and PMR[29] = 1 and |
| AL17 <sup>3</sup> | MD57            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL18 <sup>3</sup> | MD60            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL19 <sup>3</sup> | MD63            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL20              | SDCLK2          | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---  |
| AL21 <sup>3</sup> | MD24            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL22 <sup>3</sup> | MD27            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL23 <sup>3</sup> | MD31            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL24 <sup>3</sup> | MD52            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL25 <sup>3</sup> | MD49            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL26              | DQM2            | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---  |
| AL27 <sup>3</sup> | MD20            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL28 <sup>3</sup> | MD17            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL29 <sup>3</sup> | MD16            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---  |
| AL30              | V <sub>IO</sub> | PWR         | ---                                 | ---             | ---  |
| AL31              | V <sub>SS</sub> | GND         | ---                                 | ---             | ---  |

- For Buffer Type definitions, refer to Table 9-10 "Buffer Types" on page 375.
- The TFT\_PRSNR strap determines the power-on reset (POR) state of PMR[23].
- Is back-drive protected (MD[63:0], DPOS\_PORT1, DNEG\_PORT1, DPOS\_PORT2, DNEG\_PORT2, DPOS\_PORT3, DNEG\_PORT3, ACK#, AFD#/DSTRB#, BUSY/WAIT#, ERR#, INIT#, PD[7:0], PE, SLCT, SLIN#/ASTRB#, STB#/WRITE#, ONCTL#, PWRCNT[2:1]).
- Is 5V tolerant (ACK#, AFD#/DSTRB#, BUSY/WAIT#, ERR#, INIT#, PD[7:0], PE, SLCT, SLIN#/ASTRB#, STB#/WRITE#, ONCTL#, PWRCNT[2:1]).
- The LPC\_ROM strap determines the power-on reset (POR) state of PMR[14] and PMR[22].

Table 3-3. 432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name

| Signal Name | Ball No. | Signal Name           | Ball No. | Signal Name | Ball No. |
|-------------|----------|-----------------------|----------|-------------|----------|
| A0          | A17      | AD18                  | D7       | D9          | A10      |
| A1          | D16      | AD19                  | A6       | D10         | D8       |
| A2          | A18      | AD20                  | D6       | D11         | A8       |
| A3          | A15      | AD21                  | C6       | D12         | C10      |
| A4          | A16      | AD22                  | A5       | D13         | B8       |
| A5          | A14      | AD23                  | F4       | D14         | C8       |
| A6          | C15      | AD24                  | C5       | D15         | D9       |
| A7          | B14      | AD25                  | D5       | DCD2#       | AG4      |
| A8          | C14      | AD26                  | A4       | DEVSEL#     | B5       |
| A9          | B13      | AD27                  | B4       | DID0        | D4       |
| A10         | C13      | AD28                  | C4       | DID1        | D2       |
| A11         | C12      | AD29                  | A3       | DNEG_PORT1  | AG3      |
| A12         | A12      | AD30                  | C2       | DNEG_PORT2  | AG2      |
| A13         | C11      | AD31                  | B3       | DNEG_PORT3  | AF3      |
| A14         | A11      | AFD#/DSTRB#           | AB2      | DOCCS#      | H3, AJ13 |
| A15         | B10      | AV <sub>CC</sub> USB  | AF4      | DOCR#       | F1       |
| A16         | A7       | AV <sub>SS</sub> PLL2 | R3       | DOCW#       | G3       |
| A17         | C7       | AV <sub>SS</sub> PLL3 | E28      | DPOS_PORT1  | AH2      |
| A18         | D7       | AV <sub>SS</sub> USB  | AG1      | DPOS_PORT2  | AH1      |
| A19         | A6       | BA0                   | P30      | DPOS_PORT3  | AE4      |
| A20         | D6       | BA1                   | P31      | DQM0        | M31      |
| A21         | C6       | BHE#                  | B5       | DQM1        | AF31     |
| A22         | A5       | BIT_CLK               | AL14     | DQM2        | AL26     |
| A23         | F4       | BOOT16                | G4       | DQM3        | AJ21     |
| AB1C        | AJ13     | BUSY/WAIT#            | T1       | DQM4        | T28      |
| AB1D        | AL12     | C/BE0#                | A13      | DQM5        | AC30     |
| AB2C        | AJ12     | C/BE1#                | A10      | DQM6        | AJ26     |
| AB2D        | AL11     | C/BE2#                | D8       | DQM7        | AJ20     |
| AC97_CLK    | AJ14     | C/BE3#                | A8       | DSR2#       | AJ1      |
| AC97_RST#   | AJ15     | CASA#                 | N30      | DTR1#/BOUT1 | A28      |
| ACK#        | U3       | CKEA                  | AC28     | DTR2#/BOUT2 | AH3      |
| AD0         | A17      | CLK27M                | A23      | ERR#        | AA3      |
| AD1         | D16      | CLK32                 | H29      | F_AD0       | AA1      |
| AD2         | A18      | CLKSEL0               | F3       | F_AD1       | Y1       |
| AD3         | A15      | CLKSEL1               | B27      | F_AD2       | W3       |
| AD4         | A16      | CLKSEL2               | AK3      | F_AD3       | W2       |
| AD5         | A14      | CLKSEL3               | AL13     | F_AD4       | V1       |
| AD6         | C15      | CS0#                  | P29      | F_AD5       | V2       |
| AD7         | B14      | CS1#                  | AK29     | F_AD6       | V3       |
| AD8         | C14      | CTS2#                 | AJ2      | F_AD7       | U1       |
| AD9         | B13      | D0                    | C5       | F_C/BE0#    | AA3      |
| AD10        | C13      | D1                    | D5       | F_C/BE1#    | T1       |
| AD11        | C12      | D2                    | A4       | F_C/BE2#    | T3       |
| AD12        | A12      | D3                    | B4       | F_C/BE3#    | T4       |
| AD13        | C11      | D4                    | C4       | F_DEVSEL#   | AL15     |
| AD14        | A11      | D5                    | A3       | F_FRAME#    | AB1      |
| AD15        | B10      | D6                    | C2       | F_GNT0#     | AK14     |
| AD16        | A7       | D7                    | B3       | F_IRDY#     | W1       |
| AD17        | C7       | D8                    | A13      | F_STOP#     | AJ15     |

Table 3-3. 432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)

| Signal Name  | Ball No.  | Signal Name | Ball No. | Signal Name | Ball No. |
|--------------|-----------|-------------|----------|-------------|----------|
| F_TRDY#      | AL14      | IDE_DATA2   | D23      | LPCPD#      | AJ9      |
| FP_VDD_ON    | B23, AL16 | IDE_DATA3   | C23      | MA0         | R31      |
| FPCI_MON     | D3        | IDE_DATA4   | B23      | MA1         | T31      |
| FPCICLK      | U3        | IDE_DATA5   | A23      | MA2         | T29      |
| FRAME#       | E1        | IDE_DATA6   | C22      | MA3         | AE28     |
| GNT0#        | D4        | IDE_DATA7   | B22      | MA4         | AE29     |
| GNT1#        | D2        | IDE_DATA8   | A21      | MA5         | AE31     |
| GPIO0        | H1        | IDE_DATA9   | C20      | MA6         | AD28     |
| GPIO1        | H2, AL12  | IDE_DATA10  | A20      | MA7         | AD29     |
| GPIO6        | AH3       | IDE_DATA11  | C19      | MA8         | AD30     |
| GPIO7        | AH4       | IDE_DATA12  | B19      | MA9         | AD31     |
| GPIO8        | AJ2       | IDE_DATA13  | A19      | MA10        | R29      |
| GPIO9        | AG4       | IDE_DATA14  | C18      | MA11        | AG28     |
| GPIO10       | AJ1       | IDE_DATA15  | B18      | MA12        | AH29     |
| GPIO11       | H30       | IDE_DREQ0   | C24      | MD0         | J30      |
| GPIO12       | AJ12      | IDE_DREQ1   | AJ2      | MD1         | J31      |
| GPIO13       | AL11      | IDE_IOR0#   | C21      | MD2         | K29      |
| GPIO14       | F1        | IDE_IOR1#   | AH3      | MD3         | K30      |
| GPIO15       | G3        | IDE_IORDY0  | A25      | MD4         | K31      |
| GPIO16       | AL15      | IDE_IORDY1  | AJ1      | MD5         | L29      |
| GPIO17       | J4        | IDE_IOW0#   | D24      | MD6         | L31      |
| GPIO18       | A28       | IDE_IOW1#   | AG4      | MD7         | M29      |
| GPIO19       | H4        | IDE_RST#    | A22      | MD8         | AG30     |
| GPIO20       | H3, AJ13  | INIT#       | Y3       | MD9         | AG29     |
| GPIO32       | AJ11      | INTA#       | AE3      | MD10        | AH31     |
| GPIO33       | AL10      | INTB#       | AF1      | MD11        | AH30     |
| GPIO34       | AK10      | INTC#       | H4       | MD12        | AJ31     |
| GPIO35       | AJ10      | INTD#       | B22      | MD13        | AG31     |
| GPIO36       | AL9       | INTR_O      | AB2      | MD14        | AF28     |
| GPIO37       | AK9       | IOCHRDY     | H4       | MD15        | AF29     |
| GPIO38/IRRX2 | AJ9       | IOCS0#      | J4       | MD16        | AL29     |
| GPIO39       | AL8       | IOCS1#      | H2, AL12 | MD17        | AL28     |
| GPIO40       | A21       | IOR#        | F1       | MD18        | AK28     |
| GPIO41       | C19       | IOW#        | G3       | MD19        | AJ28     |
| GPWIO0       | E31       | IRDY#       | C8       | MD20        | AL27     |
| GPWIO1       | G28       | IRQ14       | D25      | MD21        | AK27     |
| GPWIO2       | G29       | IRQ15       | H30      | MD22        | AJ27     |
| GTEST        | AL5       | IRQ9        | C22      | MD23        | AH27     |
| GXCLK        | AL16      | IRRX1       | J28      | MD24        | AL21     |
| HSYNC        | J1        | IRTX        | J3       | MD25        | AJ22     |
| IDE_ADDR0    | A26       | LAD0        | AJ11     | MD26        | AK22     |
| IDE_ADDR1    | C26       | LAD1        | AL10     | MD27        | AL22     |
| IDE_ADDR2    | C17       | LAD2        | AK10     | MD28        | AH23     |
| IDE_CS0#     | A27       | LAD3        | AJ10     | MD29        | AJ23     |
| IDE_CS1#     | C16       | LDRQ#       | AL9      | MD30        | AK23     |
| IDE_DACK0#   | C25       | LED#        | D31      | MD31        | AL23     |
| IDE_DACK1#   | AH4       | LFRAME#     | AK9      | MD32        | U31      |
| IDE_DATA0    | B24       | LOCK#       | C9       | MD33        | U29      |
| IDE_DATA1    | A24       | LPC_ROM     | E4       | MD34        | V31      |

Table 3-3. 432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)

| Signal Name      | Ball No.  | Signal Name  | Ball No. | Signal Name                     | Ball No.   |
|------------------|---|--------------|----------|---------------------------------|--|
| MD35             | V30   | PE           | T3       | TDN                             | AL3  |
| MD36             | V29   | PERR#        | B9       | TDO                             | AH6  |
| MD37             | W31   | PLL2B        | D28      | TDP                             | AH5  |
| MD38             | W30   | PLL5B        | B29      | TEST0                           | D28  |
| MD39             | W29   | PLL6B        | C28      | TEST1                           | C28  |
| MD40             | AC31  | POR#         | J29      | TEST2                           | B29  |
| MD41             | AB29  | POWER_EN     | B28      | TEST3                           | AL16   |
| MD42             | AB30  | PWRBTN#      | E29      | TFT_PRSENT                      | AK13   |
| MD43             | AB31  | PWRCNT1      | F31      | TFTD0                           | C25, H3  |
| MD44             | AA29  | PWRCNT2      | G31      | TFTD1                           | D25, V3  |
| MD45             | AA31  | RASA#        | N31      | TFTD10                          | C21, V1  |
| MD46             | Y29   | RD#          | F3       | TFTD11                          | A25, V2  |
| MD47             | Y31   | REQ0#        | C1       | TFTD12                          | C23, H2  |
| MD48             | AH26  | REQ1#        | E3       | TFTD13                          | B19, U1  |
| MD49             | AL25  | RI2#         | H30      | TFTD14                          | D23, T3  |
| MD50             | AJ25  | ROMCS#       | G4       | TFTD15                          | A19, T4  |
| MD51             | AH25  | RTS2#        | AH4      | TFTD16                          | A24, W1  |
| MD52             | AL24  | SDATA_IN     | AK14     | TFTD17                          | C18, AB1   |
| MD53             | AK24  | SDATA_IN2    | H31      | TFTD2                           | C26, AB2   |
| MD54             | AJ24  | SDATA_OUT    | AK13     | TFTD3                           | A26, T1  |
| MD55             | AH24  | SDCLK_IN     | AJ30     | TFTD4                           | C17, AA3   |
| MD56             | AJ17  | SDCLK_OUT    | AH28     | TFTD5                           | A27, Y3  |
| MD57             | AL17  | SDCLK0       | AC29     | TFTD6                           | B24, AA1   |
| MD58             | AJ18  | SDCLK1       | AH16     | TFTD7                           | B18, Y1  |
| MD59             | AK18  | SDCLK2       | AL20     | TFTD8                           | C24, W3  |
| MD60             | AL18  | SDCLK3       | AJ16     | TFTD9                           | D24, W2  |
| MD61             | AJ19  | SDTEST0      | AH4      | TFTDCK                          | A22, J4  |
| MD62             | AK19  | SDTEST1      | AJ1      | TFTDE                           | C16, U3  |
| MD63             | AL19  | SDTEST2      | AG4      | THRM#                           | F28  |
| NC (Total of 13) | K1, M3, N2, P1,<br>P2, AB3, AC1,<br>AC2, AD1, AD2,<br>AD3, AD4, AE1 | SDTEST3      | AJ4      | TMS                             | AJ5  |
| ONCTL#           | E30   | SDTEST4      | AJ2      | TRDE#                           | H1   |
| OVER_CUR#        | C27   | SDTEST5      | AH3      | TRDY#                           | B8   |
| PAR              | C10   | SERIRQ       | AL8      | TRST#                           | AK4  |
| PC_BEEP          | AL15  | SERR#        | A9       | V <sub>BAT</sub>                | D30  |
| PCICLK           | E2  | SIN1         | D26      | V <sub>CORE</sub> (Total of 26) | D11, D13, D15,<br>D17, D19, D21,<br>K3, L4, L28, N4,<br>N28, R4, R28,<br>T30, U4, U28,<br>W4, W28, AA4,<br>AA28, AH11,<br>AH13, AH15,<br>AH17, AH19,<br>AH21 |
| PCICLK0          | D3  | SIN2         | AJ4      |                                 |  |
| PCICLK1          | E4  | SIN3         | J28      |                                 |  |
| PCIRST#          | D1  | SLCT         | T4       |                                 |  |
| PD0              | AA1   | SLIN#/ASTRB# | W1       |                                 |  |
| PD1              | Y1  | SMI_O        | Y3       |                                 |  |
| PD2              | W3  | SOUT1        | B27      |                                 |  |
| PD3              | W2  | SOUT2        | AK3      |                                 |  |
| PD4              | V1  | SOUT3        | J3       |                                 |  |
| PD5              | V2  | STB#/WRITE#  | AB1      |                                 |  |
| PD6              | V3  | STOP#        | D9       |                                 |  |
| PD7              | U1  | SYNC         | AL13     |                                 |  |
|                  |   | TCK          | AL4      |                                 |  |
|                  |   | TDI          | AK5      |                                 |  |



**Table 3-3. 432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)**

| Signal Name                   | Ball No.   | Signal Name                   | Ball No.  | Signal Name       | Ball No. |
|-------------------------------|--|-------------------------------|---|-------------------|----------|
| V <sub>IO</sub> (Total of 35) | A2, A30, B1, B6, B11, B16, B20, B25, B31, C3, C29, G2, G30, L3, M1, M2, M30, N1, T2, Y2, Y30, AC3, AE2, AE30, AJ3, AJ29, AK1, AK6, AK11, AK16, AK20, AK25, AK31, AL2, AL30 | V <sub>PLL3</sub>             | C31   | VS <sub>YNC</sub> | J2       |
| VPCKIN                        | AH7  | V <sub>SB</sub>               | F29   | WEA#              | N29      |
| VPD0                          | AH9  | V <sub>SBL</sub>              | H28   | WR#               | G1       |
| VPD1                          | AK8  | V <sub>SS</sub> (Total of 61) | A1, A31, B2, B7, B12, B15, B17, B21, B26, B30, D10, D12, D14, D18, D20, D22, F2, F30, K2, K4, K28, L1, L2, L30, M4, M28, N3, P3, P4, P28, R2, R30, U2, U30, V4, V28, Y4, Y28, AA2, AA30, AB4, AB28, AC4, AF2, AF30, AH10, AH12, AH14, AH18, AH20, AH22, AK2, AK7, AK12, AK15, AK17, AK21, AK26, AK30, AL1, AL31 | X27I              | A29      |
| VPD2                          | AJ8  |                               |   | X27O              | D27      |
| VPD3                          | AL7  |                               |   | X32I              | C30      |
| VPD4                          | AH8  |                               |   | X32O              | D29      |
| VPD5                          | AL6  |                               |   |                   |          |
| VPD6                          | AJ7  |                               |   |                   |          |
| VPD7                          | AJ6  |                               |   |                   |          |
| V <sub>PLL2</sub>             | R1   |                               |   |                   |          |

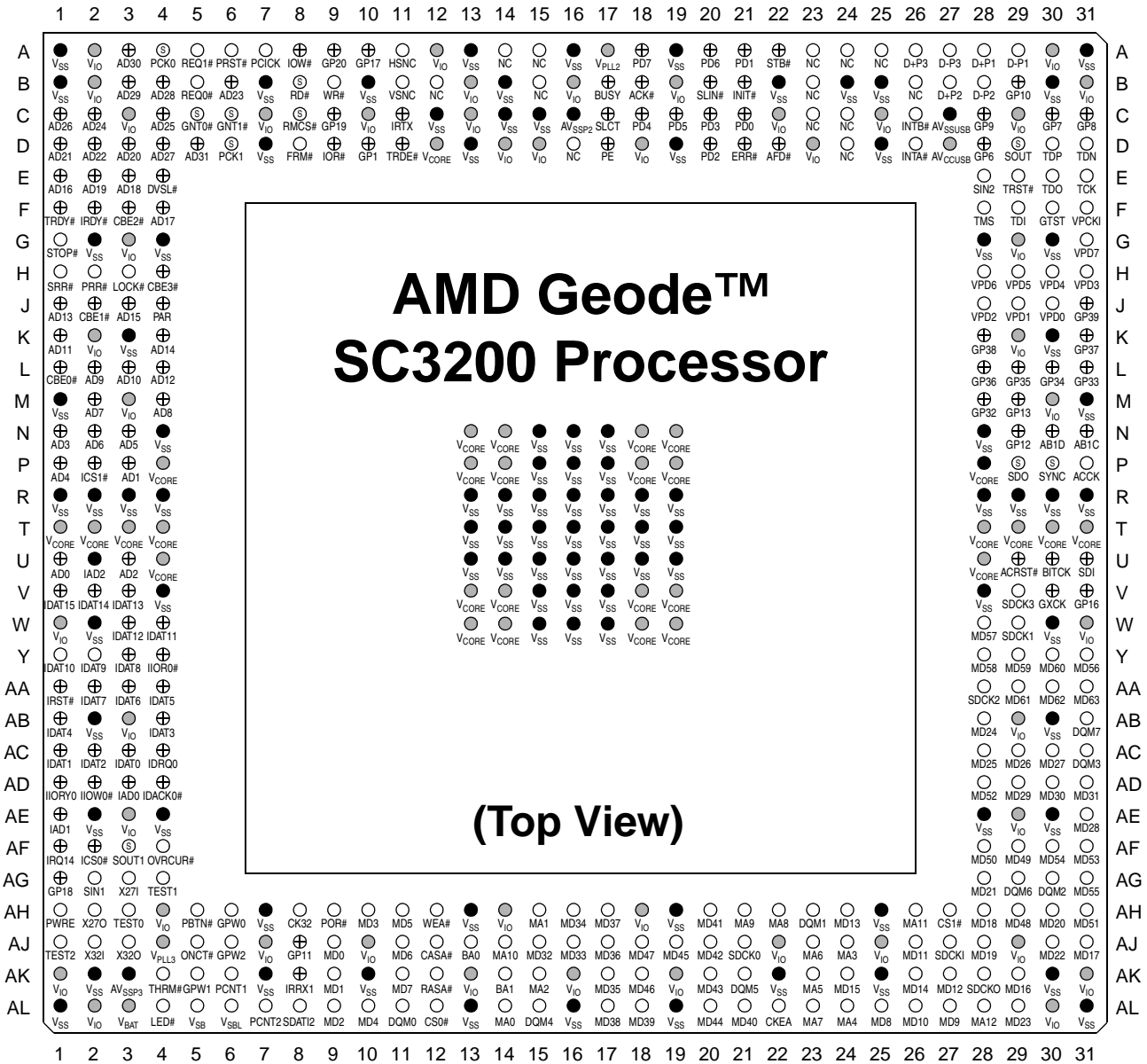


Figure 3-3. 481-TEPBGA Ball Assignment Diagram

Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number

| Ball No.            | Signal Name       | I/O (PU/PD)                  | Buffer <sup>1</sup> Type                | Power Rail      | Configuration   |
|---------------------|-------------------|------------------------------|---|-----------------|---|
| A1                  | V <sub>SS</sub>   | GND                          | ---                                     | ---             | ---   |
| A2                  | V <sub>IO</sub>   | PWR                          | ---                                     | ---             | ---   |
| A3                  | AD30              | I/O                          | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | D6                | I/O                          | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> |                 |   |
| A4                  | PCICLK0           | O                            | O <sub>PCI</sub>                        | V <sub>IO</sub> | ---   |
|                     | FPCI_MON          | I<br>(PD <sub>100</sub> )    | INSTRP                                  |                 |   |
| A5                  | REQ1#             | I<br>(PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                       | V <sub>IO</sub> | ---   |
| A6                  | PCIRST#           | O                            | O <sub>PCI</sub>                        | V <sub>IO</sub> | ---   |
| A7                  | PCICLK            | I                            | IN <sub>T</sub>                         | V <sub>IO</sub> | ---   |
| A8                  | IOW#              | O                            | O <sub>3/5</sub>                        | V <sub>IO</sub> | PMR[21] = 0 and<br>PMR[2] = 0                                     |
|                     | DOCW#             | O                            | O <sub>3/5</sub>                        |                 | PMR[21] = 0 and<br>PMR[2] = 1                                     |
|                     | GPIO15            | I/O<br>(PU <sub>22.5</sub> ) | IN <sub>TS</sub> ,<br>O <sub>3/5</sub>  |                 | PMR[21] = 1 and<br>PMR[2] = 1                                     |
| A9                  | GPIO20            | I/O<br>(PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>      | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and<br>PMR[7] = 0                        |
|                     | DOCCS#            | O<br>(PU <sub>22.5</sub> )   | O <sub>3/5</sub>                        |                 | PMR[23] <sup>3</sup> = 0 and<br>PMR[7] = 1                        |
|                     | TFTD0             | O<br>(PU <sub>22.5</sub> )   | O <sub>1/4</sub>                        |                 | PMR[23] <sup>3</sup> = 1  |
| A10                 | GPIO17            | I/O<br>(PU <sub>22.5</sub> ) | IN <sub>TS</sub> ,<br>O <sub>3/5</sub>  | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and<br>PMR[5] = 0                        |
|                     | IOCS0#            | O<br>(PU <sub>22.5</sub> )   | O <sub>3/5</sub>                        |                 | PMR[23] <sup>3</sup> = 0 and<br>PMR[5] = 1                        |
|                     | TFTDCK            | O<br>(PU <sub>22.5</sub> )   | O <sub>1/4</sub>                        |                 | PMR[23] <sup>3</sup> = 1  |
| A11                 | HSYNC             | O                            | O <sub>1/4</sub>                        | V <sub>IO</sub> | ---   |
| A12                 | V <sub>IO</sub>   | PWR                          | ---                                     | ---             | ---   |
| A13                 | V <sub>SS</sub>   | GND                          | ---                                     | ---             | ---   |
| A14                 | NC                | ---                          | ---                                     | ---             | ---   |
| A15                 | NC                | ---                          | ---                                     | ---             | ---   |
| A16                 | V <sub>SS</sub>   | GND                          | ---                                     | ---             | ---   |
| A17                 | V <sub>PLL2</sub> | PWR                          | ---                                     | ---             | ---   |
| A18 <sup>5, 2</sup> | PD7               | I/O                          | IN <sub>T</sub> ,<br>O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | TFTD13            | O                            | O <sub>1/4</sub>                        |                 | PMR[23] <sup>3</sup> = 1 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | F_AD7             | O                            | O <sub>14/14</sub>                      |                 | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 1 or<br>FPCI_MON = 1)  |
| A19                 | V <sub>SS</sub>   | GND                          | ---                                     | ---             | ---   |

| Ball No.            | Signal Name     | I/O (PU/PD)                | Buffer <sup>1</sup> Type                | Power Rail                | Configuration   |
|---------------------|-----------------|----------------------------|---|---------------------------|---|
| A20 <sup>5, 2</sup> | PD6             | I/O                        | IN <sub>T</sub> ,<br>O <sub>14/14</sub> | V <sub>IO</sub>           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | TFTD1           | O                          | O <sub>1/4</sub>                        |                           | PMR[23] <sup>3</sup> = 1 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | F_AD6           | O                          | O <sub>14/14</sub>                      |                           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 1 or<br>FPCI_MON = 1)  |
| A21 <sup>5, 2</sup> | PD1             | I/O                        | IN <sub>T</sub> ,<br>O <sub>14/14</sub> | V <sub>IO</sub>           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | TFTD7           | O                          | O <sub>1/4</sub>                        |                           | PMR[23] <sup>3</sup> = 1 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | F_AD1           | O                          | O <sub>14/14</sub>                      |                           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 1 or<br>FPCI_MON = 1)  |
| A22 <sup>5, 2</sup> | STB#/WRITE#     | O                          | O <sub>14/14</sub>                      | V <sub>IO</sub>           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | TFTD17          | O                          | O <sub>1/4</sub>                        |                           | PMR[23] <sup>3</sup> = 1 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) |
|                     | F_FRAME#        | O                          | O <sub>14/14</sub>                      |                           | PMR[23] <sup>3</sup> = 0 and<br>(PMR[27] = 1 or<br>FPCI_MON = 1)  |
| A23                 | NC              | ---                        | ---                                     | ---                       | ---   |
| A24                 | NC              | ---                        | ---                                     | ---                       | ---   |
| A25                 | NC              | ---                        | ---                                     | ---                       | ---   |
| A26 <sup>5</sup>    | DPOS_PORT3      | I/O                        | IN <sub>USB</sub> ,<br>O <sub>USB</sub> | AV <sub>C</sub> ,<br>CUSB | ---   |
| A27 <sup>5</sup>    | DNEG_PORT3      | I/O                        | IN <sub>USB</sub> ,<br>O <sub>USB</sub> | AV <sub>C</sub> ,<br>CUSB | ---   |
| A28 <sup>5</sup>    | DPOS_PORT1      | I/O                        | IN <sub>USB</sub> ,<br>O <sub>USB</sub> | AV <sub>C</sub> ,<br>CUSB | ---   |
| A29 <sup>5</sup>    | DNEG_PORT1      | I/O                        | IN <sub>USB</sub> ,<br>O <sub>USB</sub> | AV <sub>C</sub> ,<br>CUSB | ---   |
| A30                 | V <sub>IO</sub> | PWR                        | ---                                     | ---                       | ---   |
| A31                 | V <sub>SS</sub> | GND                        | ---                                     | ---                       | ---   |
| B1                  | V <sub>SS</sub> | GND                        | ---                                     | ---                       | ---   |
| B2                  | V <sub>IO</sub> | PWR                        | ---                                     | ---                       | ---   |
| B3                  | AD29            | I/O                        | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> | V <sub>IO</sub>           | Cycle Multiplexed   |
|                     | D5              | I/O                        | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> |                           |   |
| B4                  | AD28            | I/O                        | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> | V <sub>IO</sub>           | Cycle Multiplexed   |
|                     | D4              | I/O                        | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> |                           |   |
| B5                  | REQ0#           | I<br>(PU <sub>22.5</sub> ) | IN <sub>PCI</sub>                       | V <sub>IO</sub>           | ---   |

**Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.           | Signal Name     | I/O (PU/PD)            | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|--------------------|-----------------|------------------------|--------------------------------------|-----------------|---|
| B6                 | AD23            | I/O                    | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | A23             | O                      | O <sub>PCI</sub>                     |                 |   |
| B7                 | V <sub>SS</sub> | GND                    | ---                                  | ---             | ---   |
| B8                 | RD#             | O                      | O <sub>3/5</sub>                     | V <sub>IO</sub> | ---   |
|                    | CLKSELO         | I (PD <sub>100</sub> ) | IN <sub>STRP</sub>                   |                 |   |
| B9                 | WR#             | O                      | O <sub>3/5</sub>                     | V <sub>IO</sub> |   |
| B10                | V <sub>SS</sub> | GND                    | ---                                  | ---             | ---   |
| B11                | VSYNC           | O                      | O <sub>1/4</sub>                     | V <sub>IO</sub> | ---   |
| B12                | NC              | ---                    | ---                                  | ---             | ---   |
| B13                | V <sub>IO</sub> | PWR                    | ---                                  | ---             | ---   |
| B14                | V <sub>SS</sub> | GND                    | ---                                  | ---             | ---   |
| B15                | NC              | ---                    | ---                                  | ---             | ---   |
| B16                | V <sub>IO</sub> | PWR                    | ---                                  | ---             | ---   |
| B17 <sup>5,2</sup> | BUSY/WAIT#      | I                      | IN <sub>T</sub>                      | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD3           | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_C/BE1#        | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| B18 <sup>5,2</sup> | ACK#            | I                      | IN <sub>T</sub>                      | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTDE           | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | FPCICLK         | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| B19                | V <sub>IO</sub> | PWR                    | ---                                  | ---             | ---   |
| B20 <sup>5,2</sup> | SLIN#/ASTRB#    | O                      | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD16          | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_IRDY#         | O                      | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| B21 <sup>5,2</sup> | INIT#           | O                      | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD5           | O                      | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | SMI_O           | O                      | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| B22                | V <sub>SS</sub> | GND                    | ---                                  | ---             | ---   |
| B23                | NC              | ---                    | ---                                  | ---             | ---   |
| B24                | V <sub>SS</sub> | GND                    | ---                                  | ---             | ---   |

| Ball No.         | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail             | Configuration              |
|------------------|-----------------|---------------------------|--------------------------------------|------------------------|----------------------------|
| B25              | V <sub>SS</sub> | GND                       | ---                                  | ---                    | ---                        |
| B26              | NC              | ---                       | ---                                  | ---                    | ---                        |
| B27 <sup>5</sup> | DPOS_PORT2      | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| B28 <sup>5</sup> | DNEG_PORT2      | I/O                       | IN <sub>USB</sub> , O <sub>USB</sub> | AV <sub>C</sub> , CUSB | ---                        |
| B29              | GPIO10          | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>  | V <sub>IO</sub>        | PMR[18] = 0 and PMR[8] = 0 |
|                  | DSR2#           | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                        | PMR[18] = 1 and PMR[8] = 0 |
|                  | IDE_IORDY1      | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                    |                        | PMR[18] = 0 and PMR[8] = 1 |
|                  | SDTEST1         | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                        | PMR[18] = 1 and PMR[8] = 1 |
| B30              | V <sub>SS</sub> | GND                       | ---                                  | ---                    | ---                        |
| B31              | V <sub>IO</sub> | PWR                       | ---                                  | ---                    | ---                        |
| C1               | AD26            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub>        | Cycle Multiplexed          |
|                  | D2              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                        |                            |
| C2               | AD24            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub>        | Cycle Multiplexed          |
|                  | D0              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                        |                            |
| C3               | V <sub>IO</sub> | PWR                       | ---                                  | ---                    | ---                        |
| C4               | AD25            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub>        | Cycle Multiplexed          |
|                  | D1              | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                        |                            |
| C5               | GNT0#           | O                         | O <sub>PCI</sub>                     | V <sub>IO</sub>        | ---                        |
|                  | DID0            | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                        |                            |
| C6               | GNT1#           | O                         | O <sub>PCI</sub>                     | V <sub>IO</sub>        | ---                        |
|                  | DID1            | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                        |                            |
| C7               | V <sub>IO</sub> | PWR                       | ---                                  | ---                    | ---                        |
| C8               | ROMCS#          | O                         | O <sub>3/5</sub>                     | V <sub>IO</sub>        | ---                        |
|                  | BOOT16          | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                        |                            |
| C9               | GPIO19          | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>  | V <sub>IO</sub>        | PMR[9] = 0 and PMR[4] = 0  |
|                  | INTC#           | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                        | PMR[9] = 0 and PMR[4] = 1  |
|                  | IOCHRDY         | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                    |                        | PMR[9] = 1 and PMR[4] = 1  |
| C10              | V <sub>IO</sub> | PWR                       | ---                                  | ---                    | ---                        |
| C11              | IRTX            | O                         | O <sub>8/8</sub>                     | V <sub>IO</sub>        | PMR[6] = 0                 |
|                  | SOUT3           | O                         | O <sub>8/8</sub>                     |                        | PMR[6] = 1                 |
| C12              | V <sub>SS</sub> | GND                       | ---                                  | ---                    | ---                        |
| C13              | V <sub>IO</sub> | PWR                       | ---                                  | ---                    | ---                        |
| C14              | V <sub>SS</sub> | GND                       | ---                                  | ---                    | ---                        |

Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.           | Signal Name          | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|--------------------|----------------------|---------------------------|--------------------------------------|-----------------|---|
| C15                | V <sub>SS</sub>      | GND                       | ---                                  | ---             | ---   |
| C16                | AV <sub>SSPLL2</sub> | GND                       | ---                                  | ---             | ---   |
| C17 <sup>5,2</sup> | SLCT                 | I                         | IN <sub>T</sub>                      | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD15               | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_C/BE3#             | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| C18                | PD4                  | I/O                       | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD10               | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD4                | O                         | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| C19 <sup>5,2</sup> | PD5                  | I/O                       | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD11               | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD5                | O                         | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| C20 <sup>5,2</sup> | PD3                  | I/O                       | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD9                | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD3                | O                         | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| C21 <sup>5,2</sup> | PD0                  | I/O                       | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | TFTD6                | O                         | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0) |
|                    | F_AD0                | O                         | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)  |
| C22                | V <sub>IO</sub>      | PWR                       | ---                                  | ---             | ---   |
| C23                | NC                   | ---                       | ---                                  | ---             | ---   |
| C24                | NC                   | ---                       | ---                                  | ---             | ---   |
| C25                | V <sub>IO</sub>      | PWR                       | ---                                  | ---             | ---   |
| C26                | INTB#                | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| C27                | AV <sub>SSUSB</sub>  | GND                       | ---                                  | ---             | ---   |
| C28                | GPIO9                | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>1/4</sub>  | V <sub>IO</sub> | PMR[18] = 0 and PMR[8] = 0                                  |
|                    | DCD2#                | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                 | PMR[18] = 1 and PMR[8] = 0                                  |
|                    | IDE_IOW1#            | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                     |                 | PMR[18] = 0 and PMR[8] = 1                                  |
|                    | SDTEST2              | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                 | PMR[18] = 1 and PMR[8] = 1                                  |
| C29                | V <sub>IO</sub>      | PWR                       | ---                                  | ---             | ---   |
| C30                | GPIO7                | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>1/4</sub>  | V <sub>IO</sub> | PMR[17] = 0 and PMR[8] = 0                                  |
|                    | RTS2#                | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                     |                 | PMR[17] = 1 and PMR[8] = 0                                  |
|                    | IDE_DACK1#           | O (PU <sub>22.5</sub> )   | O <sub>1/4</sub>                     |                 | PMR[17] = 0 and PMR[8] = 1                                  |
|                    | SDTEST0              | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                 | PMR[17] = 1 and PMR[8] = 1                                  |
| C31                | GPIO8                | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>  | V <sub>IO</sub> | PMR[17] = 0 and PMR[8] = 0                                  |
|                    | CTS2#                | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                     |                 | PMR[17] = 1 and PMR[8] = 0                                  |
|                    | IDE_DREQ1            | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                    |                 | PMR[17] = 0 and PMR[8] = 1                                  |
|                    | SDTEST4              | O (PU <sub>22.5</sub> )   | O <sub>2/5</sub>                     |                 | PMR[17] = 1 and PMR[8] = 1                                  |
| D1                 | AD21                 | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | A21                  | O                         | O <sub>PCI</sub>                     |                 |   |
| D2                 | AD22                 | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | A22                  | O                         | O <sub>PCI</sub>                     |                 |   |
| D3                 | AD20                 | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | A20                  | O                         | O <sub>PCI</sub>                     |                 |   |
| D4                 | AD27                 | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | D3                   | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |   |
| D5                 | AD31                 | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                    | D7                   | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |   |
| D6                 | PCICLK1              | O                         | O <sub>PCI</sub>                     | V <sub>IO</sub> | ---   |
|                    | LPC_ROM              | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 |   |
| D7                 | V <sub>SS</sub>      | GND                       | ---                                  | ---             | ---   |
| D8                 | FRAME#               | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | ---   |
| D9                 | IOR#                 | O                         | O <sub>3/5</sub>                     | V <sub>IO</sub> | PMR[21] = 0 and PMR[2] = 0                                  |
|                    | DOCR#                | O                         | O <sub>3/5</sub>                     |                 | PMR[21] = 0 and PMR[2] = 1                                  |
|                    | GPIO14               | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>3/5</sub>  |                 | PMR[21] = 1 and PMR[2] = 1                                  |

**Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.            | Signal Name         | I/O (PU/PD)                                  | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|---------------------|---------------------|--|--------------------------------------|-----------------|---|
| D10                 | GPIO1               | I/O (PU <sub>22.5</sub> )                    | IN <sub>T</sub> , O <sub>3/5</sub>   | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and PMR[13] = 0  |
|                     | IOCS1#              | O (PU <sub>22.5</sub> )                      | O <sub>3/5</sub>                     | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and PMR[13] = 1  |
|                     | TFTD12              | O (PU <sub>22.5</sub> )                      | O <sub>1/4</sub>                     | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 1  |
| D11                 | TRDE#               | O  | O <sub>3/5</sub>                     | V <sub>IO</sub> | PMR[12] = 0   |
|                     | GPIO0               | I/O (PU <sub>22.5</sub> )                    | IN <sub>TS</sub> , O <sub>3/5</sub>  | V <sub>IO</sub> | PMR[12] = 1   |
| D12                 | V <sub>CORE</sub>   | PWR  | ---                                  | ---             | ---   |
| D13                 | V <sub>SS</sub>     | GND  | ---                                  | ---             | ---   |
| D14                 | V <sub>IO</sub>     | PWR  | ---                                  | ---             | ---   |
| D15                 | V <sub>IO</sub>     | PWR  | ---                                  | ---             | ---   |
| D16                 | NC                  | ---  | ---                                  | ---             | ---   |
| D17 <sup>5, 2</sup> | PE                  | I (PU <sub>22.5</sub> , PD <sub>22.5</sub> ) | IN <sub>T</sub>                      | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0) (PU/PD under software control.) |
|                     | TFTD14              | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | F_C/BE2#            | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| D18                 | V <sub>IO</sub>     | PWR  | ---                                  | ---             | ---   |
| D19                 | V <sub>SS</sub>     | GND  | ---                                  | ---             | ---   |
| D20 <sup>5, 2</sup> | PD2                 | I/O  | IN <sub>T</sub> , O <sub>14/14</sub> | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | TFTD8               | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | F_AD2               | O  | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| D21 <sup>5, 2</sup> | ERR#                | I  | IN <sub>T</sub> , O <sub>1/4</sub>   | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | TFTD4               | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | F_C/BE0#            | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| D22 <sup>5, 2</sup> | AFD#/DSTRB#         | O  | O <sub>14/14</sub>                   | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | TFTD2               | O  | O <sub>1/4</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and (PMR[27] = 0 and FPCI_MON = 0)                                 |
|                     | INTR_O              | O  | O <sub>14/14</sub>                   |                 | PMR[23] <sup>3</sup> = 0 and (PMR[27] = 1 or FPCI_MON = 1)                                  |
| D23                 | V <sub>IO</sub>     | PWR  | ---                                  | ---             | ---   |
| D24                 | NC                  | ---  | ---                                  | ---             | ---   |
| D25                 | V <sub>SS</sub>     | GND  | ---                                  | ---             | ---   |
| D26                 | INTA#               | I (PU <sub>22.5</sub> )                      | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| D27                 | AV <sub>CCUSB</sub> | PWR  | ---                                  | ---             | ---   |
| D28                 | GPIO6               | I/O (PU <sub>22.5</sub> )                    | IN <sub>TS</sub> , O <sub>1/4</sub>  | V <sub>IO</sub> | PMR[18] = 0 and PMR[8] = 0  |
|                     | DTR2#/BOUT2         | O (PU <sub>22.5</sub> )                      | O <sub>1/4</sub>                     |                 | PMR[18] = 1 and PMR[8] = 0  |
|                     | IDE_IOR1#           | O (PU <sub>22.5</sub> )                      | O <sub>1/4</sub>                     |                 | PMR[18] = 0 and PMR[8] = 1  |
|                     | SDTEST5             | O (PU <sub>22.5</sub> )                      | O <sub>2/5</sub>                     |                 | PMR[18] = 1 and PMR[8] = 1  |
| D29                 | SOUT2               | O  | O <sub>8/8</sub>                     | V <sub>IO</sub> | ---   |
|                     | CLKSEL2             | I (PD <sub>100</sub> )                       | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)   |
| D30                 | TDP                 | I/O  | Diode                                | ---             | ---   |
| D31                 | TDN                 | I/O  | WIRE                                 | V <sub>IO</sub> | ---   |
| E1                  | AD16                | I/O  | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | A16                 | O  | O <sub>PCI</sub>                     |                 |   |
| E2                  | AD19                | I/O  | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | A19                 | O  | O <sub>PCI</sub>                     |                 |   |
| E3                  | AD18                | I/O  | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | A18                 | O  | O <sub>PCI</sub>                     |                 |   |
| E4                  | DEVSEL#             | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | BHE#                | O  | O <sub>PCI</sub>                     |                 |   |
| E28                 | SIN2                | I  | IN <sub>TS</sub>                     | V <sub>IO</sub> | PMR[28] = 0   |
|                     | SDTEST3             | O  | O <sub>2/5</sub>                     |                 | PMR[28] = 1   |
| E29                 | TRST#               | I (PU <sub>22.5</sub> )                      | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| E30                 | TDO                 | O  | O <sub>PCI</sub>                     | V <sub>IO</sub> | ---   |
| E31                 | TCK                 | I (PU <sub>22.5</sub> )                      | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |
| F1                  | TRDY#               | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | D13                 | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |   |
| F2                  | IRDY#               | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | D14                 | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |   |
| F3                  | C/BE2#              | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | D10                 | I/O (PU <sub>22.5</sub> )                    | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |   |
| F4                  | AD17                | I/O  | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed   |
|                     | A17                 | O  | O <sub>PCI</sub>                     |                 |   |
| F28                 | TMS                 | I (PU <sub>22.5</sub> )                      | IN <sub>PCI</sub>                    | V <sub>IO</sub> | ---   |

Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No. | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail      | Configuration     |
|----------|-----------------|---------------------------|---------------------------------------|-----------------|-------------------|
| F29      | TDI             | I (PU <sub>22.5</sub> )   | IN <sub>PCI</sub>                     | V <sub>IO</sub> | ---               |
| F30      | GTEST           | I (PD <sub>22.5</sub> )   | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| F31      | VPCKIN          | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| G1       | STOP#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D15             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                   |
| G2       | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---               |
| G3       | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---               |
| G4       | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---               |
| G28      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---               |
| G29      | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---               |
| G30      | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---               |
| G31      | VPD7            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| H1       | SERR#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , OD <sub>PCI</sub> | V <sub>IO</sub> | ---               |
| H2       | PERR#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | ---               |
| H3       | LOCK#           | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | ---               |
| H4       | C/BE3#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D11             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                   |
| H28      | VPD6            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| H29      | VPD5            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| H30      | VPD4            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| H31      | VPD3            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| J1       | AD13            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A13             | O                         | O <sub>PCI</sub>                      |                 |                   |
| J2       | C/BE1#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D9              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                   |
| J3       | AD15            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | A15             | O                         | O <sub>PCI</sub>                      |                 |                   |
| J4       | PAR             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  | V <sub>IO</sub> | Cycle Multiplexed |
|          | D12             | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub>  |                 |                   |
| J28      | VPD2            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| J29      | VPD1            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |
| J30      | VPD0            | I                         | IN <sub>T</sub>                       | V <sub>IO</sub> | ---               |

| Ball No. | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration  |
|----------|-----------------|---------------------------|--------------------------------------|-----------------|--|
| J31      | GPIO39          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0  |
|          | SERIRQ          | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1  |
| K1       | AD11            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | A11             | O                         | O <sub>PCI</sub>                     |                 |  |
| K2       | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---  |
| K3       | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---  |
| K4       | AD14            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | A14             | O                         | O <sub>PCI</sub>                     |                 |  |
| K28      | GPIO38/IRR2     | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0. The IRR2 input is connected to the input path of GPIO38. There is no logic required to enable IRR2, just a simple connection. Hence, when GPIO38 is the selected function, IRR2 is also selected. |
|          | LPCPD#          | O                         | O <sub>PCI</sub>                     |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1  |
| K29      | V <sub>IO</sub> | PWR                       | ---                                  | ---             | ---  |
| K30      | V <sub>SS</sub> | GND                       | ---                                  | ---             | ---  |
| K31      | GPIO37          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0  |
|          | LFRAME#         | O                         | O <sub>PCI</sub>                     |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1  |
| L1       | C/BE0#          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | D8              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 |  |
| L2       | AD9             | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | A9              | O                         | O <sub>PCI</sub>                     |                 |  |
| L3       | AD10            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | A10             | O                         | O <sub>PCI</sub>                     |                 |  |
| L4       | AD12            | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed  |
|          | A12             | O                         | O <sub>PCI</sub>                     |                 |  |
| L28      | GPIO36          | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0  |
|          | LDRQ#           | I                         | IN <sub>PCI</sub>                    |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1  |

**Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No. | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration   |
|----------|-------------------|---------------------------|--------------------------------------|-----------------|---|
| L29      | GPIO35            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0 |
|          | LAD3              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1 |
| L30      | GPIO34            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0 |
|          | LAD2              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1 |
| L31      | GPIO33            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0 |
|          | LAD1              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1 |
| M1       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| M2       | AD7               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                                     |
|          | A7                | O                         | O <sub>PCI</sub>                     |                 |   |
| M3       | V <sub>IO</sub>   | PWR                       | ---                                  | ---             | ---   |
| M4       | AD8               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                                     |
|          | A8                | O                         | O <sub>PCI</sub>                     |                 |   |
| M28      | GPIO32            | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | PMR[14] <sup>4</sup> = 0 and PMR[22] <sup>4</sup> = 0 |
|          | LAD0              | I/O (PU <sub>22.5</sub> ) | IN <sub>PCI</sub> , O <sub>PCI</sub> |                 | PMR[14] <sup>4</sup> = 1 and PMR[22] <sup>4</sup> = 1 |
| M29      | GPIO13            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8/8</sub>  | V <sub>IO</sub> | PMR[19] = 0   |
|          | AB2D              | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    |                 | PMR[19] = 1   |
| M30      | V <sub>IO</sub>   | PWR                       | ---                                  | ---             | ---   |
| M31      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| N1       | AD3               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                                     |
|          | A3                | O                         | O <sub>PCI</sub>                     |                 |   |
| N2       | AD6               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                                     |
|          | A6                | O                         | O <sub>PCI</sub>                     |                 |   |
| N3       | AD5               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                                     |
|          | A5                | O                         | O <sub>PCI</sub>                     |                 |   |
| N4       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| N13      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---   |
| N14      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---   |
| N15      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| N16      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| N17      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |
| N18      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---   |
| N19      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---   |
| N28      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---   |

| Ball No. | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type             | Power Rail      | Configuration                            |
|----------|-------------------|---------------------------|--------------------------------------|-----------------|--|
| N29      | GPIO12            | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8/8</sub>  | V <sub>IO</sub> | PMR[19] = 0                              |
|          | AB2C              | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    |                 | PMR[19] = 1                              |
| N30      | AB1D              | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0                 |
|          | GPIO1             | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>   |                 | PMR[23] <sup>3</sup> = 1 and PMR[13] = 0 |
|          | IOCS1#            | O                         | O <sub>3/5</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and PMR[13] = 1 |
| N31      | AB1C              | I/O (PU <sub>22.5</sub> ) | IN <sub>AB</sub> , O <sub>8</sub>    | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0                 |
|          | GPIO20            | I/O (PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>3/5</sub>   |                 | PMR[23] <sup>3</sup> = 1 and PMR[7] = 0  |
|          | DOCCS#            | O                         | O <sub>3/5</sub>                     |                 | PMR[23] <sup>3</sup> = 1 and PMR[7] = 1  |
| P1       | AD4               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                        |
|          | A4                | O                         | O <sub>PCI</sub>                     |                 |  |
| P2       | IDE_CS1#          | O                         | O <sub>1/4</sub>                     | V <sub>IO</sub> | PMR[24] = 0                              |
|          | TFTDE             | O                         | O <sub>1/4</sub>                     |                 | PMR[24] = 1                              |
| P3       | AD1               | I/O                       | IN <sub>PCI</sub> , O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed                        |
|          | A1                | O                         | O <sub>PCI</sub>                     |                 |  |
| P4       | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P13      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P14      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P15      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| P16      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| P17      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| P18      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P19      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P28      | V <sub>CORE</sub> | PWR                       | ---                                  | ---             | ---                                      |
| P29      | SDATA_OUT         | O                         | O <sub>AC97</sub>                    | V <sub>IO</sub> | ---                                      |
|          | TFT_PRSN          | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)        |
| P30      | SYNC              | O                         | O <sub>AC97</sub>                    | V <sub>IO</sub> | ---                                      |
|          | CLKSEL3           | I (PD <sub>100</sub> )    | IN <sub>STRP</sub>                   |                 | Strap (See Table 3-6 on page 58.)        |
| P31      | AC97_CLK          | O                         | O <sub>2/5</sub>                     | V <sub>IO</sub> | PMR[25] = 1                              |
| R1       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R2       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R3       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R4       | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R13      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R14      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R15      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R16      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |
| R17      | V <sub>SS</sub>   | GND                       | ---                                  | ---             | ---                                      |



Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No. | Signal Name       | I/O (PU/PD) | Buffer <sup>1</sup> Type                | Power Rail      | Configuration     |
|----------|-------------------|-------------|---|-----------------|-------------------|
| R18      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| R19      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| R28      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| R29      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| R30      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| R31      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T1       | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T2       | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T3       | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T4       | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T13      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T14      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T15      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T16      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T17      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T18      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T19      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| T28      | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T29      | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T30      | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| T31      | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| U1       | AD0               | I/O         | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed |
|          | A0                | O           | O <sub>PCI</sub>                        |                 |                   |
| U2       | IDE_ADDR2         | O           | O <sub>1/4</sub>                        | V <sub>IO</sub> | PMR[24] = 0       |
|          | TFTD4             | O           | O <sub>1/4</sub>                        |                 | PMR[24] = 1       |
| U3       | AD2               | I/O         | IN <sub>PCI</sub> ,<br>O <sub>PCI</sub> | V <sub>IO</sub> | Cycle Multiplexed |
|          | A2                | O           | O <sub>PCI</sub>                        |                 |                   |
| U4       | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| U13      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U14      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U15      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U16      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U17      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U18      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U19      | V <sub>SS</sub>   | GND         | ---                                     | ---             | ---               |
| U28      | V <sub>CORE</sub> | PWR         | ---                                     | ---             | ---               |
| U29      | AC97_RST#         | O           | O <sub>2/5</sub>                        | V <sub>IO</sub> | FPCI_MON = 0      |
|          | F_STOP#           | O           | O <sub>2/5</sub>                        |                 | FPCI_MON = 1      |
| U30      | BIT_CLK           | I           | IN <sub>T</sub>                         | V <sub>IO</sub> | FPCI_MON = 0      |
|          | F_TRDY#           | O           | O <sub>1/4</sub>                        |                 | FPCI_MON = 1      |
| U31      | SDATA_IN          | I           | IN <sub>T</sub>                         | V <sub>IO</sub> | FPCI_MON = 0      |
|          | F_GNT0#           | O           | O <sub>2/5</sub>                        |                 | FPCI_MON = 1      |

| Ball No.         | Signal Name       | I/O (PU/PD)                  | Buffer <sup>1</sup> Type                 | Power Rail      | Configuration                               |
|------------------|-------------------|------------------------------|--|-----------------|---|
| V1               | IDE_DATA15        | I/O                          | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                                 |
|                  | TFTD7             | O                            | O <sub>1/4</sub>                         |                 | PMR[24] = 1                                 |
| V2               | IDE_DATA14        | I/O                          | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                                 |
|                  | TFTD17            | O                            | O <sub>1/4</sub>                         |                 | PMR[24] = 1                                 |
| V3               | IDE_DATA13        | I/O                          | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                                 |
|                  | TFTD15            | O                            | O <sub>1/4</sub>                         |                 | PMR[24] = 1                                 |
| V4               | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| V13              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| V14              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| V15              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| V16              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| V17              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| V18              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| V19              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| V28              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| V29              | SDCLK3            | O                            | O <sub>2/5</sub>                         | V <sub>IO</sub> | ---   |
| V30              | GXCLK             | O                            | O <sub>2/5</sub>                         | V <sub>IO</sub> | PMR[23] <sup>3</sup> = 0 and<br>PMR[29] = 0 |
|                  | FP_VDD_ON         | O                            | O <sub>1/4</sub>                         |                 | PMR[23] <sup>3</sup> = 1                    |
|                  | TEST3             | O                            | O <sub>2/5</sub>                         |                 | PMR[23] <sup>3</sup> = 0 and<br>PMR[29] = 1 |
| V31              | GPIO16            | I/O<br>(PU <sub>22.5</sub> ) | IN <sub>T</sub> , O <sub>2/5</sub>       | V <sub>IO</sub> | PMR[0] = 0 and<br>FPCI_MON = 0              |
|                  | PC_BEEP           | O                            | O <sub>2/5</sub>                         |                 | PMR[0] = 1 = 0 and<br>FPCI_MON = 0          |
|                  | F_DEVSEL#         | O                            | O <sub>2/5</sub>                         |                 | FPCI_MON = 1                                |
| W1               | V <sub>IO</sub>   | PWR                          | ---                                      | ---             | ---   |
| W2               | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| W3               | IDE_DATA12        | I/O                          | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                                 |
|                  | TFTD13            | O                            | O <sub>1/4</sub>                         |                 | PMR[24] = 1                                 |
| W4               | IDE_DATA11        | I/O                          | IN <sub>TS1</sub> ,<br>TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0                                 |
|                  | GPIO41            | I/O                          | IN <sub>TS1</sub> ,<br>O <sub>1/4</sub>  |                 | PMR[24] = 1                                 |
| W13              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| W14              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| W15              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| W16              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| W17              | V <sub>SS</sub>   | GND                          | ---                                      | ---             | ---   |
| W18              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| W19              | V <sub>CORE</sub> | PWR                          | ---                                      | ---             | ---   |
| W28 <sup>5</sup> | MD57              | I/O                          | IN <sub>T</sub> ,<br>TS <sub>2/5</sub>   | V <sub>IO</sub> | ---   |
| W29              | SDCLK1            | O                            | O <sub>2/5</sub>                         | V <sub>IO</sub> | ---   |

**Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.          | Signal Name     | I/O (PU/PD) | Buffer <sup>1</sup> Type              | Power Rail      | Configuration |
|-------------------|-----------------|-------------|---------------------------------------|-----------------|---------------|
| W30               | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| W31               | V <sub>IO</sub> | PWR         | ---                                   | ---             | ---           |
| Y1                | IDE_DATA10      | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
| Y2                | IDE_DATA9       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
| Y3                | IDE_DATA8       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | GPIO40          | I/O         | IN <sub>TS1</sub> , O <sub>1/4</sub>  |                 | PMR[24] = 1   |
| Y4                | IDE_IOR0#       | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD10          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| Y28 <sup>5</sup>  | MD58            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| Y29 <sup>5</sup>  | MD59            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| Y30 <sup>5</sup>  | MD60            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| Y31 <sup>5</sup>  | MD56            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AA1               | IDE_RST#        | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTDCK          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AA2               | IDE_DATA7       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | INTD#           | I           | IN <sub>TS</sub>                      |                 | PMR[24] = 1   |
| AA3               | IDE_DATA6       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | IRQ9            | I           | IN <sub>TS1</sub>                     |                 | PMR[24] = 1   |
| AA4               | IDE_DATA5       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | CLK27M          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AA28              | SDCLK2          | O           | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AA29 <sup>5</sup> | MD61            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AA30 <sup>5</sup> | MD62            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AA31 <sup>5</sup> | MD63            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AB1               | IDE_DATA4       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | FP_VDD_ON       | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AB2               | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| AB3               | V <sub>IO</sub> | PWR         | ---                                   | ---             | ---           |
| AB4               | IDE_DATA3       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD12          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AB28 <sup>5</sup> | MD24            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AB29              | V <sub>IO</sub> | PWR         | ---                                   | ---             | ---           |
| AB30              | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |

| Ball No.          | Signal Name     | I/O (PU/PD) | Buffer <sup>1</sup> Type              | Power Rail      | Configuration |
|-------------------|-----------------|-------------|---------------------------------------|-----------------|---------------|
| AB31              | DQM7            | O           | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AC1               | IDE_DATA1       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD16          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AC2               | IDE_DATA2       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD14          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AC3               | IDE_DATA0       | I/O         | IN <sub>TS1</sub> , TS <sub>1/4</sub> | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD6           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AC4               | IDE_DREQ0       | I           | IN <sub>TS1</sub>                     | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD8           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AC28 <sup>5</sup> | MD25            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AC29 <sup>5</sup> | MD26            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AC30 <sup>5</sup> | MD27            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AC31              | DQM3            | O           | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AD1               | IDE_IORDY0      | I           | IN <sub>TS1</sub>                     | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD11          | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AD2               | IDE_IOW0#       | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD9           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AD3               | IDE_ADDR0       | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD3           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AD4               | IDE_DACK0#      | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD0           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AD28 <sup>5</sup> | MD52            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AD29 <sup>5</sup> | MD29            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AD30 <sup>5</sup> | MD30            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AD31 <sup>5</sup> | MD31            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AE1               | IDE_ADDR1       | O           | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD2           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |
| AE2               | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| AE3               | V <sub>IO</sub> | PWR         | ---                                   | ---             | ---           |
| AE4               | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| AE28              | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| AE29              | V <sub>IO</sub> | PWR         | ---                                   | ---             | ---           |
| AE30              | V <sub>SS</sub> | GND         | ---                                   | ---             | ---           |
| AE31 <sup>5</sup> | MD28            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AF1               | IRQ14           | I           | IN <sub>TS1</sub>                     | V <sub>IO</sub> | PMR[24] = 0   |
|                   | TFTD1           | O           | O <sub>1/4</sub>                      |                 | PMR[24] = 1   |

Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.          | Signal Name     | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail      | Configuration                     |
|-------------------|-----------------|---------------------------|---------------------------------------|-----------------|-----------------------------------|
| AF2               | IDE_CS0#        | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub> | PMR[24] = 0                       |
|                   | TFTD5           | O                         | O <sub>1/4</sub>                      |                 | PMR[24] = 1                       |
| AF3               | SOUT1           | O                         | O <sub>8/8</sub>                      | V <sub>IO</sub> | ---                               |
|                   | CLKSEL1         | I (PD <sub>100</sub> )    | INSTRP                                |                 | Strap (See Table 3-6 on page 58.) |
| AF4               | OVER_CUR#       | I                         | IN <sub>TS</sub>                      | V <sub>IO</sub> | ---                               |
| AF28 <sup>5</sup> | MD50            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AF29 <sup>5</sup> | MD49            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AF30 <sup>5</sup> | MD54            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AF31 <sup>5</sup> | MD53            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AG1               | GPIO18          | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>   | V <sub>IO</sub> | PMR[16] = 0                       |
|                   | DTR1#/BOUT1     | O (PU <sub>22.5</sub> )   | O <sub>8/8</sub>                      |                 | PMR[16] = 1                       |
| AG2               | SIN1            | I                         | IN <sub>TS</sub>                      | V <sub>IO</sub> | ---                               |
| AG3               | X27I            | I                         | WIRE                                  | V <sub>IO</sub> | ---                               |
| AG4               | TEST1           | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | PMR[29] = 1                       |
|                   | PLL6B           | I/O                       | IN <sub>TS</sub> , TS <sub>2/5</sub>  |                 | PMR[29] = 0                       |
| AG28 <sup>5</sup> | MD21            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AG29              | DQM6            | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---                               |
| AG30              | DQM2            | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---                               |
| AG31 <sup>5</sup> | MD55            | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AH1               | POWER_EN        | O                         | O <sub>1/4</sub>                      | V <sub>IO</sub> | ---                               |
| AH2               | X27O            | O                         | WIRE                                  | V <sub>IO</sub> | ---                               |
| AH3               | TEST0           | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | PMR[29] = 1                       |
|                   | PLL2B           | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   |                 | PMR[29] = 0                       |
| AH4               | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |
| AH5               | PWRBTN#         | I (PU <sub>100</sub> )    | IN <sub>BTN</sub>                     | V <sub>SB</sub> | ---                               |
| AH6               | GPWIO0          | I/O (PU <sub>100</sub> )  | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub> | ---                               |
| AH7               | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| AH8               | CLK32           | O                         | O <sub>2/5</sub>                      | V <sub>SB</sub> | ---                               |
| AH9               | POR#            | I                         | IN <sub>TS</sub>                      | V <sub>IO</sub> | ---                               |
| AH10 <sup>5</sup> | MD3             | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AH11 <sup>5</sup> | MD5             | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---                               |
| AH12              | WEA#            | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---                               |
| AH13              | V <sub>SS</sub> | GND                       | ---                                   | ---             | ---                               |
| AH14              | V <sub>IO</sub> | PWR                       | ---                                   | ---             | ---                               |

| Ball No.            | Signal Name       | I/O (PU/PD)               | Buffer <sup>1</sup> Type              | Power Rail       | Configuration              |
|---------------------|-------------------|---------------------------|---------------------------------------|------------------|----------------------------|
| AH15                | MA1               | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH16 <sup>5</sup>   | MD34              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH17 <sup>5</sup>   | MD37              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH18                | V <sub>IO</sub>   | PWR                       | ---                                   | ---              | ---                        |
| AH19                | V <sub>SS</sub>   | GND                       | ---                                   | ---              | ---                        |
| AH20 <sup>5</sup>   | MD41              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH21                | MA9               | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH22                | MA8               | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH23                | DQM1              | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH24 <sup>5</sup>   | MD13              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH25                | V <sub>SS</sub>   | GND                       | ---                                   | ---              | ---                        |
| AH26                | MA11              | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH27                | CS1#              | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AH28 <sup>5</sup>   | MD18              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH29 <sup>5</sup>   | MD48              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH30 <sup>5</sup>   | MD20              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AH31 <sup>5</sup>   | MD51              | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AJ1                 | TEST2             | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | PMR[29] = 1                |
|                     | PLL5B             | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   |                  | PMR[29] = 0                |
| AJ2                 | X32I              | I                         | WIRE                                  | V <sub>BAT</sub> | ---                        |
| AJ3                 | X32O              | O                         | WIRE                                  | V <sub>BAT</sub> | ---                        |
| AJ4                 | V <sub>PLL3</sub> | PWR                       | ---                                   | ---              | ---                        |
| AJ5 <sup>5, 2</sup> | ONCTL#            | O                         | OD <sub>14</sub>                      | V <sub>SB</sub>  | ---                        |
| AJ6                 | GPWIO2            | I/O (PU <sub>100</sub> )  | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub>  | ---                        |
| AJ7                 | V <sub>IO</sub>   | PWR                       | ---                                   | ---              | ---                        |
| AJ8                 | GPIO11            | I/O (PU <sub>22.5</sub> ) | IN <sub>TS</sub> , O <sub>8/8</sub>   | V <sub>IO</sub>  | PMR[18] = 0 and PMR[8] = 0 |
|                     | RI2#              | I (PU <sub>22.5</sub> )   | IN <sub>TS</sub>                      |                  | PMR[18] = 1 and PMR[8] = 0 |
|                     | IRQ15             | I (PU <sub>22.5</sub> )   | IN <sub>TS1</sub>                     |                  | PMR[18] = 0 and PMR[8] = 1 |
| AJ9 <sup>5</sup>    | MD0               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AJ10                | V <sub>IO</sub>   | PWR                       | ---                                   | ---              | ---                        |
| AJ11 <sup>5</sup>   | MD6               | I/O                       | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub>  | ---                        |
| AJ12                | CASA#             | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AJ13                | BA0               | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |
| AJ14                | MA10              | O                         | O <sub>2/5</sub>                      | V <sub>IO</sub>  | ---                        |

**Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)**

| Ball No.            | Signal Name          | I/O (PU/PD)              | Buffer <sup>1</sup> Type              | Power Rail      | Configuration |
|---------------------|----------------------|--------------------------|---------------------------------------|-----------------|---------------|
| AJ15 <sup>5</sup>   | MD32                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ16 <sup>5</sup>   | MD33                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ17 <sup>5</sup>   | MD36                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ18 <sup>5</sup>   | MD47                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ19 <sup>5</sup>   | MD45                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ20 <sup>5</sup>   | MD42                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ21                | SDCLK0               | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AJ22                | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |
| AJ23                | MA6                  | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AJ24                | MA3                  | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AJ25                | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |
| AJ26 <sup>5</sup>   | MD11                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ27                | SDCLK_IN             | I                        | IN <sub>T</sub>                       | V <sub>IO</sub> | ---           |
| AJ28 <sup>5</sup>   | MD19                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ29                | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |
| AJ30 <sup>5</sup>   | MD22                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AJ31 <sup>5</sup>   | MD17                 | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AK1                 | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |
| AK2                 | V <sub>SS</sub>      | GND                      | ---                                   | ---             | ---           |
| AK3                 | AV <sub>SSPLL3</sub> | GND                      | ---                                   | ---             | ---           |
| AK4                 | THRM#                | I                        | IN <sub>TS</sub>                      | V <sub>SB</sub> | ---           |
| AK5                 | GPWIO1               | I/O (PU <sub>100</sub> ) | IN <sub>TS</sub> , TS <sub>2/14</sub> | V <sub>SB</sub> | ---           |
| AK6 <sup>5, 2</sup> | PWRCNT1              | O                        | OD <sub>14</sub>                      | V <sub>SB</sub> | ---           |
| AK7                 | V <sub>SS</sub>      | GND                      | ---                                   | ---             | ---           |
| AK8                 | IRRX1                | I                        | IN <sub>TS</sub>                      | V <sub>SB</sub> | PMR[6] = 0    |
|                     | SIN3                 | I                        | IN <sub>TS</sub>                      | V <sub>IO</sub> | PMR[6] = 1    |
| AK9 <sup>5</sup>    | MD1                  | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AK10                | V <sub>SS</sub>      | GND                      | ---                                   | ---             | ---           |
| AK11 <sup>5</sup>   | MD7                  | I/O                      | IN <sub>T</sub> , TS <sub>2/5</sub>   | V <sub>IO</sub> | ---           |
| AK12                | RASA#                | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AK13                | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |
| AK14                | BA1                  | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AK15                | MA2                  | O                        | O <sub>2/5</sub>                      | V <sub>IO</sub> | ---           |
| AK16                | V <sub>IO</sub>      | PWR                      | ---                                   | ---             | ---           |

| Ball No.            | Signal Name      | I/O (PU/PD) | Buffer <sup>1</sup> Type            | Power Rail      | Configuration                    |
|---------------------|------------------|-------------|-------------------------------------|-----------------|----------------------------------|
| AK17 <sup>5</sup>   | MD35             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK18 <sup>5</sup>   | MD46             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK19                | V <sub>IO</sub>  | PWR         | ---                                 | ---             | ---                              |
| AK20 <sup>5</sup>   | MD43             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK21                | DQM5             | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AK22                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AK23                | MA5              | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AK24 <sup>5</sup>   | MD15             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK25                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AK26 <sup>5</sup>   | MD14             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK27 <sup>5</sup>   | MD12             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK28                | SDCLK_OUT        | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AK29 <sup>5</sup>   | MD16             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AK30                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AK31                | V <sub>IO</sub>  | PWR         | ---                                 | ---             | ---                              |
| AL1                 | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AL2                 | V <sub>IO</sub>  | PWR         | ---                                 | ---             | ---                              |
| AL3                 | V <sub>BAT</sub> | PWR         | ---                                 | ---             | ---                              |
| AL4                 | LED#             | O           | OD <sub>14</sub>                    | V <sub>SB</sub> | ---                              |
| AL5                 | V <sub>SB</sub>  | PWR         | ---                                 | ---             | ---                              |
| AL6                 | V <sub>SBL</sub> | PWR         | ---                                 | ---             | ---                              |
| AL7 <sup>5, 2</sup> | PWRCNT2          | O           | OD <sub>14</sub>                    | V <sub>SB</sub> | ---                              |
| AL8                 | SDATA_IN2        | I           | IN <sub>TS</sub>                    | V <sub>SB</sub> | F3BAR0+Memory Offset 08h[21] = 1 |
| AL9 <sup>5</sup>    | MD2              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AL10 <sup>5</sup>   | MD4              | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AL11                | DQM0             | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AL12                | CS0#             | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AL13                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AL14                | MA0              | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AL15                | DQM4             | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---                              |
| AL16                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AL17 <sup>5</sup>   | MD38             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AL18 <sup>5</sup>   | MD39             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |
| AL19                | V <sub>SS</sub>  | GND         | ---                                 | ---             | ---                              |
| AL20 <sup>5</sup>   | MD44             | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---                              |

Table 3-4. 481-TEPBGA Ball Assignment - Sorted by Ball Number (Continued)

| Ball No.          | Signal Name | I/O (PU/PD) | Buffer <sup>1</sup> Type            | Power Rail      | Configuration |
|-------------------|-------------|-------------|-------------------------------------|-----------------|---------------|
| AL21 <sup>5</sup> | MD40        | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---           |
| AL22              | CKEA        | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---           |
| AL23              | MA7         | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---           |
| AL24              | MA4         | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---           |
| AL25 <sup>5</sup> | MD8         | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---           |
| AL26 <sup>5</sup> | MD10        | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---           |
| AL27 <sup>5</sup> | MD9         | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---           |
| AL28              | MA12        | O           | O <sub>2/5</sub>                    | V <sub>IO</sub> | ---           |

| Ball No.          | Signal Name     | I/O (PU/PD) | Buffer <sup>1</sup> Type            | Power Rail      | Configuration |
|-------------------|-----------------|-------------|-------------------------------------|-----------------|---------------|
| AL29 <sup>5</sup> | MD23            | I/O         | IN <sub>T</sub> , TS <sub>2/5</sub> | V <sub>IO</sub> | ---           |
| AL30              | V <sub>IO</sub> | PWR         | ---                                 | ---             | ---           |
| AL31              | V <sub>SS</sub> | GND         | ---                                 | ---             | ---           |

- For Buffer Type definitions, refer to Table 9-10 "Buffer Types" on page 375.
- Is 5V tolerant (ACK#, AFD#/DSTRB#, BUSY/WAIT#, ERR#, INIT#, PD[7:0], PE, SLCT, SLIN#/ASTRB#, STB#/WRITE#, ONCTL#, PWRCNT[2:1]).
- The TFT\_PRSNNT strap determines the power-on reset (POR) state of PMR[23].
- The LPC\_ROM strap determines the power-on reset (POR) state of PMR[14] and PMR[22].
- Is back-drive protected (MD[63:0], DPOS\_PORT1, DNEG\_PORT1, DPOS\_PORT2, DNEG\_PORT2, DPOS\_PORT3, DNEG\_PORT3, ACK#, AFD#/DSTRB#, BUSY/WAIT#, ERR#, INIT#, PD[7:0], PE, SLCT, SLIN#/ASTRB#, STB#/WRITE#, ONCTL#, PWRCNT[2:1]).

Table 3-5. 481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name

| Signal Name | Ball No. | Signal Name           | Ball No. | Signal Name | Ball No. |
|-------------|----------|-----------------------|----------|-------------|----------|
| A0          | U1       | AD18                  | E3       | D8          | L1       |
| A1          | P3       | AD19                  | E2       | D9          | J2       |
| A2          | U3       | AD20                  | D3       | D10         | F3       |
| A3          | N1       | AD21                  | D1       | D11         | H4       |
| A4          | P1       | AD22                  | D2       | D12         | J4       |
| A5          | N3       | AD23                  | B6       | D13         | F1       |
| A6          | N2       | AD24                  | C2       | D14         | F2       |
| A7          | M2       | AD25                  | C4       | D15         | G1       |
| A8          | M4       | AD26                  | C1       | DCD2#       | C28      |
| A9          | L2       | AD27                  | D4       | DEVSEL#     | E4       |
| A10         | L3       | AD28                  | B4       | DID0        | C5       |
| A11         | K1       | AD29                  | B3       | DID1        | C6       |
| A12         | L4       | AD30                  | A3       | DNEG_PORT1  | A29      |
| A13         | J1       | AD31                  | D5       | DNEG_PORT2  | B28      |
| A14         | K4       | AFD#/DSTRB#           | D22      | DNEG_PORT3  | A27      |
| A15         | J3       | AV <sub>CC</sub> USB  | D27      | DOCCS#      | A9, N31  |
| A16         | E1       | AV <sub>SS</sub> PLL2 | C16      | DOCR#       | D9       |
| A17         | F4       | AV <sub>SS</sub> PLL3 | AK3      | DOCW#       | A8       |
| A18         | E3       | AV <sub>SS</sub> USB  | C27      | DPOS_PORT1  | A28      |
| A19         | E2       | BA0                   | AJ13     | DPOS_PORT2  | B27      |
| A20         | D3       | BA1                   | AK14     | DPOS_PORT3  | A26      |
| A21         | D1       | BHE#                  | E4       | DQM0        | AL11     |
| A22         | D2       | BIT_CLK               | U30      | DQM1        | AH23     |
| A23         | B6       | BOOT16                | C8       | DQM2        | AG30     |
| AB1C        | N31      | BUSY/WAIT#            | B17      | DQM3        | AC31     |
| AB1D        | N30      | C/BE0#                | L1       | DQM4        | AL15     |
| AB2C        | N29      | C/BE1#                | J2       | DQM5        | AK21     |
| AB2D        | M29      | C/BE2#                | F3       | DQM6        | AG29     |
| AC97_CLK    | P31      | C/BE3#                | H4       | DQM7        | AB31     |
| AC97_RST#   | U29      | CASA#                 | AJ12     | DSR2#       | B29      |
| ACK#        | B18      | CKEA                  | AL22     | DTR1#/BOUT1 | AG1      |
| AD0         | U1       | CLK27M                | AA4      | DTR2#/BOUT2 | D28      |
| AD1         | P3       | CLK32                 | AH8      | ERR#        | D21      |
| AD2         | U3       | CLKSEL0               | B8       | F_AD0       | C21      |
| AD3         | N1       | CLKSEL1               | AF3      | F_AD1       | A21      |
| AD4         | P1       | CLKSEL2               | D29      | F_AD2       | D20      |
| AD5         | N3       | CLKSEL3               | P30      | F_AD3       | C20      |
| AD6         | N2       | CS0#                  | AL12     | F_AD4       | C18      |
| AD7         | M2       | CS1#                  | AH27     | F_AD5       | C19      |
| AD8         | M4       | CTS2#                 | C31      | F_AD6       | A20      |
| AD9         | L2       | D0                    | C2       | F_AD7       | A18      |
| AD10        | L3       | D1                    | C4       | F_C/BE0#    | D21      |
| AD11        | K1       | D2                    | C1       | F_C/BE1#    | B17      |
| AD12        | L4       | D3                    | D4       | F_C/BE2#    | D17      |
| AD13        | J1       | D4                    | B4       | F_C/BE3#    | C17      |
| AD14        | K4       | D5                    | B3       | F_DEVSEL#   | V31      |
| AD15        | J3       | D6                    | A3       | F_FRAME#    | A22      |
| AD16        | E1       | D7                    | D5       | F_GNT0#     | U31      |
| AD17        | F4       |                       |          | F_IRDY#     | B20      |

**Table 3-5. 481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)**

| Signal Name  | Ball No. | Signal Name | Ball No. | Signal Name | Ball No. |
|--------------|----------|-------------|----------|-------------|----------|
| F_STOP#      | U29      | IDE_DATA1   | AC1      | LOCK#       | H3       |
| F_TRDY#      | U30      | IDE_DATA2   | AC2      | LPC_ROM     | D6       |
| FP_VDD_ON    | V30, AB1 | IDE_DATA3   | AB4      | LPCPD#      | K28      |
| FPCI_MON     | A4       | IDE_DATA4   | AB1      | MA0         | AL14     |
| FPCICLK      | B18      | IDE_DATA5   | AA4      | MA1         | AH15     |
| FRAME#       | D8       | IDE_DATA6   | AA3      | MA2         | AK15     |
| GNT0#        | C5       | IDE_DATA7   | AA2      | MA3         | AJ24     |
| GNT1#        | C6       | IDE_DATA8   | Y3       | MA4         | AL24     |
| GPIO0        | D11      | IDE_DATA9   | Y2       | MA5         | AK23     |
| GPIO1        | D10, N30 | IDE_DATA10  | Y1       | MA6         | AJ23     |
| GPIO6        | D28      | IDE_DATA11  | W4       | MA7         | AL23     |
| GPIO7        | C30      | IDE_DATA12  | W3       | MA8         | AH22     |
| GPIO8        | C31      | IDE_DATA13  | V3       | MA9         | AH21     |
| GPIO9        | C28      | IDE_DATA14  | V2       | MA10        | AJ14     |
| GPIO10       | B29      | IDE_DATA15  | V1       | MA11        | AH26     |
| GPIO11       | AJ8      | IDE_DREQ0   | AC4      | MA12        | AL28     |
| GPIO12       | N29      | IDE_DREQ1   | C31      | MD0         | AJ9      |
| GPIO13       | M29      | IDE_IOR0#   | Y4       | MD1         | AK9      |
| GPIO14       | D9       | IDE_IOR1#   | D28      | MD2         | AL9      |
| GPIO15       | A8       | IDE_IORDY0  | AD1      | MD3         | AH10     |
| GPIO16       | V31      | IDE_IORDY1  | B29      | MD4         | AL10     |
| GPIO17       | A10      | IDE_IOW0#   | AD2      | MD5         | AH11     |
| GPIO18       | AG1      | IDE_IOW1#   | C28      | MD6         | AJ11     |
| GPIO19       | C9       | IDE_RST#    | AA1      | MD7         | AK11     |
| GPIO20       | A9, N31  | INIT#       | B21      | MD8         | AL25     |
| GPIO32       | M28      | INTA#       | D26      | MD9         | AL27     |
| GPIO33       | L31      | INTB#       | C26      | MD10        | AL26     |
| GPIO34       | L30      | INTC#       | C9       | MD11        | AJ26     |
| GPIO35       | L29      | INTD#       | AA2      | MD12        | AK27     |
| GPIO36       | L28      | INTR_O      | D22      | MD13        | AH24     |
| GPIO37       | K31      | IOCHRDY     | C9       | MD14        | AK26     |
| GPIO38/IRRX2 | K28      | IOCS0#      | A10      | MD15        | AK24     |
| GPIO39       | J31      | IOCS1#      | D10      | MD16        | AK29     |
| GPIO40       | Y3       | IOCS1#      | N30      | MD17        | AJ31     |
| GPIO41       | W4       | IOR#        | D9       | MD18        | AH28     |
| GPWIO0       | AH6      | IOW#        | A8       | MD19        | AJ28     |
| GPWIO1       | AK5      | IRDY#       | F2       | MD20        | AH30     |
| GPWIO2       | AJ6      | IRQ9        | AA3      | MD21        | AG28     |
| GTEST        | F30      | IRQ14       | AF1      | MD22        | AJ30     |
| GXCLK        | V30      | IRQ15       | AJ8      | MD23        | AL29     |
| HSYNC        | A11      | IRRX1       | AK8      | MD24        | AB28     |
| IDE_ADDR0    | AD3      | IRTX        | C11      | MD25        | AC28     |
| IDE_ADDR1    | AE1      | LAD0        | M28      | MD26        | AC29     |
| IDE_ADDR2    | U2       | LAD1        | L31      | MD27        | AC30     |
| IDE_CS0#     | AF2      | LAD2        | L30      | MD28        | AE31     |
| IDE_CS1#     | P2       | LAD3        | L29      | MD29        | AD29     |
| IDE_DACK0#   | AD4      | LDRQ#       | L28      | MD30        | AD30     |
| IDE_DACK1#   | C30      | LED#        | AL4      | MD31        | AD31     |
| IDE_DATA0    | AC3      | LFRAME#     | K31      | MD32        | AJ15     |

Table 3-5. 481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)

| Signal Name      | Ball No.  | Signal Name  | Ball No. | Signal Name                     | Ball No.  |
|------------------|---|--------------|----------|---------------------------------|---|
| MD33             | AJ16  | PD4          | C18      | STB#/WRITE#                     | A22   |
| MD34             | AH16  | PD5          | C19      | STOP#                           | G1  |
| MD35             | AK17  | PD6          | A20      | SYNC                            | P30   |
| MD36             | AJ17  | PD7          | A18      | TCK                             | E31   |
| MD37             | AH17  | PE           | D17      | TDI                             | F29   |
| MD38             | AL17  | PERR#        | H2       | TDN                             | D31   |
| MD39             | AL18  | PLL2B        | AH3      | TDO                             | E30   |
| MD40             | AL21  | PLL5B        | AJ1      | TDP                             | D30   |
| MD41             | AH20  | PLL6B        | AG4      | TEST0                           | AH3   |
| MD42             | AJ20  | POR#         | AH9      | TEST1                           | AG4   |
| MD43             | AK20  | POWER_EN     | AH1      | TEST2                           | AJ1   |
| MD44             | AL20  | PWRBTN#      | AH5      | TEST3                           | V30   |
| MD45             | AJ19  | PWRCNT1      | AK6      | TFT_PRSN                        | P29   |
| MD46             | AK18  | PWRCNT2      | AL7      | TFTD0                           | A9, AD4   |
| MD47             | AJ18  | RASA#        | AK12     | TFTD1                           | A20, AF1  |
| MD48             | AH29  | RD#          | B8       | TFTD2                           | D22, AE1  |
| MD49             | AF29  | REQ0#        | B5       | TFTD3                           | B17, AD3  |
| MD50             | AF28  | REQ1#        | A5       | TFTD4                           | D21, U2   |
| MD51             | AH31  | RI2#         | AJ8      | TFTD5                           | B21, AF2  |
| MD52             | AD28  | ROMCS#       | C8       | TFTD6                           | C21, AC3  |
| MD53             | AF31  | RTS2#        | C30      | TFTD7                           | A21, V1   |
| MD54             | AF30  | SDATA_IN     | U31      | TFTD8                           | D20, AC4  |
| MD55             | AG31  | SDATA_IN2    | AL8      | TFTD9                           | C20, AD2  |
| MD56             | Y31   | SDATA_OUT    | P29      | TFTD10                          | C18, Y4   |
| MD57             | W28   | SDCLK_IN     | AJ27     | TFTD11                          | C19, AD1  |
| MD58             | Y28   | SDCLK_OUT    | AK28     | TFTD12                          | D10, AB4  |
| MD59             | Y29   | SDCLK0       | AJ21     | TFTD13                          | A18, W3   |
| MD60             | Y30   | SDCLK1       | W29      | TFTD14                          | D17, AC2  |
| MD61             | AA29  | SDCLK2       | AA28     | TFTD15                          | C17, V3   |
| MD62             | AA30  | SDCLK3       | V29      | TFTD16                          | B20, AC1  |
| MD63             | AA31  | SDTEST0      | C30      | TFTD17                          | A22, V2   |
| NC (Total of 13) | A14, A15, A23,<br>A24, A25, B12,<br>B15, B23, B26,<br>C23, C24, D16,<br>D24 | SDTEST1      | B29      | TFTDCK                          | A10, AA1  |
| ONCTL#           | AJ5   | SDTEST2      | C28      | TFTDE                           | B18, P2   |
| OVER_CUR#        | AF4   | SDTEST3      | E28      | THRM#                           | AK4   |
| PAR              | J4  | SDTEST4      | C31      | TMS                             | F28   |
| PC_BEEP          | V31   | SDTEST5      | D28      | TRDE#                           | D11   |
| PCICLK           | A7  | SERIRQ       | J31      | TRDY#                           | F1  |
| PCICLK0          | A4  | SERR#        | H1       | TRST#                           | E29   |
| PCICLK1          | D6  | SIN1         | AG2      | V <sub>BAT</sub>                | AL3   |
| PCIRST#          | A6  | SIN2         | E28      | V <sub>CORE</sub> (Total of 29) | D12, N13, N14,<br>N18, N19, P4,<br>P13, P14, P18,<br>P19, P28, T1, T2,<br>T3, T4, T28, T29,<br>T30, T31, U4,<br>U28, V13, V14,<br>V18, V19, W13,<br>W14, W18, W19 |
| PD0              | C21   | SIN3         | AK8      |                                 |   |
| PD1              | A21   | SLCT         | C17      |                                 |   |
| PD2              | D20   | SLIN#/ASTRB# | B20      |                                 |   |
| PD3              | C20   | SMI_O        | B21      |                                 |   |
|                  |   | SOUT1        | AF3      |                                 |   |
|                  |   | SOUT2        | D29      |                                 |   |
|                  |   | SOUT3        | C11      |                                 |   |



**Table 3-5. 481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name (Continued)**

| Signal Name                   | Ball No.  | Signal Name                   | Ball No.  | Signal Name | Ball No. |     |    |
|-------------------------------|---|-------------------------------|---|-------------|----------|-----|----|
| V <sub>IO</sub> (Total of 46) | A2, A12, A30, B2, B13, B16, B19, B31, C3, C7, C10, C13, C22, C25, C29, D14, D15, D18, D23, G3, G29, K2, K29, M3, M30, W1, W31, AB3, AB29, AE3, AE29, AH4, AH14, AH18, AJ7, AJ10, AJ22, AJ25, AJ29, AK1, AK13, AK16, AK19, AK31, AL2, AL30 | V <sub>SS</sub> (Total of 96) | A1, A13, A16, A19, A31, B1, B7, B10, B14, B22, B24, B25, B30, C12, C14, C15, D7, D13, D19, D25, G2, G4, G28, G30, K3, K30, M1, M31, N4, N15, N16, N17, N28, P15, P16, P17, R1, R2, R3, R4, R13, R14, R15, R16, R17, R18, R19, R28, R29, R30, R31, T13, T14, T15, T16, T17, T18, T19, U13, U14, U15, U16, U17, U18, U19, V4, V15, V16, V17, V28, W2, W15, W16, W17, W30, AB2, AB30, AE2, AE4, AE28, AE30, AH7, AH13, AH19, AH25, AK2, AK7, AK10, AK22, AK25, AK30, AL1, AL13, AL16, AL19, AL31 | WEA#        | AH12     | WR# | B9 |
| VPCKIN                        | F31   |                               |   | X27I        | AG3      |     |    |
| VPD0                          | J30   |                               |   | X27O        | AH2      |     |    |
| VPD1                          | J29   |                               |   | X32I        | AJ2      |     |    |
| VPD2                          | J28   |                               |   | X32O        | AJ3      |     |    |
| VPD3                          | H31   |                               |   |             |          |     |    |
| VPD4                          | H30   |                               |   |             |          |     |    |
| VPD5                          | H29   |                               |   |             |          |     |    |
| VPD6                          | H28   |                               |   |             |          |     |    |
| VPD7                          | G31   |                               |   |             |          |     |    |
| V <sub>PLL2</sub>             | A17   |                               |   |             |          |     |    |
| V <sub>PLL3</sub>             | AJ4   |                               |   |             |          |     |    |
| V <sub>SB</sub>               | AL5   |                               |   |             |          |     |    |
| V <sub>SBL</sub>              | AL6   | VSYNC                         | B11   |             |          |     |    |

## 3.2 Strap Options

Several balls are read at power-up that set up the state of the SC3200. These balls are typically multiplexed with other functions that are outputs after the power-up sequence is complete. The SC3200 must read the state of the balls at power-up and the internal PU or PD resistors do not guarantee the correct state will be read. Therefore, it is required that an external PU or PD resistor with a value

of 1.5 K $\Omega$  be placed on the balls listed in Table 3-6. The value of the resistor is important to ensure that the proper state is read during the power-up sequence. If the ball is not read correctly at power-up, the SC3200 may default to a state that causes it to function improperly, possibly resulting in application failure.

**Table 3-6. Strap Options**

| Strap Option   | Muxed With | Ball No. |        | Nominal Internal PU or PD | External PU/PD Strap Settings                           |   | Register References   |
|--|------------|----------|--------|---------------------------|---|---|---|
|  |            | EBGA     | TEPBGA |                           | Strap = 0 (PD)  | Strap = 1 (PU)  |   |
| CLKSEL0  | RD#        | F3       | B8     | PD <sub>100</sub>         | See Table 4-7 on page 101 for CLKSEL strap options.     |   | GCB+I/O Offset 1Eh[9:8] (aka CCFC register bits [9:8]) (RO): Value programmed at reset by CLKSEL[1:0].  |
| CLKSEL1  | SOUT1      | B27      | AF3    | PD <sub>100</sub>         |   |   |   |
| CLKSEL2  | SOUT2      | AK3      | D29    | PD <sub>100</sub>         |   |   |   |
| CLKSEL3  | SYNC       | AL13     | P30    | PD <sub>100</sub>         |   |   |   |
| BOOT16   | ROMCS#     | G4       | C8     | PD <sub>100</sub>         | Enable boot from 8-bit ROM                              | Enable boot from 16-bit ROM   | GCB+I/O Offset 34h[3] (aka MCR register bit 3) (RO): Reads back strap setting.<br>GCB+I/O Offset 34h[14] (R/W): Used to allow the ROMCS# width to be changed under program control.                               |
| TFT_PRSENT   | SDATA_OUT  | AK13     | P29    | PD <sub>100</sub>         | TFT not muxed onto Parallel Port                        | TFT muxed onto Parallel Port  | GCB+I/O Offset 30h[23] (aka PMR register bit 23) (R/W): Reads back strap setting.   |
| LPC_ROM  | PCICLK1    | E4       | D6     | PD <sub>100</sub>         | Disable boot from ROM on LPC bus                        | Enable boot from ROM on LPC bus   | F0BAR1+I/O Offset 10h[15] (R/W): Reads back strap setting and allows LPC ROM to be changed under program control.   |
| FPCI_MON   | PCICLK0    | D3       | A4     | PD <sub>100</sub>         | Disable Fast-PCI, INTR_O, and SMI_O monitoring signals. | Enable Fast-PCI, INTR_O, and SMI_O monitoring signals. (Useful during debug.) | GCB+I/O Offset 34h[30] (aka MCR register bit 30) (RO): Reads back strap setting.<br><b>Note:</b> For normal operation, strap this signal low using a 1.5 K $\Omega$ resistor.                                     |
| DID0   | GNT0#      | D4       | C5     | PD <sub>100</sub>         | Defines the system-level chip ID.                       |   | GCB+I/O Offset 34h[31,29] (aka MCR register bits 31 and 29) (RO): Reads back strap setting.<br><b>Note:</b> GNT0# must have a PU resistor of 1.5 K $\Omega$ and GNT1# must have a PU resistor of 1.5 K $\Omega$ . |
| DID1   | GNT1#      | D2       | C6     | PD <sub>100</sub>         |   |   |   |
| <b>Note:</b> Accuracy of internal PU/PD resistors: 80K to 250K.<br>Location of the GCB (General Configuration Block) cannot be determined by software. See the <i>AMD Geode™ SC3200 Specification Update</i> document. |            |          |        |                           |   |   |   |

### 3.3 Multiplexing Configuration

The tables that follow list multiplexing options and their configurations. Certain multiplexing options may be chosen per signal; others are available only for a group of signals.

Where ever a GPIO pin is multiplexed with another function, there is an optional pull-up resistor on this pin; after

system reset, the pull-up is present. This pull-up resistor can be disabled by writing Core Logic registers. The configuration is without regard to the selected ball function. The above applies to all pins multiplexed with GPIO, except GPIO12, GPIO13, and GPIO16.

**Table 3-7. Two-Signal/Group Multiplexing**

| EBGA     | TEPBGA | Default    |               | Alternate              |               |
|----------|--------|------------|---------------|------------------------|---------------|
|          |        | Signal     | Configuration | Signal                 | Configuration |
| Ball No. |        | IDE        |               | TFT, PCI, GPIO, System |               |
| A26      | AD3    | IDE_ADDR0  | PMR[24] = 0   | TFTD3                  | PMR[24] = 1   |
| C26      | AE1    | IDE_ADDR1  |               | TFTD2                  |               |
| C17      | U2     | IDE_ADDR2  |               | TFTD4                  |               |
| B24      | AC3    | IDE_DATA0  |               | TFTD6                  |               |
| A24      | AC1    | IDE_DATA1  |               | TFTD16                 |               |
| D23      | AC2    | IDE_DATA2  |               | TFTD14                 |               |
| C23      | AB4    | IDE_DATA3  |               | TFTD12                 |               |
| B23      | AB1    | IDE_DATA4  |               | FP_VDD_ON              |               |
| A23      | AA4    | IDE_DATA5  |               | CLK27M                 |               |
| C22      | AA3    | IDE_DATA6  |               | IRQ9                   |               |
| B22      | AA2    | IDE_DATA7  |               | INTD#                  |               |
| A21      | Y3     | IDE_DATA8  |               | GPIO40                 |               |
| C20      | Y2     | IDE_DATA9  |               | DDC_SDA                |               |
| A20      | Y1     | IDE_DATA10 |               | DDC_SCL                |               |
| C19      | W4     | IDE_DATA11 |               | GPIO41                 |               |
| B19      | W3     | IDE_DATA12 |               | TFTD13                 |               |
| A19      | V3     | IDE_DATA13 |               | TFTD15                 |               |
| C18      | V2     | IDE_DATA14 |               | TFTD17                 |               |
| B18      | V1     | IDE_DATA15 |               | TFTD7                  |               |
| C21      | Y4     | IDE_IOR0#  |               | TFTD10                 |               |
| A25      | AD1    | IDE_IORDY0 |               | TFTD11                 |               |
| C24      | AC4    | IDE_DREQ0  |               | TFTD8                  |               |
| D24      | AD2    | IDE_IOW0#  |               | TFTD9                  |               |
| A27      | AF2    | IDE_CS0#   |               | TFTD5                  |               |
| C16      | P2     | IDE_CS1#   |               | TFTDE                  |               |
| C25      | AD4    | IDE_DACK0# | TFTD0         |                        |               |
| A22      | AA1    | IDE_RST#   | TFTDCK        |                        |               |
| D25      | AF1    | IRQ14      | TFTD1         |                        |               |
| Ball No. |        | Sub-ISA    |               | GPIO                   |               |
| H1       | D11    | TRDE#      | PMR[12] = 0   | GPIO0                  | PMR[12] = 1   |

**Table 3-7. Two-Signal/Group Multiplexing (Continued)**

| EBGA            | TEPBGA | Default              |                                | Alternate              |                                |
|-----------------|--------|----------------------|--------------------------------|------------------------|--------------------------------|
|                 |        | Signal               | Configuration                  | Signal                 | Configuration                  |
| <b>Ball No.</b> |        | <b>GPIO</b>          |                                | <b>ACCESS.bus</b>      |                                |
| AJ12            | N29    | GPIO12               | PMR[19] = 0                    | AB2C                   | PMR[19] = 1                    |
| AL11            | M29    | GPIO13               |                                | AB2D                   |                                |
| <b>Ball No.</b> |        | <b>GPIO</b>          |                                | <b>UART</b>            |                                |
| A28             | AG1    | GPIO18               | PMR[16] = 0                    | DTR1#/BOUT1            | PMR[16] = 1                    |
| <b>Ball No.</b> |        | <b>Infrared</b>      |                                | <b>UART</b>            |                                |
| J3              | C11    | IRTX                 | PMR[6] = 0                     | SOUT3                  | PMR[6] = 1                     |
| J28             | AK8    | IRRX1                |                                | SIN3                   |                                |
| <b>Ball No.</b> |        | <b>GPIO</b>          |                                | <b>LPC</b>             |                                |
| AJ11            | M28    | GPIO32               | PMR[14] = 0 and<br>PMR[22] = 0 | LAD0                   | PMR[14] = 1 and<br>PMR[22] = 1 |
| AL10            | L31    | GPIO33               |                                | LAD1                   |                                |
| AK10            | L30    | GPIO34               |                                | LAD2                   |                                |
| AJ10            | L29    | GPIO35               |                                | LAD3                   |                                |
| AL9             | L28    | GPIO36               |                                | LDRQ#                  |                                |
| AK9             | K31    | GPIO37               |                                | LFRAME#                |                                |
| AJ9             | K28    | GPIO38/IRRX2         |                                | LPCPD#                 |                                |
| AL8             | J31    | GPIO39               |                                | SERIRQ                 |                                |
| <b>Ball No.</b> |        | <b>UART</b>          |                                | <b>Internal Test</b>   |                                |
| AJ4             | E28    | SIN2                 | PMR[28] = 0                    | SDTEST3                | PMR[28] = 1                    |
| <b>Ball No.</b> |        | <b>AC97</b>          |                                | <b>FPCI Monitoring</b> |                                |
| AJ15            | U29    | AC97_RST#            | FPCI_MON = 0                   | F_STOP#                | FPCI_MON = 1                   |
| AK14            | U31    | SDATA_IN             |                                | F_GNT0#                |                                |
| AL14            | U30    | BIT_CLK              |                                | F_TRDY#                |                                |
| <b>Ball No.</b> |        | <b>Internal Test</b> |                                | <b>Internal Test</b>   |                                |
| C28             | AG4    | PLL6B                | PMR[29] = 0                    | TEST1                  | PMR[29] = 1                    |
| B29             | AJ1    | PLL5B                |                                | TEST2                  |                                |
| D28             | AH3    | PLL2B                |                                | TEST0                  |                                |

**Table 3-8. Three-Signal/Group Multiplexing**

| EBGA            | TEPBGA | Default        |                               | Alternate1                 |                               | Alternate2             |                               |
|-----------------|--------|----------------|-------------------------------|----------------------------|-------------------------------|------------------------|-------------------------------|
|                 |        | Signal         | Configuration                 | Signal                     | Configuration                 | Signal                 | Configuration                 |
| <b>Ball No.</b> |        | <b>Sub-ISA</b> |                               | <b>Sub-ISA<sup>1</sup></b> |                               | <b>GPIO</b>            |                               |
| F1              | D9     | IOR#           | PMR[21] = 0 and<br>PMR[2] = 0 | DOCR#                      | PMR[21] = 0 and<br>PMR[2] = 1 | GPIO14                 | PMR[21] = 1 and<br>PMR[2] = 1 |
| G3              | A8     | IOW#           |                               | DOCV#                      |                               | GPIO15                 |                               |
| <b>Ball No.</b> |        | <b>GPIO</b>    |                               | <b>AC97</b>                |                               | <b>FPCI Monitoring</b> |                               |

Table 3-8. Three-Signal/Group Multiplexing (Continued)

| EBGA            | TEPBGA | Default              |  | Alternate1             |  | Alternate2             |   |
|-----------------|--------|----------------------|--|------------------------|--|------------------------|---|
|                 |        | Signal               | Configuration  | Signal                 | Configuration  | Signal                 | Configuration                                       |
| AL15            | V31    | GPIO16               | PMR[0] = 0 and<br>FPCI_MON = 0                       | PC_BEEP                | PMR[0] = 1 = 0 and<br>FPCI_MON = 0                   | F_DEVSEL               | FPCI_MON = 1  |
| <b>Ball No.</b> |        | <b>GPIO</b>          |  | <b>PCI<sup>2</sup></b> |  | <b>Sub-ISA</b>         |   |
| H4              | C9     | GPIO19               | PMR[9] = 0 and<br>PMR[4] = 0                         | INTC#                  | PMR[9] = 0 and<br>PMR[4] = 1                         | IOCHRDY                | PMR[9] = 1 and<br>PMR[4] = 1                        |
| <b>Ball No.</b> |        | <b>Parallel Port</b> |  | <b>TFT<sup>3</sup></b> |  | <b>FPCI Monitoring</b> |   |
| U3              | B18    | ACK#                 | PMR[23] = 0 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) | TFTDE                  | PMR[23] = 1 and<br>(PMR[27] = 0 and<br>FPCI_MON = 0) | FPCI_CLK               | PMR[23] = 0 and<br>(PMR[27] = 1 or<br>FPCI_MON = 1) |
| AB2             | D22    | AFD#/DSTRB#          |  | TFTD2                  |  | INTR_O                 |   |
| T1              | B17    | BUSY/WAIT#           |  | TFTD3                  |  | F_C/BE1#               |   |
| AA3             | D21    | ERR#                 |  | TFTD4                  |  | F_C/BE0#               |   |
| Y3              | B21    | INIT#                |  | TFTD5                  |  | SMI_O                  |   |
| AA1             | C21    | PD0                  |  | TFTD6                  |  | F_AD0                  |   |
| Y1              | A21    | PD1                  |  | TFTD7                  |  | F_AD1                  |   |
| W3              | D20    | PD2                  |  | TFTD8                  |  | F_AD2                  |   |
| W2              | C20    | PD3                  |  | TFTD9                  |  | F_AD3                  |   |
| V1              | C18    | PD4                  |  | TFTD10                 |  | F_AD4                  |   |
| V2              | C19    | PD5                  |  | TFTD11                 |  | F_AD5                  |   |
| V3              | A20    | PD6                  |  | TFTD1                  |  | F_AD6                  |   |
| U1              | A18    | PD7                  |  | TFTD13                 |  | F_AD7                  |   |
| T3              | D17    | PE                   |  | TFTD14                 |  | F_C/BE2#               |   |
| T4              | C17    | SLCT                 |  | TFTD15                 |  | F_C/BE3#               |   |
| W1              | B20    | SLIN#<br>/ASTRB#     |  | TFTD16                 |  | F_IRDY                 |   |
| AB1             | A22    | STB#/WRITE#          |  | TFTD17                 |  | F_FRAME#               |   |
| <b>Ball No.</b> |        | <b>GPIO</b>          |  | <b>Sub-ISA</b>         |  | <b>TFT<sup>3</sup></b> |   |
| J4              | A10    | GPIO17               | PMR[23] = 0 and<br>PMR[5] = 0                        | IOCS0#                 | PMR[23] = 0 and<br>PMR[5] = 1                        | TFTDCK                 | PMR[23] = 1   |
| H3              | A9     | GPIO20               | PMR[23] = 0 and<br>PMR[7] = 0                        | DOCCS#                 | PMR[23] = 0 and<br>PMR[7] = 1                        | TFTD0                  | PMR[23] = 1   |
| H2              | D10    | GPIO1                | PMR[23] = 0 and<br>PMR[13] = 0                       | IOCS1#                 | PMR[23] = 0 and<br>PMR[13] = 1                       | TFTD12                 | PMR[23] = 1   |
| <b>Ball No.</b> |        | <b>AB1</b>           |  | <b>GPIO</b>            |  | <b>Sub-ISA</b>         |   |
| AJ13            | N31    | AB1C                 | PMR[23] = 0  | GPIO20                 | PMR[23] = 1 and<br>PMR[7] = 0                        | DOCCS#                 | PMR[23] = 1 and<br>PMR[7] = 1                       |
| AL12            | N30    | AB1D                 | PMR[23] = 0  | GPIO1                  | PMR[23] = 1 and<br>PMR[13] = 0                       | IOCS1#                 | PMR[23] = 1 and<br>PMR[13] = 1                      |
| <b>Ball No.</b> |        | <b>GPIO</b>          |  | <b>UART2</b>           |  | <b>IDE2</b>            |   |
| H30             | AJ8    | GPIO11               | PMR[18] = 0 and<br>PMR[8] = 0                        | RI2#                   | PMR[18] = 1 and<br>PMR[8] = 0                        | IRQ15                  | PMR[18] = 0 and<br>PMR[8] = 1                       |
| <b>Ball No.</b> |        | <b>Internal Test</b> |  | <b>Internal Test</b>   |  | <b>TFT</b>             |   |
| AL16            | V30    | GXCLK                | PMR[23] = 0 and<br>PMR[29] = 0                       | TEST3                  | PMR[23] = 0 and<br>PMR[29] = 1                       | FP_VDD_ON              | PMR[23] = 1   |

1. The combination of PMR[21] = 1 and PMR[2] = 0 is undefined and should not be used.
2. The combination of PMR[9] = 1 and PMR[4] = 0 is undefined and should not be used.
3. These TFT outputs are reset to 0 by POR# if the TFT\_PRSN strap is pulled high or PMR[10] = 0. This relates to signals TFTD[17:0], TFTDE, TFTDCK.

**Table 3-9. Four-Signal/Group Multiplexing**

| EBGA     | TEPBGA | Default |                                  | Alternate1  |                                  | Alternate2 |                                  | Alternate3    |                                  |
|----------|--------|---------|----------------------------------|-------------|----------------------------------|------------|----------------------------------|---------------|----------------------------------|
|          |        | Signal  | Configuration                    | Signal      | Configuration                    | Signal     | Configuration                    | Signal        | Configuration                    |
| Ball No. |        | GPIO    |                                  | UART2       |                                  | IDE2       |                                  | Internal Test |                                  |
| AH4      | C30    | GPIO7   | PMR[17] = 0<br>and<br>PMR[8] = 0 | RTS2#       | PMR[17] = 1<br>and<br>PMR[8] = 0 | IDE_DACK1# | PMR[17] = 0<br>and<br>PMR[8] = 1 | SDTEST0       | PMR[17] = 1<br>and<br>PMR[8] = 1 |
| AJ2      | C31    | GPIO8   |                                  | CTS2#       |                                  | IDE_DREQ1  |                                  | SDTEST4       |                                  |
| AH3      | D28    | GPIO6   | PMR[18] = 0<br>and<br>PMR[8] = 0 | DTR2#/BOUT2 | PMR[18] = 1<br>and<br>PMR[8] = 0 | IDE_IOR1#  | PMR[18] = 0<br>and<br>PMR[8] = 1 | SDTEST5       | PMR[18] = 1<br>and<br>PMR[8] = 1 |
| AG4      | C28    | GPIO9   |                                  | DCD2#       |                                  | IDE_IOW1#  |                                  | SDTEST2       |                                  |
| AJ1      | B29    | GPIO10  |                                  | DSR2#       |                                  | IDE_IORDY1 |                                  | SDTEST1       |                                  |

### 3.4 Signal Descriptions

Information in the tables that follow may have duplicate information in multiple tables. Multiple references all contain identical information.

#### 3.4.1 System Interface

| Signal Name | Ball No. |        | Type | Description   | Mux       |
|-------------|----------|--------|------|---|-----------|
|             | EBGA     | TEPBGA |      |   |           |
| CLKSEL1     | B27      | AF3    | I    | <b>Fast-PCI Clock Selects.</b> These strap signals are used to set the internal Fast-PCI clock.<br>00 = 33.3 MHz<br>01 = 48 MHz<br>10 = 66.7 MHz<br>11 = 33.3 MHz<br><br>During system reset, an internal pull-down resistor of 100 K $\Omega$ exists on these balls. An external pull-up or pull-down resistor of 1.5 K $\Omega$ must be used.                                       | SOUT1     |
| CLKSEL0     | F3       | B8     |      |   | RD#       |
| CLKSEL3     | AL13     | P30    | I    | <b>Maximum Core Clock Multiplier.</b> These strap signals are used to set the maximum allowed multiplier value for the core clock.<br><br>During system reset, an internal pull-down resistor of 100 K $\Omega$ exists on these balls. An external pull-up or pull-down resistor of 1.5 K $\Omega$ must be used.  | SYNC      |
| CLKSEL2     | AK3      | D29    |      |   | SOUT2     |
| BOOT16      | G4       | C8     | I    | <b>Boot ROM is 16 Bits Wide.</b> This strap signal enables the optional 16-bit wide Sub-ISA bus.<br><br>During system reset, an internal pull-down resistor of 100 K $\Omega$ exists on these balls. An external pull-up or pull-down resistor of 1.5 K $\Omega$ must be used.  | ROMCS#    |
| LPC_ROM     | E4       | D6     | I    | <b>LPC_ROM.</b> This strap signal forces selecting of the LPC bus and sets bit F0BAR1+I/O Offset 10h[15], LPC ROM Addressing Enable. It enables the SC3200 to boot from a ROM connected to the LPC bus.<br><br>During system reset, an internal pull-down resistor of 100 K $\Omega$ exists on these balls. An external pull-up or pull-down resistor of 1.5 K $\Omega$ must be used. | PCICLK1   |
| TFT_PRSNT   | AK13     | P29    | I    | <b>TFT Present.</b> A strap used to select multiplexing of TFT signals at power-up. Enables using TFT instead of Parallel Port, ACB1, and GPIO17.<br><br>During system reset, an internal pull-down resistor of 100 K $\Omega$ exists on these balls. An external pull-up or pull-down resistor of 1.5 K $\Omega$ must be used.   | SDATA_OUT |

## 3.4.1 System Interface (Continued)

| Signal Name | Ball No. |        | Type | Description   | Mux       |
|-------------|----------|--------|------|---|-----------|
|             | EBGA     | TEPBGA |      |   |           |
| FPCI_MON    | D3       | A4     | I    | <b>Fast-PCI Monitoring.</b> The strap on this ball forces selection of Fast-PCI monitoring signals. For normal operation, strap this signal low using a 1.5 K $\Omega$ resistor. The value of this strap can be read on the MCR[30].  | PCICLK0   |
| DID1        | D2       | C6     | I    | <b>Device ID.</b> Together, the straps on these signals define the system-level chip ID. The value of DID1 can be read in the MCR[29]. The value of DID0 can be read in the MCR[31]. DID0 and DID1 must have a pull-up resistor of 1.5 K $\Omega$ .   | GNT1#     |
| DID0        | D4       | C5     | I    |   | GNT0#     |
| POR#        | J29      | AH9    | I    | <b>Power On Reset.</b> POR# is the system reset signal generated from the power supply to indicate that the system should be reset.   | ---       |
| X32I        | C30      | AJ2    | I/O  | <b>Crystal Connections.</b> Connected directly to a 32.768 KHz crystal. This clock input is required even if the internal RTC is not being used. Some of the internal clocks are derived from this clock. If an external clock is used, it should be connected to X32I, using a voltage level of 0 volts to V <sub>CORE</sub> +10% maximum. X32O should remain unconnected. | ---       |
| X32O        | D29      | AJ3    |      |   | ---       |
| X27I        | A29      | AG3    | I/O  | <b>Crystal Connections.</b> Connected directly to a 27.000 MHz crystal. Some of the internal clocks are derived from this clock. If an external clock is used, it should be connected to X27I, using a voltage level of 0 volts to V <sub>IO</sub> and X27O should be remain unconnected.   | ---       |
| X27O        | D27      | AH2    |      |   | ---       |
| CLK27M      | A23      | AA4    | O    | <b>27 MHz Output Clock.</b> Output of crystal oscillator.   | IDE_DATA5 |
| PCIRST#     | D1       | A6     | O    | <b>PCI and System Reset.</b> PCIRST# is the reset signal for the PCI bus and system. It is asserted for approximately 100 $\mu$ s after POR# is negated.  | ---       |



### 3.4.2 Memory Interface Signals

| Signal Name | Ball No.                  |                           | Type | Description   | Mux |
|-------------|---------------------------|---------------------------|------|---|-----|
|             | EBGA                      | TEPBGA                    |      |   |     |
| MD[63:0]    | See Table 3-3 on page 38. | See Table 3-5 on page 54. | I/O  | <b>Memory Data Bus.</b> The data bus lines driven to/from system memory.  | --- |
| MA[12:0]    | See Table 3-3 on page 38. | See Table 3-5 on page 54. | O    | <b>Memory Address Bus.</b> The multiplexed row/column address lines driven to the system memory. Supports 256-Mbit SDRAM.   | --- |
| BA1         | P31                       | AK14                      | O    | <b>Bank Address Bits.</b> These bits are used to select the component bank within the SDRAM.  | --- |
| BA0         | P30                       | AJ13                      |      |   | --- |
| CS1#        | AK29                      | AH27                      | O    | <b>Chip Selects.</b> These bits are used to select the module bank within system memory. Each chip select corresponds to a specific module bank. If CS# is high, the bank(s) do not respond to RAS#, CAS#, and WE# until the bank is selected again.  | --- |
| CS0#        | P29                       | AL12                      |      |   | --- |
| RASA#       | N31                       | AK12                      | O    | <b>Row Address Strobe.</b> RAS#, CAS#, WE# and CKE are encoded to support the different SDRAM commands. RASA# is used with CS[1:0]#.  | --- |
| CASA#       | N30                       | AJ12                      | O    | <b>Column Address Strobe.</b> RAS#, CAS#, WE# and CKE are encoded to support the different SDRAM commands. CASA# is used with CS[1:0]#.   | --- |
| WEA#        | N29                       | AH12                      | O    | <b>Write Enable.</b> RAS#, CAS#, WE# and CKE are encoded to support the different SDRAM commands. WEA# is used with CS[1:0]#.   | --- |
| DQM7        | AJ20                      | AB31                      | O    | <b>Data Mask Control Bits.</b> During memory read cycles, these outputs control whether SDRAM output buffers are driven on the MD bus or not. All DQM signals are asserted during read cycles.<br><br>During memory write cycles, these outputs control whether or not MD data is written into SDRAM.<br><br>DQM[7:0] connect directly to the [DQM7:0] pins of each DIMM connector.   | --- |
| DQM6        | AJ26                      | AG29                      |      |   | --- |
| DQM5        | AC30                      | AK21                      |      |   | --- |
| DQM4        | T28                       | AL15                      |      |   | --- |
| DQM3        | AJ21                      | AC31                      |      |   | --- |
| DQM2        | AL26                      | AG30                      |      |   | --- |
| DQM1        | AF31                      | AH23                      |      |   | --- |
| DQM0        | M31                       | AL11                      |      |   | --- |
| CKEA        | AC28                      | AL22                      | O    | <b>Clock Enable.</b> These signals are used to enter Suspend/power-down mode. CKEA is used with CS[1:0]#.<br><br>If CKE goes low when no read or write cycle is in progress, the SDRAM enters power-down mode. To ensure that SDRAM data remains valid, the self-refresh command is executed. To exit this mode, and return to normal operation, drive CKE high.<br><br>These signals should have an external pull-down resistor of 33 K $\Omega$ . | --- |

### 3.4.2 Memory Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| SDCLK3      | AJ16     | V29    | O    | <b>SDRAM Clocks.</b> SDRAM uses these clocks to sample all control, address, and data lines. To ensure that the Suspend mode functions correctly, SDCLK3 and SDCLK1 should be used with CS1#. SDCLK2 and SDCLK0 should be used together with CS0#. | --- |
| SDCLK2      | AL20     | AA28   |      |  | --- |
| SDCLK1      | AH16     | W29    |      |  | --- |
| SDCLK0      | AC29     | AJ21   |      |  | --- |
| SDCLK_IN    | AJ30     | AJ27   | I    | <b>SDRAM Clock Input.</b> The SC3200 samples the memory read data on this clock. Works in conjunction with the SDCLK_OUT signal.   | --- |
| SDCLK_OUT   | AH28     | AK28   | O    | <b>SDRAM Clock Output.</b> This output is routed back to SDCLK_IN. The board designer should vary the length of the board trace to control skew between SDCLK_IN and SDCLK.  | --- |

### 3.4.3 Video Port Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| VPD7        | AJ6      | G31    | I    | <b>Video Port Data.</b> The data is input from the CCIR-656 video decoder. | --- |
| VPD6        | AJ7      | H28    |      |  | --- |
| VPD5        | AL6      | H29    |      |  | --- |
| VPD4        | AH8      | H30    |      |  | --- |
| VPD3        | AL7      | H31    |      |  | --- |
| VPD2        | AJ8      | J28    |      |  | --- |
| VPD1        | AK8      | J29    |      |  | --- |
| VPD0        | AH9      | J30    |      |  | --- |
| VPCKIN      | AH7      | F31    | I    | <b>Video Port Clock Input.</b> The clock input from the video decoder.     | --- |

### 3.4.4 TFT Interface Signals

| Signal Name | Ball No.                  |                           | Type | Description   | Mux  |
|-------------|---------------------------|---------------------------|------|---|--|
|             | EBGA                      | TEPBGA                    |      |   |  |
| HSYNC       | J1                        | A11                       | O    | <b>Horizontal Sync</b>  | ---  |
| VSYNC       | J2                        | B11                       | O    | <b>Vertical Sync</b>  | ---  |
| TFTDCK      | A22                       | AA1                       | O    | <b>TFT Clock.</b>   | IDE_RST#   |
|             | J4                        | A10                       |      |   | GPIO17+ IOCS0#   |
| TFTDE       | C16                       | P2                        | O    | <b>TFT Data Enable.</b>   | IDE_CS1#   |
|             | U3                        | B18                       |      |   | ACK#+FPCICLK   |
| FP_VDD_ON   | B23                       | AB1                       | O    | <b>TFT Power Control.</b> Used to enable power to the flat panel display, with power sequence timing.   | IDE_DATA4  |
|             | AL16                      | V30                       |      |   | GXCLK+TEST3  |
| TFTD[17:0]  | See Table 3-3 on page 38. | See Table 3-5 on page 54. | O    | <b>Digital RGB Data to TFT.</b><br>TFTD[5:0] - Connect to the BLUE TFT inputs.<br>TFTD[11:6] - Connect to GREEN TFT inputs.<br>TFTD[17:12] - Connect to RED TFT inputs. | The TFT interface is muxed with the IDE interface or the Parallel Port. See Table 3-7 on page 59 and Table 3-8 on page 60 for details. |

### 3.4.5 ACCESS.bus Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux           |
|-------------|----------|--------|------|--|---------------|
|             | EBGA     | TEPBGA |      |  |               |
| AB1C        | AJ13     | N31    | I/O  | <b>ACCESS.bus 1 Serial Clock.</b> This is the serial clock for the interface.<br><b>Note:</b> If selected as AB1C function but not used, tie AB1C high.                    | GPIO20+DOCCS# |
| AB1D        | AL12     | N30    | I/O  | <b>ACCESS.bus 1 Serial Data.</b> This is the bidirectional serial data signal for the interface.<br><b>Note:</b> If AB1D function is selected but not used, tie AB1D high. | GPIO1+IOCS1#  |
| AB2C        | AJ12     | N29    | I/O  | <b>ACCESS.bus 2 Serial Clock.</b> This is the serial clock for the interface.<br><b>Note:</b> If AB2C function is selected but not used, tie AB2C high.                    | GPIO12        |
| AB2D        | AL11     | M29    | I/O  | <b>ACCESS.bus 2 Serial Data.</b> This is the bidirectional serial data signal for the interface.<br><b>Note:</b> If AB2D function is selected but not used, tie AB2D high. | GPIO13        |

## 3.4.6 PCI Bus Interface Signals

| Signal Name | Ball No.                  |                           | Type | Description   | Mux              |
|-------------|---------------------------|---------------------------|------|---|------------------|
|             | EBGA                      | TEPBGA                    |      |   |                  |
| PCICLK      | E2                        | A7                        | I    | <b>PCI Clock.</b> PCICLK provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.  | ---              |
| PCICLK0     | D3                        | A4                        | O    | <b>PCI Clock Outputs.</b> PCICLK0 and PCICLK1 provide clock drives for the system at 33 MHz. These clocks are asynchronous to PCI signals. There is low skew between all outputs. One of these clock signals should be connected to the PCICLK input. All PCI clock users in the system (including PCICLK) should receive the clock with as low a skew as possible.   | FPCI_MON (Strap) |
| PCICLK1     | E4                        | D6                        | O    |   | LPC_ROM (Strap)  |
| AD[31:24]   | See Table 3-3 on page 38. | See Table 3-5 on page 54. | I/O  | <b>Multiplexed Address and Data.</b> A bus transaction consists of an address phase in the cycle in which FRAME# is asserted followed by one or more data phases. During the address phase, AD[31:0] contain a physical 32-bit address. For I/O, this is a byte address. For configuration and memory, it is a DWORD address. During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB). | D[7:0]           |
| AD[23:0]    |                           |                           |      |   | A[23:0]          |
| C/BE3#      | A8                        | H4                        | I/O  | <b>Multiplexed Command and Byte Enables.</b> During the address phase of a transaction when FRAME# is active, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte 0 (LSB) and C/BE3# applies to byte 3 (MSB).  | D11              |
| C/BE2#      | D8                        | F3                        |      |   | D10              |
| C/BE1#      | A10                       | J2                        |      |   | D9               |
| C/BE0#      | A13                       | L1                        |      |   | D8               |
| INTA#       | AE3                       | D26                       | I    | <b>PCI Interrupts.</b> The SC3200 provides inputs for the optional "level-sensitive" PCI interrupts (also known in industry terms as PIRQ#). These interrupts can be mapped to IRQs of the internal 8259A interrupt controllers using PCI Interrupt Steering Registers 1 and 2 (F0 Index 5Ch and 5Dh).<br><br><b>Note:</b> If selected as INTC# or INTD# function(s) but not used, tie INTC# and INTD# high.  | ---              |
| INTB#       | AF1                       | C26                       |      |   | ---              |
| INTC#       | H4                        | C9                        |      |   | GPIO19+IOCHRDY   |
| INTD#       | B22                       | AA2                       |      |   | IDE_DATA7        |

### 3.4.6 PCI Bus Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| PAR         | C10      | J4     | I/O  | <p><b>Parity.</b> Parity generation is required by all PCI agents. The master drives PAR for address- and write-data phases. The target drives PAR for read-data phases. Parity is even across AD[31:0] and C/BE[3:0]#.</p> <p>For address phases, PAR is stable and valid one PCI clock after the address phase. It has the same timing as AD[31:0] but is delayed by one PCI clock.</p> <p>For data phases, PAR is stable and valid one PCI clock after either IRDY# is asserted on a write transaction or after TRDY# is asserted on a read transaction.</p> <p>Once PAR is valid, it remains valid until one PCI clock after the completion of the data phase. (Also see PERR#.)</p> | D12 |
| FRAME#      | E1       | D8     | I/O  | <p><b>Frame Cycle.</b> Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. FRAME# is de-asserted when the transaction is in the final data phase.</p> <p>This signal is internally connected to a pull-up resistor.</p>   | --- |
| IRDY#       | C8       | F2     | I/O  | <p><b>Initiator Ready.</b> IRDY# is asserted to indicate that the bus master is able to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any PCI clock in which both IRDY# and TRDY# are sampled as asserted. During a write, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.</p> <p>This signal is internally connected to a pull-up resistor.</p>  | D14 |

## 3.4.6 PCI Bus Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description   | Mux |
|-------------|----------|--------|------|---|-----|
|             | EBGA     | TEPBGA |      |   |     |
| TRDY#       | B8       | F1     | I/O  | <p><b>Target Ready.</b> TRDY# is asserted to indicate that the target agent is able to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is complete on any PCI clock in which both TRDY# and IRDY# are sampled as asserted. During a read, TRDY# indicates that valid data is present on AD[31:0]. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.</p> <p>This signal is internally connected to a pull-up resistor.</p>   | D13 |
| STOP#       | D9       | G1     | I/O  | <p><b>Target Stop.</b> STOP# is asserted to indicate that the current target is requesting that the master stop the current transaction. This signal is used with DEVSEL# to indicate retry, disconnect, or target abort. If STOP# is sampled active by the master, FRAME# is deasserted and the cycle is stopped within three PCI clock cycles. As an input, STOP# can be asserted in the following cases:</p> <ol style="list-style-type: none"> <li>1) If a PCI master tries to access memory that has been locked by another master. This condition is detected if FRAME# and LOCK# are asserted during an address phase.</li> <li>2) If the PCI write buffers are full or if a previously buffered cycle has not completed.</li> <li>3) On read cycles that cross cache line boundaries. This is conditional based upon the programming of GX1 module's PCI Configuration Register, Index 41h[1].</li> </ol> <p>This signal is internally connected to a pull-up resistor.</p> | D15 |

## 3.4.6 PCI Bus Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux  |
|-------------|----------|--------|------|--|------|
|             | EBGA     | TEPBGA |      |  |      |
| LOCK#       | C9       | H3     | I/O  | <p><b>Lock Operation.</b> LOCK# indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked (at least 16 bytes must be locked). A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#.</p> <p>It is possible for different agents to use PCI while a single master retains ownership of LOCK#. The arbiter can implement a complete system lock. In this mode, if LOCK# is active, no other master can gain access to the system until the LOCK# is de-asserted.</p> <p>This signal is internally connected to a pull-up resistor.</p> | ---  |
| DEVSEL#     | B5       | E4     | I/O  | <p><b>Device Select.</b> DEVSEL# indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected. DEVSEL# is also driven by any agent that has the ability to accept cycles on a subtractive decode basis. As a master, if no DEVSEL# is detected within and up to the subtractive decode clock, a master abort cycle is initiated (except for special cycles which do not expect a DEVSEL# returned).</p> <p>This signal is internally connected to a pull-up resistor.</p>   | BHE# |
| PERR#       | B9       | H2     | I/O  | <p><b>Parity Error.</b> PERR# is used for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR# line is driven two PCI clocks after the data in which the error was detected. This is one PCI clock after the PAR that is attached to the data. The minimum duration of PERR# is one PCI clock for each data phase in which a data parity error is detected. PERR# must be driven high for one PCI clock before being placed in TRI-STATE. A target asserts PERR# on write cycles if it has claimed the cycle with DEVSEL#. The master asserts PERR# on read cycles.</p> <p>This signal is internally connected to a pull-up resistor.</p>  | ---  |

## 3.4.6 PCI Bus Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux          |
|-------------|----------|--------|------|--|--------------|
|             | EBGA     | TEPBGA |      |  |              |
| SERR#       | A9       | H1     | I/O  | <p><b>System Error.</b> SERR# can be asserted by any agent for reporting errors other than PCI parity. When the PFS bit is enabled in the GX1 module's PCI Control Function 2 register (Index 41h[5]), SERR# is asserted upon assertion of PERR#.</p> <p>This signal is internally connected to a pull-up resistor.</p>  | ---          |
| REQ1#       | E3       | A5     | I    | <p><b>Request Lines.</b> REQ[1:0]# indicate to the arbiter that an agent requires the bus. Each master has its own REQ# line. REQ# priorities (in order) are:</p> <ol style="list-style-type: none"> <li>1) VIP</li> <li>2) IDE Channel 0</li> <li>3) IDE Channel 1</li> <li>4) Audio</li> <li>5) USB</li> <li>6) External REQ0#</li> <li>7) External REQ1#.</li> </ol> <p>Each REQ# is internally connected to a pull-up resistor.</p>  | ---          |
| REQ0#       | C1       | B5     |      |  | ---          |
| GNT1#       | D2       | C6     | O    | <p><b>Grant Lines.</b> GNT[1:0]# indicate to the requesting master that it has been granted access to the bus. Each master has its own GNT# line. GNT# can be retracted at any time a higher REQ# is received or if the master does not begin a cycle within a minimum period of time (16 PCI clocks).</p> <p>Each of these signals is internally connected to a pull-up resistor.</p> <p>GNT0# must have a pull-up resistor of 1.5 K<math>\Omega</math> and GNT1# must have a pull-up resistor of 1.5 K<math>\Omega</math>.</p> | DID1 (Strap) |
| GNT0#       | D4       | C5     |      |  | DID0 (Strap) |



### 3.4.7 Sub-ISA Interface Signals

| Signal Name | Ball No.                  |                           | Type | Description   | Mux             |
|-------------|---------------------------|---------------------------|------|---|-----------------|
|             | EBGA                      | TEPBGA                    |      |   |                 |
| A[23:0]     | See Table 3-3 on page 38. | See Table 3-5 on page 54. | O    | <b>Address Lines</b>  | AD[23:0]        |
| D15         | See Table 3-3 on page 38. | See Table 3-5 on page 54. | I/O  | <b>Data Bus</b>   | STOP#           |
| D14         |                           |                           |      |   | IRDY#           |
| D13         |                           |                           |      |   | TRDY#           |
| D12         |                           |                           |      |   | PAR             |
| D11         |                           |                           |      |   | C/BE3#          |
| D10         |                           |                           |      |   | C/BE2#          |
| D9          |                           |                           |      |   | C/BE1#          |
| D8          |                           |                           |      |   | C/BE0#          |
| D[7:0]      |                           |                           |      |   | AD[31:24]       |
| BHE#        | B5                        | E4                        | O    | <b>Byte High Enable.</b> With A0, defines byte accessed for 16 bit wide bus cycles.   | DEVSEL#         |
| IOCS1#      | H2                        | D10                       | O    | <b>I/O Chip Selects</b>   | GPIO1+TFTD12    |
|             | AL12                      | N30                       |      |   | AB1D+GPIO1      |
| IOCS0#      | J4                        | A10                       |      |   | GPIO17+TFTDCK   |
| ROMCS#      | G4                        | C30                       | O    | <b>ROM or Flash ROM Chip Select</b>   | BOOT16 (Strap)  |
| DOCCS#      | H3                        | A9                        | O    | <b>DiskOnChip or NAND Flash Chip Select</b>   | GPIO20+TFTD0    |
|             | AJ13                      | N31                       |      |   | AB1C+GPIO20     |
| TRDE#       | H1                        | D11                       | O    | <p><b>Transceiver Data Enable Control.</b> Active low for Sub-ISA data transfers. The signal timing is as follows:</p> <ul style="list-style-type: none"> <li>In a read cycle, TRDE# has the same timing as RD#.</li> <li>In a write cycle, TRDE# is asserted (to active low) at the time WR# is asserted. It continues being asserted for one PCI clock cycle after WR# has been negated, then it is negated.</li> </ul> | GPIO0           |
| RD#         | F3                        | B8                        | O    | <b>Memory or I/O Read.</b> Active on any read cycle.  | CLKSEL0 (Strap) |
| WR#         | G1                        | B9                        | O    | <b>Memory or I/O Write.</b> Active on any write cycle.  | ---             |
| IOR#        | F1                        | D9                        | O    | <b>I/O Read.</b> Active on any I/O read cycle.  | DOCR#+GPIO14    |
| IOW#        | G3                        | A8                        | O    | <b>I/O Write.</b> Active on any I/O write cycle.  | DOCW#+GPIO15    |
| DOCR#       | F1                        | D9                        | O    | <b>DiskOnChip or NAND Flash Read.</b> Active on any memory read cycle to DiskOnChip.  | IOR#+GPIO14     |
| DOCW#       | G3                        | A8                        | O    | <b>DiskOnChip or NAND Flash Write.</b> Active on any memory write cycle to DiskOnChip.  | IOW#+GPIO15     |

## 3.4.7 Sub-ISA Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description   | Mux          |
|-------------|----------|--------|------|---|--------------|
|             | EBGA     | TEPBGA |      |   |              |
| IRQ9        | C22      | AA3    | I    | <b>Interrupt 9 Request Input.</b> Active high.<br><b>Note:</b> If IRQ9 function is selected but not used, tie IRQ9 low. | IDE_DATA6    |
| IOCHRDY     | H4       | C9     | I    | <b>I/O Channel Ready</b><br><b>Note:</b> If IOCHRDY function is selected but not used, tie IOCHRDY high.                | GPIO19+INTC# |

## 3.4.8 Low Pin Count (LPC) Bus Interface Signals

| Signal Name | Ball No. |        | Type | Description   | Mux         |
|-------------|----------|--------|------|---|-------------|
|             | EBGA     | TEPBGA |      |   |             |
| LAD3        | AJ10     | L29    | I/O  | <b>LPC Address-Data.</b> Multiplexed command, address, bidirectional data, and cycle status.  | GPIO35      |
| LAD2        | AK10     | L30    |      |   | GPIO34      |
| LAD1        | AL10     | L31    |      |   | GPIO33      |
| LAD0        | AJ11     | M28    |      |   | GPIO32      |
| LDRQ#       | AL9      | L28    | I    | <b>LPC DMA Request.</b> Encoded DMA request for LPC interface.<br><b>Note:</b> If LDRQ# function is selected but not used, tie LDRQ# high.  | GPIO36      |
| LFRAME#     | AK9      | K31    | O    | <b>LPC Frame.</b> A low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.  | GPIO37      |
| LPCPD#      | AJ9      | K28    | O    | <b>LPC Power-Down.</b> Signals the LPC device to prepare for power shut-down on the LPC interface.  | GPIO38/IRR2 |
| SERIRQ      | AL8      | J31    | I/O  | <b>Serial IRQ.</b> The interrupt requests are serialized over a single signal, where each IRQ level is delivered during a designated time slot.<br><b>Note:</b> If SERIRQ function is selected but not used, tie SERIRQ high. | GPIO39      |

## 3.4.9 IDE Interface Signals

| Signal Name    | Ball No.                  |                           | Type | Description   | Mux  |
|----------------|---------------------------|---------------------------|------|---|--|
|                | EBGA                      | TEPBGA                    |      |   |  |
| IDE_RST#       | A22                       | AA1                       | O    | <b>IDE Reset.</b> This signal resets all the devices that are attached to the IDE interface.  | TFTDCK   |
| IDE_ADDR2      | C17                       | U2                        | O    | <b>IDE Address Bits.</b> These address bits are used to access a register or data port in a device on the IDE bus.  | TFTD4  |
| IDE_ADDR1      | C26                       | AE1                       |      |   | TFTD2  |
| IDE_ADDR0      | A26                       | AD3                       |      |   | TFTD3  |
| IDE_DATA[15:0] | See Table 3-3 on page 38. | See Table 3-5 on page 54. | I/O  | <b>IDE Data Lines.</b> IDE_DATA[15:0] transfers data to/from the IDE devices.   | The IDE interface is muxed with the TFT interface. See Table 3-7 on page 59 for details. |
| IDE_IOR0#      | C21                       | Y4                        | O    | <b>IDE I/O Read Channels 0 and 1.</b> IDE_IOR0# is the read signal for Channel 0 and IDE_IOR1# is the read signal for Channel 1. Each signal is asserted at read accesses to the corresponding IDE port addresses.  | TFTD10   |
| IDE_IOR1#      | AH3                       | D28                       | O    |   | GPIO6+DTR2#/<br>BOUT2+SDTEST5#   |
| IDE_IOW0#      | D24                       | AD2                       | O    | <b>IDE I/O Write Channels 0 and 1.</b> IDE_IOW0# is the write signal for Channel 0. IDE_IOW1# is the write signal for Channel 1. Each signal is asserted at write accesses to corresponding IDE port addresses.   | TFTD9  |
| IDE_IOW1#      | AG4                       | C28                       | O    |   | GPIO9+DCD2#+<br>SDTEST2  |
| IDE_CS0#       | A27                       | AF2                       | O    | <b>IDE Chip Selects 0 and 1.</b> These signals are used to select the command block registers in an IDE device.   | TFTD5  |
| IDE_CS1#       | C16                       | P2                        | O    |   | TFTDE  |
| IDE_IORDY0     | A25                       | AD1                       | I    | <b>I/O Ready Channels 0 and 1.</b> When de-asserted, these signals extend the transfer cycle of any host register access if the required device is not ready to respond to the data transfer request.<br><b>Note:</b> If selected as IDE_IORDY0 or IDE_IORDY1 function(s) but not used, then signal(s) should be tied high. | TFTD11   |
| IDE_IORDY1     | AJ1                       | B29                       | I    |   | GPIO10+DSR2#+<br>SDTEST1   |
| IDE_DREQ0      | C24                       | AC4                       | I    | <b>DMA Request Channels 0 and 1.</b> The IDE_DREQ signals are used to request a DMA transfer from the SC3200. The direction of transfer is determined by the IDE_IOR/IOW signals.<br><b>Note:</b> If selected as IDE_DREQ0/IDE_DREQ1 function but not used, tie IDE_DREQ0/IDE_DREQ1 low.                                    | TFTD8  |
| IDE_DREQ1      | AJ2                       | C31                       | I    |   | GPIO8+CTS2#+<br>+SDTEST5   |
| IDE_DACK0#     | C25                       | AD4                       | O    | <b>DMA Acknowledge Channels 0 and 1.</b> The IDE_DACK# signals acknowledge the DREQ request to initiate DMA transfers.  | TFTD0  |
| IDE_DACK1#     | AH4                       | C30                       | O    |   | GPIO7+RTS2#+<br>+SDTEST0   |

### 3.4.9 IDE Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description   | Mux         |
|-------------|----------|--------|------|---|-------------|
|             | EBGA     | TEPBGA |      |   |             |
| IRQ14       | D25      | AF1    | I    | <b>Interrupt Request Channels 0 and 1.</b><br>These input signals are edge-sensitive interrupts that indicate when the IDE device is requesting a CPU interrupt service.<br><br><b>Note:</b> If selected as IRQ14/IRQ15 function but not used, tie IRQ14/IRQ15 low. | TFTD1       |
| IRQ15       | H30      | AJ8    | I    |   | GPIO11+RI2# |

### 3.4.10 Universal Serial Bus (USB) Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| POWER_EN    | B28      | AH1    | O    | <b>Power Enable.</b> This signal enables the power to a self-powered USB hub.                      | --- |
| OVER_CUR#   | C27      | AF4    | I    | <b>Overcurrent.</b> This signal indicates that the USB hub has detected an overcurrent on the USB. | --- |
| DPOS_PORT1  | AH2      | A28    | I/O  | <b>USB Port 1 Data Positive for Port 1.</b> <sup>1</sup>   | --- |
| DNEG_PORT1  | AG3      | A29    | I/O  | <b>USB Port 1 Data Negative for port 1.</b> <sup>1</sup>   | --- |
| DPOS_PORT2  | AH1      | B27    | I/O  | <b>USB Port 2 Data Positive for Port 2.</b> <sup>1</sup>   | --- |
| DNEG_PORT2  | AG2      | B28    | I/O  | <b>USB Port 2 Data Negative for Port 2.</b> <sup>1</sup>   | --- |
| DPOS_PORT3  | AE4      | A26    | I/O  | <b>USB Port 3 Data Positive for Port 3.</b> <sup>1</sup>   | --- |
| DNEG_PORT3  | AF3      | A27    | I/O  | <b>USB Port 3 Data Negative for Port 3.</b> <sup>1</sup>   | --- |

1. A 15K ohm pull-down resistor is required on all ports (even if unused).

### 3.4.11 Serial Ports (UARTs) Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux             |
|-------------|----------|--------|------|--|-----------------|
|             | EBGA     | TEPBGA |      |  |                 |
| SIN1        | D26      | AG2    | I    | <b>Serial Inputs.</b> Receive composite serial data from the communications link (peripheral device, modem or other data transfer device).<br><br><b>Note:</b> If selected as SIN2 or SIN3 function(s) but not used, then signal(s) should be tied high. | ---             |
| SIN2        | AJ4      | E28    |      |  | SDTEST3         |
| SIN3        | J28      | AK8    |      |  | IRRX1           |
| SOUT1       | B27      | AF3    | O    | <b>Serial Outputs.</b> Send composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.   | CLKSEL1 (Strap) |
| SOUT2       | AK3      | D29    |      |  | CLKSEL2 (Strap) |
| SOUT3       | J3       | C11    |      |  | IRTX            |

### 3.4.11 Serial Ports (UARTs) Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description   | Mux                         |
|-------------|----------|--------|------|---|-----------------------------|
|             | EBGA     | TEPBGA |      |   |                             |
| RTS2#       | AH4      | C30    | O    | <b>Request to Send.</b> When low, indicates to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.   | GPIO7+<br>IDE_DACK1#        |
| CTS2#       | AJ2      | C31    | I    | <b>Clear to Send.</b> When low, indicates that the modem or other data transfer device is ready to exchange data.<br><br><b>Note:</b> If selected as CTS2# function but not used, tie CTS2# low.  | GPIO8+<br>IDE_DREQ1         |
| DTR1#/BOUT1 | A28      | AG1    | O    | <b>Data Terminal Ready Outputs.</b> When low, indicate to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these balls provide the DTR# function and set these signals to inactive high. Loopback operation drive them inactive.<br><br><b>Baud Outputs.</b> Provide the associated serial channel baud rate generator output signal if test mode is selected (i.e., bit 7 of the EXCR1 Register is set). | GPIO18                      |
| DTR2#/BOUT2 | AH3      | D28    |      |   | GPIO6+IDE_IOR1#             |
| RI2#        | H30      | AJ8    | I    | <b>Ring Indicator.</b> When low, indicates to the modem that a telephone ring signal has been received by the modem. They are monitored during power-off for wakeup event detection.<br><br><b>Note:</b> If selected as RI2# function but not used, tie RI2# high.  | GPIO11+IRQ15                |
| DCD2#       | AG4      | C28    | I    | <b>Data Carrier Detected.</b> When low, indicates that the data transfer device (e.g., modem) is ready to establish a communications link.<br><br><b>Note:</b> If selected as DCD2# function but not used, tie DCD2# high.  | GPIO9+IDE_IOW1#<br>+SDTEST2 |
| DSR2#       | AJ1      | B29    | I    | <b>Data Set Ready.</b> When low, indicates that the data transfer device (e.g., modem) is ready to establish a communications link.<br><br><b>Note:</b> If selected as DSR2# function but not used, tie DSR2# low.  | GPIO10+<br>IDE_IORDY1       |

## 3.4.12 Parallel Port Interface Signals

| Signal Name  | Ball No. |        | Type | Description  | Mux             |
|--------------|----------|--------|------|--|-----------------|
|              | EBGA     | TEPBGA |      |  |                 |
| ACK#         | U3       | B18    | I    | <b>Acknowledge.</b> Pulsed low by the printer to indicate that it has received data from the Parallel Port.  | TFTDE+FPCICLK   |
| AFD#/DSTRB#  | AB2      | D22    | O    | <b>Automatic Feed.</b> When low, instructs the printer to automatically feed a line after printing each line. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 K $\Omega$ pull-up resistor should be attached to this ball.<br><b>Data Strobe (EPP).</b> Active low, used in EPP mode to denote a data cycle. When the cycle is aborted, DSTRB# becomes inactive (high). | TFTD2+INTR_O    |
| BUSY/WAIT#   | T1       | B17    | I    | <b>Busy.</b> Set high by the printer when it cannot accept another character.<br><b>Wait.</b> In EPP mode, the Parallel Port device uses this active low signal to extend its access cycle.  | TFTD3+F_C/BE1#  |
| ERR#         | AA3      | D21    | I    | <b>Error.</b> Set active low by the printer when it detects an error.  | TFTD4+F_C/BE0#  |
| INIT#        | Y3       | B21    | O    | <b>Initialize.</b> When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. Use an external 4.7 K $\Omega$ pull-up resistor.  | TFTD5+SMI_O     |
| PD7          | U1       | A18    | I/O  | <b>Parallel Port Data.</b> Transfer data to and from the peripheral data bus and the appropriate Parallel Port data register. These signals have a high current drive capability.  | TFTD13+F_AD7    |
| PD6          | V3       | A20    |      |  | TFTD1+F_AD6     |
| PD5          | V2       | C19    |      |  | TFTD11+F_AD5    |
| PD4          | V1       | C18    |      |  | TFTD10+F_AD4    |
| PD3          | W2       | C20    |      |  | TFTD9+F_AD3     |
| PD2          | W3       | D20    |      |  | TFTD8+F_AD2     |
| PD1          | Y1       | A21    |      |  | TFTD7+F_AD1     |
| PD0          | AA1      | C21    |      |  | TFTD6+F_AD0     |
| PE           | T3       | D17    | I    | <b>Paper End.</b> Set high by the printer when it is out of paper.<br><br>This ball has an internal weak pull-up or pull-down resistor that is programmed by software.   | TFTD14+F_C/BE2# |
| SLCT         | T4       | C17    | I    | <b>Select.</b> Set active high by the printer when the printer is selected.  | TFTD15+F_C/BE3# |
| SLIN#/ASTRB# | W1       | B20    | O    | <b>Select Input.</b> When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Uses an external 4.7 K $\Omega$ pull-up resistor.<br><b>Address Strobe (EPP).</b> Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, ASTRB# becomes inactive (high).   | TFTD16+F_IRDY#  |

### 3.4.12 Parallel Port Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux                 |
|-------------|----------|--------|------|--|---------------------|
|             | EBGA     | TEPBGA |      |  |                     |
| STB#/WRITE# | AB1      | A22    | O    | <p><b>Data Strobe.</b> When low, indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 K<math>\Omega</math> pull-up resistor should be employed.</p> <p><b>Write Strobe.</b> Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, WRITE# becomes inactive (high).</p> | TFTD17+<br>F_FRAME# |

### 3.4.13 Fast Infrared (IR) Port Interface Signals

| Signal Name  | Ball No. |        | Type | Description   | Mux    |
|--------------|----------|--------|------|---|--------|
|              | EBGA     | TEPBGA |      |   |        |
| IRRX1        | J28      | AK8    | I    | <p><b>IR Receive.</b> Primary input to receive serial data from the IR transceiver. Monitored during power-off for wakeup event detection.</p> <p><b>Note:</b> If selected as IRRX1 function but not used, tie IRRX1 high.</p>                      | SIN3   |
| IRRX2/GPIO38 | AJ9      | K28    | I    | <p><b>IR Receive 2.</b> Auxiliary IR receiver input to support a second transceiver. This input signal can be used when GPIO38 is selected using PMR[14], and when AUX_IRRX bit in register IRCR2 of the IR module in internal SuperI/O is set.</p> | LPCPD# |
| IRTX         | J3       | C11    | O    | <b>IR Transmit.</b> IR serial output data.  | SOUT3  |

## 3.4.14 AC97 Audio Interface Signals

| Signal Name | Ball No. |        | Type | Description   | Mux                  |
|-------------|----------|--------|------|---|----------------------|
|             | EBGA     | TEPBGA |      |   |                      |
| BIT_CLK     | AL14     | U30    | I    | <b>Audio Bit Clock.</b> The serial bit clock from the codec.<br><b>Note:</b> If selected as BIT_CLK function but not used, tie BIT_CLK low.   | F_TRDY#              |
| SDATA_OUT   | AK13     | P29    | O    | <b>Serial Data Output.</b> This output transmits audio serial data to the codec.  | TFT_PRSN (Strap)     |
| SDATA_IN    | AK14     | U31    | I    | <b>Serial Data Input.</b> This input receives serial data from the primary codec.<br><b>Note:</b> If selected as SDATA_IN function but not used, tie SDATA_IN low.  | F_GNT0#              |
| SDATA_IN2   | H31      | AL8    | I    | <b>Serial Data Input 2.</b> This input receives serial data from the secondary codec. This signal has wakeup capability.  | ---                  |
| SYNC        | AL13     | P30    | O    | <b>Serial Bus Synchronization.</b> This bit is asserted to synchronize the transfer of data between the SC3200 and the AC97 codec.  | CLKSEL3 (Strap)      |
| AC97_CLK    | AJ14     | P31    | O    | <b>Codec Clock.</b> It is twice the frequency of the Audio Bit Clock.   | ---                  |
| AC97_RST#   | AJ15     | U29    | O    | <b>Codec Reset.</b> S3 to S5 wakeup is not supported because AC97_RST# is powered by V <sub>IO</sub> . If wakeup from states S3 to S5 are needed, a circuit in the system board should be used to reset the AC97 codec. | F_STOP#              |
| PC_BEEP     | AL15     | V31    | O    | <b>PC BEEP.</b> Legacy PC/AT speaker output.  | GPIO16+<br>F_DEVSEL# |

## 3.4.15 Power Management Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| CLK32       | H29      | AH8    | O    | <b>32.768 KHz Output Clock</b>   | --- |
| GPWIO0      | E31      | AH6    | I/O  | <b>General Purpose Wakeup I/Os.</b> These signals each have an internal pull-up of 100 K $\Omega$ .  | --- |
| GPWIO1      | G28      | AK5    |      |  | --- |
| GPWIO2      | G29      | AJ6    |      |  | --- |
| LED#        | D31      | AL4    | O    | <b>LED Control.</b> Drives an externally connected LED (on, off or a 1 Hz blink). Sleeping / Working indicator. This signal is an open-drain output. | --- |
| ONCTL#      | E30      | AJ5    | O    | <b>On / Off Control.</b> This signal indicates to the main power supply that power should be turned on. This signal is an open-drain output.         | --- |



### 3.4.15 Power Management Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux |
|-------------|----------|--------|------|--|-----|
|             | EBGA     | TEPBGA |      |  |     |
| PWRBTN#     | E29      | AH5    | I    | <p><b>Power Button.</b> Input used by the power management logic to monitor external system events, most typically a system on/off button or switch.</p> <p>The signal has an internal pull-up of 100 K<math>\Omega</math>, a Schmitt-trigger input buffer and debounce protection of at least 16 ms.</p> <p>ACPI is non-functional and all ACPI outputs are undefined when the power-up sequence does not include using the power button. SUSP# is an internal signal generated from the ACPI block. Without an ACPI reset, SUSP# can be permanently asserted. If the USE_SUSP bit in CCR2 of GX1 module is enabled (Index C2h[7] = 1), the CPU will stop.</p> <p>If ACPI functionality is desired, or the situation described above avoided, the power button must be toggled. This can be done externally or internally. GPIO63 is internally connected to PWRBTN#. To toggle the power button with software, GPIO63 must be programmed as an output using the normal GPIO programming protocol (see Section 6.4.1.1 "GPIO Support Registers" on page 240). GPIO63 must be pulsed low for at least 16 ms and not more than 4 sec.</p> <p>Asserting POR# has no effect on ACPI. If POR# is asserted and ACPI was active prior to POR#, then ACPI will remain active after POR#. Therefore, BIOS must ensure that ACPI is inactive before GPIO63 is pulsed low.</p> | --- |
| PWRCNT1     | F31      | AK6    | O    | <p><b>Suspend Power Plane Control 1 and 2.</b> Control signal asserted during power management Suspend states. These signals are open-drain outputs.</p>   | --- |
| PWRCNT2     | G31      | AL7    | O    |  | --- |
| THRM#       | F28      | AK4    | I    | <p><b>Thermal Event.</b> Active low signal generated by external hardware indicating that the system temperature is too high.</p>  | --- |

## 3.4.16 GPIO Interface Signals

| Signal Name  | Ball No. |        | Type       | Description  | Mux                                   |
|--------------|----------|--------|------------|--|---------------------------------------|
|              | EBGA     | TEPBGA |            |  |                                       |
| GPIO0        | H1       | D11    | I/O        | <p><b>GPIO Port 0.</b> Each signal is configured independently as an input or I/O, with or without static pull-up, and with either open-drain or totem-pole output type.</p> <p>A debouncer and an interrupt can be enabled or masked for each of signals GPIO[00:01] and [06:15] independently.</p> <p><b>Note:</b> GPIO12, GPIO13, GPIO16 inputs: If GPIOx function is selected but not used, tie GPIOx low.</p> | TRDE#                                 |
| GPIO1        | H2       | D10    |            |  | IOCS1#+TFTD12                         |
|              | AL12     | N30    |            |  | AB1D+IOCS1#                           |
| GPIO6        | AH3      | D28    |            |  | DTR2#/BOUT2+<br>IDE_IOR1#+<br>SDTEST5 |
| GPIO7        | AH4      | C30    |            |  | RTS2#+IDE_DACK1#<br>+SDTEST0          |
| GPIO8        | AJ2      | C31    |            |  | CTS2#+IDE_DREQ1<br>+SDTEST4           |
| GPIO9        | AG4      | C28    |            |  | DCD2#+IDE_IOW1#+<br>SDTEST2           |
| GPIO10       | AJ1      | B29    |            |  | DSR2#+IDE_IORDY1<br>+SDTEST1          |
| GPIO11       | H30      | AJ8    |            |  | RI2#+IRQ15                            |
| GPIO12       | AJ12     | N29    |            |  | AB2C                                  |
| GPIO13       | AL11     | M29    |            |  | AB2D                                  |
| GPIO14       | F1       | D9     |            |  | IOR#+DOCR#                            |
| GPIO15       | G3       | A8     |            |  | IOW#+DOCW#                            |
| GPIO16       | AL15     | V31    |            |  | PC_BEEP+<br>F_DEVSEL#                 |
| GPIO17       | J4       | A10    |            |  | IOCS0#+TFTDCK                         |
| GPIO18       | A28      | AG1    |            |  | DTR1#/BOUT1                           |
| GPIO19       | H4       | C9     |            |  | INTC#+IOCHRDY                         |
| GPIO20       | H3       | A9     |            |  | DOCCS#+TFTD0                          |
|              | AJ13     | N31    |            |  | AB1C+DOCCS#                           |
| GPIO32       | AJ11     | M28    |            |  | I/O                                   |
| GPIO33       | AL10     | L31    | LAD1       |  |                                       |
| GPIO34       | AK10     | L30    | LAD2       |  |                                       |
| GPIO35       | AJ10     | L29    | LAD3       |  |                                       |
| GPIO36       | AL9      | L28    | LDRQ#      |  |                                       |
| GPIO37       | AK9      | K31    | LFRAME#    |  |                                       |
| GPIO38/IRRX2 | AJ9      | K28    | LPCPD#     |  |                                       |
| GPIO39       | AL8      | J31    | SERIRQ     |  |                                       |
| GPIO40       | A21      | Y3     | IDE_DATA8  |  |                                       |
| GPIO41       | C19      | W4     | IDE_DATA11 |  |                                       |

### 3.4.17 Debug Monitoring Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux                     |
|-------------|----------|--------|------|--|-------------------------|
|             | EBGA     | TEPBGA |      |  |                         |
| FPCICLK     | U3       | B18    | O    | <b>Fast-PCI Bus Monitoring Signals.</b> When enabled, this group of signals provides for monitoring of the internal Fast-PCI bus for debug purposes. To enable, pull up FPCI_MON (EBGA ball D3 / TEPBGA ball A4).                              | ACK#+TFTDE              |
| F_AD7       | U1       | A18    | O    |  | PD7+TFTD13              |
| F_AD6       | V3       | A20    | O    |  | PD6+TFTD1               |
| F_AD5       | V2       | C19    | O    |  | PD5+TFTD11              |
| F_AD4       | V1       | C18    | O    |  | PD4+TFTD10              |
| F_AD3       | W2       | C20    | O    |  | PD3+TFTD9               |
| F_AD2       | W3       | D20    | O    |  | PD2+TFTD8               |
| F_AD1       | Y1       | A21    | O    |  | PD1+TFTD7               |
| F_AD0       | AA1      | C21    | O    |  | PD0+TFTD6               |
| F_C/BE3#    | T4       | C17    | O    |  | SLCT+TFTD15             |
| F_C/BE2#    | T3       | D17    | O    |  | PE+TFTD14               |
| F_C/BE1#    | T1       | B17    | O    |  | BUSY/WAIT#+<br>TFTD3    |
| F_C/BE0#    | AA3      | D21    | O    |  | ERR#+TFTD4+             |
| F_FRAME#    | AB1      | A22    | O    |  | STB#/WRITE#+<br>TFTD17  |
| F_IRDY#     | W1       | B20    | O    |  | SLIN#/ASTRB#+<br>TFTD16 |
| F_STOP#     | AJ15     | U29    | O    |  | AC97_RST#               |
| F_DEVSEL#   | AL15     | V31    | O    | GPIO16+<br>PC_BEEP   |                         |
| F_GNT0#     | AK14     | U31    | O    | SDATA_IN   |                         |
| F_TRDY#     | AL14     | U30    | O    | BIT_CLK  |                         |
| INTR_O      | AB2      | D22    | O    | <b>CPU Core Interrupt.</b> When enabled, this signal provides for monitoring of the internal GX1 core INTR signal for debug purposes. To enable, pull up FPCI_MON (EBGA ball D3 / TEPBGA ball A4).   | AFD#/DSTRB#+<br>TFTD2   |
| SMI_O       | Y3       | B21    | O    | <b>System Management Interrupt.</b> This is the input to the GX1 core. When enabled, this signal provides for monitoring of the internal GX1 core SMI# signal for debug purposes. To enable, pull up FPCI_MON (EBGA ball D3 / TEPBGA ball A4). | INIT#+TFTD5+            |

### 3.4.18 JTAG Interface Signals

| Signal Name | Ball No. |        | Type | Description   | Mux |
|-------------|----------|--------|------|---|-----|
|             | EBGA     | TEPBGA |      |   |     |
| TCK         | AL4      | E31    | I    | <b>JTAG Test Clock.</b> This signal has an internal weak pull-up resistor.  | --- |
| TDI         | AK5      | F29    | I    | <b>JTAG Test Data Input.</b> This signal has an internal weak pull-up resistor.   | --- |
| TDO         | AH6      | E30    | O    | <b>JTAG Test Data Output</b>  | --- |
| TMS         | AJ5      | F28    | I    | <b>JTAG Test Mode Select.</b> This signal has an internal weak pull-up resistor.  | --- |
| TRST#       | AK4      | E29    | I    | <b>JTAG Test Reset.</b> This signal has an internal weak pull-up resistor.<br>For normal JTAG operation, this signal should be active at power-up.<br>If the JTAG interface is not being used, this signal can be tied low. | --- |

### 3.4.19 Test and Measurement Interface Signals

| Signal Name | Ball No. |        | Type | Description  | Mux                 |
|-------------|----------|--------|------|--|---------------------|
|             | EBGA     | TEPBGA |      |  |                     |
| GXCLK       | AL16     | V30    | O    | <b>GX Clock.</b> This signal is for internal testing only. For normal operation either program as FP_VDD_ON or leave unconnected.  | FP_VDD_ON+<br>TEST3 |
| TEST3       | AL16     | V30    | O    | <b>Internal Test Signal.</b> This signal is used for internal testing only. For normal operation leave unconnected, unless programmed as FP_VDD_ON.                      | FP_VDD_ON+<br>GXCLK |
| TEST2       | B29      | AJ1    | O    | <b>Internal Test Signals.</b> These signals are used for internal testing only. For normal operation, leave unconnected unless programmed as one of their muxed options. | PLL5B               |
| TEST1       | C28      | AG4    | O    |  | PLL6B               |
| TEST0       | D28      | AH3    | O    |  | PLL2B               |
| GTEST       | AL5      | F30    | I    | <b>Global Test.</b> This signal is used for internal testing only. For normal operation this signal should be pulled down with 1.5 K $\Omega$ .                          | ---                 |
| PLL6B       | C28      | AG4    | I/O  | <b>PLL6, PLL5 and PLL2 Bypass.</b> These signals are used for internal testing only. For normal operation leave unconnected.   | TEST1               |
| PLL5B       | B29      | AJ1    | I/O  |  | TEST2               |
| PLL2B       | D28      | AH3    | I/O  |  | TEST0               |

### 3.4.19 Test and Measurement Interface Signals (Continued)

| Signal Name | Ball No. |        | Type | Description  | Mux  |
|-------------|----------|--------|------|--|--|
|             | EBGA     | TEPBGA |      |  |  |
| SDTEST5     | AH3      | D28    | O    | <b>Memory Internal Test Signals.</b> These signals are used for internal testing only. For normal operation, these signals should be programmed as one of their muxed options. | GPIO6+DTR2#/BOUT2+IDE_IOR1#  |
| SDTEST4     | AJ2      | C31    | O    |  | GPIO8+CTS2#+IDE_DREQ1  |
| SDTEST3     | AJ4      | E28    | O    |  | SIN2   |
| SDTEST2     | AG4      | C28    | O    |  | GPIO9+DCD2#+IDE_IOW1#  |
| SDTEST1     | AJ1      | B29    | O    |  | GPIO10+DSR2#+IDE_IORDY1  |
| SDTEST0     | AH4      | C30    | O    |  | GPIO7+RTS2#+IDE_DACK1#   |
| TDP         | AH5      | D30    | I/O  |  | <b>Thermal Diode Positive / Negative.</b> These signals are for internal testing only. For normal operation leave unconnected. |
| TDN         | AL3      | D31    | I/O  | ---  |  |

3.4.20 Power, Ground and No Connections<sup>1</sup>

| Signal Name          | Ball No.                                |   | Type | Description  |
|----------------------|---|---|------|--|
|                      | EBGA                                    | TEPBGA                                  |      |  |
| AV <sub>SSPLL2</sub> | R3                                      | C16                                     | GND  | <b>Analog PLL2 Ground Connection.</b>  |
| AV <sub>SSPLL3</sub> | E28                                     | AK3                                     | GND  | <b>Analog PLL3 Ground Connection.</b>  |
| V <sub>PLL2</sub>    | R1                                      | A17                                     | PWR  | <b>3.3V PLL2 Analog Power Connection.</b> Low noise power for PLL2 and PLL5.   |
| V <sub>PLL3</sub>    | C31                                     | AJ4                                     | PWR  | <b>3.3V PLL3 Analog Power Connection.</b> Low noise power for PLL3, PLL4, and PLL6.  |
| AV <sub>CCUSB</sub>  | AF4                                     | D27                                     | PWR  | <b>3.3V Analog USB Power Connection.</b> Low noise power.  |
| AV <sub>SSUSB</sub>  | AG1                                     | C27                                     | GND  | <b>Analog USB Ground Connection.</b>   |
| V <sub>BAT</sub>     | D30                                     | AL3                                     | PWR  | <b>Battery.</b> Provides battery back-up to the RTC and ACPI registers, when V <sub>SB</sub> is lower than the minimum value (see Table 9-3 on page 370). The ball is connected to the internal logic through a series resistor for UL protection. If battery backup is not desired, connect V <sub>BAT</sub> to V <sub>SS</sub> . |
| V <sub>SB</sub>      | F29                                     | AL5                                     | PWR  | <b>3.3V Standby Power Supply.</b> Provides power to the Real-Time Clock (RTC) and ACPI circuitry while the main power supply is turned off.  |
| V <sub>SBL</sub>     | H28                                     | AL6                                     | PWR  | <b>1.8V Standby Power Supply.</b> Provides power to the internal logic while the main power supply is turned off. This signal requires a 0.1 $\mu$ F bypass capacitor to V <sub>SS</sub> . This supply must be present when V <sub>SB</sub> is present.  |
| V <sub>CORE</sub>    | See Table 3-3 on page 38. (Total of 26) | See Table 3-5 on page 54. (Total of 29) | PWR  | <b>1.8V Core Processor Power Connections.</b>  |
| V <sub>IO</sub>      | See Table 3-3 on page 38. (Total of 35) | See Table 3-5 on page 54. (Total of 46) | PWR  | <b>3.3V I/O Power Connections.</b>   |
| V <sub>SS</sub>      | See Table 3-3 on page 38. (Total of 61) | See Table 3-5 on page 54. (Total of 96) | GND  | <b>Ground Connections.</b>   |
| NC                   | See Table 3-3 on page 38. (Total of 13) | See Table 3-5 on page 54. (Total of 13) | ---  | <b>No Connections.</b> These lines should be left disconnected. Connecting a pull-up/-down resistor or to an active signal could cause unexpected results and possible malfunctions.   |

1. All power sources except V<sub>BAT</sub> must be connected, even if the function is not used.

# General Configuration Block

The General Configuration block includes registers for:

- Pin Multiplexing and Miscellaneous Configuration
- WATCHDOG Timer
- High-Resolution Timer
- Clock Generators

A selectable interrupt is shared by all these functions.

## 4.1 Configuration Block Addresses

Registers of the General Configuration block are I/O mapped in a 64-byte address range. These registers are physically connected to the internal Fast-PCI bus, but do

not have a register block in PCI configuration space (i.e., they do not appear to software as PCI registers).

After system reset, the Base Address register is located at I/O address 02EAh. This address can be used only once. Before accessing any PCI registers, the BOOT code must program this 16-bit register to the I/O base address for the General Configuration block registers. All subsequent writes to this address, are ignored until system reset.

**Note:** Location of the General Configuration Block cannot be determined by software. See the *AMD Geode™ SC3200 Specification Update* document.

Reserved bits in the General Configuration block should read as written unless otherwise specified.

**Table 4-1. General Configuration Block Register Summary**

| Offset  | Width (Bits) | Type | Name   | Reset Value    | Reference |
|---------|--------------|------|--|----------------|-----------|
| 00h-01h | 16           | R/W  | <b>WDTO.</b> WATCHDOG Timeout                    | 0000h          | Page 96   |
| 02h-03h | 16           | R/W  | <b>WDCNFG.</b> WATCHDOG Configuration            | 0000h          | Page 96   |
| 04h     | 8            | R/WC | <b>WDSTS.</b> WATCHDOG Status                    | 00h            | Page 97   |
| 05h-07h | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 08h-0Bh | 32           | RO   | <b>TMVALUE.</b> TIMER Value                      | xxxxxxxxh      | Page 98   |
| 0Ch     | 8            | R/W  | <b>TMSTS.</b> TIMER Status                       | 00h            | Page 98   |
| 0Dh     | 8            | R/W  | <b>TMCNFG.</b> TIMER Configuration               | 00h            | Page 98   |
| 0Eh-0Fh | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 10h     | 8            | RO   | <b>MCCM.</b> Maximum Core Clock Multiplier       | Strapped Value | Page 103  |
| 11h     | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 12h     | 8            | R/W  | <b>PPCR.</b> PLL Power Control                   | 2Fh            | Page 103  |
| 13h-17h | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 18h-1Bh | 32           | R/W  | <b>PLL3C.</b> PLL3 Configuration                 | E1040005h      | Page 103  |
| 1Ch-1Dh | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 1Eh-1Fh | 16           | R/W  | <b>CCFC.</b> Core Clock Frequency Control        | Strapped Value | Page 104  |
| 20h-2Fh | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 30h-33h | 32           | R/W  | <b>PMR.</b> Pin Multiplexing Register            | 00000000h      | Page 88   |
| 34h-37h | 32           | R/W  | <b>MCR.</b> Miscellaneous Configuration Register | 00000001h      | Page 92   |
| 38h     | 8            | R/W  | <b>INTSEL.</b> Interrupt Selection               | 00h            | Page 94   |
| 39h-3Bh | ---          | ---  | <b>RSVD.</b> Reserved                            | ---            | ---       |
| 3Ch     | 8            | RO   | <b>ID.</b> Device ID                             | xxh            | Page 94   |
| 3Dh     | 8            | RO   | <b>REV.</b> Revision                             | xxh            | Page 94   |
| 3Eh-3Fh | 16           | RO   | <b>CBA.</b> Configuration Base Address           | xxxxh          | Page 94   |

## 4.2 Multiplexing, Interrupt Selection, and Base Address Registers

The registers described in Table 4-2 are used to determine general configuration for the SC3200. These registers also indicate which multiplexed signals are issued via balls from which more than one signal may be output. For more infor-

mation about multiplexed signals and the appropriate configurations, see Section 3.1 "Ball Assignments" on page 27.

**Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers**

| Bit   | Description  |  |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
|---|--|--|-----------------------------|--------------------|--------------------------|---|---|------|--------------------|--|--------------------|-----------|--|------|---------|--|-----------|-----------------|--------------|--------------------|----------|-----------|------------|-------------|----------|-------|------------|-------------|-------------|-------|-------------|-------------|----------|-------|------------|-------------|----------|-------|------------|-------------|----------|-------|-----------|-------------|----------|-------|-----------|-------------|----------|-------|-----------|-------------|-----------|-------|-----------|-------------|----------|----------|-------------|-------------|----------|----------|-----------|-------------|----------|----------|------------------|-------------|-----------|----------|------------|-------------|-----------|----------|-------------------|-------------|----------|---------|---------------------|-------------|-----------|--------|-------------------|-------------|----------|-------|-------------|-------------|------------|-----------|----------------|-----------------------------|------------|---------|-----------|--------------|------------|---------|----------|--------------|------------|---------|---------|--------------|
| <b>Offset 30h-33h</b> <span style="float:right"><b>Pin Multiplexing Register - PMR (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span><br>This register configures pins with multiple functions. See Section 3.1 on page 27 for more information about multiplexing information. |  |  |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 31:30   | <b>Reserved:</b> Always write 0.   |  |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 29  | <p><b>Test Signals.</b> Selects ball functions.</p> <table border="0"> <thead> <tr> <th>Ball #</th> <th colspan="2">0: Internal Test Signals</th> <th colspan="2">1: Internal Test Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>D28 / AH3</td> <td>PLL2B</td> <td>None</td> <td>TEST0</td> <td>None</td> </tr> <tr> <td>C28 / AG4</td> <td>PLL6B</td> <td>None</td> <td>TEST1</td> <td>None</td> </tr> <tr> <td>B29 / AJ1</td> <td>PLL5B</td> <td>None</td> <td>TEST2</td> <td>None</td> </tr> <tr> <td>AL16 / V30</td> <td>GXCLK</td> <td>See PMR[23]</td> <td>TEST3</td> <td>PMR[23] = 0</td> </tr> </tbody> </table>  | Ball #   | 0: Internal Test Signals    |                    | 1: Internal Test Signals |   | EBGA / TEPBGA                           | Name | Add'l Dependencies | Name                                   | Add'l Dependencies | D28 / AH3 | PLL2B  | None | TEST0   | None                                   | C28 / AG4 | PLL6B           | None         | TEST1              | None     | B29 / AJ1 | PLL5B      | None        | TEST2    | None  | AL16 / V30 | GXCLK       | See PMR[23] | TEST3 | PMR[23] = 0 |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| Ball #  | 0: Internal Test Signals   |  | 1: Internal Test Signals    |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| EBGA / TEPBGA   | Name   | Add'l Dependencies   | Name                        | Add'l Dependencies |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| D28 / AH3   | PLL2B  | None   | TEST0                       | None               |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| C28 / AG4   | PLL6B  | None   | TEST1                       | None               |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| B29 / AJ1   | PLL5B  | None   | TEST2                       | None               |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AL16 / V30  | GXCLK  | See PMR[23]  | TEST3                       | PMR[23] = 0        |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 28  | <p><b>Test Signals.</b> Selects ball function.</p> <table border="0"> <thead> <tr> <th>Ball #</th> <th colspan="2">0: AC97 Signal</th> <th colspan="2">1: Internal Test Signal</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>AJ4 / E28</td> <td>SIN2</td> <td>None</td> <td>SDTEST3</td> <td>See Note.</td> </tr> </tbody> </table> <p><b>Note:</b> If this bit is set, PMR[8] and PMR[18] must be set by software.</p>   | Ball #   | 0: AC97 Signal              |                    | 1: Internal Test Signal  |   | EBGA / TEPBGA                           | Name | Add'l Dependencies | Name                                   | Add'l Dependencies | AJ4 / E28 | SIN2   | None | SDTEST3 | See Note.                              |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| Ball #  | 0: AC97 Signal   |  | 1: Internal Test Signal     |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| EBGA / TEPBGA   | Name   | Add'l Dependencies   | Name                        | Add'l Dependencies |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AJ4 / E28   | SIN2   | None   | SDTEST3                     | See Note.          |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 27  | <p><b>FPCI_MON (Fast-PCI Monitoring).</b> Selects Fast-PCI monitoring output signals instead of Parallel Port signals.</p> <p>Fast-PCI monitoring output signals can be enabled in two ways: by setting this bit to 1 or by strapping FPCI_MON (EBGA ball D3 / TEPBGA ball A4) high. (The strapped value can be read back at MCR[30].) Listed below is how these two options work together and the signals that are enabled (enabling overrides add'l dependencies except FPCI_MON = 1). Note that the FPCI monitoring signals that are muxed with Audio signals are not enabled via this bit. They are only enabled using the strap option.</p> <table border="0"> <thead> <tr> <th>PMR[27]</th> <th>FPCI_MON</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disable all Fast-PCI monitoring signals</td> </tr> <tr> <td>0</td> <td>1</td> <td>Enable all Fast-PCI monitoring signals</td> </tr> <tr> <td>1</td> <td>0</td> <td>Enable Fast-PCI monitoring signals muxed with Parallel Port signals only</td> </tr> <tr> <td>1</td> <td>1</td> <td>Enable all Fast-PCI monitoring signals</td> </tr> </tbody> </table> <table border="0"> <thead> <tr> <th>Ball #</th> <th>FPCI_MON Signal</th> <th>Other Signal</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>U3 / B18</td> <td>FPCICLK</td> <td>ACK#+TFTDE</td> <td>See PMR[23]</td> </tr> <tr> <td>U1 / A18</td> <td>F_AD7</td> <td>PD7+TFTD13</td> <td>See PMR[23]</td> </tr> <tr> <td>V3 / A20</td> <td>F_AD6</td> <td>PD6+TFTD1</td> <td>See PMR[23]</td> </tr> <tr> <td>V2 / C19</td> <td>F_AD5</td> <td>PD5+TFTD11</td> <td>See PMR[23]</td> </tr> <tr> <td>V1 / C18</td> <td>F_AD4</td> <td>PD4+TFTD10</td> <td>See PMR[23]</td> </tr> <tr> <td>W2 / C20</td> <td>F_AD3</td> <td>PD3+TFTD9</td> <td>See PMR[23]</td> </tr> <tr> <td>W3 / D20</td> <td>F_AD2</td> <td>PD2+TFTD8</td> <td>See PMR[23]</td> </tr> <tr> <td>Y1 / A21</td> <td>F_AD1</td> <td>PD1+TFTD7</td> <td>See PMR[23]</td> </tr> <tr> <td>AA1 / C21</td> <td>F_AD0</td> <td>PD0_TFTD5</td> <td>See PMR[23]</td> </tr> <tr> <td>T4 / C17</td> <td>F_C/BE3#</td> <td>SLCT+TFTD15</td> <td>See PMR[23]</td> </tr> <tr> <td>T3 / D17</td> <td>F_C/BE2#</td> <td>PE+TFTD14</td> <td>See PMR[23]</td> </tr> <tr> <td>T1 / B17</td> <td>F_C/BE1#</td> <td>BUSY/WAIT#+TFTD3</td> <td>See PMR[23]</td> </tr> <tr> <td>AA3 / D21</td> <td>F_C/BE0#</td> <td>ERR#+TFTD4</td> <td>See PMR[23]</td> </tr> <tr> <td>AB1 / A22</td> <td>F_FRAME#</td> <td>STB#/WRITE#+TFTD7</td> <td>See PMR[23]</td> </tr> <tr> <td>W1 / B20</td> <td>F_IRDY#</td> <td>SLIN#/ASTRB#+TFTD16</td> <td>See PMR[23]</td> </tr> <tr> <td>AB2 / D22</td> <td>INTR_O</td> <td>AFD#/DSTRB#+TFTD2</td> <td>See PMR[23]</td> </tr> <tr> <td>Y3 / B21</td> <td>SML_O</td> <td>INIT#+TFTD5</td> <td>See PMR[23]</td> </tr> <tr> <td>AL15 / V31</td> <td>F_DEVSEL#</td> <td>GPIO16+PC_BEEP</td> <td>FPCI_MON = 1 and see PMR[0]</td> </tr> <tr> <td>AJ15 / U29</td> <td>F_STOP#</td> <td>AC97_RST#</td> <td>FPCI_MON = 1</td> </tr> <tr> <td>AK14 / U31</td> <td>F_GNT0#</td> <td>SDATA_IN</td> <td>FPCI_MON = 1</td> </tr> <tr> <td>AL14 / U30</td> <td>F_TRDY#</td> <td>BIT_CLK</td> <td>FPCI_MON = 1</td> </tr> </tbody> </table> | PMR[27]  | FPCI_MON                    |                    | 0                        | 0 | Disable all Fast-PCI monitoring signals | 0    | 1                  | Enable all Fast-PCI monitoring signals | 1                  | 0         | Enable Fast-PCI monitoring signals muxed with Parallel Port signals only | 1    | 1       | Enable all Fast-PCI monitoring signals | Ball #    | FPCI_MON Signal | Other Signal | Add'l Dependencies | U3 / B18 | FPCICLK   | ACK#+TFTDE | See PMR[23] | U1 / A18 | F_AD7 | PD7+TFTD13 | See PMR[23] | V3 / A20    | F_AD6 | PD6+TFTD1   | See PMR[23] | V2 / C19 | F_AD5 | PD5+TFTD11 | See PMR[23] | V1 / C18 | F_AD4 | PD4+TFTD10 | See PMR[23] | W2 / C20 | F_AD3 | PD3+TFTD9 | See PMR[23] | W3 / D20 | F_AD2 | PD2+TFTD8 | See PMR[23] | Y1 / A21 | F_AD1 | PD1+TFTD7 | See PMR[23] | AA1 / C21 | F_AD0 | PD0_TFTD5 | See PMR[23] | T4 / C17 | F_C/BE3# | SLCT+TFTD15 | See PMR[23] | T3 / D17 | F_C/BE2# | PE+TFTD14 | See PMR[23] | T1 / B17 | F_C/BE1# | BUSY/WAIT#+TFTD3 | See PMR[23] | AA3 / D21 | F_C/BE0# | ERR#+TFTD4 | See PMR[23] | AB1 / A22 | F_FRAME# | STB#/WRITE#+TFTD7 | See PMR[23] | W1 / B20 | F_IRDY# | SLIN#/ASTRB#+TFTD16 | See PMR[23] | AB2 / D22 | INTR_O | AFD#/DSTRB#+TFTD2 | See PMR[23] | Y3 / B21 | SML_O | INIT#+TFTD5 | See PMR[23] | AL15 / V31 | F_DEVSEL# | GPIO16+PC_BEEP | FPCI_MON = 1 and see PMR[0] | AJ15 / U29 | F_STOP# | AC97_RST# | FPCI_MON = 1 | AK14 / U31 | F_GNT0# | SDATA_IN | FPCI_MON = 1 | AL14 / U30 | F_TRDY# | BIT_CLK | FPCI_MON = 1 |
| PMR[27]   | FPCI_MON   |  |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 0   | 0  | Disable all Fast-PCI monitoring signals                                  |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 0   | 1  | Enable all Fast-PCI monitoring signals                                   |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 1   | 0  | Enable Fast-PCI monitoring signals muxed with Parallel Port signals only |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| 1   | 1  | Enable all Fast-PCI monitoring signals                                   |                             |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| Ball #  | FPCI_MON Signal  | Other Signal   | Add'l Dependencies          |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| U3 / B18  | FPCICLK  | ACK#+TFTDE   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| U1 / A18  | F_AD7  | PD7+TFTD13   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| V3 / A20  | F_AD6  | PD6+TFTD1  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| V2 / C19  | F_AD5  | PD5+TFTD11   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| V1 / C18  | F_AD4  | PD4+TFTD10   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| W2 / C20  | F_AD3  | PD3+TFTD9  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| W3 / D20  | F_AD2  | PD2+TFTD8  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| Y1 / A21  | F_AD1  | PD1+TFTD7  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AA1 / C21   | F_AD0  | PD0_TFTD5  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| T4 / C17  | F_C/BE3#   | SLCT+TFTD15  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| T3 / D17  | F_C/BE2#   | PE+TFTD14  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| T1 / B17  | F_C/BE1#   | BUSY/WAIT#+TFTD3   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AA3 / D21   | F_C/BE0#   | ERR#+TFTD4   | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AB1 / A22   | F_FRAME#   | STB#/WRITE#+TFTD7  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| W1 / B20  | F_IRDY#  | SLIN#/ASTRB#+TFTD16  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AB2 / D22   | INTR_O   | AFD#/DSTRB#+TFTD2  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| Y3 / B21  | SML_O  | INIT#+TFTD5  | See PMR[23]                 |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AL15 / V31  | F_DEVSEL#  | GPIO16+PC_BEEP   | FPCI_MON = 1 and see PMR[0] |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AJ15 / U29  | F_STOP#  | AC97_RST#  | FPCI_MON = 1                |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AK14 / U31  | F_GNT0#  | SDATA_IN   | FPCI_MON = 1                |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |
| AL14 / U30  | F_TRDY#  | BIT_CLK  | FPCI_MON = 1                |                    |                          |   |   |      |                    |  |                    |           |  |      |         |  |           |                 |              |                    |          |           |            |             |          |       |            |             |             |       |             |             |          |       |            |             |          |       |            |             |          |       |           |             |          |       |           |             |          |       |           |             |           |       |           |             |          |          |             |             |          |          |           |             |          |          |                  |             |           |          |            |             |           |          |                   |             |          |         |                     |             |           |        |                   |             |          |       |             |             |            |           |                |                             |            |         |           |              |            |         |          |              |            |         |         |              |



**Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)**

| Bit           | Description  |                         |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
|---------------|--|-------------------------|----------------|-------------------------|---------------|------|------|-----------|-----------|-------|-----------|-----------|-------|----------|-----------|-------|-----------|-----------|-------|-----------|-----------|--------|-----------|-----------|--------|-----------|-----------|--------|-----------|-----------|-----------|-----------|-----------|--------|-----------|-----------|------|-----------|-----------|-------|----------|-----------|--------|----------|-----------|---------|----------|------------|---------|----------|------------|--------|----------|------------|--------|----------|------------|--------|----------|------------|--------|----------|------------|-------|-----------|----------|-------|----------|----------|-------|----------|-----------|--------|-----------|-----------|-------|-----------|-----------|-------|-----------|------------|-------|-----------|----------|--------|-----------|------------|--------|-----------|-------|-------|
| 26            | <b>Reserved.</b> Always write 0.   |                         |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| 25            | <b>AC97CKEN (Enable AC97_CLK Output).</b> This bit enables the output drive of AC97_CLK (EBGA ball AJ14 / TEPBGA ball P31).<br>0: AC97_CLK output is HiZ.<br>1: AC97_CLK output is enabled.  |                         |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| 24            | <p><b>TFTIDE (TFT/IDE).</b> Determines whether certain balls are used for TFT signals or for IDE signals. Note that there are no additional dependencies.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: IDE Signals</th> <th>1: GPIO and TFT Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>A26 / AD3</td> <td>IDE_ADDR0</td> <td>TFTD3</td> </tr> <tr> <td>C26 / AE1</td> <td>IDE_ADDR1</td> <td>TFTD2</td> </tr> <tr> <td>C17 / U2</td> <td>IDE_ADDR2</td> <td>TFTD4</td> </tr> <tr> <td>B24 / AC3</td> <td>IDE_DATA0</td> <td>TFTD6</td> </tr> <tr> <td>A24 / AC1</td> <td>IDE_DATA1</td> <td>TFTD16</td> </tr> <tr> <td>D23 / AC2</td> <td>IDE_DATA2</td> <td>TFTD14</td> </tr> <tr> <td>C23 / AB4</td> <td>IDE_DATA3</td> <td>TFTD12</td> </tr> <tr> <td>B23 / AB1</td> <td>IDE_DATA4</td> <td>FP_VDD_ON</td> </tr> <tr> <td>A23 / AA4</td> <td>IDE_DATA5</td> <td>CLK27M</td> </tr> <tr> <td>C22 / AA3</td> <td>IDE_DATA6</td> <td>IRQ9</td> </tr> <tr> <td>B22 / AA2</td> <td>IDE_DATA7</td> <td>INTD#</td> </tr> <tr> <td>A21 / Y3</td> <td>IDE_DATA8</td> <td>GPIO40</td> </tr> <tr> <td>C20 / Y2</td> <td>IDE_DATA9</td> <td>DDC_SDA</td> </tr> <tr> <td>A20 / Y1</td> <td>IDE_DATA10</td> <td>DDC_SCL</td> </tr> <tr> <td>C19 / W4</td> <td>IDE_DATA11</td> <td>GPIO41</td> </tr> <tr> <td>B19 / W3</td> <td>IDE_DATA12</td> <td>TFTD13</td> </tr> <tr> <td>A19 / V3</td> <td>IDE_DATA13</td> <td>TFTD15</td> </tr> <tr> <td>C18 / V2</td> <td>IDE_DATA14</td> <td>TFTD17</td> </tr> <tr> <td>B18 / V1</td> <td>IDE_DATA15</td> <td>TFTD7</td> </tr> <tr> <td>A27 / AF2</td> <td>IDE_CS0#</td> <td>TFTD5</td> </tr> <tr> <td>C16 / P2</td> <td>IDE_CS1#</td> <td>TFTDE</td> </tr> <tr> <td>C21 / Y4</td> <td>IDE_IOR0#</td> <td>TFTD10</td> </tr> <tr> <td>D24 / AD2</td> <td>IDE_IOW0#</td> <td>TFTD9</td> </tr> <tr> <td>C24 / AC4</td> <td>IDE_DREQ0</td> <td>TFTD8</td> </tr> <tr> <td>C25 / AD4</td> <td>IDE_DACK0#</td> <td>TFTD0</td> </tr> <tr> <td>A22 / AA1</td> <td>IDE_RST#</td> <td>TFTDCK</td> </tr> <tr> <td>A25 / AD1</td> <td>IDE_IORDY0</td> <td>TFTD11</td> </tr> <tr> <td>D25 / AF1</td> <td>IRQ14</td> <td>TFTD1</td> </tr> </tbody> </table> | Ball #                  | 0: IDE Signals | 1: GPIO and TFT Signals | EBGA / TEPBGA | Name | Name | A26 / AD3 | IDE_ADDR0 | TFTD3 | C26 / AE1 | IDE_ADDR1 | TFTD2 | C17 / U2 | IDE_ADDR2 | TFTD4 | B24 / AC3 | IDE_DATA0 | TFTD6 | A24 / AC1 | IDE_DATA1 | TFTD16 | D23 / AC2 | IDE_DATA2 | TFTD14 | C23 / AB4 | IDE_DATA3 | TFTD12 | B23 / AB1 | IDE_DATA4 | FP_VDD_ON | A23 / AA4 | IDE_DATA5 | CLK27M | C22 / AA3 | IDE_DATA6 | IRQ9 | B22 / AA2 | IDE_DATA7 | INTD# | A21 / Y3 | IDE_DATA8 | GPIO40 | C20 / Y2 | IDE_DATA9 | DDC_SDA | A20 / Y1 | IDE_DATA10 | DDC_SCL | C19 / W4 | IDE_DATA11 | GPIO41 | B19 / W3 | IDE_DATA12 | TFTD13 | A19 / V3 | IDE_DATA13 | TFTD15 | C18 / V2 | IDE_DATA14 | TFTD17 | B18 / V1 | IDE_DATA15 | TFTD7 | A27 / AF2 | IDE_CS0# | TFTD5 | C16 / P2 | IDE_CS1# | TFTDE | C21 / Y4 | IDE_IOR0# | TFTD10 | D24 / AD2 | IDE_IOW0# | TFTD9 | C24 / AC4 | IDE_DREQ0 | TFTD8 | C25 / AD4 | IDE_DACK0# | TFTD0 | A22 / AA1 | IDE_RST# | TFTDCK | A25 / AD1 | IDE_IORDY0 | TFTD11 | D25 / AF1 | IRQ14 | TFTD1 |
| Ball #        | 0: IDE Signals   | 1: GPIO and TFT Signals |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| EBGA / TEPBGA | Name   | Name                    |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A26 / AD3     | IDE_ADDR0  | TFTD3                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C26 / AE1     | IDE_ADDR1  | TFTD2                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C17 / U2      | IDE_ADDR2  | TFTD4                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| B24 / AC3     | IDE_DATA0  | TFTD6                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A24 / AC1     | IDE_DATA1  | TFTD16                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| D23 / AC2     | IDE_DATA2  | TFTD14                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C23 / AB4     | IDE_DATA3  | TFTD12                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| B23 / AB1     | IDE_DATA4  | FP_VDD_ON               |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A23 / AA4     | IDE_DATA5  | CLK27M                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C22 / AA3     | IDE_DATA6  | IRQ9                    |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| B22 / AA2     | IDE_DATA7  | INTD#                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A21 / Y3      | IDE_DATA8  | GPIO40                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C20 / Y2      | IDE_DATA9  | DDC_SDA                 |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A20 / Y1      | IDE_DATA10   | DDC_SCL                 |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C19 / W4      | IDE_DATA11   | GPIO41                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| B19 / W3      | IDE_DATA12   | TFTD13                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A19 / V3      | IDE_DATA13   | TFTD15                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C18 / V2      | IDE_DATA14   | TFTD17                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| B18 / V1      | IDE_DATA15   | TFTD7                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A27 / AF2     | IDE_CS0#   | TFTD5                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C16 / P2      | IDE_CS1#   | TFTDE                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C21 / Y4      | IDE_IOR0#  | TFTD10                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| D24 / AD2     | IDE_IOW0#  | TFTD9                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C24 / AC4     | IDE_DREQ0  | TFTD8                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| C25 / AD4     | IDE_DACK0#   | TFTD0                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A22 / AA1     | IDE_RST#   | TFTDCK                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| A25 / AD1     | IDE_IORDY0   | TFTD11                  |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |
| D25 / AF1     | IRQ14  | TFTD1                   |                |                         |               |      |      |           |           |       |           |           |       |          |           |       |           |           |       |           |           |        |           |           |        |           |           |        |           |           |           |           |           |        |           |           |      |           |           |       |          |           |        |          |           |         |          |            |         |          |            |        |          |            |        |          |            |        |          |            |        |          |            |       |           |          |       |          |          |       |          |           |        |           |           |       |           |           |       |           |            |       |           |          |        |           |            |        |           |       |       |

Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)

| Bit                     | Description   |                            |                         |                            |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
|-------------------------|---|----------------------------|-------------------------|----------------------------|----------------|--------------------|----------|-----------------|----------------------------|--------|------|---------|------------------|--------------------------|-------|------|----------|------------------|--------------------------|--------|------|----------|------------------------|------------------|-------|------|----------|----------------|------------------|--------|--------|----------|------------------|------------------|--------|--------|----------|--------------|------------------|--------|--------|----------|-----------------|------------------|-------|--------|----------|--------------|------------------|--------|--------|----------|--------------|------------------|--------|--------|----------|--------------|------------------|-------|--------|----------|-------------------------|------------------|--------|--------|----------|--------------|------------------|-------|--------|----------|--------------|------------------|-------|--------|----------|--------------|------------------|-------|--------|----------|----------------|------------------|-------|--------|-----------|--------------|------------------|-------|--------|-----------|------------------|------------------|-------|--------|-----------|-------------------------|------------------|--------|------|-----------|-----------------------|------------------|-------|--------|------------|------|------|------------------|--------------------------|------------|------|------|-----------------|----------------------------|------------|----------------|----------------------------|-----------|------|
| 23                      | <p><b>TFTPP (TFT/Parallel Port).</b> Determines whether certain balls are used for TFT or PP/ACB1/FPCI. This bit is set to 1 at power-on if the TFT_PRSENT strap (EBGA ball AK13 / TEPBGA ball P29) is pulled high.</p> <table border="1"> <thead> <tr> <th>Ball #<br/>EBGA / TEPBGA</th> <th>0: PP/ACB1/FPCI<br/>Name</th> <th>Add'l Dependencies</th> <th>1: TFT<br/>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>H2 / D10</td> <td>GPIO1<br/>IOCS1#</td> <td>PMR[13] = 0<br/>PMR[13] = 1</td> <td>TFTD12</td> <td>None</td> </tr> <tr> <td>H3 / A9</td> <td>GPIO20<br/>DOCCS#</td> <td>PMR[7] = 0<br/>PMR[7] = 1</td> <td>TFTD0</td> <td>None</td> </tr> <tr> <td>J4 / A10</td> <td>GPIO17<br/>IOCS0#</td> <td>PMR[5] = 0<br/>PMR[5] = 1</td> <td>TFTDCK</td> <td>None</td> </tr> <tr> <td>T1 / B17</td> <td>BUSY/WAIT#<br/>F_C/BE1#</td> <td>Note 1<br/>Note 2</td> <td>TFTD3</td> <td>None</td> </tr> <tr> <td>T3 / D17</td> <td>PE<br/>F_C/BE2#</td> <td>Note 1<br/>Note 2</td> <td>TFTD14</td> <td>Note 1</td> </tr> <tr> <td>T4 / C17</td> <td>SLCT<br/>F_C/BE3#</td> <td>Note 1<br/>Note 2</td> <td>TFTD15</td> <td>Note 1</td> </tr> <tr> <td>U1 / A18</td> <td>PD7<br/>F_AD7</td> <td>Note 1<br/>Note 2</td> <td>TFTD13</td> <td>Note 1</td> </tr> <tr> <td>U3 / B18</td> <td>ACK#<br/>FPCICLK</td> <td>Note 1<br/>Note 2</td> <td>TFTDE</td> <td>Note 1</td> </tr> <tr> <td>V1 / C18</td> <td>PD4<br/>F_AD4</td> <td>Note 1<br/>Note 2</td> <td>TFTD10</td> <td>Note 1</td> </tr> <tr> <td>V2 / C19</td> <td>PD5<br/>F_AD5</td> <td>Note 1<br/>Note 2</td> <td>TFTD11</td> <td>Note 1</td> </tr> <tr> <td>V3 / A20</td> <td>PD6<br/>F_AD6</td> <td>Note 1<br/>Note 2</td> <td>TFTD1</td> <td>Note 1</td> </tr> <tr> <td>W1 / B20</td> <td>SLIN#/ASTRB#<br/>F_IRDY#</td> <td>Note 1<br/>Note 2</td> <td>TFTD16</td> <td>Note 1</td> </tr> <tr> <td>W2 / C20</td> <td>PD3<br/>F_AD3</td> <td>Note 1<br/>Note 2</td> <td>TFTD9</td> <td>Note 1</td> </tr> <tr> <td>W3 / D20</td> <td>PD2<br/>F_AD2</td> <td>Note 1<br/>Note 2</td> <td>TFTD8</td> <td>Note 1</td> </tr> <tr> <td>Y1 / A21</td> <td>PD1<br/>F_AD1</td> <td>Note 1<br/>Note 2</td> <td>TFTD7</td> <td>Note 1</td> </tr> <tr> <td>Y3 / B21</td> <td>INIT#<br/>SMI_O</td> <td>Note 1<br/>Note 2</td> <td>TFTD5</td> <td>Note 1</td> </tr> <tr> <td>AA1 / C21</td> <td>PD0<br/>F_AD0</td> <td>Note 1<br/>Note 2</td> <td>TFTD6</td> <td>Note 1</td> </tr> <tr> <td>AA3 / D21</td> <td>ERR#<br/>F_C/BE0#</td> <td>Note 1<br/>Note 2</td> <td>TFTD4</td> <td>Note 1</td> </tr> <tr> <td>AB1 / A22</td> <td>STB#/WRITE#<br/>F_FRAME#</td> <td>Note 1<br/>Note 2</td> <td>TFTD17</td> <td>None</td> </tr> <tr> <td>AB2 / D22</td> <td>AFD#/DSTRB#<br/>INTR_O</td> <td>Note 1<br/>Note 2</td> <td>TFTD2</td> <td>Note 1</td> </tr> <tr> <td>AJ13 / N31</td> <td>AB1C</td> <td>None</td> <td>GPIO20<br/>DOCCS#</td> <td>PMR[7] = 0<br/>PMR[7] = 1</td> </tr> <tr> <td>AL12 / N30</td> <td>AB1D</td> <td>None</td> <td>GPIO1<br/>IOCS1#</td> <td>PMR[13] = 0<br/>PMR[13] = 1</td> </tr> <tr> <td>AL16 / V30</td> <td>GXCLK<br/>TEST3</td> <td>PMR[29] = 0<br/>PMR[29] = 1</td> <td>FP_VDD_ON</td> <td>None</td> </tr> </tbody> </table> <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. PMR[27] = 0 and FPCI_MON = 0</li> <li>2. PMR[27] = 1 or FPCI_MON = 1</li> <li>3. ACCESS.bus interface 1 is not available if PMR[23] = 1.</li> <li>4. If FPCI_MON strap is enabled, the TFT_PRSENT strap should pulled low.</li> </ol> | Ball #<br>EBGA / TEPBGA    | 0: PP/ACB1/FPCI<br>Name | Add'l Dependencies         | 1: TFT<br>Name | Add'l Dependencies | H2 / D10 | GPIO1<br>IOCS1# | PMR[13] = 0<br>PMR[13] = 1 | TFTD12 | None | H3 / A9 | GPIO20<br>DOCCS# | PMR[7] = 0<br>PMR[7] = 1 | TFTD0 | None | J4 / A10 | GPIO17<br>IOCS0# | PMR[5] = 0<br>PMR[5] = 1 | TFTDCK | None | T1 / B17 | BUSY/WAIT#<br>F_C/BE1# | Note 1<br>Note 2 | TFTD3 | None | T3 / D17 | PE<br>F_C/BE2# | Note 1<br>Note 2 | TFTD14 | Note 1 | T4 / C17 | SLCT<br>F_C/BE3# | Note 1<br>Note 2 | TFTD15 | Note 1 | U1 / A18 | PD7<br>F_AD7 | Note 1<br>Note 2 | TFTD13 | Note 1 | U3 / B18 | ACK#<br>FPCICLK | Note 1<br>Note 2 | TFTDE | Note 1 | V1 / C18 | PD4<br>F_AD4 | Note 1<br>Note 2 | TFTD10 | Note 1 | V2 / C19 | PD5<br>F_AD5 | Note 1<br>Note 2 | TFTD11 | Note 1 | V3 / A20 | PD6<br>F_AD6 | Note 1<br>Note 2 | TFTD1 | Note 1 | W1 / B20 | SLIN#/ASTRB#<br>F_IRDY# | Note 1<br>Note 2 | TFTD16 | Note 1 | W2 / C20 | PD3<br>F_AD3 | Note 1<br>Note 2 | TFTD9 | Note 1 | W3 / D20 | PD2<br>F_AD2 | Note 1<br>Note 2 | TFTD8 | Note 1 | Y1 / A21 | PD1<br>F_AD1 | Note 1<br>Note 2 | TFTD7 | Note 1 | Y3 / B21 | INIT#<br>SMI_O | Note 1<br>Note 2 | TFTD5 | Note 1 | AA1 / C21 | PD0<br>F_AD0 | Note 1<br>Note 2 | TFTD6 | Note 1 | AA3 / D21 | ERR#<br>F_C/BE0# | Note 1<br>Note 2 | TFTD4 | Note 1 | AB1 / A22 | STB#/WRITE#<br>F_FRAME# | Note 1<br>Note 2 | TFTD17 | None | AB2 / D22 | AFD#/DSTRB#<br>INTR_O | Note 1<br>Note 2 | TFTD2 | Note 1 | AJ13 / N31 | AB1C | None | GPIO20<br>DOCCS# | PMR[7] = 0<br>PMR[7] = 1 | AL12 / N30 | AB1D | None | GPIO1<br>IOCS1# | PMR[13] = 0<br>PMR[13] = 1 | AL16 / V30 | GXCLK<br>TEST3 | PMR[29] = 0<br>PMR[29] = 1 | FP_VDD_ON | None |
| Ball #<br>EBGA / TEPBGA | 0: PP/ACB1/FPCI<br>Name   | Add'l Dependencies         | 1: TFT<br>Name          | Add'l Dependencies         |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| H2 / D10                | GPIO1<br>IOCS1#   | PMR[13] = 0<br>PMR[13] = 1 | TFTD12                  | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| H3 / A9                 | GPIO20<br>DOCCS#  | PMR[7] = 0<br>PMR[7] = 1   | TFTD0                   | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| J4 / A10                | GPIO17<br>IOCS0#  | PMR[5] = 0<br>PMR[5] = 1   | TFTDCK                  | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| T1 / B17                | BUSY/WAIT#<br>F_C/BE1#  | Note 1<br>Note 2           | TFTD3                   | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| T3 / D17                | PE<br>F_C/BE2#  | Note 1<br>Note 2           | TFTD14                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| T4 / C17                | SLCT<br>F_C/BE3#  | Note 1<br>Note 2           | TFTD15                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| U1 / A18                | PD7<br>F_AD7  | Note 1<br>Note 2           | TFTD13                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| U3 / B18                | ACK#<br>FPCICLK   | Note 1<br>Note 2           | TFTDE                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| V1 / C18                | PD4<br>F_AD4  | Note 1<br>Note 2           | TFTD10                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| V2 / C19                | PD5<br>F_AD5  | Note 1<br>Note 2           | TFTD11                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| V3 / A20                | PD6<br>F_AD6  | Note 1<br>Note 2           | TFTD1                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| W1 / B20                | SLIN#/ASTRB#<br>F_IRDY#   | Note 1<br>Note 2           | TFTD16                  | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| W2 / C20                | PD3<br>F_AD3  | Note 1<br>Note 2           | TFTD9                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| W3 / D20                | PD2<br>F_AD2  | Note 1<br>Note 2           | TFTD8                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| Y1 / A21                | PD1<br>F_AD1  | Note 1<br>Note 2           | TFTD7                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| Y3 / B21                | INIT#<br>SMI_O  | Note 1<br>Note 2           | TFTD5                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AA1 / C21               | PD0<br>F_AD0  | Note 1<br>Note 2           | TFTD6                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AA3 / D21               | ERR#<br>F_C/BE0#  | Note 1<br>Note 2           | TFTD4                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AB1 / A22               | STB#/WRITE#<br>F_FRAME#   | Note 1<br>Note 2           | TFTD17                  | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AB2 / D22               | AFD#/DSTRB#<br>INTR_O   | Note 1<br>Note 2           | TFTD2                   | Note 1                     |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AJ13 / N31              | AB1C  | None                       | GPIO20<br>DOCCS#        | PMR[7] = 0<br>PMR[7] = 1   |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AL12 / N30              | AB1D  | None                       | GPIO1<br>IOCS1#         | PMR[13] = 0<br>PMR[13] = 1 |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| AL16 / V30              | GXCLK<br>TEST3  | PMR[29] = 0<br>PMR[29] = 1 | FP_VDD_ON               | None                       |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |
| 22                      | <p><b>RSVD (Reserved).</b> Must be set equal to PMR[14] (LPCSEL). The LPC_ROM strap (EBGA ball E4 / TEPBGA ball D6) determines the power-on reset (POR) state of PMR[14] and PMR[22].</p>   |                            |                         |                            |                |                    |          |                 |                            |        |      |         |                  |                          |       |      |          |                  |                          |        |      |          |                        |                  |       |      |          |                |                  |        |        |          |                  |                  |        |        |          |              |                  |        |        |          |                 |                  |       |        |          |              |                  |        |        |          |              |                  |        |        |          |              |                  |       |        |          |                         |                  |        |        |          |              |                  |       |        |          |              |                  |       |        |          |              |                  |       |        |          |                |                  |       |        |           |              |                  |       |        |           |                  |                  |       |        |           |                         |                  |        |      |           |                       |                  |       |        |            |      |      |                  |                          |            |      |      |                 |                            |            |                |                            |           |      |

Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)

| Bit           | Description  |                         |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|---------------|--|-------------------------|------------------------|-------------------------|---------------|------|--------------------|------------|--------|-------------|------------|------------|-------------|------------|------------|-------------|------------|-----------|-------------|------------|------------|-------------|-----------|--------|-------------|-----------|--------------|-------------|-----------|--------|-------------|
| 21            | <p><b>IOCSSEL (Select I/O Commands).</b> Selects ball functions.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: I/O Command Signals</th> <th>1: GPIO Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td rowspan="2">F1 / D9</td> <td>IOR#</td> <td>PMR[2] = 0</td> </tr> <tr> <td>DOCR#</td> <td>PMR[2] = 1</td> </tr> <tr> <td rowspan="2">G3 / A8</td> <td>IOW#</td> <td>PMR[2] = 0</td> </tr> <tr> <td>DOCW#</td> <td>PMR[2] = 1</td> </tr> </tbody> </table>   | Ball #                  | 0: I/O Command Signals | 1: GPIO Signals         | EBGA / TEPBGA | Name | Add'l Dependencies | F1 / D9    | IOR#   | PMR[2] = 0  | DOCR#      | PMR[2] = 1 | G3 / A8     | IOW#       | PMR[2] = 0 | DOCW#       | PMR[2] = 1 |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| Ball #        | 0: I/O Command Signals   | 1: GPIO Signals         |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| F1 / D9       | IOR#   | PMR[2] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | DOCR#  | PMR[2] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| G3 / A8       | IOW#   | PMR[2] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | DOCW#  | PMR[2] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 20            | <b>Reserved.</b> Must be set to 0.   |                         |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 19            | <p><b>AB2SEL (Select ACCESS.bus 2).</b> Selects ball functions.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO Signals</th> <th>1: ACCESS.bus 2 Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>AJ12 / N29</td> <td>GPIO12</td> <td>None</td> </tr> <tr> <td>AL11 / M29</td> <td>GPIO13</td> <td>None</td> </tr> </tbody> </table>   | Ball #                  | 0: GPIO Signals        | 1: ACCESS.bus 2 Signals | EBGA / TEPBGA | Name | Add'l Dependencies | AJ12 / N29 | GPIO12 | None        | AL11 / M29 | GPIO13     | None        |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| Ball #        | 0: GPIO Signals  | 1: ACCESS.bus 2 Signals |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ12 / N29    | GPIO12   | None                    |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AL11 / M29    | GPIO13   | None                    |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 18            | <p><b>SP2SEL (Select SP2 Additional Pins).</b> Selects ball functions.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO, IDE Signals</th> <th>1: Serial Port Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td rowspan="2">AH3 / D28</td> <td>GPIO6</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IDE_IOR1#</td> <td>PMR[8] = 1</td> </tr> <tr> <td rowspan="2">AG4 / C28</td> <td>GPIO9</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IDE_IOW1#</td> <td>PMR[8] = 1</td> </tr> <tr> <td rowspan="2">AJ1 / B29</td> <td>GPIO10</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IDE_IORDY1</td> <td>PMR[8] = 1</td> </tr> <tr> <td rowspan="2">H30 / AJ8</td> <td>GPIO11</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IRQ15</td> <td>PMR[8] = 1</td> </tr> </tbody> </table>   | Ball #                  | 0: GPIO, IDE Signals   | 1: Serial Port Signals  | EBGA / TEPBGA | Name | Add'l Dependencies | AH3 / D28  | GPIO6  | PMR[8] = 0  | IDE_IOR1#  | PMR[8] = 1 | AG4 / C28   | GPIO9      | PMR[8] = 0 | IDE_IOW1#   | PMR[8] = 1 | AJ1 / B29 | GPIO10      | PMR[8] = 0 | IDE_IORDY1 | PMR[8] = 1  | H30 / AJ8 | GPIO11 | PMR[8] = 0  | IRQ15     | PMR[8] = 1   |             |           |        |             |
| Ball #        | 0: GPIO, IDE Signals   | 1: Serial Port Signals  |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AH3 / D28     | GPIO6  | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IDE_IOR1#  | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AG4 / C28     | GPIO9  | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IDE_IOW1#  | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ1 / B29     | GPIO10   | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IDE_IORDY1   | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| H30 / AJ8     | GPIO11   | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IRQ15  | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 17            | <p><b>SP2CRSEL (Select SP2 Flow Control).</b> Selects ball functions.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO, IDE Signals</th> <th>1: Serial Port Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td rowspan="2">AH4 / C30</td> <td>GPIO7</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IDE_DACK1#</td> <td>PMR[8] = 1</td> </tr> <tr> <td rowspan="2">AJ2 / C31</td> <td>GPIO8</td> <td>PMR[8] = 0</td> </tr> <tr> <td>IDE_DREQ1</td> <td>PMR[8] = 1</td> </tr> </tbody> </table>  | Ball #                  | 0: GPIO, IDE Signals   | 1: Serial Port Signals  | EBGA / TEPBGA | Name | Add'l Dependencies | AH4 / C30  | GPIO7  | PMR[8] = 0  | IDE_DACK1# | PMR[8] = 1 | AJ2 / C31   | GPIO8      | PMR[8] = 0 | IDE_DREQ1   | PMR[8] = 1 |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| Ball #        | 0: GPIO, IDE Signals   | 1: Serial Port Signals  |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AH4 / C30     | GPIO7  | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IDE_DACK1#   | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ2 / C31     | GPIO8  | PMR[8] = 0              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
|               | IDE_DREQ1  | PMR[8] = 1              |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 16            | <p><b>SP1SEL (Select SP1 Additional Pin).</b> Selects ball function.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO Signal</th> <th>1: Serial Port Signal</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>A28 / AG1</td> <td>GPIO18</td> <td>None</td> </tr> </tbody> </table>   | Ball #                  | 0: GPIO Signal         | 1: Serial Port Signal   | EBGA / TEPBGA | Name | Add'l Dependencies | A28 / AG1  | GPIO18 | None        |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| Ball #        | 0: GPIO Signal   | 1: Serial Port Signal   |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| A28 / AG1     | GPIO18   | None                    |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 15            | <b>RSVD (Reserved).</b> Write to 0.  |                         |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 14            | <p><b>LPCSEL (Select LPC Bus).</b> Selects ball functions. The LPC_ROM strap (EBGA ball E4 / TEPBGA ball D6) determines the power-on reset (POR) state of PMR[14] and PMR[22].</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO Signals</th> <th>1: LPC Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Add'l Dependencies</th> </tr> </thead> <tbody> <tr> <td>AJ11 / M28</td> <td>GPIO32</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AL10 / L31</td> <td>GPIO33</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AK10 / L30</td> <td>GPIO34</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AJ10 / L29</td> <td>GPIO35</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AL9 / L28</td> <td>GPIO36</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AK9 / K31</td> <td>GPIO37</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AJ9 / K28</td> <td>GPIO38/IRRX2</td> <td>PMR[22] = 0</td> </tr> <tr> <td>AL8 / J31</td> <td>GPIO39</td> <td>PMR[22] = 0</td> </tr> </tbody> </table> | Ball #                  | 0: GPIO Signals        | 1: LPC Signals          | EBGA / TEPBGA | Name | Add'l Dependencies | AJ11 / M28 | GPIO32 | PMR[22] = 0 | AL10 / L31 | GPIO33     | PMR[22] = 0 | AK10 / L30 | GPIO34     | PMR[22] = 0 | AJ10 / L29 | GPIO35    | PMR[22] = 0 | AL9 / L28  | GPIO36     | PMR[22] = 0 | AK9 / K31 | GPIO37 | PMR[22] = 0 | AJ9 / K28 | GPIO38/IRRX2 | PMR[22] = 0 | AL8 / J31 | GPIO39 | PMR[22] = 0 |
| Ball #        | 0: GPIO Signals  | 1: LPC Signals          |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| EBGA / TEPBGA | Name   | Add'l Dependencies      |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ11 / M28    | GPIO32   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AL10 / L31    | GPIO33   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AK10 / L30    | GPIO34   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ10 / L29    | GPIO35   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AL9 / L28     | GPIO36   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AK9 / K31     | GPIO37   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AJ9 / K28     | GPIO38/IRRX2   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| AL8 / J31     | GPIO39   | PMR[22] = 0             |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |
| 13            | <p><b>IOCS1SEL (Select IOCS1).</b> Selects ball functions for IOCS1# or GPIO1. Works in conjunction with PMR[23], see PMR[23] for definition.</p>  |                         |                        |                         |               |      |                    |            |        |             |            |            |             |            |            |             |            |           |             |            |            |             |           |        |             |           |              |             |           |        |             |

Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)

| Bit  | Description   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|--|---|------------------------|---------------------|------------------------|---------------|------|------|------------|--------|---------|----------|--------------------|--------------------|--|--------------------|--------------------|--|-----------|-----------|--|--------------|--------------|
| 12   | <p><b>TRDESEL (Select TRDE#).</b> Selects ball function.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: Sub-ISA Signal</th> <th>1: GPIO Signal</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>H1 / D11</td> <td>TRDE#</td> <td>GPIO0</td> </tr> <tr> <td></td> <th>Add'l Dependencies</th> <th>Add'l Dependencies</th> </tr> <tr> <td></td> <td>None</td> <td>None</td> </tr> </tbody> </table>   | Ball #                 | 0: Sub-ISA Signal   | 1: GPIO Signal         | EBGA / TEPBGA | Name | Name | H1 / D11   | TRDE#  | GPIO0   |          | Add'l Dependencies | Add'l Dependencies |  | None               | None               |  |           |           |  |              |              |
| Ball #   | 0: Sub-ISA Signal   | 1: GPIO Signal         |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| EBGA / TEPBGA  | Name  | Name                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| H1 / D11   | TRDE#   | GPIO0                  |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | Add'l Dependencies  | Add'l Dependencies     |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | None  | None                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 11   | <p><b>EIDE (Enable IDE Outputs).</b> This bit enables IDE output signals.</p> <p>0: IDE signals are HiZ. Other signals multiplexed on the same balls are HiZ until this bit is set. (without regard to bit 24 of this register). This bit does not control IDE channel 1 control signals selected by bit 8 of this register.</p> <p>1: Signals are enabled.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 10   | <p><b>ETFT (Enable TFT Outputs).</b> This bit enables TFT output signals, that are multiplexed with the Parallel Port and controlled by PMR[23].</p> <p>0: Signals TFTD[17:0], TFTDE and TFTDCK are set to 0.</p> <p>1: Signals TFTD[17:0], TFTDE and TFTDCK are enabled.</p> <p><b>Note:</b> TFTDCK that is multiplexed on IDE_RST# (EBGA ball A22 / TEPBGA ball AA1) is also enabled by this bit.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 9  | <p><b>IOCHRDY (Select IOCHRDY).</b> Selects ball function.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: PCI, GPIO Signal</th> <th>1: Sub-ISA Signal</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>H4 / C9</td> <td>GPIO19</td> <td>IOCHRDY</td> </tr> <tr> <td></td> <th>Add'l Dependencies</th> <th>Add'l Dependencies</th> </tr> <tr> <td></td> <td>PMR[4] = 0</td> <td>PMR[4] = 1</td> </tr> <tr> <td></td> <td>INTC#</td> <td>Undefined</td> </tr> <tr> <td></td> <td>PMR[4] = 1</td> <td>PMR[4] = 0</td> </tr> </tbody> </table>            | Ball #                 | 0: PCI, GPIO Signal | 1: Sub-ISA Signal      | EBGA / TEPBGA | Name | Name | H4 / C9    | GPIO19 | IOCHRDY |          | Add'l Dependencies | Add'l Dependencies |  | PMR[4] = 0         | PMR[4] = 1         |  | INTC#     | Undefined |  | PMR[4] = 1   | PMR[4] = 0   |
| Ball #   | 0: PCI, GPIO Signal   | 1: Sub-ISA Signal      |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| EBGA / TEPBGA  | Name  | Name                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| H4 / C9  | GPIO19  | IOCHRDY                |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | Add'l Dependencies  | Add'l Dependencies     |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | PMR[4] = 0  | PMR[4] = 1             |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | INTC#   | Undefined              |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | PMR[4] = 1  | PMR[4] = 0             |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 8  | <p><b>IDE1SEL (Select IDE Channel 1).</b> Selects IDE Channel 1 or GPIO ball functions. Works in conjunction with PMR[18] and PMR[17], see PMR[18] and PMR[17] for definitions.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 7  | <p><b>DOCCSEL (Select DOCCS#).</b> Selects DOCCS# or GPIO20 ball functions. Works in conjunction with PMR[23], see PMR[23] for definition.</p>  |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 6  | <p><b>SP3SEL (Select UART3).</b> Selects ball functions.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: IR Signals</th> <th>1: Serial Port Signals</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>J28 / AK8</td> <td>IRRX1</td> <td>SIN3</td> </tr> <tr> <td>J3 / C11</td> <td>IRTX</td> <td>SOUT3</td> </tr> <tr> <td></td> <th>Add'l Dependencies</th> <th>Add'l Dependencies</th> </tr> <tr> <td></td> <td>None</td> <td>None</td> </tr> <tr> <td></td> <td>None</td> <td>None</td> </tr> </tbody> </table>                                      | Ball #                 | 0: IR Signals       | 1: Serial Port Signals | EBGA / TEPBGA | Name | Name | J28 / AK8  | IRRX1  | SIN3    | J3 / C11 | IRTX               | SOUT3              |  | Add'l Dependencies | Add'l Dependencies |  | None      | None      |  | None         | None         |
| Ball #   | 0: IR Signals   | 1: Serial Port Signals |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| EBGA / TEPBGA  | Name  | Name                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| J28 / AK8  | IRRX1   | SIN3                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| J3 / C11   | IRTX  | SOUT3                  |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | Add'l Dependencies  | Add'l Dependencies     |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | None  | None                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | None  | None                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 5  | <p><b>IOCS0SEL (Select IOCS0#).</b> Selects ball function. Works in conjunction with PMR[23], see PMR[23] for definition.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 4  | <p><b>INTCSEL (Select INTC#).</b> Selects ball function. Works in conjunction with PMR[9], see PMR[9] for definition.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 3  | <p><b>Reserved.</b> Write as read.</p>  |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 2  | <p><b>DOCWRSEL (Select DiskOnChip and NAND Flash Command Lines).</b> Selects ball functions. Works in conjunction with PMR[21], see PMR[21] for definition.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 1  | <p><b>Reserved.</b> Write as read.</p>  |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 0  | <p><b>PCBEEPSEL (Select PC_BEEP).</b> Selects ball function.</p> <table border="1"> <thead> <tr> <th>Ball #</th> <th>0: GPIO Signal</th> <th>1: Audio Signal</th> </tr> <tr> <th>EBGA / TEPBGA</th> <th>Name</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>AL15 / V31</td> <td>GPIO16</td> <td>PC_BEEP</td> </tr> <tr> <td></td> <th>Add'l Dependencies</th> <th>Add'l Dependencies</th> </tr> <tr> <td></td> <td>FPCI_MON = 0</td> <td>FPCI_MON] = 0</td> </tr> <tr> <td></td> <td>F_DEVSEL#</td> <td>F_DEVSEL#</td> </tr> <tr> <td></td> <td>FPCI_MON = 1</td> <td>FPCI_MON = 1</td> </tr> </tbody> </table> | Ball #                 | 0: GPIO Signal      | 1: Audio Signal        | EBGA / TEPBGA | Name | Name | AL15 / V31 | GPIO16 | PC_BEEP |          | Add'l Dependencies | Add'l Dependencies |  | FPCI_MON = 0       | FPCI_MON] = 0      |  | F_DEVSEL# | F_DEVSEL# |  | FPCI_MON = 1 | FPCI_MON = 1 |
| Ball #   | 0: GPIO Signal  | 1: Audio Signal        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| EBGA / TEPBGA  | Name  | Name                   |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| AL15 / V31   | GPIO16  | PC_BEEP                |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | Add'l Dependencies  | Add'l Dependencies     |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | FPCI_MON = 0  | FPCI_MON] = 0          |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | F_DEVSEL#   | F_DEVSEL#              |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
|  | FPCI_MON = 1  | FPCI_MON = 1           |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| <p><b>Offset 34h-37h</b> <b>Miscellaneous Configuration Register - MCR (R/W)</b> <b>Reset Value: 000001h</b></p> <p>Power-on reset value: The BOOT16 strap pin selects "Enable 16-Bit Wide Boot Memory".</p> |   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 31   | <p><b>DID0 (EBGA Ball D4 / TEPBGA Ball C5) Strap Status. (Read Only)</b> Represents the value of the strap that is latched after power-on reset. Read in conjunction with bit 29.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 30   | <p><b>FPCI_MON (EBGA Ball D3 / TEPBGA Ball A4) Strap Status. (Read Only)</b> Represents the value of the strap that is latched after power-on reset. Indicates if Fast-PCI monitoring output signals (instead of Parallel Port and some audio signals) are enabled. The state of this bit along with PMR[27] control the Fast-PCI monitoring function. See PMR[27] definition.</p>  |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 29   | <p><b>DID1 (EBGA Ball D2 / TEPBGA Ball C6) Strap Status. (Read Only)</b> Represents the value of the strap that is latched after power-on reset. Read in conjunction with bit 31.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 28:20  | <p><b>Reserved.</b></p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 19:18  | <p><b>Reserved.</b> Write as 0.</p>   |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |
| 17   | <p><b>HSYNC Timing.</b> HSYNC timing control for TFT.</p> <p>0: Reserved.</p> <p>1: HSYNC timing suited for TFT.</p>  |                        |                     |                        |               |      |      |            |        |         |          |                    |                    |  |                    |                    |  |           |           |  |              |              |

**Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)**

| Bit | Description  |
|-----|--|
| 16  | <b>Delay HSYNC.</b> HSYNC delay by two TFT clock cycles.<br>0: There is no delay on HSYNC.<br>1: HYSNC is delayed twice by rising edge of TFT clock. Enables delay between VSYNC and HSYNC suited for TFT display.   |
| 15  | <b>Reserved.</b> Write as read.  |
| 14  | <b>IBUS16 (Invert BUS16).</b> This bit inverts the meaning of MCR[3] (bit 3 of this register).<br>0: BUS16 is as described for MCR[3].<br>1: BUS16 meaning is inverted: if MCR[3] = 0, ROMCS# access is 16 bits wide; if MCR[3] = 1, ROMCS# access is 8 bits wide.   |
| 13  | <b>Reserved.</b> Must be set to 0.   |
| 12  | <b>IO1ZWS (Enable ZWS# for IOCS1# Access).</b> This bit enables internal activation of ZWS# (Zero Wait States) control for IOCS1# access.<br>0: ZWS# is not active for IOCS1# access.<br>1: ZWS# is active for IOCS1# access.  |
| 11  | <b>IO0ZWS (Enable ZWS# for IOCS0# Access).</b> This bit enables internal activation of ZWS# (Zero Wait States) control for IOCS0# access.<br>0: ZWS# is not active for IOCS0# access.<br>1: ZWS# is active for IOCS0# access.  |
| 10  | <b>DOCZWS (Enable ZWS# for DOCCS# Access).</b> This bit enables internal activation of ZWS# (Zero Wait States) control for DOCCS# access.<br>0: ZWS# is not active for DOCCS# access.<br>1: ZWS# is active for DOCCS# access.  |
| 9   | <b>ROMZWS (Enable ZWS# for ROMCS# Access).</b> This bit enables internal activation of ZWS# (Zero Wait States) control for ROMCS# access.<br>0: ZWS# is not active for ROMCS# access.<br>1: ZWS# is active for ROMCS# access.  |
| 8   | <b>IO1_16 (Enable 16-Bit Wide IOCS1# Access).</b> This bit enables the 16-line access to IOCS1# in the Sub-ISA interface.<br>0: 8-bit wide IOCS1# access is used.<br>1: 16-bit wide IOCS1# access is used.   |
| 7   | <b>IO0_16 (Enable 16-Bit Wide IOCS0# Access).</b> This bit enables the 16-line access to IOCS0# in the Sub-ISA interface.<br>0: 8-bit wide IOCS0# access is used.<br>1: 16-bit wide IOCS0# access is used.   |
| 6   | <b>DOC16 (Enable 16-Bit Wide DOCCS# Access).</b> This bit enables the 16-line access to DOCCS# in the Sub-ISA interface.<br>0: 8-bit wide DOCCS# access is used.<br>1: 16-bit wide DOCCS# access is used.  |
| 5   | <b>Reserved.</b> Write as read.  |
| 4   | <b>IRTXEN (Infrared Transmitter Enable).</b> This bit enables drive of Infrared transmitter output.<br>0: IRTX+SOUT3 line (EBGA ball J3 / TEPBGA ball C11) is HiZ.<br>1: IRTX+SOUT3 line (EBGA ball J3 / TEPBGA ball C11) is enabled.  |
| 3   | <b>BUS16 (16-Bit Wide Boot Memory). (Read Only)</b> This bit reports the status of the BOOT16 strap (EBGA ball G4 / TEPBGA ball C8). If the BOOT16 strap is pulled high, at reset 16-bit access to ROM in the Sub-ISA interface is enabled. MCR[14] = 1 inverts the meaning of this register.<br>0: 8-bit wide ROM.<br>1: 16-bit wide ROM. |
| 2:1 | <b>Reserved.</b> Write as read.  |

**Table 4-2. Multiplexing, Interrupt Selection, and Base Address Registers (Continued)**

| Bit   | Description   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
|---|---|---------------|----------------|-------------|-------------|------------|------------|------------|----------------|----------------|------------|-------------|-------------|------------|------------|-------------|-------------|
| 0   | <p><b>SDBE0 (Slave Disconnect Boundary Enable).</b> Works in conjunction with the GX1 module's PCI Control Function 2 Register (Index 41h), bit 1 (SDBE1). Sets boundaries for when the GX1 module is a PCI slave.</p> <p>SDBE[1:0]</p> <p>00: Read and Write disconnect on boundaries set by bits [3:2] of the GX1 module's PCI Control Function 2 register (Index 41h).</p> <p>01: Write disconnects on boundaries set by bits [3:2] of the GX1 module's PCI Control Function 2 register. Read disconnects on cache line boundary of 16 bytes.</p> <p>1x: Read and Write disconnect on cache line boundary of 16 bytes.</p> <p>This bit is reset to 1.</p> <p>All PCI bus masters (including SC3200's on-chip PCI bus masters, e.g., the USB Controller) must be disabled while modifying this bit. When accessing this register while any PCI bus master is enabled, use read-modify-write to ensure these bit contents are unchanged.</p> |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Offset 38h</b> <b>Interrupt Selection Register - INTSEL (R/W)</b> <b>Reset Value: 00h</b></p> <p>This register selects the IRQ signal of the combined WATCHDOG and High-Resolution timer interrupt. This interrupt is shareable with other interrupt sources.</p> |   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 7:4   | <b>Reserved.</b> Write as read.   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 3:0   | <p><b>CBIRQ.</b> Configuration Block Interrupt.</p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: IRQ8#</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: Reserved</td> </tr> <tr> <td>0010: Reserved</td> <td>0110: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0111: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table>  | 0000: Disable | 0100: IRQ4     | 1000: IRQ8# | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: Reserved | 0010: Reserved | 0110: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0111: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable   | 0100: IRQ4  | 1000: IRQ8#   | 1100: IRQ12    |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0001: IRQ1  | 0101: IRQ5  | 1001: IRQ9    | 1101: Reserved |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0010: Reserved  | 0110: IRQ6  | 1010: IRQ10   | 1110: IRQ14    |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0011: IRQ3  | 0111: IRQ7  | 1011: IRQ11   | 1111: IRQ15    |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Offset 39h-3Bh</b> <b>Reserved - RSVD</b></p>   |   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Offset 3Ch</b> <b>Device Identification Number Register - ID (RO)</b> <b>Reset Value: xxh</b></p> <p>This register identifies the device. SC3200 = 04h.</p>   |   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Offset 3Dh</b> <b>Revision Register - REV (RO)</b> <b>Reset Value: xxh</b></p> <p>This register identifies the device revision. See the <i>AMD Geode™ SC3200 Specification Update</i> document for value.</p>   |   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Offset 3Eh-3Fh</b> <b>Configuration Base Address Register - CBA (RO)</b> <b>Reset Value: xxh</b></p> <p>This register sets the base address of the Configuration block.</p>   |   |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 15:6  | <b>Configuration Base Address.</b> These bits are the high bits of the Configuration Base Address.  |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 5:0   | <b>Configuration Base Address.</b> These bits are the low bits of the Configuration Base Address. These bits are set to 0.  |               |                |             |             |            |            |            |                |                |            |             |             |            |            |             |             |

### 4.3 WATCHDOG

The SC3200 includes a WATCHDOG function to serve as a fail-safe mechanism in case the system becomes hung. When triggered, the WATCHDOG mechanism returns the system to a known state by generating an interrupt, an SMI, or a system reset (depending on configuration).

#### 4.3.1 Functional Description

WATCHDOG is enabled when the WATCHDOG Timeout (WDTO) register (Offset 00h) is set to a non-zero value. The WATCHDOG timer starts with this value and counts down until either the count reaches 0, or a trigger event restarts the count (with the WDTO register value).

The WATCHDOG timer is restarted in any of the following cases:

- The WDTO register is set with a non-zero value.
- The WATCHDOG timer reaches 0 and the WATCHDOG Overflow bit, WDOVF (Offset 04h[0]), is 0.

The WATCHDOG function is disabled in any of the following cases:

- System reset occurs.
- The WDTO register is set to 0.
- The WDOVF bit is already 1 when the timer reaches 0.

##### 4.3.1.1 WATCHDOG Timer

The WATCHDOG timer is a 16-bit down counter. Its input clock is a 32 KHz clock divided by a predefined value (see WDPRES field, Offset 02h[3:0]). The 32 KHz input clock is enabled when either:

- The GX1 module's internal SUSPA# signal is 1.
- or
- The GX1 module's internal SUSPA# signal is 0 and the WD32KPD bit (Offset 02h[8]) is 0.

The 32 KHz input clock is disabled, when:

- The GX1 module's internal SUSPA# signal is 0 and the WD32KPD bit is 1.

For more information about signal SUSPA#, refer to the *AMD Geode™ GX1 Processor Data Book*.

When the WATCHDOG timer reaches 0:

- If the WDOVF bit in the WDSTS register (Offset 04h[0]) is 0, an interrupt, an SMI or a system reset is generated, depending on the value of the WDTYPE1 field in the WDCNFG register (Offset 02h[5:4]).
- If the WDOVF bit in the WDSTS register is already 1 when the WATCHDOG timer reaches 0, an interrupt, an SMI or a system reset is generated according to the WDTYPE2 field (Offset 02h[7:6]), and the timer is disabled. The WATCHDOG timer is re-enabled when a non-zero value is written to the WDTO register (Offset 00h).

The interrupt or SMI is de-asserted when the WDOVF bit is set to 0. The reset generated by the WATCHDOG function is used to trigger a system reset via the Core Logic module. The value of the WDOVF bit, the WDTYPE1 field, and the WDTYPE2 field are not affected by a system reset (except when generated by power-on reset).

The SC3200 also allows no action to be taken when the timer reaches 0 (according to WDTYPE1 field and WDTYPE2 field). In this case only the WDOVF bit is set to 1.

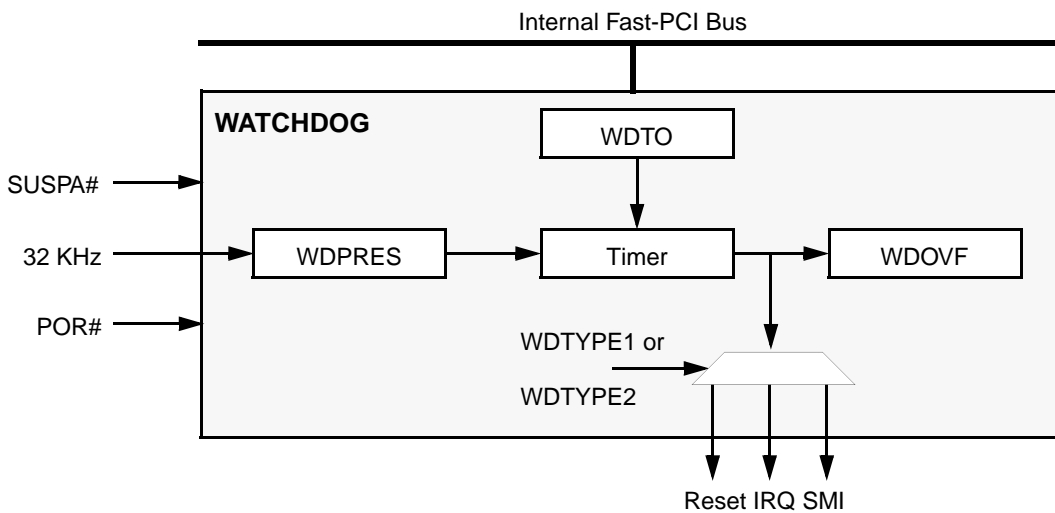


Figure 4-1. WATCHDOG Block Diagram

### WATCHDOG Interrupt

The WATCHDOG interrupt (if configured and enabled) is routed to an IRQ signal. The IRQ signal is programmable via the INTSEL register (Offset 38h, described in Table 4-2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88). The WATCHDOG interrupt is a shareable, active low, level interrupt.

### WATCHDOG SMI

The WATCHDOG SMI is recognized by the Core Logic module as internal input signal EXT\_SMI0#. To use the WATCHDOG SMI, Core Logic registers must be configured appropriately.

### 4.3.2 WATCHDOG Registers

Table 4-3 describes the WATCHDOG registers.

#### 4.3.2.1 Usage Hints

- SMM code should set bit 8 of the WDCNFG register to 1 when entering ACPI C3 state, if the WATCHDOG timer is to be suspended. If this is not done, the WATCHDOG timer is functional during C3 state.
- SMM code should set bit 8 of the WDCNFG register to 1, when entering ACPI S1 and S2 states if the WATCHDOG timer is to be suspended. If this is not done, the WATCHDOG timer is functional during S1 and S2 states.

**Table 4-3. WATCHDOG Registers**

| Bit  | Description   |
|--|---|
| <b>Offset 00h-01h</b> <b>WATCHDOG Timeout Register - WDTO (R/W)</b> <b>Reset Value: 0000h</b>  |   |
| This register specifies the programmed WATCHDOG timeout period.  |   |
| 15:0   | <b>Programmed timeout period.</b>   |
| <b>Offset 02h-03h</b> <b>WATCHDOG Configuration Register - WDCNFG (R/W)</b> <b>Reset Value: 0000h</b>  |   |
| This register selects the signal to be generated when the timer reaches 0, whether or not to disable the 32 KHz input clock during low power states, and the prescaler value of the clock input. |   |
| 15:9   | <b>Reserved.</b> Write as read.   |
| 8  | <b>WD32KPD (WATCHDOG 32 KHz Power Down).</b><br>0: 32 KHz clock is enabled.<br>1: 32 KHz clock is disabled, when the GX1 module asserts its internal SUSPA# signal.<br>This bit is cleared to 0, when POR# is asserted or when the GX1 module de-asserts its internal SUSPA# signal (i.e., on SUSPA# rising edge). See Section 4.3.2.1 "Usage Hints" on page 96.            |
| 7:6  | <b>WDTYPE2 (WATCHDOG Event Type 2).</b><br>00: No action<br>01: Interrupt<br>10: SMI<br>11: System reset<br>This field is reset to 0 when POR# is asserted. Other system resets do not affect this field.   |
| 5:4  | <b>WDTYPE1 (WATCHDOG Event Type 1).</b><br>00: No action<br>01: Interrupt<br>10: SMI<br>11: System reset<br>This field is reset to 0 when POR# is asserted. Other system resets do not affect this field.   |
| 3:0  | <b>WDPRES (WATCHDOG Timer Prescaler).</b> Divide 32 KHz by:<br>0000: 1            0100: 16            1000: 256            1100: 4096<br>0001: 2            0101: 32            1001: 512            1101: 8192<br>0010: 4            0110: 64            1010: 1024           1110: Reserved<br>0011: 8            0111: 128           1011: 2048           1111: Reserved |



Table 4-3. WATCHDOG Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 04h</b> <b>WATCHDOG Status Register - WDSTS (R/WC)</b> <b>Reset Value: 00h</b> |  |
| This register contains WATCHDOG status information.                                      |  |
| 7:4  | <b>Reserved.</b> Write as read.  |
| 3  | <b>WDRST (WATCHDOG Reset Asserted). (Read Only)</b> This bit is set to 1 when WATCHDOG Reset is asserted. It is set to 0 when POR# is asserted, or when the WDOVF bit is set to 0.   |
| 2  | <b>WDSMI (WATCHDOG SMI Asserted). (Read Only)</b> This bit is set to 1 when WATCHDOG SMI is asserted. It is set to 0 when POR# is asserted, or when the WDOVF bit is set to 0.   |
| 1  | <b>WDINT (WATCHDOG Interrupt Asserted). (Read Only)</b> This bit is set to 1 when the WATCHDOG Interrupt is asserted. It is set to 0 when POR# is asserted, or when the WDOVF bit is set to 0.                                     |
| 0  | <b>WDOVF (WATCHDOG Overflow).</b> This bit is set to 1 when the WATCHDOG Timer reaches 0. It is set to 0 when POR# is asserted, or when a 1 is written to this bit by software. Other system reset sources do not affect this bit. |
| <b>Offset 05h-07h</b> <b>Reserved - RSVD</b>   |  |

## 4.4 High-Resolution Timer

The SC3200 provides an accurate time value that can be used as a time stamp by system software. This time is called the High-Resolution Timer. The length of the timer value can be extended via software. It is normally enabled while the system is in the C0 and C1 states. Optionally, software can be programmed to enable use of the High-Resolution Timer during C3 state and/or S1 state as well. In all other power states the High-Resolution Timer is disabled.

### 4.4.1 Functional Description

The High-Resolution Timer is a 32-bit free-running count-up timer that uses the oscillator clock or the oscillator clock divided by 27. Bit TMCLKSEL of the TMCNFG register (Offset 0Dh[1]) can be set via software to determine which clock should be used for the High-Resolution Timer.

When the most significant bit (bit 31) of the timer changes from 1 to 0, bit TMSTS of the TMSTS register (Offset 0Ch[0]) is set to 1. When both bit TMSTS and bit TMEN (Offset 0Dh[0]) are 1, an interrupt is asserted. Otherwise, the interrupt is de-asserted. This interrupt enables software emulation of a larger timer.

The High-Resolution Timer interrupt is routed to an IRQ signal. The IRQ signal is programmable via the INTSEL register (Offset 38h). For more information about this register, see section Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88.

System software uses the read-only TMVALUE register (Offset 08h[31:0]) to read the current value of the timer. The TMVALUE register has no default value.

The input clock (derived from the 27 MHz crystal oscillator) is enabled when:

- The GX1 module's internal SUSPA# signal is 1.

or

- The GX1 module's internal SUSPA# signal is 0 and bit TM27MPD (Offset 0Dh[2]) is 0.

The input clock is disabled, when the GX1 module's internal SUSPA# signal is 0 and the TM27MPD bit is 1.

For more information about signal SUSPA# see Section 4.4.2.1 "Usage Hints" on page 97 and the *AMD Geode™ GX1 Processor Data Book*.

The High-Resolution Timer function resides on the internal Fast-PCI bus and its registers are in General Configuration Block address space. Only one complete register should be accessed at-a-time (e.g., DWORD access should be used for DWORD wide registers and byte access should be used for byte-wide registers).

### 4.4.2 High-Resolution Timer Registers

Table 4-4 on page 98 describes the registers for the High-Resolution Timer (TIMER).

#### 4.4.2.1 Usage Hints

- SMM code should set bit 2 of the TMCNFG register to 1 when entering ACPI C3 state if the High-Resolution Timer should be disabled. If this is not done, the High-Resolution Timer is functional during C3 state.
- SMM code should set bit 2 of the TMCNFG register to 1 when entering ACPI S1 state if the High-Resolution Timer should be disabled. If this is not done, the High-Resolution Timer is functional during S1 state.

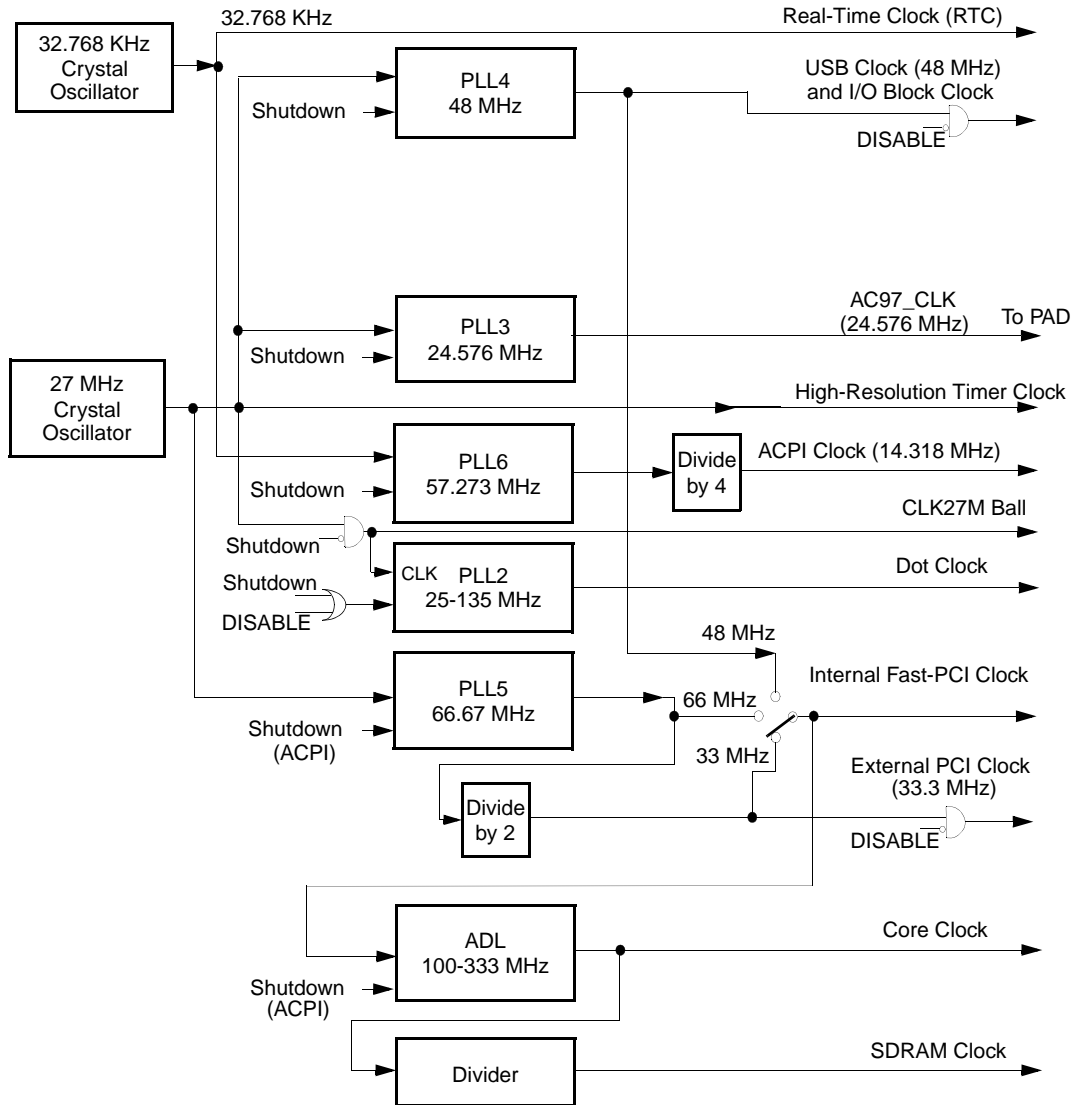
Table 4-4. High-Resolution Timer Registers

| Bit   | Description  |
|---|--|
| <b>Offset 08h-0Bh</b>   |  |
| <b>TIMER Value Register - TMVALUE (RO)</b>  |  |
| <b>Reset Value: xxxxxxxh</b>  |  |
| This register contains the current value of the High-Resolution Timer.  |  |
| 31:0  | <b>Current Timer Value.</b>  |
| <b>Offset 0Ch</b>   |  |
| <b>TIMER Status Register - TMSTS (R/W)</b>  |  |
| <b>Reset Value: 00h</b>   |  |
| This register supplies the High-Resolution Timer status information.  |  |
| 7:1   | <b>Reserved.</b>   |
| 0   | <b>TMSTS (TIMER Status).</b> This bit is set to 1 when the most significant bit (bit 31) of the timer changes from 1 to 0. It is cleared to 0 upon system reset or when 1 is written by software to this bit.  |
| <b>Offset 0Dh</b>   |  |
| <b>TIMER Configuration Register - TMCNFG (R/W)</b>  |  |
| <b>Reset Value: 00h</b>   |  |
| This register enables the High-Resolution Timer interrupt; selects the Timer clock; and disables the 27 MHz internal clock during low power states. |  |
| 7:3   | <b>Reserved.</b>   |
| 2   | <b>TM27MPD (TIMER 27 MHz Power Down).</b> This bit is cleared to 0 when POR# is asserted or when the GX1 module de-asserts its internal SUSPA# signal (i.e., on SUSPA# rising edge). See Section 4.4.2.1 "Usage Hints" on page 97.<br>0: 27 MHz input clock is enabled.<br>1: 27 MHz input clock is disabled when the GX1 module asserts its internal SUSPA# signal. |
| 1   | <b>TMCLKSEL (TIMER Clock Select).</b><br>0: Count-up timer uses the oscillator clock divided by 27.<br>1: Count-up timer uses the oscillator clock, 27 MHz clock.  |
| 0   | <b>TMEN (TIMER Interrupt Enable).</b><br>0: High-Resolution Timer interrupt is disabled.<br>1: High-Resolution Timer interrupt is enabled.   |
| <b>Offset 0Eh-0Fh</b>   |  |
| <b>Reserved - RSVD</b>  |  |

### 4.5 Clock Generators and PLLs

This section describes the registers for the clocks required by the GX1 module, Core Logic module, and the Video Processor, and how these clocks are generated. See Figure 4-2 for a clock generation diagram.

The clock generators are based on 32.768 KHz and 27.000 MHz crystal oscillators. The 32.768 KHz crystal oscillator is described in Section 5.5.2 "RTC Clock Generation" on page 121 (functional description of the RTC).



**Note:**  $V_{PLL2}$  powers PLL2 and PLL5.  $V_{PLL3}$  powers PLL3, PLL4, and PLL6.

**Figure 4-2. Clock Generation Block Diagram**

### 4.5.1 27 MHz Crystal Oscillator

The internal oscillator employs an external crystal connected to the on-chip amplifier. The on-chip amplifier is accessible on the X27I input and X27O output signals. See Figure 4-3 for the recommended external circuit and Table 4-5 for a list of the circuit components.

Choose  $C_1$  and  $C_2$  capacitors to match the crystal's load capacitance. The load capacitance  $C_L$  "seen" by crystal Y is comprised of  $C_1$  in series with  $C_2$  and in parallel with the parasitic capacitance of the circuit. The parasitic capacitance is caused by the chip package, board layout and socket (if any), and can vary from 0 to 10 pF. The rule of thumb in choosing these capacitors is:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{PARASITIC}$$

Example 1:

$$\begin{aligned} \text{Crystal } C_L &= 10 \text{ pF, } C_{PARASITIC} = 8.2 \text{ pF} \\ C_1 &= 3.6 \text{ pF, } C_2 = 3.6 \text{ pF} \end{aligned}$$

Example 2:

$$\begin{aligned} \text{Crystal } C_L &= 20 \text{ pF, } C_{PARASITIC} = 8 \text{ pF} \\ C_1 &= 24 \text{ pF, } C_2 = 24 \text{ pF} \end{aligned}$$

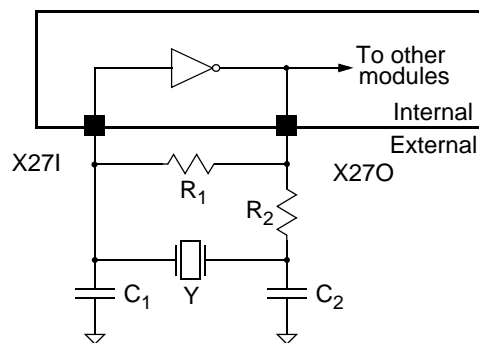


Figure 4-3. Recommended Oscillator External Circuitry

Table 4-5. Crystal Oscillator Circuit Components

| Component                    | Parameters              | Values                  | Tolerance        |
|------------------------------|-------------------------|-------------------------|------------------|
| Crystal                      | Resonance Frequency     | 27.00 MHz Parallel mode | 50 PPM or better |
|                              | Type                    | AT-cut or BT-cut        |                  |
|                              | Serial Resistance       | 40 $\Omega$             | Max              |
|                              | Shunt Capacitance       | 7 pF                    | Max              |
|                              | Load Capacitance, $C_L$ | 10-20 pF                |                  |
|                              | Temperature Coefficient | User-defined            |                  |
| Resistor $R_1$               | Resistance              | 20 M $\Omega$           | 5%               |
| Resistor $R_2$ <sup>1</sup>  | Resistance              | 100 $\Omega$            | 5%               |
| Capacitor $C_1$ <sup>1</sup> | Capacitance             | 3-24 pF                 | 5%               |
| Capacitor $C_2$ <sup>1</sup> | Capacitance             | 3-24 pF                 | 5%               |

1. The value of these components is recommended. It should be tuned according to crystal and board parameters.

#### 4.5.2 GX1 Module Core Clock

The core clock is generated by an Analog Delay Loop (ADL) clock generator from the internal Fast-PCI clock. The clock can be any whole-number multiple of the input clock between 4 and 10. Possible values are listed in Table 4-6.

At power-on reset, the core clock multiplier value is set according to the value of four strapped balls - CLKSEL[3:0] (EBGA balls AL13, AK3, B27, F3 / TEPBGA balls P30, D29, AF3, B8). These balls also select the clock which is used as input to the multiplier, as shown in Table 4-7.

#### 4.5.3 Internal Fast-PCI Clock

The internal Fast-PCI clock can be configured to 33, 48, or 66 MHz via strap options on the CLKSEL1 and CLKSEL0 balls. These can be read in the internal Fast-PCI Clock field in the CCFC register (GCB+I/O Offset 1Eh[9:8]). (See Table 4-8 on page 103 details on the CCFC register.)

**Table 4-6. Core Clock Frequency**

| ADL Multiplier Value | Internal Fast-PCI Clock Freq. (MHz) |     |       |
|----------------------|-------------------------------------|-----|-------|
|                      | 33.33                               | 48  | 66.67 |
| 4                    | 133.3                               | 192 | 266.7 |
| 5                    | 166.7                               | 240 | ---   |
| 6                    | 200                                 | 288 | ---   |
| 7                    | 233.3                               | --- | ---   |
| 8                    | 266.7                               | --- | ---   |
| 9                    | ---                                 | --- | ---   |
| 10                   | ---                                 | --- | ---   |

**Table 4-7. Strapped Core Clock Frequency**

| CLKSEL[3:0] Straps | Internal Fast-PCI Clock Freq. (MHz) (GCB+I/O Offset 1Eh[9:8]) | Default ADL Multiplier |  | Maximum Core Clock Freq. (MHz) |
|--------------------|---|------------------------|--|--------------------------------|
|                    |   | Multiply By            | Multiplier Value (GCB+I/O Offset 1Eh[3:0]) |                                |
| 0111               | 33.33   | 4                      | 0100                                       | 133                            |
| 1011               |   | 5                      | 0101                                       | 167                            |
| 1111               |   | 6                      | 0110                                       | 200                            |
| 0000               |   | 7                      | 0111                                       | 233                            |
| 0100               |   | 8                      | 1000                                       | 266                            |
| 1000               |   | 9                      | 1001                                       | Reserved                       |
| 1100               |   | 10                     | 1010                                       | Reserved                       |
| 0001               |   | 48                     | 4  | 0100                           |
| 0101               | 5   |                        | 0101                                       | 240                            |
| 1001               | 6   |                        | 0110                                       | 288                            |
| 1101               | 7   |                        | 0111                                       | Reserved                       |
| 0110               | 66.67   | 4                      | 0100                                       | 266                            |
| 1010               |   | 5                      | 0101                                       | Reserved                       |

**Note:** Not all speeds are supported. For information on supported speeds, see Section A.1 "Order Information" on page 443.

#### 4.5.4 SuperI/O Clocks

The SuperI/O module requires a 48 MHz input for Fast infrared (FIR), UART, and other functions. This clock is supplied by PLL4 using a multiplier value of 576/(108x3) to generate 48 MHz.

#### 4.5.5 Core Logic Module Clocks

The Core Logic module requires the following clock sources:

##### Real-Time Clock (RTC)

RTC requires a 32.768 KHz clock which is supplied directly from an internal low-power crystal oscillator. This oscillator uses battery power and has very low current consumption.

##### USB

The USB requires a 48 MHz input which is supplied by PLL4. The required total frequency accuracy and slow jitter for USB is 500 PPM; edge to edge jitter is  $\pm 1.2\%$ .

##### ACPI

The ACPI logic block uses a 14.32 MHz clock supplied by PLL6. PLL6 creates this clock from the 32.768 KHz clock, with a multiplier value of 6992/4 to output a 57.278 MHz clock that is divided by 4.

##### External PCI

The PCI Interface uses a 33.3 MHz clock that is created by PLL5 and divided by 2. PLL5 uses the 27 MHz clock, to output a 66.67 MHz clock. PLL5 has a frequency accuracy of  $\pm 0.1\%$ .

##### AC97

The SC3200 generates the 24.576 MHz clock required by the audio codec. Therefore, no crystal need be included for the audio codec on the system board.

PLL3 uses the crystal oscillator clock, to generate a 24.576 MHz clock. This clock is driven on the AC97\_CLK ball. The accuracy of the clock supplied by the SC3200 is 50 PPM.

#### 4.5.6 Video Processor Clocks

The Video processor requires the following clock sources:

##### Dot

The Dot clock is generated by PLL2. It is supplied to the Display Controller in the GX1 module (DCLK) that creates the pixel information, and is returned to the Graphics block (PCLK) with this information. PLL2 uses the 27 MHz clock to generate the Dot clock.

##### Video

The Video clock source depends on the source of the video data.

- If the video data is coming from the GX1 module (Capture Video mode), the video clock is generated by the Display Controller.
- If the video data is coming directly from the VIP block (Direct Video mode), the Video Clock is generated by the VIP block.

### 4.5.7 Clock Registers

Table 4-8 describes the registers of the clock generator and PLL.

**Table 4-8. Clock Generator Configuration**

| Bit   | Description   |
|---|---|
| <b>Offset 10h</b> <b>Maximum Core Clock Multiplier Register - MCCM (RO)</b> <b>Reset Value: Strapped Value</b>  |   |
| This register holds the maximum core clock multiplier value. The maximum clock frequency allowed by the core, is the Fast-PCI clock multiplied by this value. |   |
| 7:4   | <b>Reserved.</b>  |
| 3:0   | <b>MCM (Maximum Clock Multiplier).</b> This 4-bit value is the maximum multiplier value allowed for the core clock generator. It is derived from strap pins CLKSEL[3:0] based on the multiplier value in Table 4-7 on page 101. |
| <b>Offset 11h</b> <b>Reserved - RSVD</b>  |   |
| <b>Offset 12h</b> <b>PLL Power Control Register - PPCR (R/W)</b> <b>Reset Value: 2Fh</b>  |   |
| This register controls operation of the PLLs.   |   |
| 7   | <b>Reserved.</b>  |
| 6   | <b>EXPCID (Disable External PCI Clock).</b><br>0: External PCI clock is enabled.<br>1: External PCI clock is disabled.  |
| 5   | <b>GPD (Disable Graphic Pixel Reference Clock).</b><br>0: PLL2 input clock is enabled.<br>1: PLL2 input clock is disabled.  |
| 4   | <b>Reserved.</b>  |
| 3   | <b>PLL3SD (Shut Down PLL3).</b> AC97 codec clock.<br>0: PLL3 is enabled.<br>1: PLL3 is shutdown.  |
| 2   | <b>FM1SD (Shut Down PLL4).</b><br>0: PLL4 is enabled.<br>1: PLL4 is shutdown, unless internal Fast-PCI clock is strapped to 48 MHz.   |
| 1   | <b>C48MD (Disable SuperI/O and USB Clock).</b><br>0: USB and SuperI/O clock is enabled.<br>1: USB and SuperI/O clock is disabled.   |
| 0   | <b>Reserved.</b> Write as read.   |
| <b>Offset 13h-17h</b> <b>Reserved - RSVD</b>  |   |
| <b>Offset 18h-1Bh</b> <b>PLL3 Configuration Register - PLL3C (R/W)</b> <b>Reset Value: E1040005h</b>  |   |
| 31:24   | <b>MFFC (MFF Counter Value).</b><br>$F_{vco} = OSCCLK * MFBC / (MFFC * MOC)$<br>OSCCLK = 27 MHz   |
| 23:19   | <b>Reserved.</b> Write as read.   |
| 18:8  | <b>MFBC (MFB Counter Value).</b><br>$F_{vco} = OSCCLK * MFBC / (MFFC * MOC)$<br>OSCCLK = 27 MHz<br><b>Note:</b> Bits 18, 9, and 8 cannot be changed. Bit 18 is always a 1; bits 9 and 8 are always 0.                           |
| 7   | <b>Reserved.</b> Write as read.   |
| 6   | <b>Reserved.</b> Must be set to 0.  |
| 5:0   | <b>MOC (MO Counter Value).</b><br>$F_{vco} = OSCCLK * MFBC / (MFFC * MOC)$<br>OSCCLK = 27 MHz   |

Table 4-8. Clock Generator Configuration (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 1Eh-1Fh</b>   |  |
| <b>Core Clock Frequency Control Register - CCFC (R/W)</b>                                       |  |
| <b>Reset Value: Strapped Value</b>  |  |
| This register controls the configuration of the core clock multiplier and the reference clocks. |  |
| 15:14   | <b>Reserved.</b>   |
| 13  | <b>Reserved.</b> Must be set to 0.   |
| 12  | <b>Reserved.</b> Must be set to 0.   |
| 11:10   | <b>Reserved.</b>   |
| 9:8   | <b>FPCICK (Internal Fast-PCI Clock). (Read Only)</b> Reflects the internal Fast-PCI clock and is the input to the GX1 module that is used to generate the core clock. These bits reflect the value of strap pins CLKSEL[1:0].<br>00: 33.3 MHz<br>01: 48 MHz<br>10: 66.7 MHz<br>11: 33.3 MHz  |
| 7:4   | <b>Reserved.</b>   |
| 3:0   | <b>MVAL (Multiplier Value).</b> This 4-bit value controls the multiplier in ADL. The value is set according to the Maximum Clock Multiplier bits of the MCCM register (Offset 10h). The multiplier value should never be written with a multiplier which is different from the multiplier indicated in the MCCM register.<br>0100: Multiply by 4<br>0101: Multiply by 5<br>0110: Multiply by 6<br>0111: Multiply by 7<br>1000: Multiply by 8<br>1001: Multiply by 9<br>1010: Multiply by 10<br>Other: Reserved |



# SuperI/O Module

The SuperI/O (SIO) module is a PC98 and ACPI compliant SIO that offers a single-cell solution to the most commonly used ISA peripherals.

The SIO module incorporates: two Serial Ports, an Infrared Communication Port that supports FIR, MIR, HP-SIR, Sharp-IR, and Consumer Electronics-IR, a full IEEE 1284 Parallel Port, two ACCESS.bus Interface (ACB) ports, System Wakeup Control (SWC), and a Real-Time Clock (RTC) that provides RTC timekeeping.

### Outstanding Features

- Full compatibility with ACPI Revision 1.0 requirements.
- System Wakeup Control powered by  $V_{SB}$ , generates power-up request and a PME (power management event) in response to SDATA\_IN2 (an audio codec), IRRX1 (a pre-programmed CEIR), or a RI2# (serial port ring indicate) event.
- Advanced RTC, Y2K compliant.

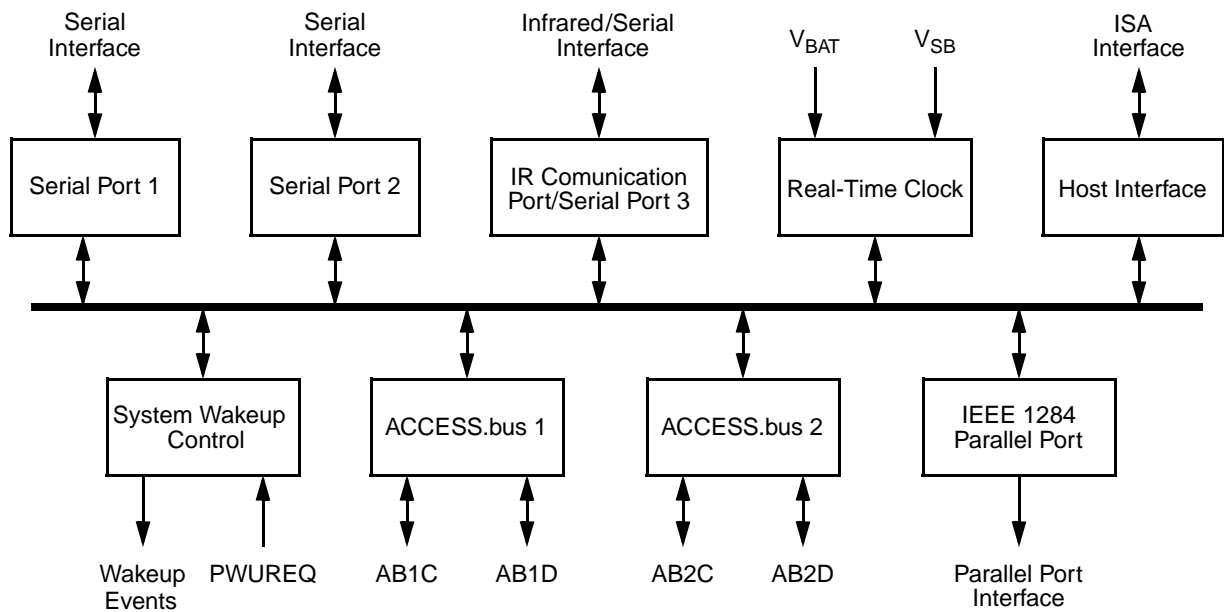


Figure 5-1. SIO Block Diagram

## 5.1 Features

### PC98 and ACPI Compliant

- PnP Configuration Register structure
- Flexible resource allocation for all logical devices:
  - Relocatable base address
  - 9 Parallel IRQ routing options
  - 3 optional 8-bit DMA channels (where applicable)

### Parallel Port

- Software or hardware control
- Enhanced Parallel Port (EPP) compatible with version EPP 1.9 and IEEE 1284 compliant
- EPP support for version EPP 1.7 of the Xircom specification
- EPP support as mode 4 of the Extended Capabilities Port (ECP)
- IEEE 1284 compliant ECP, including level 2
- Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
- PCI bus utilization reduction by supporting a demand DMA mode mechanism and a DMA fairness mechanism
- Protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages, even if the device is in power-down
- Output buffers that can sink and source 14 mA

### Serial Port 1

- 16550A compatible (SIN1, SOUT1, DTR1#/BOUT1 signals only)

### Serial Port 2

- 16550A compatible

### Serial Port 3 / Infrared (IR) Communication Port

- Serial Port 3
  - SIN and SOUT signals only
  - Data rate of up to 1.5-Mbps
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - DMA support
- IR Communication Port
  - IrDA 1.1 and 1.0 compatible
  - Data rate of up to 115.2 Kbps (HP-SIR)
  - Data rate of 1.152 Mbps (MIR)
  - Data rate of 4.0 Mbps (FIR)
  - Selectable internal or external modulation/demodulation (ASK-IR and DASK-IR options of SHARP-IR)
  - Consumer-IR (TV-Remote) mode
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - DMA support

### System Wakeup Control (SWC)

- Power-up request upon detection of RI2#, CEIR, or SDATA\_IN2 activity:
  - Optional routing of power-up request on IRQ line
- Pre-programmed CEIR address in a pre-selected standard (any NEC, RCA or RC-5)
- Powered by  $V_{SB}$
- Battery-backed wakeup setup
- Power-fail recovery support

### Real-Time Clock

- A modifiable address that is referenced by a 16-bit programmable register
- DS1287, MC146818 and PC87911 compatibility
- 242 bytes of battery backed up CMOS RAM in two banks
- Selective lock mechanisms for the CMOS RAM
- Battery backed up century calendar in days, day of the week, date of month, months, years and century, with automatic leap-year adjustment
- Battery backed-up time of day in seconds, minutes and hours that allows a 12 or 24 hour format and adjustments for daylight savings time
- BCD or binary format for time keeping
- Three different maskable interrupt flags:
  - Periodic interrupts - At intervals from 122 ms to 500 ms
  - Time-of-Month alarm - At intervals from once per second to once per month
  - Update Ended Interrupt - Once per second upon completion of update
- Separate battery pin, 3.0V operation that includes an internal UL protection resistor
- 7  $\mu$ A typical power consumption during power down
- Double-buffer time registers
- Y2K Compliant

### Clock Sources

- 48 MHz clock input
- On-chip low frequency clock generator for wakeup
- 32.768 KHz crystal with an internal frequency multiplier to generate all required internal frequencies

## 5.2 Module Architecture

The SIO module comprises a collection of generic functional blocks. Each functional block is described in detail later in this chapter. The beginning of this chapter describes the SIO structure and provides all device specific information, including special implementation of generic blocks, system interface and device configuration.

The SIO module is based on eight logical devices, the host interface, and a central configuration register set, all built around a central, internal 8-bit bus.

The host interface serves as a bridge between the external ISA interface and the internal bus. It supports 8-bit I/O read, 8-bit I/O write and 8-bit DMA transactions, as defined in *Personal Computer Bus Standard P996*.

The central configuration register set supports ACPI compliant PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard Registers, defined in Appendix A of the *Plug and Play ISA Specification Version 1.0a* by Intel and Microsoft®. All system resources assigned to the functional blocks (I/O address space, DMA channels and IRQ lines) are configured in, and managed by, the central configuration register set. In addition, some function-specific parameters are configurable through this unit and distributed to the functional blocks through special control signals.

The source of the device internal clocks is the 48 MHz clock signal or through the 32.768 KHz crystal with an internal frequency multiplier. RTC operates on a 32 KHz clock.

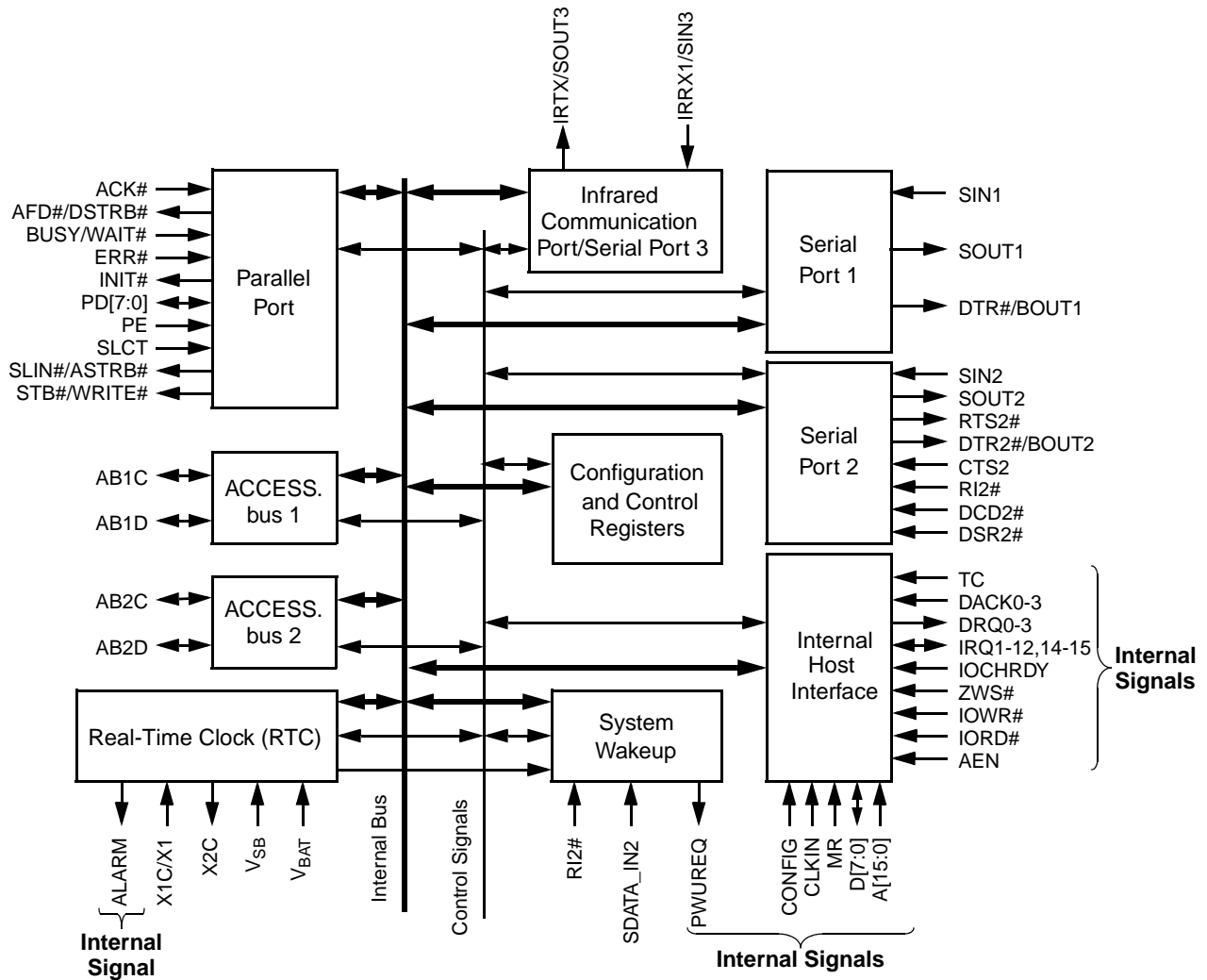


Figure 5-2. Detailed SIO Block Diagram

### 5.3 Configuration Structure / Access

This section describes the structure of the configuration register file, and the method of accessing the configuration registers.

#### 5.3.1 Index-Data Register Pair

The SIO configuration access is performed via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined according to the state of the IO\_SIOCFG\_IN bit field of the Core Logic module (F5BAR0+I/O Offset 00h[26:25]). Table 5-1 shows the selected base addresses as a function of the IO\_SIOCFG\_IN bit field.

**Table 5-1. SIO Configuration Options**

| IO_SIOCFG_IN Settings | I/O Address    |               | Description                   |
|-----------------------|----------------|---------------|-------------------------------|
|                       | Index Register | Data Register |                               |
| 00                    | -              | -             | SIO disabled                  |
| 01                    | -              | -             | Configuration access disabled |
| 10                    | 002Eh          | 002Fh         | Base address 1 selected       |
| 11                    | 015Ch          | 015Dh         | Base address 2 selected       |

The Index Register is an 8-bit R/W register located at the selected base address (Base+0). It is used as a pointer to the configuration register file, and holds the index of the configuration register that is currently accessible via the Data Register. Reading the Index Register returns the last value written to it (or the default of 00h after reset).

The Data Register is an 8-bit virtual register, used as a data path to any configuration register. Accessing the data register results with physically accessing the configuration register that is currently pointed by the Index Register.

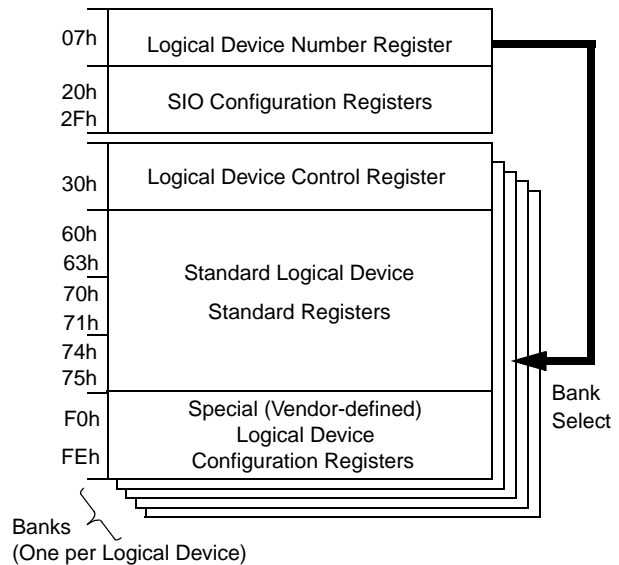
#### 5.3.2 Banked Logical Device Registers

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 5-2 shows the LDNs of the device functional blocks.

**Table 5-2. LDN Assignments**

| LDN | Functional Block  | Reference |
|-----|---|-----------|
| 00h | Real-Time Clock (RTC)                                     | Page 114  |
| 01h | System Wakeup Control (SWC)                               | Page 116  |
| 02h | Infrared Communication Port (IRCP) or Serial Port 3 (SP3) | Page 117  |
| 03h | Serial Port 1 (SP1)                                       | Page 118  |
| 05h | ACCESS.bus 1 (ACB1)                                       | Page 119  |
| 06h | ACCESS.bus 2 (ACB2)                                       |           |
| 07h | Parallel Port (PP)  | Page 120  |
| 08h | Serial Port 2 (SP2)                                       | Page 118  |

Figure 5-3 shows the structure of the standard PnP configuration register file. The SIO Control And Configuration registers are not banked and are accessed by the Index-Data register pair only (as described above). However, the Logical Device Control and Configuration registers are duplicated over eight banks for eight logical devices. Therefore, accessing a specific register in a specific bank is performed by two-dimensional indexing, where the LDN register selects the bank (or logical device), and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher results in a physical access to the Logical Device Configuration registers currently pointed to by the Index register, within the logical device bank currently selected by the LDN register.



**Figure 5-3. Structure of the Standard Configuration Register File**

Write accesses to unimplemented registers (i.e., accessing the Data register while the Index register points to a non-existing register or the LDN is 07h or higher than 08h), are ignored and a read returns 00h on all addresses except for 74h and 75h (DMA configuration registers) which returns 04h (indicating no DMA channel is active). The configuration registers are accessible immediately after reset.

### 5.3.3 Default Configuration Setup

The device has four reset types:

#### Software Reset

This reset is generated by bit 1 of the SIOCF1 register, which resets all logical devices. A software reset also resets most bits in the SIO Configuration and Control registers (see Section 5.4.1 on page 113 for the bits not affected). This reset does not affect register bits that are locked for write access.

#### Hardware Reset

This reset is activated by the system reset signal. This resets all logical devices, with the exception of the RTC and the SWC, and all SIO Configuration and Control registers, with the exception of the SIOCF2 register. It also resets all SuperI/O control and configuration registers, except for those that are battery-backed.

#### V<sub>PP</sub> Power-Up Reset

This reset is activated when either V<sub>SB</sub> or V<sub>BAT</sub> is powered on after both have been off. V<sub>PP</sub> is an internal voltage which is a combination of V<sub>SB</sub> and V<sub>BAT</sub>. V<sub>PP</sub> is taken from V<sub>SB</sub> if V<sub>SB</sub> is greater than the minimum (Min) value defined in Section 9.1.4 "Operating Conditions" on page 370; otherwise, V<sub>BAT</sub> is used as the V<sub>PP</sub> source. This reset resets all registers whose values are retained by V<sub>PP</sub>.

#### V<sub>SB</sub> Power-Up Reset

This is an internally generated reset that resets the SWC, excluding those SWC registers whose values are retained by V<sub>PP</sub>. This reset is activated after V<sub>SB</sub> is powered up.

The SIO module wakes up with the default setup, as follows:

- When a hardware reset occurs:
  - The configuration base address is 2Eh, 15Ch or None, according to the IO\_SIOCFG\_IN bit values, as shown in Table 5-1 on page 108.
  - All Logical devices are disabled, with the exception of the RTC and the SWC, which remains functional but whose registers cannot be accessed.
- When either a hardware or a software reset occurs:
  - The legacy devices are assigned with their legacy system resource allocation.
  - The AMD proprietary functions are not assigned with any default resources and the default values of their base addresses are all 00h.

### 5.3.4 Address Decoding

A full 16-bit address decoding is applied when accessing the configuration I/O space, as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers vary for each device.

The lower 1, 2, 3 or 4 address bits are decoded within the functional block to determine the offset of the accessed register, within the device's I/O range of 2, 4, 8 or 16 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the device. Therefore the lower bits of the base address register are forced to 0 (RO), and the base address is forced to be 2, 4, 8 or 16 byte aligned, according to the size of the I/O range.

The base address of the RTC, Serial Port 1, Serial Port 2, and the Infrared Communication Port are limited to the I/O address range of 00h to 7F<sub>x</sub>h only (bits [15:11] are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F<sub>8</sub>h. The addresses of the non-legacy devices are configurable within the full 16-bit address range (up to FFF<sub>x</sub>h).

In some special cases, other address bits are used for internal decoding (such as 10 in the Parallel Port). For more details, please see the detailed description of the base address register for each specific logical device.

## 5.4 Standard Configuration Registers

As illustrated in Figure 5-4, the Standard Configuration registers are broadly divided into two categories: SIO Control and Configuration registers and Logical Device Control and Configuration registers (one per logical device, some are optional).

### SIO Control and Configuration Registers

The only PnP control register in the SIO module is the Logical Device Number register at Index 07h. All other standard PnP control registers are associated with PnP protocol for ISA add-in cards, and are not supported by the SIO module.

The SIO Configuration registers at Index 20h-27h are mainly used for part identification. (See Section 5.4.1 "SIO Control and Configuration Registers" on page 113 for further details.)

### Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. (See Table 5-2 on page 108 for LDN assignment and Section 5.4.2 "Logical Device Control and Configuration" on page 114 for register details.)

**Logical Device Control Register (Index 30h):** The only implemented Logical Device Control register is the Activate register at Index 30. Bit 0 of the Activate register and bit 0 of the SIO Configuration 1 register (Global Device Enable bit) control the activation of the associated function block

(except for the RTC and the SWC). Activation of the block enables access to the block's registers, and attaches its system resources, which are unused as long as the block is not activated. Activation of the block may also result in other effects (e.g., clock enable and active signaling), for certain functions.

### Standard Logical Device Configuration Registers (Index 60h-75h):

These registers are used to manage the resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60h-61h, holding the (first or only) 16-bit base address for the register set of the functional block. An optional second base-address (descriptor 1) at Index 62h-63h is used for devices with more than one continuous register set. Interrupt Number Select (Index 70h) and Interrupt Type Select (Index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (Index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (Index 75h) allocates a second DMA channel, where applicable.

### Special Logical Device Configuration Registers (F0h-F3h):

The vendor-defined registers, starting at Index F0h are used to control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection, and non-standard extensions to generic functions.

| Index | Register Name                                  |
|-------|--|
| 07h   | Logical Device Number                          |
| 20h   | SIO ID   |
| 21h   | SIO Configuration 1                            |
| 22h   | SIO Configuration 2                            |
| 27h   | SIO Revision ID                                |
| 2Eh   | Reserved exclusively for AMD use               |
| 30h   | Logical Device Control (Activate)              |
| 60h   | I/O Port Base Address Descriptor 0 Bits [15:8] |
| 61h   | I/O Port Base Address Descriptor 0 Bits [7:0]  |
| 62h   | I/O Port Base Address Descriptor 1 Bits [15:8] |
| 63h   | I/O Port Base Address Descriptor 1 Bits [7:0]  |
| 70h   | Interrupt Number Select                        |
| 71h   | Interrupt Type Select                          |
| 74h   | DMA Channel Select 0                           |
| 75h   | DMA Channel Select 1                           |
| F0h   | Device Specific Logical Device Configuration 1 |
| F1h   | Device Specific Logical Device Configuration 2 |
| F2h   | Device Specific Logical Device Configuration 3 |
| F3h   | Device Specific Logical Device Configuration 4 |

Figure 5-4. Standard Configuration Registers Map

Table 5-3 provides the bit definitions for the Standard Configuration registers.

- All reserved bits return 0 on reads, except where noted otherwise. They must not be modified as such modification may cause unpredictable results. Use read-modify-

write to prevent the values of reserved bits from being changed during write.

- Write only registers should not use read-modify-write during updates.

**Table 5-3. Standard Configuration Registers**

| Bit   | Description   |
|---|---|
| <b>Index 07h Logical Device Number (R/W)</b>  |   |
| This register selects the current logical device. See Table 5-2 for valid numbers. All other values are reserved.                     |   |
| 7:0   | <b>Logical Device number.</b>   |
| <b>Index 20h-2Fh SIO Configuration (R/W)</b>  |   |
| SIO configuration and ID registers. See Section 5.4.1 "SIO Control and Configuration Registers" on page 113 for register/bit details. |   |
| <b>Index 30h Activate (R/W)</b>   |   |
| 7:1   | <b>Reserved.</b>  |
| 0   | <b>Logical Device Activation Control.</b><br>0: Disable<br>1: Enable  |
| <b>Index 60h I/O Port Base Address Bits [15:8] Descriptor 0 (R/W)</b>   |   |
| 7:0   | <b>Descriptor 0 A[15:8].</b> Selects I/O lower limit address bits [15:8] for I/O Descriptor 0.  |
| <b>Index 61h I/O Port Base Address Bits [7:0] Descriptor 0 (R/W)</b>  |   |
| 7:0   | <b>Descriptor 0 A[7:0].</b> Selects I/O lower limit address bits [7:0] for I/O Descriptor 0.  |
| <b>Index 62h I/O Port Base Address Bits [15:8] Descriptor 1 (R/W)</b>   |   |
| 7:0   | <b>Descriptor 1 A[15:8].</b> Selects I/O lower limit address bits [15:8] for I/O Descriptor 1.  |
| <b>Index 63h I/O Port Base Address Bits [7:0] Descriptor 1 (R/W)</b>  |   |
| 7:0   | <b>Descriptor 1 A[7:0].</b> Selects I/O lower limit address bits [7:0] for I/O Descriptor 1.  |
| <b>Index 70h Interrupt Number (R/W)</b>   |   |
| 7:4   | <b>Reserved.</b>  |
| 3:0   | <b>Interrupt Number.</b> These bits select the interrupt number. A value of 1 selects IRQ1, a value of 2 selects IRQ2, etc. (up to IRQ12).<br><b>Note:</b> IRQ0 is not a valid interrupt selection.   |
| <b>Index 71h Interrupt Request Type Select (R/W)</b>  |   |
| Selects the type and level of the interrupt request number selected in the previous register.   |   |
| 7:2   | <b>Reserved.</b>  |
| 1   | <b>Interrupt Level Requested.</b> Level of interrupt request selected in previous register.<br>0: Low polarity.<br>1: High polarity.<br>This bit must be set to 1 (high polarity), except for IRQ8#, that must be low polarity.                                       |
| 0   | <b>Interrupt Type Requested.</b> Type of interrupt request selected in previous register.<br>0: Edge.<br>1: Level.  |
| <b>Index 74h DMA Channel Select 0 (R/W)</b>   |   |
| Selects selected DMA channel for DMA 0 of the logical device (0 - the first DMA channel in case of using more than one DMA channel).  |   |
| 7:3   | <b>Reserved.</b>  |
| 2:0   | <b>DMA 0 Channel Select.</b> This bit field selects the DMA channel for DMA 0.<br>The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc.<br>A value of 4 indicates that no DMA channel is active.<br>Values 5-7 are reserved. |

**Table 5-3. Standard Configuration Registers (Continued)**

| Bit   | Description   |
|---|---|
| <b>Index 75h DMA Channel Select 1 (R/W)</b>   |   |
| Indicates selected DMA channel for DMA 1 of the logical device (1 - the second DMA channel in case of using more than one DMA channel). |   |
| 7:3   | <b>Reserved.</b>  |
| 2:0   | <b>DMA 1 Channel Select:</b> This bit field selects the DMA channel for DMA 1.<br>The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc.<br>A value of 4 indicates that no DMA channel is active.<br>Values 5-7 are reserved. |
| <b>Index F0h-FEh Logical Device Configuration (R/W)</b>   |   |
| Special (vendor-defined) configuration options.   |   |



### 5.4.1 SIO Control and Configuration Registers

Table 5-4 lists the SIO Control and Configuration registers and Table 5-5 provides their bit formats.

**Table 5-4. SIO Control and Configuration Register Map**

| Index | Type | Name   | Power Rail        | Reset Value |
|-------|------|--|-------------------|-------------|
| 20h   | RO   | <b>SID.</b> SIO ID                             | V <sub>CORE</sub> | F5h         |
| 21h   | R/W  | <b>SIOCF1.</b> SIO Configuration 1             | V <sub>CORE</sub> | 01h         |
| 22h   | R/W  | <b>SIOCF2.</b> SIO Configuration 2             | V <sub>PP</sub>   | 02h         |
| 27h   | RO   | <b>SRID.</b> SIO Revision ID                   | V <sub>CORE</sub> | 01h         |
| 2Eh   | ---  | <b>RSVD.</b> Reserved exclusively for AMD use. | ---               | ---         |

**Table 5-5. SIO Control and Configuration Registers**

| Bit   | Description   |
|---|---|
| <b>Index 20h SIO ID Register - SID (RO) Reset Value: F5h</b>                    |   |
| 7:0   | <b>Chip ID.</b> Contains the identity number of the module. The SIO module is identified by the value F5h.  |
| <b>Index 21h SIO Configuration 1 Register - SIOCF1 (RW) Reset Value: 01h</b>    |   |
| 7:6   | <b>General Purpose Scratch.</b> When bit 5 is set to 1, these bits are RO. After reset, these bits can be read or write. Once changed to RO, the bits can be changed back to R/W only by a hardware reset.  |
| 5   | <b>Lock Scratch.</b> This bit controls bits 7 and 6 of this register. Once this bit is set to 1 by software, it can be cleared to 0 only by a hardware reset.<br>0: Bits 7 and 6 of this register are R/W bits. (Default)<br>1: Bits 7 and 6 of this register are RO bits.  |
| 4:2   | <b>Reserved.</b>  |
| 1   | <b>SW Reset.</b> Read always returns 0.<br>0: Ignored. (Default)<br>1: Resets all devices that are reset by MR (with the exception of the lock bits) and the registers of the SWC.  |
| 0   | <b>Global Device Enable.</b> This bit controls the function enable of all the logical devices in the SIO module, except the SWC and the RTC. It allows them to be disabled simultaneously by writing to a single bit.<br>0: All logical devices in the SIO module are disabled, except the SWC and the RTC.<br>1: Each logical device is enabled according to its Activate register at Index 30h. (Default) |
| <b>Index 22h SIO Configuration 2 Register - SIOCF2 (R/W) Reset Value: 02h</b>   |   |
| <b>Note:</b> This register is reset only when V <sub>PP</sub> is first applied. |   |
| 7   | <b>Reserved.</b>  |
| 6:4   | <b>General Purpose Scratch.</b> Battery-backed.   |
| 3:2   | <b>Reserved.</b>  |
| 1   | <b>Reserved.</b>  |
| 0   | <b>Reserved. (RO)</b>   |
| <b>Index 27h SIO Revision ID Register - SRID (RO) Reset Value: 01h</b>          |   |
| 7:0   | <b>SIO Revision ID. (RO)</b> This RO register contains the identity number of the chip revision. SRID is incremented on each revision.  |

## 5.4.2 Logical Device Control and Configuration

As described in Section 5.3.2 "Banked Logical Device Registers" on page 108, each functional block is associated with a Logical Device Number (LDN). This section provides the register descriptions for each LDN.

The register descriptions in this subsection use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

### 5.4.2.1 LDN 00h - Real-Time Clock

Table 5-6 lists the registers which are relevant to configuration of the Real-Time Clock (RTC). Only the last registers (F0h-F3h) are described here (Table 5-7). See Table 5-3 "Standard Configuration Registers" on page 111 for descriptions of the other registers.

**Table 5-6. Relevant RTC Configuration Registers**

| Index | Type | Configuration Register or Action   | Reset Value |
|-------|------|--|-------------|
| 30h   | R/W  | <b>Activate.</b> When bit 0 is cleared, the registers of this logical device are not accessible. <sup>1</sup>                | 00h         |
| 60h   | R/W  | <b>Standard Base Address MSB register.</b> Bits [7:3] (for A[15:11]) are RO, 00000b.   | 00h         |
| 61h   | R/W  | <b>Standard Base Address LSB register.</b> Bit 0 (for A0) is RO, 0b.   | 70h         |
| 62h   | R/W  | <b>Extended Base Address MSB register.</b> Bits [7:3] (for A[15:11]) are RO, 00000b.   | 00h         |
| 63h   | R/W  | <b>Extended Base Address LSB register.</b> Bit 0 (for A0) is RO, 0b.   | 72h         |
| 70h   | R/W  | <b>Interrupt Number.</b>   | 08h         |
| 71h   | R/W  | <b>Interrupt Type.</b> Bit 1 is R/W; other bits are RO.  | 00h         |
| 74h   | RO   | <b>Report no DMA assignment.</b>   | 04h         |
| 75h   | RO   | <b>Report no DMA assignment.</b>   | 04h         |
| F0h   | R/W  | <b>RAM Lock register (RLR).</b>  | 00h         |
| F1h   | R/W  | <b>Date of Month Alarm Offset register (DOMAO).</b> Sets index of Date of Month Alarm register in the standard base address. | 00h         |
| F2h   | R/W  | <b>Month Alarm Offset register (MONAO).</b> Sets index of Month Alarm register in the standard base address.                 | 00h         |
| F3h   | R/W  | <b>Century Offset register (CENO).</b> Sets index of Century register in the standard base address.                          | 00h         |

1. The logical device registers are maintained, and all RTC mechanisms are functional.

Table 5-7. RTC Configuration Registers

| Bit   | Description   |
|---|---|
| <b>Index F0h</b> <span style="float: right;"><b>RAM Lock Register - RLR (R/W)</b></span>                              |   |
| When any non-reserved bit in this register is set to 1, it can be cleared only by hardware reset.                     |   |
| 7   | <b>Block Standard RAM.</b><br>0: No effect on Standard RAM access. (Default)<br>1: Read and write to locations 38h-3Fh of the Standard RAM are blocked, writes ignored, and reads return FFh.                                       |
| 6   | <b>Block RAM Write.</b><br>0: No effect on RAM access. (Default)<br>1: Writes to RAM (Standard and Extended) are ignored.   |
| 5   | <b>Block Extended RAM Write.</b> This bit controls writes to bytes 00h-1Fh of the Extended RAM.<br>0: No effect on the Extended RAM access. (Default)<br>1: Writes to bytes 00h-1Fh of the Extended RAM are ignored.                |
| 4   | <b>Block Extended RAM Read.</b> This bit controls read from bytes 00h-1Fh of the Extended RAM.<br>0: No effect on Extended RAM access. (Default)<br>1: Reads to bytes 00h-1Fh of the Extended RAM are ignored.                      |
| 3   | <b>Block Extended RAM.</b> This bit controls access to the Extended RAM 128 bytes.<br>0: No effect on Extended RAM access. (Default)<br>1: Read and write to the Extended RAM are blocked: writes are ignored and reads return FFh. |
| 2:0   | <b>Reserved.</b>  |
| <b>Index F1h</b> <span style="float: right;"><b>Date Of Month Alarm Register Offset Register - DOMAO (R/W)</b></span> |   |
| 7   | <b>Reserved.</b>  |
| 6:0   | <b>Date of Month Alarm Register Offset Value.</b>   |
| <b>Index F2h</b> <span style="float: right;"><b>Month Alarm Register Offset Register - MANAO (R/W)</b></span>         |   |
| 7   | <b>Reserved.</b>  |
| 6:0   | <b>Month Alarm Register Offset Value.</b>   |
| <b>Index F3h</b> <span style="float: right;"><b>Century Register Offset Register - CENO (R/W)</b></span>              |   |
| 7   | <b>Reserved.</b>  |
| 6:0   | <b>Century Register Offset Value.</b>   |

#### 5.4.2.2 LDN 01h - System Wakeup Control

Table 5-8 lists registers that are relevant to the configuration of System Wakeup Control (SWC). These registers are

described earlier in Table 5-3 "Standard Configuration Registers" on page 111.

**Table 5-8. Relevant SWC Registers**

| Index | Type | Configuration Register or Action  | Reset Value |
|-------|------|---|-------------|
| 30h   | R/W  | <b>Activate.</b> When bit 0 is cleared, the registers of this logical device are not accessible. <sup>1</sup> | 00h         |
| 60h   | R/W  | <b>Base Address MSB register.</b>   | 00h         |
| 61h   | R/W  | <b>Base Address LSB register.</b> Bits [3:0] (for A[3:0]) are RO, 0000b.                                      | 00h         |
| 70h   | R/W  | <b>Interrupt Number.</b> (For routing the internal PWUREQ signal.)  | 00h         |
| 71h   | R/W  | <b>Interrupt Type.</b> Bit 1 is R/W. Other bits are RO.   | 03h         |
| 74h   | RO   | <b>Report no DMA assignment.</b>  | 04h         |
| 75h   | RO   | <b>Report no DMA assignment.</b>  | 04h         |

1. The logical device registers are maintained, and all wakeup detection mechanisms are functional.

### 5.4.2.3 LDN 02h - Infrared Communication Port or Serial Port 3

Table 5-9 lists the configuration registers which affect the Infrared Communication Port or Serial Port 3 (IRCP/SP3).

Only the last register (F0h) is described here (Table 5-10). See Table 5-3 "Standard Configuration Registers" on page 111 for descriptions of the other registers listed.

**Table 5-9. Relevant IRCP/SP3 Registers**

| Index | Type | Configuration Register or Action  | Reset Value |
|-------|------|---|-------------|
| 30h   | R/W  | <b>Activate.</b> See also bit 0 of the SIOCF1 register.                     | 00h         |
| 60h   | R/W  | <b>Base Address MSB register.</b> Bits [7:3] (for A[15:11]) are RO, 00000b. | 03h         |
| 61h   | R/W  | <b>Base Address LSB register.</b> Bit [2:0] (for A[2:0]) are RO, 000b.      | E8h         |
| 70h   | R/W  | <b>Interrupt Number.</b>  | 00h         |
| 71h   | R/W  | <b>Interrupt Type.</b> Bit 1 is R/W; other bits are RO.                     | 03h         |
| 74h   | R/W  | <b>DMA Channel Select 0 (RX_DMA).</b>                                       | 04h         |
| 75h   | R/W  | <b>DMA Channel Select 1 (TX_DMA).</b>                                       | 04h         |
| F0h   | R/W  | <b>Infrared Communication Port/Serial Port 3 Configuration register.</b>    | 02h         |

**Table 5-10. IRCP/SP3 Configuration Register**

| Bit              | Description  |
|------------------|--|
| <b>Index F0h</b> | <b>Infrared Communication Port/Serial Port 3 Configuration Register (R/W)</b> <span style="float: right;"><b>Reset Value: 02h</b></span>   |
| 7                | <b>Bank Select Enable.</b> Enables bank switching.<br>0: All attempts to access the extended registers are ignored. (Default)<br>1: Enables bank switching.  |
| 6:3              | <b>Reserved.</b>   |
| 2                | <b>Busy Indicator.</b> (RO) This bit can be used by power management software to decide when to power-down the device.<br>0: No transfer in progress. (Default)<br>1: Transfer in progress.  |
| 1                | <b>Power Mode Control.</b> When the logical device is active in:<br>0: Low power mode - Clock disabled. The output signals are set to their default states. Registers are maintained. (Unlike Active bit in Index 30h that also prevents access to device registers.)<br>1: Normal power mode - Clock enabled. The device is functional when the logical device is active. (Default) |
| 0                | <b>TRI-STATE Control.</b> When enabled and the device is inactive, the logical device output pins are in TRI-STATE. One exception is the IRTX/SOUT3 pin, which is driven to 0 when the Infrared Communication Port or Serial Port 3 is inactive and is not affected by this bit.<br>0: Disabled. (Default)<br>1: Enabled (when the device is inactive).                              |

#### 5.4.2.4 LDN 03h and 08h - Serial Ports 1 and 2

Serial Ports 1 and 2 are identical, except for their reset values.

Serial Port 1 is designated as LDN 03h and Serial Port 2 as LDN 08h. Table 5-11 lists the configuration registers which

affect Serial Ports 1 and 2. Only the last register (F0h) is described here (Table 5-12). See Table 5-3 "Standard Configuration Registers" on page 111 for descriptions of the others.

**Table 5-11. Relevant Serial Ports 1 and 2 Registers**

| Index | Type | Configuration Register or Action  | Reset Value |        |
|-------|------|---|-------------|--------|
|       |      |   | Port 1      | Port 2 |
| 30h   | R/W  | <b>Activate.</b> See also bit 0 of the SIOCF1 register.                     | 00h         | 00h    |
| 60h   | R/W  | <b>Base Address MSB register.</b> Bits [7:3] (for A[15:11]) are RO, 00000b. | 03h         | 02h    |
| 61h   | R/W  | <b>Base Address LSB register.</b> Bit [2:0] (for A[2:0]) are RO, 000b.      | F8h         | F8h    |
| 70h   | R/W  | <b>Interrupt Number.</b>  | 04h         | 03h    |
| 71h   | R/W  | <b>Interrupt Type.</b> Bit 1 is R/W; other bits are RO.                     | 03h         | 03h    |
| 74h   | RO   | <b>Report no DMA assignment.</b>  | 04h         | 04h    |
| 75h   | RO   | <b>Report no DMA assignment.</b>  | 04h         | 04h    |
| F0h   | R/W  | <b>Serial Ports 1 and 2 Configuration register.</b>                         | 02h         | 02h    |

**Table 5-12. Serial Ports 1 and 2 Configuration Register**

| Bit              | Description   |
|------------------|---|
| <b>Index F0h</b> | <b>Serial Ports 1 and 2 Configuration Register (R/W)</b> <span style="float: right;"><b>Reset Value: 02h</b></span>   |
| 7                | <b>Bank Select Enable.</b> Enables bank switching for Serial Ports 1 and 2.<br>0: Disabled. (Default)<br>1: Enabled.  |
| 6:3              | <b>Reserved.</b>  |
| 2                | <b>Busy Indicator. (RO)</b> This bit can be used by power management software to decide when to power-down Serial Ports 1 and 2 logical devices.<br>0: No transfer in progress. (Default)<br>1: Transfer in progress.   |
| 1                | <b>Power Mode Control.</b> When the logical device is active in:<br>0: Low power mode - Serial Ports 1 and 2 Clock disabled. The output signals are set to their default states. Registers are maintained. (Unlike Active bit in Index 30h that also prevents access to Serial Ports 1 or 2 registers.)<br>1: Normal power mode - Serial Ports 1 and 2 clock enabled. Serial Ports 1 and 2 are functional when the respective logical devices are active. (Default) |
| 0                | <b>TRI-STATE Control.</b> This bit controls the TRI-STATE status of the device output pins when it is inactive (disabled).<br>0: Disabled. (Default)<br>1: Enabled when device inactive.  |

#### 5.4.2.5 LDN 05h and 06h - ACCESS.bus Ports 1 and 2

ACCESS.bus ports 1 and 2 (ACB1 and ACB2) are identical. Each ACB is a two-wire synchronous serial interface compatible with the ACCESS.bus physical layer. ACB1 and ACB2 use a 24 MHz internal clock. Six runtime registers for each ACCESS.bus are described in Section 5.7 "ACCESS.bus Interface" on page 137.

ACB1 is designated as LDN 05h and ACB2 as LDN 06h. Table 5-13 lists the configuration registers which affect the ACCESS.bus ports. Only the last register (F0h) is described here (Table 5-14). See Table 5-3 "Standard Configuration Registers" on page 111 for descriptions of the others.

**Table 5-13. Relevant ACB1 and ACB2 Registers**

| Index | Type | Configuration Register or Action  | Reset Value |
|-------|------|---|-------------|
| 30h   | R/W  | <b>Activate.</b> See also bit 0 of the SIOCF1 register                  | 00h         |
| 60h   | R/W  | <b>Base Address MSB register.</b>                                       | 00h         |
| 61h   | R/W  | <b>Base Address LSB register.</b> Bits [2:0] (for A[2:0]) are RO, 000b. | 00h         |
| 70h   | R/W  | <b>Interrupt Number.</b>  | 00h         |
| 71h   | R/W  | <b>Interrupt Type.</b> Bit 1 is R/W. Other bits are RO.                 | 03h         |
| 74h   | RO   | <b>Report no DMA assignment.</b>  | 04h         |
| 75h   | RO   | <b>Report no DMA assignment.</b>  | 04h         |
| F0h   | R/W  | <b>ACB1 and ACB2 Configuration register.</b>                            | 00h         |

**Table 5-14. ACB1 and ACB2 Configuration Register**

| Bit              | Description  |
|------------------|--|
| <b>Index F0h</b> | <b>ACB1 and ACB2 Configuration Register (R/W)</b><br>This register is reset by hardware to 00h.  |
| 7:3              | <b>Reserved.</b>   |
| 2                | <b>Internal Pull-Up Enable.</b><br>0: No internal pull-up resistors on AB1C/AB2C and AB1D/AB2D. (Default)<br>1: Internal pull-up resistors on AB1C/AB2C and AB1D/AB2D. |
| 1:0              | <b>Reserved.</b>   |

#### 5.4.2.6 LDN 07h - Parallel Port

The Parallel Port supports all IEEE 1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at Offset 403h, 404h, and 405h) are used only in the Extended ECP mode.

- A group of four registers, used only in the Extended ECP mode, accessed by a second level offset.

The desired mode is selected by the ECR runtime register (Offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. (See Section 5.8.1 on page 145 for further details regarding the runtime registers.)

Table 5-15 lists the configuration registers which affect the Parallel Port. Only the last register (F0h) is described here (Table 5-16). See Table 5-3 "Standard Configuration Registers" on page 111 for descriptions of the others.

**Table 5-15. Relevant Parallel Port Registers**

| Index | Type | Configuration Register or Action  | Reset Value |
|-------|------|---|-------------|
| 30h   | R/W  | <b>Activate.</b> See also bit 0 of the SIOCF1 register.   | 00h         |
| 60h   | R/W  | <b>Base Address MSB register.</b> Bits [7:3] (for A[15:11]) are RO, 00000b. Bit 2 (for A10) should be 0b.   | 02h         |
| 61h   | R/W  | <b>Base Address LSB register.</b> Bits 1 and 0 (A1 and A0) are RO, 00b. For ECP Mode 4 (EPP) or when using the Extended registers, bit 2 (A2) should also be 0b.  | 78h         |
| 70h   | R/W  | <b>Interrupt Number.</b>  | 07h         |
| 71h   | R/W  | <b>Interrupt Type.</b><br>Bits [7:2] are RO.<br>Bit 1 is R/W.<br>Bit 0 is RO. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended Mode and cleared (edge interrupt) in all other modes. | 02h         |
| 74h   | R/W  | <b>DMA Channel Select.</b>  | 04h         |
| 75h   | RO   | <b>Report no second DMA assignment.</b>   | 04h         |
| F0h   | R/W  | <b>Parallel Port Configuration register.</b> (See Table 5-16.)  | F2h         |

**Table 5-16. Parallel Port Configuration Register**

| Bit              | Description  |
|------------------|--|
| <b>Index F0h</b> | <b>Parallel Port Configuration Register (R/W)</b> <span style="float: right;"><b>Reset Value: F2h</b></span><br>This register is reset by hardware to F2h.   |
| 7:5              | <b>Reserved.</b> Must be 11.   |
| 4                | <b>Extended Register Access.</b><br>0: Registers at base (address)+403h, base+404h and base+405h are not accessible (reads and writes are ignored).<br>1: Registers at base (address)+403h, base+404h and base+405h are accessible. This option supports run-time configuration within the Parallel Port address space.        |
| 3:2              | <b>Reserved.</b>   |
| 1                | <b>Power Mode Control.</b> When the logical device is active:<br>0: Parallel port clock disabled. ECP modes and EPP timeout are not functional when the logical device is active. Registers are maintained.<br>1: Parallel port clock enabled. All operation modes are functional when the logical device is active. (Default) |
| 0                | <b>TRI-STATE Control.</b> When enabled and the device is inactive, the logical device output pins are in TRI-STATE.<br>0: Disable. (Default)<br>1: Enable.   |



## 5.5 Real-Time Clock (RTC)

The RTC provides timekeeping and calendar management capabilities. The RTC uses a 32.768 KHz signal as the basic clock for timekeeping. It also includes 242 bytes of battery-backed RAM for general-purpose use.

The RTC provides the following functions:

- Accurate timekeeping and calendar management
- Alarm at a predetermined time and/or date
- Three programmable interrupt sources
- Valid timekeeping during power-down, by utilizing external battery backup
- 242 bytes of battery-backed RAM
- RAM lock schemes to protect its content
- Internal oscillator circuit (the crystal itself is off-chip), or external clock supply for the 32.768 KHz clock
- A century counter
- PnP support:
  - Relocatable Index and Data registers
  - Module access enable/disable option
  - Host interrupt enable/disable option
- Additional low-power features such as:
  - Automatic switching from battery to  $V_{SB}$
  - Internal power monitoring on the VRT bit
  - Oscillator disabling to save battery during storage
- Software compatible with the DS1287 and MC146818

### 5.5.1 Bus Interface

The RTC function is initially mapped to the default SuperI/O locations at Indexes 70h to 73h (two Index/Data pairs). These locations may be reassigned, in compliance with Plug and Play requirements.

### 5.5.2 RTC Clock Generation

The RTC uses a 32.768 KHz clock signal as the basic clock for timekeeping. The 32.768 KHz clock can be supplied by the internal oscillator circuit, or by an external oscillator (see Section 5.5.2.2 "External Oscillator" on page 122).

#### 5.5.2.1 Internal Oscillator

The internal oscillator employs an external crystal connected to the on-chip amplifier. The on-chip amplifier is accessible on the X32I input and X32O output. See Figure 5-5 for the recommended external circuit and Table 5-17 for a listing of the circuit components. The oscillator may be disabled in certain conditions. See Section 5.5.2.8 "Oscillator Activity" on page 125 for more details.

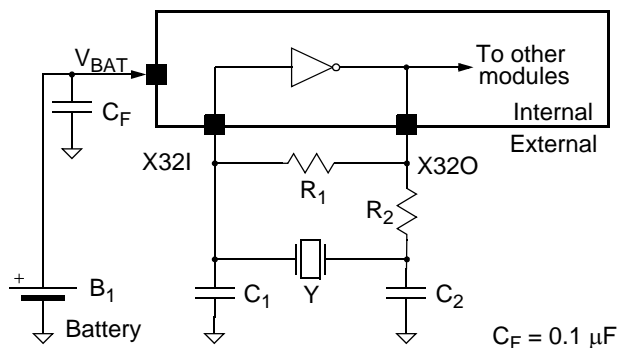


Figure 5-5. Recommended Oscillator External Circuitry

Table 5-17. Crystal Oscillator Circuit Components

| Component       | Parameters              | Values                   | Tolerance    |
|-----------------|-------------------------|--------------------------|--------------|
| Crystal         | Resonance Frequency     | 32.768 KHz Parallel mode | User-defined |
|                 | Type                    | N-cut or XY-bar          |              |
|                 | Serial Resistance       | 40 K $\Omega$            | Max          |
|                 | Quality Factor, Q       | 35000                    | Min          |
|                 | Shunt Capacitance       | 2 pF                     | Max          |
|                 | Load Capacitance, $C_L$ | 9-13 pF                  |              |
|                 | Temperature Coefficient | User-defined             |              |
| Resistor $R_1$  | Resistance              | 20 M $\Omega$            | 5%           |
| Resistor $R_2$  | Resistance              | 120 K $\Omega$           | 5%           |
| Capacitor $C_1$ | Capacitance             | 3 to 10 pF               | 5%           |
| Capacitor $C_2$ | Capacitance             | 3 to 10 pF               | 5%           |

**External Elements**

Choose  $C_1$  and  $C_2$  capacitors (see Figure 5-5 on page 121) to match the crystal’s load capacitance. The load capacitance  $C_L$  “seen” by crystal Y is comprised of  $C_1$  in series with  $C_2$  and in parallel with the parasitic capacitance of the circuit. The parasitic capacitance is caused by the chip package, board layout and socket (if any), and can vary from 0 to 10 pF. The rule of thumb in choosing these capacitors is:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{PARASITIC}$$

Example:

Crystal  $C_L = 10$  pF,  $C_{PARASITIC} = 8.2$  pF  
 $C_1 = 3.6$  pF,  $C_2 = 3.6$  pF

**Oscillator Startup**

The oscillator starts to generate 32.768 KHz pulses to the RTC after about 100 ms from when  $V_{BAT}$  is higher than  $V_{BATMIN}$  (2.4V) or  $V_{SB}$  is higher than  $V_{SBMIN}$  (3.0V). The oscillation amplitude on the X32O pin stabilizes to its final value (approximately 0.4V peak-to-peak around 0.7V DC) in about 1 s.

$C_1$  can be trimmed to achieve precisely 32.768 KHz. To achieve a high time accuracy, use crystal and capacitors with low tolerance and temperature coefficients.

**5.5.2.2 External Oscillator**

32.768 KHz can be applied from an external clock source, as shown in Figure 5-6.

**Connections**

Connect the clock to the X32I ball, leaving the oscillator output, X32O, unconnected.

**Signal Parameters**

The signal levels should conform to the voltage level requirements for X32I, of square or sine wave of 0.0V to  $V_{CORE}$  amplitude. The signal should have a duty cycle of approximately 50%. It should be sourced from a battery-backed source in order to oscillate during power-down. This assures that the RTC delivers updated time/calendar information.

**5.5.2.3 Timing Generation**

The timing generation function divides the 32.768 KHz clock by  $2^{15}$  to derive a 1 Hz signal, which serves as the input for the seconds counter. This is performed by a divider chain composed of 15 divide-by-two latches, as shown in Figure 5-7.

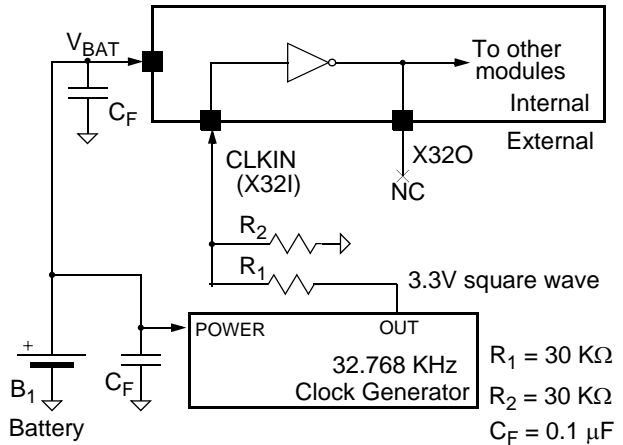
Bits [6:4] (DV[2:0]) of the CRA Register control the following functions:

- Normal operation of the divider chain (counting).
- Divider chain reset to 0.
- Oscillator activity when only  $V_{BAT}$  power is present (backup state).

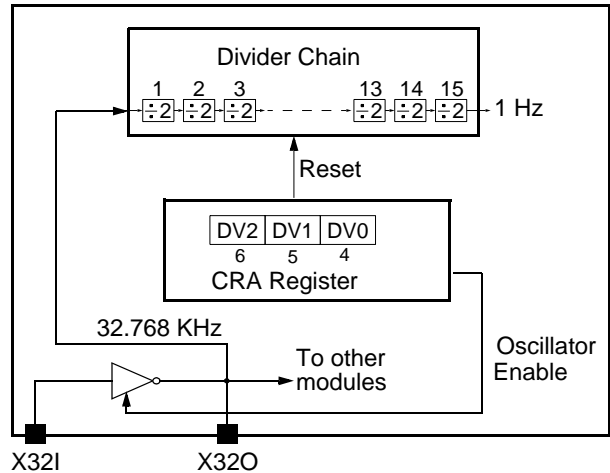
The divider chain can be activated by setting normal operational mode (bits [6:4] of CRA = 01x or 100). The first update occurs 500 ms after divider chain activation.

Bits [3:0] of CRA select one the of fifteen taps from the divider chain to be used as a periodic interrupt. The periodic flag becomes active after half of the programmed period has elapsed, following divider chain activation.

See Table 5-20 on page 127 for more details.



**Figure 5-6. External Oscillator Connections**



**Figure 5-7. Divider Chain Control**

### 5.5.2.4 Timekeeping

#### Data Format

Time is kept in BCD or binary format, as determined by bit 2 (DM) of Control Register B (CRB), and in either 12 or 24-hour format, as determined by bit 1 of this register.

**Note:** When changing the above formats, re-initialize all the time registers.

#### Daylight Saving

Daylight saving time exceptions are handled automatically, as described in Table 5-20 on page 127.

#### Leap Years

Leap year exceptions are handled automatically by the internal calendar function. Every four years, February is extended to 29 days.

#### Updating

The time and calendar registers are updated once per second regardless of bit 7 (SET) of CRB. Since the time and calendar registers are updated serially, unpredictable results may occur if they are accessed during the update. Therefore, you must ensure that reading or writing to the time storage locations does not coincide with a system update of these locations. There are several methods to avoid this contention.

#### Method 1

- 1) Set bit 7 of CRB to 1. This takes a “snapshot” of the internal time registers and loads them into the user copy registers. The user copy registers are seen when accessing the RTC from outside, and are part of the double buffering mechanism. You may keep this bit set for up to 1 second, since the time/calendar chain continue to be updated once per second.
- 2) Read or write the required registers (since bit 1 is set, you are accessing the user copy registers). If you perform a read operation, the information you read is correct from the time when bit 1 was set. If you perform a write operation, you write only to the user copy registers.
- 3) Reset bit 1 to 0. During the transition, the user copy registers update the internal registers, using the double buffering mechanism to ensure that the update is performed between two time updates. This mechanism enables new time parameters to be loaded in the RTC.

#### Method 2

- 1) Access the RTC registers after detection of an Update Ended interrupt. This implies that an update has just been completed and 999 ms remain until the next update.
- 2) To detect an Update Ended interrupt, you may either:
  - Poll bit 4 of CRC.
  - Use the following interrupt routine:
    - Set bit 4 of CRB.
    - Wait for an interrupt from interrupt pin.
    - Clear the IRQF flag of CRC before exiting the interrupt routine.

#### Method 3

Poll bit 7 of CRA. The update occurs 244  $\mu$ s after this bit goes high. Therefore, if a 0 is read, the time registers remain stable for at least 244  $\mu$ s.

#### Method 4

Use a periodic interrupt routine to determine if an update cycle is in progress, as follows:

- 1) Set the periodic interrupt to the desired period.
- 2) Set bit 6 of CRB to enable the interrupt from periodic interrupt.
- 3) Wait for the periodic interrupt appearance. This indicates that the period represented by the following expression remains until another update occurs:
 
$$[(\text{Period of periodic interrupt} / 2) + 244 \mu\text{s}]$$

### 5.5.2.5 Alarms

The timekeeping function can be set to generate an alarm when the current time reaches a stored alarm time. After each RTC time update (every 1 second), the seconds, minutes, hours, date of month and month counters are compared with their corresponding registers in the alarm settings. If equal, bit 5 of CRC is set. If the Alarm Interrupt Enable bit was previously set (CRB bit 5), interrupt request pin is also active.

Any alarm register may be set to “Unconditional Match” by setting bits [7:6] to 11. This combination, not used by any BCD or binary time codes, results in a periodic alarm. The rate of this periodic alarm is determined by the registers that were set to “Unconditional Match”.

For example, if all but the seconds and minutes alarm registers are set to “Unconditional Match”, an interrupt is generated every hour at the specified minute and second. If all but the seconds, minutes and hours alarm registers are set to “Unconditional Match”, an interrupt is generated every day at the specified hour, minute and second.

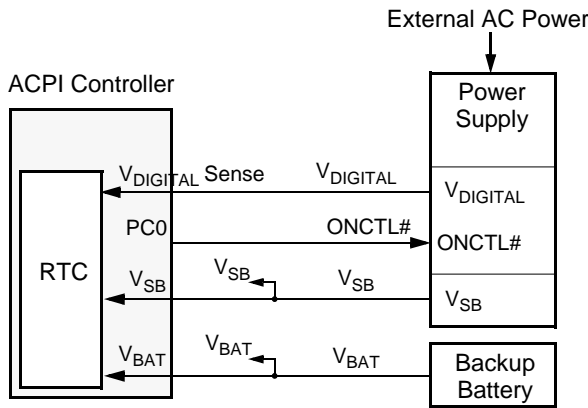
**5.5.2.6 Power Supply**

The device is supplied from two supply voltages, as shown in Figure 5-8:

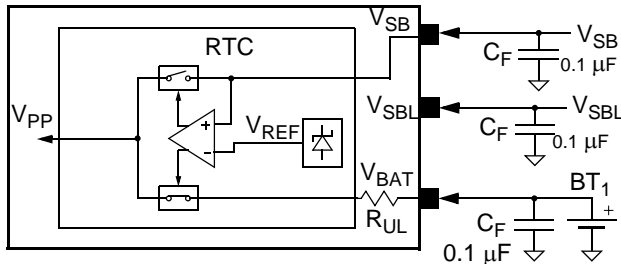
- System standby power supply voltage,  $V_{SB}$
- Backup voltage, from low capacity Lithium battery

A standby voltage,  $V_{SB}$ , from the external AC/DC power supply powers the RTC under normal conditions.

Figure 5-9 represents a typical battery configuration. No external diode is required to meet the UL standard, due to the internal switch and internal serial resistor  $R_{UL}$ .



**Figure 5-8. Power Supply Connections**



**Note:** Place a 0.1  $\mu\text{F}$  capacitor on each  $V_{SB}$ ,  $V_{SBL}$  power supply pin as close as possible to the pin, and also on  $V_{BAT}$ .

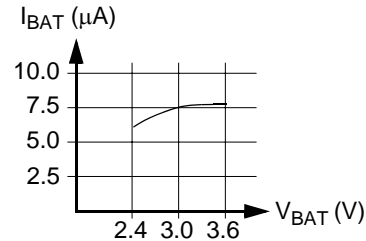
**Figure 5-9. Typical Battery Configuration**

The RTC is supplied from one of two power supplies,  $V_{SB}$  or  $V_{BAT}$ , according to their levels. An internal voltage comparator delivers the control signals to a pair of switches. Battery backup voltage  $V_{BAT}$  maintains the correct time and saves the CMOS memory when the  $V_{SB}$  voltage is absent, due to power failure or disconnection of the external AC/DC input power supply or  $V_{SB}$  main battery.

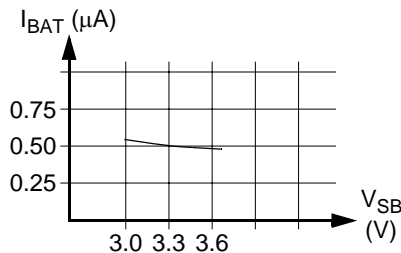
To assure that the module uses power from  $V_{SB}$  and not from  $V_{BAT}$ , the  $V_{SB}$  voltage should be maintained above its minimum, as detailed in Section 9.0 "Electrical Specifications" on page 369.

The actual voltage point where the module switches from  $V_{BAT}$  to  $V_{SB}$  is lower than the minimum workable battery voltage, but high enough to guarantee the correct functionality of the oscillator and the CMOS RAM.

Figure 5-10 shows typical battery current consumption during battery-backed operation, and Figure 5-11 during normal operation.



**Figure 5-10. Typical Battery Current: Battery Backed Power Mode @  $T_C = 25^\circ\text{C}$**



**Note:** Battery voltage in this test is 3.0V.

**Figure 5-11. Typical Battery Current: Normal Operation Mode**

### 5.5.2.7 System Power States

The system power state may be No Power, Power On, Power Off or Power Failure. Table 5-18 indicates the power-source combinations for each state. No other power-source combinations are valid.

In addition, the power sources and distribution for the entire system are illustrated in Figure 5-8 on page 124.

**Table 5-18. System Power States**

| $V_{\text{DIGITAL}}$ | $V_{\text{SB}}$ | $V_{\text{BAT}}$ | Power State   |
|----------------------|-----------------|------------------|---------------|
| -                    | -               | -                | No Power      |
| -                    | -               | +                | Power Failure |
| -                    | +               | + or -           | Power Off     |
| +                    | +               | + or -           | Power On      |

#### No Power

This state exists when no external or battery power is connected to the device. This condition does not occur once a backup battery has been connected, except in the case of a malfunction.

#### Power On

This is the normal state when the system is active. This state may be initiated by various events in addition to the normal physical switching on of the system. In this state, the system power supply is powered by external AC power and produces  $V_{\text{DIGITAL}}$  and  $V_{\text{SB}}$ . The system and the part are powered by  $V_{\text{DIGITAL}}$ , with the exception of the RTC logical device, which is powered by  $V_{\text{SB}}$ .

#### Power Off (Suspended)

This is the normal state when the system has been switched off and is not required to be active, but is still connected to a live external AC input power source. This state may be initiated directly or by software. The system is powered down. The RTC logical device remains active, powered by  $V_{\text{SB}}$ .

#### Power Failure

This state occurs when the external power source to the system stops supplying power, due to disconnection or power failure on the external AC input power source. The RTC continues to maintain timekeeping and RAM data under battery power ( $V_{\text{BAT}}$ ), unless the oscillator stop bit was set in the RTC. In this case, the oscillator stops functioning if the system goes to battery power, and timekeeping data becomes invalid.

#### System Bus Lockout

During power on or power off, spurious bus transactions from the host may occur. To protect the RTC internal registers from corruption, all inputs are automatically locked out. The lockout condition is asserted when  $V_{\text{SB}}$  is lower than  $V_{\text{SBON}}$ .

### Power-Up Detection

When system power is restored after a power failure or power off state ( $V_{\text{SB}} = 0$ ), the lockout condition continues for a delay of 62 ms (minimum) to 125 ms (maximum) after the RTC switches from battery to system power.

The lockout condition is switched off immediately in the following situations:

- If the Divider Chain Control bits, DV[2:0], (CRA bits [6:4]) specify a normal operation mode (01x or 100), all input signals are enabled immediately upon detection of system voltage above  $V_{\text{SBON}}$ .
- When battery voltage is below  $V_{\text{BATDCT}}$  and HMR is 1, all input signals are enabled immediately upon detection of system voltage above  $V_{\text{SBON}}$ . This also initializes registers at offsets 00h through 0Dh.
- If bit 7 (VRT) of CRD is 0, all input signals are enabled immediately upon detection of system voltage above  $V_{\text{SBON}}$ .

### 5.5.2.8 Oscillator Activity

The RTC oscillator is active if:

- $V_{\text{SB}}$  power supply is higher than  $V_{\text{SBON}}$ , independent of the battery voltage,  $V_{\text{BAT}}$

-or-

- $V_{\text{BAT}}$  power supply is higher than  $V_{\text{BATMIN}}$ , regardless if  $V_{\text{SB}}$  is present or not.

The RTC oscillator is disabled if:

- During power-down ( $V_{\text{BAT}}$  only), the battery voltage drops below  $V_{\text{BATMIN}}$ . When this occurs, the oscillator may be disabled and its functionality cannot be guaranteed.

-or-

- Software wrote 00x to DV[2:0] bits of the CRA Register and  $V_{\text{SB}}$  is removed. This disables the oscillator and decreases the power consumption from the battery connected to  $V_{\text{BAT}}$ . When disabling the oscillator, the CMOS RAM is not affected as long as the battery is present at a correct voltage level.

If the RTC oscillator becomes inactive, the following features are dysfunctional/disabled:

- Timekeeping.
- Periodic interrupt.
- Alarm.

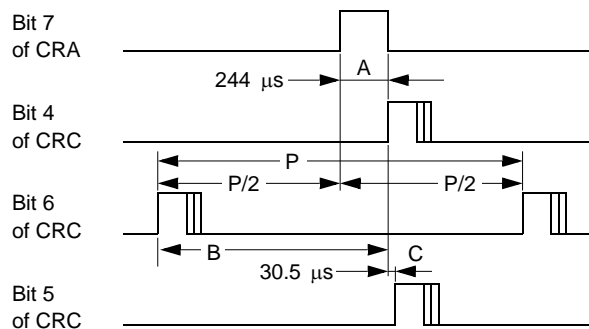
### 5.5.2.9 Interrupt Handling

The RTC has a single Interrupt Request line which handles the following three interrupt conditions:

- Periodic interrupt.
- Alarm interrupt.
- Update end interrupt.

The interrupts are generated if the respective enable bits in the CRB register are set prior to an interrupt event occurrence. Reading the CRC register clears all interrupt flags. Thus, when multiple interrupts are enabled, the interrupt service routine should first read and store the CRC register, and then deal with all pending interrupts by referring to this stored status.

If an interrupt is not serviced before a second occurrence of the same interrupt condition, the second interrupt event is lost. Figure 5-12 illustrates the interrupt timing in the RTC.



Flags (and IRQ) are reset at the conclusion of CRC read or by reset.

A = Update In Progress bit high before update occurs = 244  $\mu$ s

B = Periodic interrupt to update = Period (periodic int) / 2 + 244  $\mu$ s

C = Update to Alarm Interrupt = 30.5  $\mu$ s

P = Period is programmed by RS[3:0] of CRA

**Figure 5-12. Interrupt/Status Timing**

### 5.5.2.10 Battery-Backed RAMs and Registers

The RTC has two battery-backed RAMs and 17 registers, used by the logical units themselves. Battery-backup power enables information retention during system power down.

The RAMs are:

- Standard RAM
- Extended RAM

The memory maps and register content of the RAMs is provided in Section 5.5.4 "RTC General-Purpose RAM Map" on page 131.

The first 14 bytes and 3 programmable bytes of the Standard RAM are overlaid by time, alarm data and control registers. The remaining 111 bytes are general-purpose memory.

Registers with reserved bits should be written using the read-modify-write method.

All register locations within the device are accessed by the RTC Index and Data registers (at base address and base address+1). The Index register points to the register location being accessed, and the Data register contains the data to be transferred to or from the location. An additional 128 bytes of battery-backed RAM (also called Extended RAM) may be accessed via a second pair of Index and Data registers.

Access to the two RAMs may be locked. For details see Table 5-7 on page 115.

### 5.5.3 RTC Registers

The RTC registers can be accessed (see Section 5.4.2.1 "LDN 00h - Real-Time Clock" on page 114) at any time during normal operation mode (i.e., when  $V_{SB}$  is within the recommended operation range). This access is disabled during battery-backed operation. The write operation to these registers is also disabled if bit 7 of the CRD Register is 0.

**Note:** Before attempting to perform any start-up procedures, read about bit 7 (VRT) of the CRD Register.

This section describes the RTC Timing and Control Registers that control basic RTC functionality.

**Table 5-19. RTC Register Map**

| Index                     | Type | Name                                      | Reset Type   |
|---------------------------|------|---|--------------|
| 00h                       | R/W  | <b>SEC.</b> Seconds Register              | $V_{PP}$ PUR |
| 01h                       | R/W  | <b>SECA.</b> Seconds Alarm Register       | $V_{PP}$ PUR |
| 02h                       | R/W  | <b>MIN.</b> Minutes Register              | $V_{PP}$ PUR |
| 03h                       | R/W  | <b>MINA.</b> Minutes Alarm Register       | $V_{PP}$ PUR |
| 04h                       | R/W  | <b>HOR.</b> Hours Register                | $V_{PP}$ PUR |
| 05h                       | R/W  | <b>HORA.</b> Hours Alarm Register         | $V_{PP}$ PUR |
| 06h                       | R/W  | <b>DOW.</b> Day Of Week Register          | $V_{PP}$ PUR |
| 07h                       | R/W  | <b>DOM.</b> Date Of Month Register        | $V_{PP}$ PUR |
| 08h                       | R/W  | <b>MON.</b> Month Register                | $V_{PP}$ PUR |
| 09h                       | R/W  | <b>YER.</b> Year Register                 | $V_{PP}$ PUR |
| 0Ah                       | R/W  | <b>CRA.</b> RTC Control Register A        | Bit specific |
| 0Bh                       | R/W  | <b>CRB.</b> RTC Control Register B        | Bit specific |
| 0Ch                       | RO   | <b>CRC.</b> RTC Control Register C        | Bit specific |
| 0Dh                       | RO   | <b>CRD.</b> RTC Control Register D        | $V_{PP}$ PUR |
| Programmable <sup>1</sup> | R/W  | <b>DOMA.</b> Date of Month Alarm Register | $V_{PP}$ PUR |
| Programmable <sup>1</sup> | R/W  | <b>MONA.</b> Month Alarm Register         | $V_{PP}$ PUR |
| Programmable <sup>1</sup> | R/W  | <b>CEN.</b> Century Register              | $V_{PP}$ PUR |

1. Overlaid on RAM bytes in range 0Eh-7Fh. See Section 5.4.2.1 "LDN 00h - Real-Time Clock" on page 114.

**Table 5-20. RTC Registers**

| Bit              | Description   |
|------------------|---|
| <b>Index 00h</b> | <b>Seconds Register - SEC (R/W)</b> <span style="float: right;"><b>Reset Type: <math>V_{PP}</math> PUR</b></span>   |
| 7:0              | <b>Seconds Data.</b> Values may be 00 to 59 in BCD format or 00 to 3B in binary format.   |
| <b>Index 01h</b> | <b>Seconds Alarm Register - SECA (R/W)</b> <span style="float: right;"><b>Reset Type: <math>V_{PP}</math> PUR</b></span>  |
| 7:0              | <b>Seconds Alarm Data.</b> Values may be 00 to 59 in BCD format or 00 to 3B in binary format.<br>When bits 7 and 6 are both set to one ("11"), unconditional match is selected. |
| <b>Index 02h</b> | <b>Minutes Register - MIN (R/W)</b> <span style="float: right;"><b>Reset Type: <math>V_{PP}</math> PUR</b></span>   |
| 7:0              | <b>Minutes Data.</b> Values can be 00 to 59 in BCD format, or 00 to 3B in binary format.  |

Table 5-20. RTC Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Index 03h</b> <b>Minutes Alarm Register - MINA (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>  |  |
| 7:0  | <b>Minutes Alarm Data.</b> Values can be 00 to 59 in BCD format, or 00 to 3B in binary format.<br>When bits 7 and 6 are both set to 1, unconditional match is selected. See Section 5.5.2.5 "Alarms" on page 123 for more information about "unconditional" matches.   |
| <b>Index 04h</b> <b>Hours Register - HOR (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>   |  |
| 7:0  | <b>Hours Data.</b> For 12-hour mode, values can be 01 to 12 (AM) and 81 to 92 (PM) in BCD format, or 01 to 0C (AM) and 81 to 8C (PM) in binary format. For 24-hour mode, values can be 0- to 23 in BCD format or 00 to 17 in binary format.  |
| <b>Index 05h</b> <b>Hours Alarm Register - HORA (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>  |  |
| 7:0  | <b>Hours Alarm Data.</b> For 12-hour mode, values may be 01 to 12 (AM) and 81 to 92 (PM) in BCD format or 01 to 0C (AM) and 81 to 8C (PM) in Binary format. For 24-hour mode, values may be 0- to 23 in BCD format or 00 to 17 in Binary format.<br>When bits 7 and 6 are both set to one ("11"), unconditional match is selected. |
| <b>Index 06h</b> <b>Day of Week Register - DOW (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>   |  |
| 7:0  | <b>Day Of Week Data.</b> Values may be 01 to 07 in BCD format or 01 to 07 in binary format.  |
| <b>Index 07h</b> <b>Date of Month Register - DOM (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>   |  |
| 7:0  | <b>Date Of Month Data.</b> Values may be 01 to 31 in BCD format or 01 to 1F in binary format.  |
| <b>Index 08h</b> <b>Month Register - MON (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b><br>Width: Byte  |  |
| 7-0  | <b>Month Data.</b> Values may be 01 to 12 in BCD format or 01 to 0C in binary format.  |
| <b>Index 09h</b> <b>Year Register - YER (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>  |  |
| 7:0  | <b>Year Data.</b> Values may be 00 to 99 in BCD format or 00 to 63 in binary format.   |
| <b>Index 0Ah</b> <b>RTC Control Register A - CRA (R/W)</b> <b>Reset Type: Bit Specific</b><br>This register controls test selection, among other functions. This register cannot be written before reading bit 7 of CRD. |  |
| 7  | <b>Update in Progress. (RO)</b> This bit is not affected by reset. This bit reads 0 when bit 7 of the CRB Register is 1.<br>0: Timing registers not updated within 244 $\mu$ s.<br>1: Timing registers updated within 244 $\mu$ s.   |
| 6:4  | <b>Divider Chain Control.</b> These bits control the configuration of the divider chain for timing generation and register bank selection. See Table 5-21 on page 130. They are cleared to 000 as long as bit 7 of CRD is 0.   |
| 3:0  | <b>Periodic Interrupt Rate Select.</b> These bits select one of fifteen output taps from the clock divider chain to control the rate of the periodic interrupt. See Table 5-22 on page 130 and Figure 5-7 on page 122. They are cleared to 000 as long as bit 7 of CRD is 0.   |
| <b>Index 0Bh</b> <b>RTC Control Register B - CRB (R/W)</b> <b>Reset Type: Bit Specific</b>   |  |
| 7  | <b>Set Mode.</b> This bit is reset at V <sub>PP</sub> power-up reset only.<br>0: Timing updates occur normally.<br>1: User copy of time is "frozen", allowing the time registers to be accessed whether or not an update occurs.   |
| 6  | <b>Periodic Interrupt.</b> Bits [3:0] of the CRA Register determine the rate at which this interrupt is generated. It is cleared to 0 on RTC reset (i.e., hardware or software reset) or when RTC is disable.<br>0: Disable.<br>1: Enable.   |
| 5  | <b>Alarm Interrupt.</b> This interrupt is generated immediately after a time update in which the seconds, minutes, hours, date and month time equal their respective alarm counterparts. It is cleared to 0 as long as bit 7 of the CRD Register is reads 0.<br>0: Disable.<br>1: Enable.  |
| 4  | <b>Update Ended Interrupt.</b> This interrupt is generated when an update occurs. It is cleared to 0 on RTC reset (i.e., hardware or software reset) or when the RTC is disable.<br>0: Disable.<br>1: Enable.  |



Table 5-20. RTC Registers (Continued)

| Bit  | Description  |
|--|--|
| 3  | <b>Reserved.</b> This bit is defined as "Square Wave Enable" by the MC146818 and is not supported by the RTC. This bit is always read as 0.  |
| 2  | <b>Data Mode.</b> This bit is reset at V <sub>PP</sub> power-up reset only.<br>0: Enable BCD format.<br>1: Enable Binary format.   |
| 1  | <b>Hour Mode.</b> This bit is reset at V <sub>PP</sub> power-up reset only.<br>0: Enable 12-hour format.<br>1: Enable 24-hour format.  |
| 0  | <b>Daylight Saving.</b> This bit is reset at V <sub>PP</sub> power-up reset only.<br>0: Disable.<br>1: Enable:<br>- In the spring, time advances from 1:59:59 AM to 3:00:00 AM on the first Sunday in April.<br>- In the fall, time returns from 1:59:59 AM to 1:00:00 AM on the last Sunday in October.   |
| <b>Index 0Ch</b> <b>RTC Control Register C - CRC (RO)</b> <b>Reset Type: Bit Specific</b>                        |  |
| 7  | <b>IRQ Flag.</b> Mirrors the value on the interrupt output signal. When interrupt is active, IRQF is 1. To clear this bit (and deactivate the interrupt pin), read the CRC Register as the flag bits UF, AF and PF are cleared after reading this register.<br>0: IRQ inactive.<br>1: Logic equation is true: ((UIE and UF) or (AIE and AF) or (PIE and PF)).                              |
| 6  | <b>Periodic Interrupt Flag.</b> Cleared to 0 on RTC reset (i.e., hardware or software reset) or the RTC disabled. In addition, this bit is cleared to 0 when this register is read.<br>0: No transition occurred on the selected tap since the last read.<br>1: Transition occurred on the selected tap of the divider chain.  |
| 5  | <b>Alarm Interrupt Flag.</b> Cleared to 0 as long as bit 7 of the CRD Register is reads 0. In addition, this bit is cleared to 0 when this register is read.<br>0: No alarm detected since the last read.<br>1: Alarm condition detected.  |
| 4  | <b>Update Ended Interrupt Flag.</b> Cleared to 0 on RTC reset (i.e., hardware or software reset) or the RTC disabled. In addition, this bit is cleared to 0 when this register is read.<br>0: No update occurred since the last read.<br>1: Time registers updated.  |
| 3:0  | <b>Reserved.</b>   |
| <b>Index 0Dh</b> <b>RTC Control Register D - CRD (RO)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>                  |  |
| 7  | <b>Valid RAM and Time.</b> This bit senses the voltage that feeds the RTC (VSB or VBAT) and indicates whether or not it was too low since the last time this bit was read. If it was too low, the RTC contents (time/calendar registers and CMOS RAM) is not valid.<br>0: The voltage that feeds the RTC was too low.<br>1: RTC contents (time/calendar registers and CMOS RAM) are valid. |
| 6:0  | <b>Reserved.</b>   |
| <b>Index Programmable</b> <b>Date of Month Alarm Register - DOMA (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b> |  |
| 7:0  | <b>Date of Month Alarm Data.</b> Values may be 01 to 31 in BCD format or 01 to 1F in Binary format.<br>When bits 7 and 6 are both set to one ("11"), unconditional match is selected. (Default)  |
| <b>Index Programmable</b> <b>Month Alarm Register - MONA (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>         |  |
| 7:0  | <b>Month Alarm Data.</b> Values may be 01 to 12 in BCD format or 01 to 0C in Binary format.<br>When bits 7 and 6 are both set to one ("11"), unconditional match is selected. (Default)  |
| <b>Index Programmable</b> <b>Century Register - CEN (R/W)</b> <b>Reset Type: V<sub>PP</sub> PUR</b>              |  |
| 7:0  | <b>Century Data.</b> Values may be 00 to 99 in BCD format or 00 to 63 in Binary format.  |

Table 5-21. Divider Chain Control / Test Selection

| DV2  | DV1  | DV0  | Configuration       |
|------|------|------|---------------------|
| CRA6 | CRA5 | CRA4 |                     |
| 0    | 0    | X    | Oscillator Disabled |
| 0    | 1    | 0    | Normal Operation    |
| 0    | 1    | 1    | Test                |
| 1    | 0    | X    |                     |
| 1    | 1    | X    | Divider Chain Reset |

Table 5-22. Periodic Interrupt Rate Encoding

| Rate Select<br>3 2 1 0 | Periodic Interrupt<br>Rate (ms) | Divider<br>Chain Output |
|------------------------|---------------------------------|-------------------------|
| 0 0 0 0                | No interrupts                   |                         |
| 0 0 0 1                | 3.906250                        | 7                       |
| 0 0 1 0                | 7.812500                        | 8                       |
| 0 0 1 1                | 0.122070                        | 2                       |
| 0 1 0 0                | 0.244141                        | 3                       |
| 0 1 0 1                | 0.488281                        | 4                       |
| 0 1 1 0                | 0.976562                        | 5                       |
| 0 1 1 1                | 1.953125                        | 6                       |
| 1 0 0 0                | 3.906250                        | 7                       |
| 1 0 0 1                | 7.812500                        | 8                       |
| 1 0 1 0                | 15.625000                       | 9                       |
| 1 0 1 1                | 31.250000                       | 10                      |
| 1 1 0 0                | 62.500000                       | 11                      |
| 1 1 0 1                | 125.000000                      | 12                      |
| 1 1 1 0                | 250.000000                      | 13                      |
| 1 1 1 1                | 500.000000                      | 14                      |

Table 5-23. BCD and Binary Formats

| Parameter | BCD Format   | Binary Format  |
|-----------|--|--|
| Seconds   | 00 to 59   | 00 to 3B   |
| Minutes   | 00 to 59   | 00 to 3B   |
| Hours     | 12-hour mode: 01 to 12 (AM)<br>81 to 92 (PM)<br>24-hour mode: 00 to 23 | 12-hour mode: 01 to 0C (AM)<br>81 to 8C (PM)<br>24-hour mode: 00 to 17 |
| Day       | 01 to 07 (Sunday = 01)   | 01 to 07   |
| Date      | 01 to 31   | 01 to 1F   |
| Month     | 01 to 12 (January = 01)  | 01 to 0C   |
| Year      | 00 to 99   | 00 to 63   |
| Century   | 00 to 99   | 00 to 63   |

### 5.5.3.1 Usage Hints

- 1) Read bit 7 of CRD at each system power-up to validate the contents of the RTC registers and the CMOS RAM. When this bit is 0, the contents of these registers and the CMOS RAM are questionable. This bit is reset when the backup battery voltage is too low. The voltage level at which this bit is reset is below the minimum recommended battery voltage, 2.4V. Although the RTC oscillator may function properly and the register contents may be correct at lower than 2.4V, this bit is reset since correct functionality cannot be guaranteed. System BIOS may use a checksum method to revalidate the contents of the CMOS-RAM. The checksum byte should be stored in the same CMOS RAM.
- 2) Change the backup battery while normal operating power is present, and not in backup mode, to maintain valid time and register information. If a low leakage capacitor is connected to  $V_{BAT}$ , the battery may be changed in backup mode.
- 3) A rechargeable NiCd battery may be used instead of a non-rechargeable Lithium battery. This is a preferred solution for portable systems, where small size components is essential.
- 4) A supercap capacitor may be used instead of the normal Lithium battery. In a portable system usually the  $V_{SB}$  voltage is always present since the power management stops the system before its voltage falls to low. The supercap capacitor in the range of 0.047-0.47 F should supply the power during the battery replacement.

### 5.5.4 RTC General-Purpose RAM Map

**Table 5-24. Standard RAM Map**

| Index     | Description                                  |
|-----------|--|
| 0Eh - 7Fh | Battery-backed general-purpose 111-byte RAM. |

**Table 5-25. Extended RAM Map**

| Index     | Description                                  |
|-----------|--|
| 00h - 7Fh | Battery-backed general-purpose 128-byte RAM. |

## 5.6 System Wakeup Control (SWC)

The SWC wakes up the system by sending a power-up request to the ACPI controller in response to the following maskable system events:

- Modem ring (RI2#)
- Audio Codec event (SDATA\_IN2)
- Programmable Consumer Electronics IR (CEIR) address

Each system event that is monitored by the SWC is fed into a dedicated detector that decides when the event is active, according to predetermined (either fixed or programmable) criteria. A set of dedicated registers is used to determine the wakeup criteria, including the CEIR address.

A Wakeup Events Status Register (WKSR) and a Wakeup Events Control Register (WKCR) hold a Status bit and Enable bit, respectively, for each possible wakeup event.

Upon detection of an active event, the corresponding Status bit is set to 1. If the event is enabled (the corresponding Enable bit is set to 1), a power-up request is issued to the ACPI controller. In addition, detection of an active wakeup event may be also routed to an arbitrary IRQ.

Disabling an event prevents it from issuing power-up requests, but does not affect the Status bits. A power-up reset is issued to the ACPI controller when both the Status and Enable bits are set to 1 for at least one event type.

SWC logic is powered by  $V_{SB}$ . The SWC control and configuration registers are battery backed, powered by  $V_{PP}$ . The setup of the wakeup events, including programmable sequences, is retained throughout power failures (no  $V_{SB}$ ) as long as the battery is connected.  $V_{PP}$  is taken from  $V_{SB}$  if  $V_{SB} > 2.0$ ; otherwise,  $V_{BAT}$  is used as the  $V_{PP}$  source.

Hardware reset does not affect the SWC registers. They are reset only by a SIO software reset or power-up of  $V_{PP}$ .

### 5.6.1 Event Detection

#### 5.6.1.1 Audio Codec Event

A low-to-high transition on SDATA\_IN2 indicates the detection of an Audio Codec event and can be used as a wakeup event.

#### 5.6.1.2 CEIR Address

A CEIR transmission received on IRRX1 in a pre-selected standard (NEC, RCA or RC-5) is matched against a programmable CEIR address. Detection of matching can be used as a wakeup event. The CEIR address detection operates independently of the serial port with the IR (which is powered down with the rest of the system).

Whenever an IR signal is detected, the receiver immediately enters the Active state. When this happens, the receiver keeps sampling the IR input signal and generates a bit string where a logic 1 indicates an idle condition and a logic 0 indicates the presence of IR energy. The received bit string is de-serialized and assembled into 8-bit characters.

The expected CEIR protocol of the received signal should be configured through bits [5:4] of the CEIR Wakeup Control register (IRWCR) (see Table 5-30 on page 135).

The CEIR Wakeup Address register (IRWAD) holds the unique address to be compared with the address contained in the incoming CEIR message. If CEIR is enabled ( $IRWCR[0] = 1$ ) and an address match occurs, then the CEIR Event Status bit of WKSR is set to 1.

The CEIR Address Shift register (ADSR) holds the received address which is compared with the address contained in the IRWAD. The comparison is affected also by the CEIR Wakeup Address Mask register (IRWAM) in which each bit determines whether to ignore the corresponding bit in the IRWAD.

If CEIR routing to interrupt request is enabled, the assigned SWC interrupt request can be used to indicate that a complete address has been received. To get this interrupt when the address is completely received, IRWAM should be written with FFh. Once the interrupt is received, the value of the address can be read from ADSR.

Another parameter that is used to determine whether a CEIR signal is to be considered valid is the bit cell time width. There are four time ranges for the different protocols and carrier frequencies. Four pairs of registers (IRWTRxL and IRWTRxH) define the low and high limits of each time range. Table 5-26 lists the recommended time ranges limits for the different protocols and their applicable ranges. The values are represented in hexadecimal code where the units are of 0.1 ms.

**Table 5-26. Time Range Limits for CEIR Protocols**

| Time Range | RC-5      |            | NEC       |            | RCA       |            |
|------------|-----------|------------|-----------|------------|-----------|------------|
|            | Low Limit | High Limit | Low Limit | High Limit | Low Limit | High Limit |
| 0          | 10h       | 14h        | 09h       | 0Dh        | 0Ch       | 12h        |
| 1          | 07h       | 0Bh        | 14h       | 19h        | 16h       | 1Ch        |
| 2          | -         | -          | 50h       | 64h        | B4h       | DCh        |
| 3          | -         | -          | 28h       | 32h        | 23h       | 2Dh        |

## 5.6.2 SWC Registers

The SWC registers are organized in two banks. The offsets are related to a base address that is determined by the SWC Base Address Register in the logical device configuration. The lower three registers are common to the two banks while the upper registers (03h-0Fh) are divided as follows:

- Bank 0 holds reserved registers.
- Bank 1 holds the CEIR Control Registers.

The active bank is selected through the Configuration Bank Select field (bits [1:0]) in the Wakeup Configuration Register (WKCFG). See Table 5-29 on page 134.

The tables that follow provide register maps and bit definitions for Banks 0 and 1.

**Table 5-27. Banks 0 and 1 - Common Control and Status Register Map**

| Offset | Type  | Name   | Reset Value |
|--------|-------|--|-------------|
| 00h    | R/W1C | <b>WKS</b> R. Wakeup Events Status Register  | 00h         |
| 01h    | R/W   | <b>WKC</b> R. Wakeup Events Control Register | 03h         |
| 02h    | R/W   | <b>WKCF</b> G. Wakeup Configuration Register | 00h         |

**Table 5-28. Bank 1 - CEIR Wakeup Configuration and Control Register Map**

| Offset | Type | Name   | Reset Value |
|--------|------|--|-------------|
| 03h    | R/W  | <b>IRWCR</b> . CEIR Wakeup Control Register                | 00h         |
| 04h    | ---  | <b>RSVD</b> . Reserved                                     | ---         |
| 05h    | R/W  | <b>IRWAD</b> . CEIR Wakeup Address Register                | 00h         |
| 06h    | R/W  | <b>IRWAM</b> . CEIR Wakeup Address Mask Register           | E0h         |
| 07h    | RO   | <b>ADSR</b> . CEIR Address Shift Register                  | 00h         |
| 08h    | R/W  | <b>IRWTR0L</b> . CEIR Wakeup, Range 0, Low Limit Register  | 10h         |
| 09h    | R/W  | <b>IRWTR0H</b> . CEIR Wakeup, Range 0, High Limit Register | 14h         |
| 0Ah    | R/W  | <b>IRWTR1L</b> . CEIR Wakeup, Range 1, Low Limit Register  | 07h         |
| 0Bh    | R/W  | <b>IRWTR1H</b> . CEIR Wakeup, Range 1, High Limit Register | 0Bh         |
| 0Ch    | R/W  | <b>IRWTR2L</b> . CEIR Wakeup, Range 2, Low Limit Register  | 50h         |
| 0Dh    | R/W  | <b>IRWTR2H</b> . CEIR Wakeup, Range 2, High Limit Register | 64h         |
| 0Eh    | R/W  | <b>IRWTR3L</b> . CEIR Wakeup, Range 3, Low Limit Register  | 28h         |
| 0Fh    | R/W  | <b>IRWTR3H</b> . CEIR Wakeup, Range 3, High Limit Register | 32h         |

**Table 5-29. Banks 0 and 1 - Common Control and Status Registers**

| Bit  | Description  |
|--|--|
| <b>Offset 00h</b> <b>Wakeup Events Status Register - WКСR (R/W1C)</b> <b>Reset Value: 00h</b><br>This register is set to 00h on power-up of V <sub>PP</sub> or software reset. It indicates which wakeup event and/or PME occurred. (See Section 6.2.9.4 "Power Management Events" on page 176.)   |  |
| 7  | <b>Reserved.</b>   |
| 6  | <b>Reserved.</b> Must be set to 0.   |
| 5  | <b>IRRX1 (CEIR) Event Status.</b> This sticky bit shows the status of the CEIR event detection.<br>0: Event not detected. (Default)<br>1: Event detected.                                      |
| 4:2  | <b>Reserved.</b>   |
| 1  | <b>RI2# Event Status.</b> This sticky bit shows the status of RI2# event detection.<br>0: Event not detected. (Default)<br>1: Event detected.  |
| 0  | <b>SDATA_IN2 Event Status.</b> This sticky bit shows the status of Audio Codec event detection.<br>0: Event not detected. (Default)<br>1: Event detected.                                      |
| <b>Offset 01h</b> <b>Wakeup Events Control Register - WKCR (R/W)</b> <b>Reset Value: 03h</b><br>This register is set to 03h on power-up of V <sub>PP</sub> or software reset. Detected wakeup events that are enabled issue a power-up request the ACPI controller and/or a PME to the Core Logic module. (See Section 6.2.9.4 "Power Management Events" on page 176.) |  |
| 7  | <b>Reserved.</b>   |
| 6  | <b>Reserved.</b> Must be set to 0.   |
| 5  | <b>IRRX1 (CEIR) Event Enable.</b><br>0: Disable. (Default)<br>1: Enable.   |
| 4:2  | <b>Reserved.</b>   |
| 1  | <b>RI2# Event Enable.</b><br>0: Disable.<br>1: Enable. (Default)   |
| 0  | <b>SDATA_IN2 Event Enable.</b><br>0: Disable.<br>1: Enable. (Default)  |
| <b>Offset 02h</b> <b>Wakeup Configuration Register - WKCFG (R/W)</b> <b>Reset Value: 00h</b><br>This register is set to 00h on power-up of V <sub>PP</sub> or software reset. It enables access to CEIR registers.   |  |
| 7:5  | <b>Reserved.</b>   |
| 4  | <b>Reserved.</b> Must be set to 0.   |
| 3  | <b>Reserved.</b> Must be set to 0.   |
| 2  | <b>Reserved.</b>   |
| 1:0  | <b>Configuration Bank Select Bits.</b><br>00: Only shared registers are accessible.<br>01: Shared registers and Bank 1 (CEIR) registers are accessible.<br>10: Bank selected.<br>11: Reserved. |

Table 5-30. Bank 1 - CEIR Wakeup Configuration and Control Registers

| Bit  | Description  |
|--|--|
| <b>Bank 1, Offset 03h</b> <span style="float:right"><b>CEIR Wakeup Control Register - IRWCR (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>  |  |
| This register is set to 00h on power-up of $V_{PP}$ or software reset.   |  |
| 7:6  | <b>Reserved.</b>   |
| 5:4  | <b>CEIR Protocol Select.</b><br>00: RC5<br>01: NEC/RCA<br>1x: Reserved   |
| 3  | <b>Reserved.</b>   |
| 2  | <b>Invert IRRX Input.</b><br>0: Not inverted. (Default)<br>1: Inverted.  |
| 1  | <b>Reserved.</b>   |
| 0  | <b>CEIR Enable.</b><br>0: Disable. (Default)<br>1: Enable.   |
| <b>Bank 1, Offset 04h</b> <span style="float:right"><b>Reserved</b></span>   |  |
| <b>Bank 1, Offset 05h</b> <span style="float:right"><b>CEIR Wakeup Address Register - IRWAD (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>  |  |
| This register defines the station address to be compared with the address contained in the incoming CEIR message. If CEIR is enabled (bit 0 of the IRWCR register is 1) and an address match occurs, then bit 5 of the WKSr register is set to 1.<br>This register is set to 00h on power-up of $V_{PP}$ or software reset.  |  |
| 7:0  | <b>CEIR Wakeup Address</b>   |
| <b>Bank 1, Offset 06h</b> <span style="float:right"><b>CEIR Wakeup Mask Register - IRWAM (R/W)</b></span> <span style="float:right"><b>Reset Value: E0h</b></span>   |  |
| Each bit in this register determines whether the corresponding bit in the IRWAD register takes part in the address comparison. Bits 5, 6, and 7 must be set to 1 if the RC-5 protocol is selected.<br>This register is set to E0h on power-up of $V_{PP}$ or software reset.   |  |
| 7:0  | <b>CEIR Wakeup Address Mask.</b> <ul style="list-style-type: none"> <li>• If the corresponding bit is 0, the address bit is not masked (enabled for compare).</li> <li>• If the corresponding bit is 1, the address bit is masked (ignored during compare).</li> </ul> |
| <b>Bank 1, Offset 07h</b> <span style="float:right"><b>CEIR Address Shift Register - ADSR (RO)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>   |  |
| This register holds the received address to be compared with the address contained in the IRWAD register.<br>This register is set to 00h on power-up of $V_{PP}$ or software reset.  |  |
| 7:0  | <b>CEIR Address.</b>   |
| <b>CEIR Wakeup Range 0 Registers</b>   |  |
| These two registers (IRWTR0L and IRWTR0H) define the low and high limits of time range 0 (see Table 5-26 on page 132). The values are represented in units of 0.1 ms. <ul style="list-style-type: none"> <li>• RC-5 protocol: The bit cell width must fall within this range for the cell to be considered valid. The nominal cell width is 1.778 ms for a 36 KHz carrier. IRWTR0L and IRWTR0H should be set to 10h and 14h, respectively. (Default)</li> <li>• NEC protocol: The time distance between two consecutive CEIR pulses that encodes a bit value of 0 must fall within this range. The nominal distance for a 0 is 1.125 ms for a 38 KHz carrier. IRWTR0L and IRWTR0H should be set to 09h and 0Dh, respectively.</li> </ul> |  |
| <b>Bank 1, Offset 08h</b> <span style="float:right"><b>IRWTR0L Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 10h</b></span>  |  |
| This register is set to 10h on power-up of $V_{PP}$ or software reset.   |  |
| 7:5  | <b>Reserved.</b>   |
| 4:0  | <b>CEIR Pulse Change, Range 0, Low Limit.</b>  |
| <b>Bank 1, Offset 09h</b> <span style="float:right"><b>IRWTR0H Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 14h</b></span>  |  |
| This register is set to 14h on power-up of $V_{PP}$ or software reset.   |  |
| 7:5  | <b>Reserved.</b>   |
| 4:0  | <b>CEIR Pulse Change, Range 0, High Limit.</b>   |

**Table 5-30. Bank 1 - CEIR Wakeup Configuration and Control Registers (Continued)**

| Bit   | Description                                    |
|---|--|
| <b>CEIR Wakeup Range 1 Registers</b>  |  |
| These two registers (IRWTR1L and IRWTR1H) define the low and high limits of time range 1 (see Table 5-26 on page 132). The values are represented in units of 0.1 ms.   |  |
| <ul style="list-style-type: none"> <li>RC-5 protocol: The pulse width defining a half-bit cell must fall within this range in order for the cell to be considered valid. The nominal pulse width is 0.889 for a 38 KHz carrier. IRWTR1L and IRWTR1H should be set to 07h and 0Bh, respectively. (Default)</li> <li>NEC protocol: The time between two consecutive CEIR pulses that encodes a bit value of 1 must fall within this range. The nominal time for a 1 is 2.25 ms for a 36 KHz carrier. IRWTR1L and IRWTR1H should be set to 14h and 19h, respectively.</li> </ul> |  |
| <b>Bank 1, Offset 0Ah</b>   |  |
| <b>IRWTR1L Register (R/W)</b>   |  |
| <b>Reset Value: 07h</b>   |  |
| This register is set to 07h on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:5   | Reserved.                                      |
| 4:0   | <b>CEIR Pulse Change, Range 1, Low Limit.</b>  |
| <b>Bank 1, Offset 0Bh</b>   |  |
| <b>IRWTR1H Register (R/W)</b>   |  |
| <b>Reset Value: 0Bh</b>   |  |
| This register is set to 0Bh on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:5   | Reserved.                                      |
| 4:0   | <b>CEIR Pulse Change, Range 1, High Limit.</b> |
| <b>CEIR Wakeup Range 2 Registers</b>  |  |
| These two registers (IRWTR2L and IRWTR2H) define the low and high limits of time range 2 (see Table 5-26 on page 132). The values are represented in units of 0.1 ms.   |  |
| <ul style="list-style-type: none"> <li>RC-5 protocol: These registers are not used when the RC-5 protocol is selected.</li> <li>NEC protocol: The header pulse width must fall within this range in order for the header to be considered valid. The nominal value is 9 ms for a 38 KHz carrier. IRWTR2L and IRWTR2H should be set to 50h and 64h, respectively. (Default)</li> </ul>   |  |
| <b>Bank 1, Offset 0Ch</b>   |  |
| <b>IRWTR2L Register (R/W)</b>   |  |
| <b>Reset Value: 50h</b>   |  |
| This register is set to 50h on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:0   | <b>CEIR Pulse Change, Range 2, Low Limit.</b>  |
| <b>Bank 1, Offset 0Dh</b>   |  |
| <b>IRWTR2H Register (R/W)</b>   |  |
| <b>Reset Value: 64h</b>   |  |
| This register is set to 64h on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:0   | <b>CEIR Pulse Change, Range 2, High Limit.</b> |
| <b>CEIR Wakeup Range 3 Registers</b>  |  |
| These two registers (IRWTR3L and IRWTR3H) define the low and high limits of time range 3 (see Table 5-26 on page 132). The values are represented in units of 0.1 ms.   |  |
| <ul style="list-style-type: none"> <li>RC-5 protocol: These registers are not used when the RC-5 protocol is selected.</li> <li>NEC protocol: The post header gap width must fall within this range in order for the gap to be considered valid. The nominal value is 4.5 ms for a 36 KHz carrier. IRWTR3L and IRWTR3H should be set to 28h and 32h, respectively. (Default)</li> </ul>   |  |
| <b>Bank 1, Offset 0Eh</b>   |  |
| <b>IRWTR3L Register (R/W)</b>   |  |
| <b>Reset Value: 28h</b>   |  |
| This register is set to 28h on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:0   | <b>CEIR Pulse Change, Range 3, Low Limit.</b>  |
| <b>Bank 1, Offset 0Fh</b>   |  |
| <b>IRWTR3H Register (R/W)</b>   |  |
| <b>Reset Value: 32h</b>   |  |
| This register is set to 32h on power-up of V <sub>PP</sub> or software reset.   |  |
| 7:0   | <b>CEIR Pulse Change, Range 3, High Limit.</b> |



## 5.7 ACCESS.bus Interface

The SC3200 has two ACCESS.bus (ACB) controllers. ACB is a two-wire synchronous serial interface compatible with the ACCESS.bus physical layer, Intel's SMBus, and Philips' I<sup>2</sup>C™. The ACB can be configured as a bus master or slave, and can maintain bidirectional communication with both multiple master and slave devices. As a slave device, the ACB may issue a request to become the bus master.

The ACB allows easy interfacing to a wide range of low-cost memories and I/O devices, including: EEPROMs, SRAMs, timers, ADC, DAC, clock chips and peripheral drivers.

The ACCESS.bus protocol uses a two-wire interface for bidirectional communication between the ICs connected to the bus. The two interface lines are the Serial Data Line (AB1D and AB2D) and the Serial Clock Line (AB1C and AB2C). (Here after referred to as ABD and ABC unless otherwise specified.) These lines should be connected to a positive supply via an internal or external pull-up resistor, and remain high even when the bus is idle.

Each IC has a unique address and can operate as a transmitter or a receiver (though some peripherals are only receivers).

During data transactions, the master device initiates the transaction, generates the clock signal and terminates the transaction. For example, when the ACB initiates a data transaction with an attached ACCESS.bus compliant peripheral, the ACB becomes the master. When the peripheral responds and transmits data to the ACB, their master/slave (data transaction initiator and clock generator) relationship is unchanged, even though their transmitter/receiver functions are reversed.

This section describes the general ACB functional block. A device may include a different implementation. For device specific implementation, see Section 5.4.2.5 "LDN 05h and 06h - ACCESS.bus Ports 1 and 2" on page 119.

### 5.7.1 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (ABC). Consequently, throughout the clock's high period, the data should remain stable (see Figure 5-13). Any changes on the ABD line during the high state of the ABC and in the middle of a transaction aborts the current transaction. New data should be sent during the low ABC state. This protocol permits a single data line to transfer both command/control information and data, using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Each byte is transferred with the most significant bit first, and after each byte (8 bits), an Acknowledge signal must follow. The following sections provide further details of this process.

During each clock cycle, the slave can stall the master while it handles the previous data or prepares new data. This can be done for each bit transferred, or on a byte boundary, by the slave holding ABC low to extend the clock-low period. Typically, slaves extend the first clock cycle of a transfer if a byte read has not yet been stored, or if the next byte to be transmitted is not yet ready. Some microcontrollers, with limited hardware support for ACCESS.bus, extend the access after each bit, thus allowing the software to handle this bit.

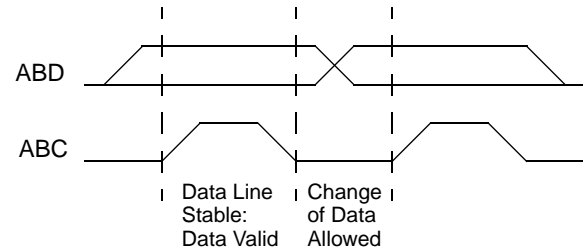


Figure 5-13. Bit Transfer

### 5.7.2 Start and Stop Conditions

The ACCESS.bus master generates Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and retains this status for a certain time after a Stop Condition is generated. A high-to-low transition of the data line (ABD) while the clock (ABC) is high indicates a Start Condition. A low-to-high transition of the ABD line while the ABC is high indicates a Stop Condition (Figure 5-14).

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a change in the direction of data transfer.

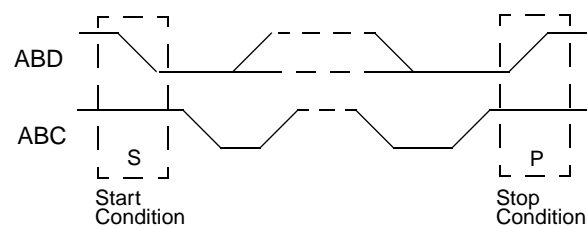


Figure 5-14. Start and Stop Conditions

### 5.7.3 Acknowledge (ACK) Cycle

The ACK cycle consists of two signals: the ACK clock pulse sent by the master with each byte transferred, and the ACK signal sent by the receiving device (see Figure 5-15).

The master generates the ACK clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases

the ABD line (permits it to go high) to allow the receiver to send the ACK signal. The receiver must pull down the ABD line during the ACK clock pulse, signalling that it has correctly received the last data byte and is ready to receive the next byte. Figure 5-16 illustrates the ACK cycle.

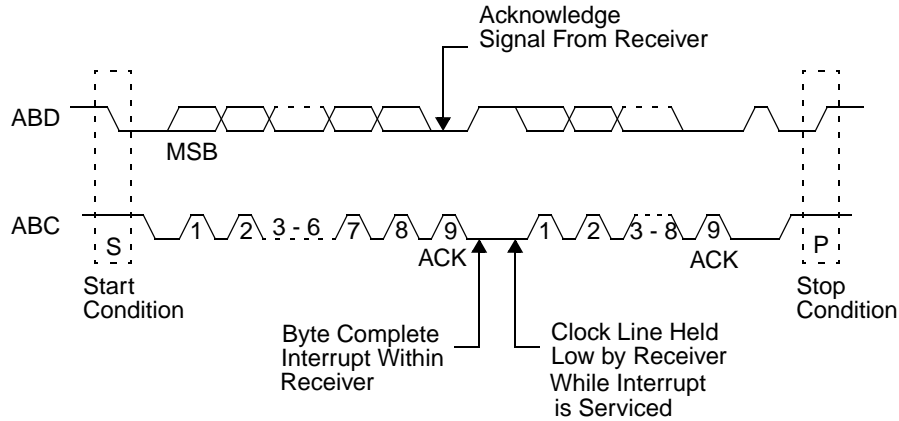


Figure 5-15. ACCESS.bus Data Transaction

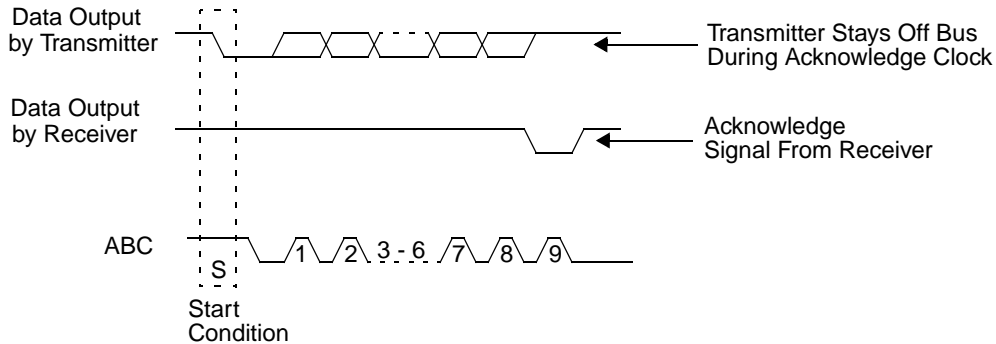


Figure 5-16. ACCESS.bus Acknowledge Cycle

### 5.7.4 Acknowledge After Every Byte Rule

According to this rule, the master generates an acknowledge clock pulse after each byte transfer, and the receiver sends an acknowledge signal after every byte received. There are two exceptions to this rule:

- When the master is the receiver, it must indicate to the transmitter the end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the ABD line is not pulled down.
- When the receiver is full, otherwise occupied, or a problem has occurred, it sends a negative acknowledge to indicate that it cannot accept additional data bytes.

### 5.7.5 Addressing Transfer Formats

Each device on the bus has a unique address. Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the ABD line, once it recognizes its address.

The address consists of the first 7 bits after a Start Condition. The direction of the data transfer (R/W#) depends on the bit sent after the address, the eighth bit. A low-to-high transition during a ABC high period indicates the Stop Condition, and ends the transaction of ABD (see Figure 5-17).

When the address is sent, each device in the system compares this address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending on the state of the R/W# bit (1 = Read, 0 = Write), the device acts either as a transmitter or a receiver.

The I<sup>2</sup>C bus protocol allows a general call address to be sent to all slaves connected to the bus. The first byte sent specifies the general call address (00h) and the second byte specifies the meaning of the general call (for example, write slave address by software only). Those slaves that require data acknowledge the call, and become slave receivers; other slaves ignore the call.

### 5.7.6 Arbitration on the Bus

Multiple master devices on the bus require arbitration between their conflicting bus access demands. Control of the bus is initially determined according to address bits and clock cycle. If the masters are trying to address the same slave, data comparisons determine the outcome of this arbitration. In master mode, the device immediately aborts a transaction if the value sampled on the ABD line differs from the value driven by the device. (An exception to this rule is ABD while receiving data. The lines may be driven low by the slave without causing an abort.)

The ABC signal is monitored for clock synchronization and to allow the slave to stall the bus. The actual clock period is set by the master with the longest clock period, or by the slave stall period. The clock high period is determined by the master with the shortest clock high period.

When an abort occurs during the address transmission, a master that identifies the conflict should give up the bus, switch to slave mode and continue to sample ABD to check if it is being addressed by the winning master on the bus.

### 5.7.7 Master Mode

#### Requesting Bus Mastership

An ACCESS.bus transaction starts with a master device requesting bus mastership. It asserts a Start Condition, followed by the address of the device it wants to access. If this transaction is successfully completed, the software may assume that the device has become the bus master.

For the device to become the bus master, the software should perform the following steps:

- 1) Configure ACBCTL1[2] to the desired operation mode. (Polling or Interrupt) and set the ACBCTL1[0]. This causes the ACB to issue a Start Condition on the ACCESS.bus when the ACCESS.bus becomes free (ACBCST[1] is cleared, or other conditions that can delay start). It then stalls the bus by holding ABC low.
- 2) If a bus conflict is detected (i.e., another device pulls down the ABC signal), the ACBST[5] is set.
- 3) If there is no bus conflict, ACBST[1] and ACBST[6] are set.
- 4) If the ACBCTL1[2] is set and either ACBST[5] or ACBST[6] is set, an interrupt is issued.

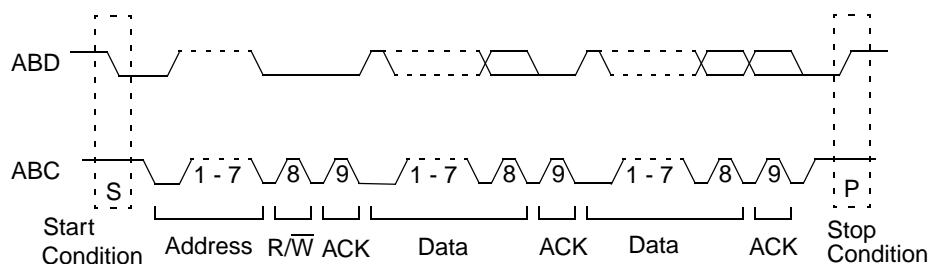


Figure 5-17. A Complete ACCESS.bus Data Transaction

### Sending the Address Byte

When the device is the active master of the ACCESS.bus (ACBST[1] is set), it can send the address on the bus.

The address sent should not be the device's own address, as defined by ACBADDR[6:0] if ACBADDR[7] is set, nor should it be the global call address if ACBST[3] is set.

To send the address byte, use the following sequence:

- 1) For a receive transaction where the software wants only one byte of data, it should set ACBCTL1[4]. If only an address needs to be sent or if the device requires stall for some other reason, set ACBCTL1[7].
- 2) Write the address byte (7-bit target device address) and the direction bit to the ACBSDA register. This causes the ACB to generate a transaction. At the end of this transaction, the acknowledge bit received is copied to ACBST[4]. During the transaction, the ABD and ABC lines are continuously checked for conflict with other devices. If a conflict is detected, the transaction is aborted, ACBST[5] is set and ACBST[1] is cleared.
- 3) If ACBCTL1[7] is set and the transaction was successfully completed (i.e., both ACBST[5] and ACBST[4] are cleared), ACBST[3] is set. In this case, the ACB stalls any further ACCESS.bus operations (i.e., holds ABC low). If ACBCTL1[2] is set, it also sends an interrupt request to the host.
- 4) If the requested direction is transmit and the start transaction was completed successfully (i.e., neither ACBST[5] nor ACBST[4] is set, and no other master has accessed the device), ACBST[6] is set to indicate that the ACB awaits attention.
- 5) If the requested direction is receive, the start transaction was completed successfully and ACBCTL1[7] is cleared, the ACB starts receiving the first byte automatically.
- 6) Check that both ACBST[5] and ACBST[4] are cleared. If ACBCTL1[2] is set, an interrupt is generated when ACBST[5] or ACBST[4] is set.

### Master Transmit

After becoming the bus master, the device can start transmitting data on the ACCESS.bus.

To transmit a byte in an interrupt or polling controlled operation, the software should:

- 1) Check that both ACBST[5] and ACBST[4] are cleared, and that ACBST[6] is set. If ACBCTL1[7] is set, also check that ACBST[3] is cleared (and clear it if required).
- 2) Write the data byte to be transmitted to the ACBSDA.

When either ACBST[5] or ACBST[4] is set, an interrupt is generated. When the slave responds with a negative acknowledge, ACBST[4] Register is set and ACBST[6] remains cleared. In this case, if ACBCTL1[2] Register is set, an interrupt is issued.

### Master Receive

After becoming the bus master, the device can start receiving data on the ACCESS.bus.

To receive a byte in an interrupt or polling operation, the software should:

- 1) Check that ACBST[6] is set and that ACBST[5] is cleared. If ACBCTL1[7] is set, also check that the ACBST[3] is cleared (and clear it if required).
- 2) Set ACBCTL1[4] to 1, if the next byte is the last byte that should be read. This causes a negative acknowledge to be sent.
- 3) Read the data byte from the ACBSDA.

Before receiving the last byte of data, set ACBCTL1[4].

#### 5.7.7.1 Master Stop

To end a transaction, set the ACBCTL1[1] before clearing the current stall flag (i.e., ACBST[6], ACBST[4], or ACBST[3]). This causes the ACB to send a Stop Condition immediately, and to clear ACBCTL1[1]. A Stop Condition may be issued only when the device is the active bus master (i.e., ACBST[1] is set).

### Master Bus Stall

The ACB can stall the ACCESS.bus between transfers while waiting for the host response. The ACCESS.bus is stalled by holding the AB1C signal low after the acknowledge cycle. Note that this is interpreted as the beginning of the following bus operation. The user must make sure that the next operation is prepared before the flag that causes the bus stall is cleared.

The flags that can cause a bus stall in master mode are:

- Negative acknowledge after sending a byte (ACBST[4] = 1).
- ACBST[6] bit is set.
- ACBCTL1[7] = 1, after a successful start (ACBST[3] = 1).

### Repeated Start

A repeated start is performed when the device is already the bus master (ACBST[1] is set). In this case, the ACCESS.bus is stalled and the ACB awaits host handling due to: negative acknowledge (ACBST[4] = 1), empty buffer (ACBST[6] = 1) and/or a stall after start (ACBST[3] = 1).

For a repeated start:

- 1) Set ACBCTL1[0] to 1.
- 2) In master receive mode, read the last data item from ACBSDA.
- 3) Follow the address send sequence, as described previously in "Sending the Address Byte". If the ACB was awaiting handling due to ACBST[3] = 1, clear it only after writing the requested address and direction to ACBSDA.

### Master Error Detection

The ACB detects illegal Start or Stop Conditions (i.e., a Start or Stop Condition within the data transfer, or the acknowledge cycle) and a conflict on the data lines of the ACCESS.bus. If an illegal condition is detected, ACBST[5] is set, and master mode is exited (ACBST[1] is cleared).

### Bus Idle Error Recovery

When a request to become the active bus master or a restart operation fails, ACBST[5] is set to indicate the error. In some cases, both the device and the other device may identify the failure and leave the bus idle. In this case, the start sequence may be incomplete and the ACCESS.bus may remain deadlocked.

To recover from deadlock, use the following sequence:

- 1) Clear ACBST[5] and ACBCST[1].
- 2) Wait for a timeout period to check that there is no other active master on the bus (i.e., ACBCST[1] remains cleared).
- 3) Disable, and re-enable the ACB to put it in the non-addressed slave mode. This completely resets the functional block.

At this point, some of the slaves may not identify the bus error. To recover, the ACB becomes the bus master: it asserts a Start Condition, sends an address byte, then asserts a Stop Condition which synchronizes all the slaves.

### 5.7.8 Slave Mode

A slave device waits in idle mode for a master to initiate a bus transaction. Whenever the ACB is enabled and it is not acting as a master (i.e., ACBST[1] is cleared), it acts as a slave device.

Once a Start Condition on the bus is detected, the device checks whether the address sent by the current master matches either:

- The ACBADDR[6:0] value if ACBADDR[7] = 1.

or

- The general call address if ACBCTL1[5] = 1.

This match is checked even when ACBST[1] is set. If a bus conflict (on ABD or ABC) is detected, ACBST[5] is set, ACBST[1] is cleared and the device continues to search the received message for a match.

If an address match or a global match is detected:

- 1) The device asserts its ABD pin during the acknowledge cycle.
- 2) ACBCST[2] and ACBST[2] are set. If ACBST[0] = 1 (i.e., slave transmit mode) ACBST[6] is set to indicate that the buffer is empty.

- 3) If ACBCTL1[2] is set, an interrupt is generated if both ACBCTL1[2] and ACBCTL16 are set.
- 4) The software then reads ACBST[0] to identify the direction requested by the master device. It clears ACBST[2] so future byte transfers are identified as data bytes.

### Slave Receive and Transmit

Slave receive and transmit are performed after a match is detected and the data transfer direction is identified. After a byte transfer, the ACB extends the acknowledge clock until the software reads or writes ACBSDA. The receive and transmit sequences are identical to those used in the master routine.

### Slave Bus Stall

When operating as a slave, the device stalls the ACCESS.bus by extending the first clock cycle of a transaction in the following cases:

- ACBST[6] is set.
- ACBST[2] and ACBCTL1[6] are set.

### Slave Error Detection

The ACB detects illegal Start and Stop Conditions on the ACCESS.bus (i.e., a Start or Stop Condition within the data transfer or the acknowledge cycle). When this occurs, ACBST[5] is set and ACBCST[3:2] are cleared, setting the ACB as an unaddressed slave.

### 5.7.9 Configuration

#### ABD and ABC Signals

The ABD and ABC are open-drain signals. The device permits the user to define whether to enable or disable the internal pull-up of each of these signals.

#### ACB Clock Frequency

The ACB permits the user to set the clock frequency for the ACCESS.bus clock. The clock is set by the ACBCTL2[7:1], which determines the ABC clock period used by the device. This clock low period may be extended by stall periods initiated by the ACB or by another ACCESS.bus device. In case of a conflict with another bus master, a shorter clock high period may be forced by the other bus master until the conflict is resolved.

### 5.7.10 ACB Registers

Each functional block is associated with a Logical Device Number (LDN) (see Section 5.3.2 "Banked Logical Device Registers" on page 108). ACCESS.Bus Port 1 is assigned

as LDN 05h and ACCESS.bus Port 2 as LDN 06h. In addition to the registers listed here, there are additional configuration registers listed in Section 5.4.2.5 "LDN 05h and 06h - ACCESS.bus Ports 1 and 2" on page 119.

**Table 5-31. ACB Register Map**

| Offset | Type | Name                              | Reset Value |
|--------|------|-----------------------------------|-------------|
| 00h    | R/W  | <b>ACBSDA.</b> ACB Serial Data    | xxh         |
| 01h    | R/W  | <b>ACBST.</b> ACB Status          | 00h         |
| 02h    | R/W  | <b>ACBCST.</b> ACB Control Status | 00h         |
| 03h    | R/W  | <b>ACBCTL1.</b> ACB Control 1     | 00h         |
| 04h    | R/W  | <b>ACBADDR.</b> ACB Own Address   | xxh         |
| 05h    | R/W  | <b>ACBCTL2.</b> ACB Control 2     | 00h         |

**Table 5-32. ACB Registers**

| Bit  | Description   |
|--|---|
| <b>Offset 00h</b> <b>ACB Serial Data Register - ACBSDA (R/W)</b> <b>Reset Value: xxh</b>   |   |
| 7:0  | <b>ACB Serial Data.</b> This shift register is used to transmit and receive data. The most significant bit is transmitted (received) first, and the least significant bit is transmitted last. Reading or writing to ACBSDA is allowed only when ACBST[6] is set, or for repeated starts after setting the ACBCTL1[0]. An attempt to access the register in other cases may produce unpredictable results.  |
| <b>Offset 01h</b> <b>ACB Status Register - ACBST (R/W)</b> <b>Reset Value: 00h</b>   |   |
| This is a read register with a special clear. Some of its bits may be cleared by software, as described below. This register maintains the current ACB status. On reset, and when the ACB is disabled, ACBST is cleared (00h). |   |
| 7  | <b>SLVSTP (Slave Stop). (R/W1C)</b> Writing 0 to SLVSTP is ignored.<br>0: Writing 1 or ACB disabled.<br>1: Stop Condition detected after a slave transfer in which ACBCST[2] or ACBCST[3] was set.  |
| 6  | <b>SDAST (SDA Status). (RO)</b><br>0: Reading from ACBSDA during a receive, or when writing to it during a transmit. When ACBCTL1[0] is set, reading ACBSDA does not clear SDAST. This enables ACB to send a repeated start in master receive mode.<br>1: SDA Data Register awaiting data (transmit - master or slave) or holds data that should be read (receive - master or slave).   |
| 5  | <b>BER (Bus Error). (R/W1C)</b> Writing 0 to this bit is ignored.<br>0: Writing 1 or ACB disabled.<br>1: Start or Stop Condition detected during data transfer (i.e., Start or Stop Condition during the transfer of bits [8:2] and acknowledge cycle), or when an arbitration problem detected.  |
| 4  | <b>NEGACK (Negative Acknowledge). (R/W1C)</b> Writing 0 to this bit is ignored.<br>0: Writing 1 or ACB disabled.<br>1: Transmission not acknowledged on the ninth clock (In this case, SDAST (bit 6) is not set).   |
| 3  | <b>STASTR (Stall After Start). (R/W1C)</b> Writing 0 to this bit is ignored.<br>0: Writing 1 or ACB disabled.<br>1: Address sent successfully (i.e., a Start Condition sent without a bus error, or Negative Acknowledge), if ACBCTL1[7] is set. This bit is ignored in slave mode. When STASTR is set, it stalls the ACCESS.bus by pulling down the ABC line, and suspends any further action on the bus (e.g., receive of first byte in master receive mode). In addition, if ACBCTL1[1] is set, it also causes the ACB to send an interrupt. |

Table 5-32. ACB Registers (Continued)

| Bit   | Description   |
|---|---|
| 2   | <b>NMATCH (New Match). (R/W1C)</b> Writing 0 to this bit is ignored. If ACBCTL1[2] is set, an interrupt is sent when this bit is set.<br>0: Software writes 1 to this bit.<br>1: Address byte follows a Start Condition or a repeated start, causing a match or a global-call match.  |
| 1   | <b>MASTER. (RO)</b><br>0: Arbitration loss (BER, bit 5, is set) or recognition of a Stop Condition.<br>1: Bus master request succeeded and master mode active.  |
| 0   | <b>XMIT (Transmit). (RO)</b> Direction bit.<br>0: Master/slave transmit mode not active.<br>1: Master/slave transmit mode active.   |
| <b>Offset 02h ACB Control Status Register - ACBCST (R/W) Reset Value: 00h</b>   |   |
| This register configures and controls the ACB functional block. It maintains the current ACB status and controls several ACB functions. On reset and when the ACB is disabled, the non-reserved bits of ACBCST are cleared. |   |
| 7:6   | <b>Reserved.</b>  |
| 5   | <b>TGABC (Toggle ABC Line). (R/W)</b> Enables toggling the ABC line during error recovery.<br>0: Clock toggle completed.<br>1: When the ABD line is low, writing 1 to this bit toggles the ABC line for one cycle. Writing 1 to TGABC while ABD is high is ignored.   |
| 4   | <b>TSDA (Test ABD Line). (RO)</b> Reads the current value of the ABD line. It can be used while recovering from an error condition in which the ABD line is constantly pulled low by an out-of-sync slave. Data written to this bit is ignored.   |
| 3   | <b>GCMTCH (Global Call Match). (RO)</b><br>0: Start Condition or repeated Start and a Stop Condition (including illegal Start or Stop Condition).<br>1: In slave mode, ACBCTL1.GCMEN is set and the address byte (the first byte transferred after a Start Condition) is 00h.   |
| 2   | <b>MATCH (Address Match). (RO)</b><br>0: Start Condition or repeated Start and a Stop Condition (including illegal Start or Stop Condition).<br>1: ACBADDR[7] is set and the first 7 bits of the address byte (the first byte transferred after a Start Condition) match the 7-bit address in ACBADDR.  |
| 1   | <b>BB (Bus Busy). (R/W1C)</b><br>0: Writing 1, ACB disabled, or Stop Condition detected.<br>1: Bus active (a low level on either ABD or ABC), or Start Condition.   |
| 0   | <b>BUSY. (RO)</b> This bit should always be written 0. This bit indicates the period between detecting a Start Condition and completing receipt of the address byte. After this, the ACB is either free or enters slave mode.<br>0: Completion of any state below or ACB disabled.<br>1: ACB is in one of the following states:<br>-Generating a Start Condition<br>-Master mode (ACBST[1] is set)<br>-Slave mode (ACBCST[2] or ACBCST[3] set). |
| <b>Offset 03h ACB Control Register 1 - ACBCTL1 (R/W) Reset Value: 00h</b>   |   |
| 7   | <b>STASTRE (Stall After Start Enable).</b><br>0: When cleared, ACBST[3] can not be set. However, if ACBST[3] is set, clearing STASTRE does not clear ACBST[3].<br>1: Stall after start mechanism enabled, and ACB stalls the bus after the address byte.  |
| 6   | <b>NMINTE (New Match Interrupt Enable).</b><br>0: No interrupt issued on a new match.<br>1: Interrupt issued on a new match only if ACBCTL1[2] set.   |
| 5   | <b>GCMEN (Global Call Match Enable).</b><br>0: Global call match disabled.<br>1: Global call match enabled.   |

Table 5-32. ACB Registers (Continued)

| Bit   | Description  |
|---|--|
| 4   | <b>ACK (Acknowledge).</b> This bit is ignored in transmit mode. When the device acts as a receiver (slave or master), this bit holds the stop transmitting instruction that is transmitted during the next acknowledge cycle.<br>0: Cleared after acknowledge cycle.<br>1: Negative acknowledge issued on next received byte.  |
| 3   | <b>Reserved.</b>   |
| 2   | <b>INTEN (Interrupt Enable).</b><br>0: ACB interrupt disabled.<br>1: ACB interrupt enabled. An interrupt is generated in response to one of the following events:<br>-Detection of an address match (ACBST[2] = 1) and ACBCTL1[6] = 1.<br>-Receipt of Bus Error (ACBST[5] = 1).<br>-Receipt of Negative Acknowledge after sending a byte (ACBST[4] = 1).<br>-Acknowledge of each transaction (same as the hardware set of the ACBST[6]).<br>-In master mode if ACBCTL1[7] = 1, after a successful start (ACBST[3] = 1).<br>-Detection of a Stop Condition while in slave mode (ACBST[7] = 1).  |
| 1   | <b>STOP (Stop).</b><br>0: Automatically cleared after Stop issued.<br>1: Setting this bit in master mode generates a Stop Condition to complete or abort current message transfer.   |
| 0   | <b>START (Start).</b> Set this bit only when in master mode or when requesting master mode.<br>0: Cleared after Start Condition sent or Bus Error (ACBST[5] = 1) detected.<br>1: Single or repeated Start Condition generated on the ACCESS.bus. If the device is not the active master of the bus (ACBST[1] = 0), setting START generates a Start Condition when the ACCESS.bus becomes free (ACBCST[1] = 0). An address transmission sequence should then be performed.<br><br>If the device is the active master of the bus (ACBST[1] = 1), setting START and then writing to ACBSDA generates a Start Condition. If a transmission is already in progress, a repeated Start Condition is generated. This condition can be used to switch the direction of the data flow between the master and the slave, or to choose another slave device without separating them with a Stop Condition. |
| <b>Offset 04h ACB Own Address Register - ACBADDR (R/W) Reset Value: xxh</b>   |  |
| 7   | <b>SAEN (Slave Address Enable).</b><br>0: ACB does not check for an address match with ACBADDR[6:0].<br>1: ACBADDR[6:0] holds a valid address and enables the match of ADDR to an incoming address byte.   |
| 6:0   | <b>ADDR (Address).</b> These bits hold the 7-bit device address of the SC3200. When in slave mode, the first 7 bits received after a Start Condition are compared with this field (first bit received is compared with bit 6, and the last bit with bit 0). If the address field matches the received data and ACBADDR[7] is 1, a match is declared.   |
| <b>Offset 05h ACB Control Register 2 - ACBCTL2 (R/W) Reset Value: 00h</b><br>This register enables/disables the functional block and determines the ACB clock rate. |  |
| 7:1   | <b>ABCFRQ (ABC Frequency).</b> This field defines the ABC period (low and high time) when the device serves as a bus master. The clock low and high times are defined as follows:<br>$t_{ABCl} = t_{ABCh} = 2 \cdot \text{ABCFRQ} \cdot t_{CLK}$<br>where $t_{CLK}$ is the module input clock cycle, as defined in the Section 5.2 "Module Architecture" on page 107.<br>ABCFRQ can be programmed to values in the range of 0001000b through 1111111b. Using any other value has unpredictable results.  |
| 0   | <b>EN (Enable).</b><br>0: ACB is disabled, ACBCTL1, ACBST and ACBCST registers are cleared, and clocks are halted.<br>1: ACB is enabled.   |



## 5.8 Legacy Functional Blocks

This section briefly describes the following blocks that provide legacy device functions:

- Parallel Port. (Similar to Parallel Port in the National Semiconductor PC87338.)
- Serial Port 1 and Serial Port 2 (SP1 and SP2), UART functionality for both SP1 and SP2. (Similar to SCC1 in the National Semiconductor PC87338.)
- Infrared Communications Port / Serial Port 3 functionality. (Similar to SCC2 in the National Semiconductor PC87338.)

The description of each Legacy block includes a general description, register maps, and bit maps.

### 5.8.1 Parallel Port

The Parallel Port supports all IEEE1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

#### 5.8.1.1 Parallel Port Register and Bit Maps

The Parallel Port register maps (Table 5-33 and Table 5-34) are grouped according to first and second level offsets. EPP and second level offset registers are available only when the base address is 8-byte aligned.

Parallel Port functional block bit maps are shown in Table 5-35 and Table 5-36.

**Table 5-33. Parallel Port Register Map for First Level Offset**

| First Level Offset | Type | Name                                  | Modes (ECR Bits) 7 6 5 |
|--------------------|------|---------------------------------------|------------------------|
| 000h               | R/W  | <b>DATAR.</b> PP Data                 | 000 or 001             |
| 000h               | W    | <b>AFIFO.</b> ECP Address FIFO        | 011                    |
| 001h               | RO   | <b>DSR.</b> Status                    | All Modes              |
| 002h               | R/W  | <b>DCR.</b> Control                   | All Modes              |
| 003h               | R/W  | <b>ADDR.</b> EPP Address              | 100                    |
| 004h               | R/W  | <b>DATA0.</b> EPP Data Port 0         | 100                    |
| 005h               | R/W  | <b>DATA1.</b> EPP Data Port 1         | 100                    |
| 006h               | R/W  | <b>DATA2.</b> EPP Data Port 2         | 100                    |
| 007h               | R/W  | <b>DATA3.</b> EPP Data Port 3         | 100                    |
| 400h               | W    | <b>CFIFO.</b> PP Data FIFO            | 010                    |
| 400h               | R/W  | <b>DFIFO.</b> ECP Data FIFO           | 011                    |
| 400h               | R/W  | <b>TFIFO.</b> Test FIFO               | 110                    |
| 400h               | RO   | <b>CNFGA.</b> Configuration A         | 111                    |
| 401h               | RO   | <b>CNFGB.</b> Configuration B         | 111                    |
| 402h               | R/W  | <b>ECR.</b> Extended Control          | All Modes              |
| 403h               | R/W  | <b>EIR.</b> Extended Index            | All Modes              |
| 404h               | R/W  | <b>EDR.</b> Extended Data             | All Modes              |
| 405h               | R/W  | <b>EAR.</b> Extended Auxiliary Status | All Modes              |

**Table 5-34. Parallel Port Register Map for Second Level Offset**

| Second Level Offset | Type | Name  |
|---------------------|------|---|
| 00h                 | R/W  | <b>Control0.</b> Control Register 0                       |
| 02h                 | R/W  | <b>Control2.</b> Control Register 2                       |
| 04h                 | R/W  | <b>Control4.</b> Control Register 4                       |
| 05h                 | R/W  | <b>PP Config0.</b> Parallel Port Configuration Register 0 |

Table 5-35. Parallel Port Bit Map for First Level Offset

| Offset | Name  | Bits  |                         |                   |                    |                     |                                |                             |                     |  |
|--------|-------|---|-------------------------|-------------------|--------------------|---------------------|--------------------------------|-----------------------------|---------------------|--|
|        |       | 7   | 6                       | 5                 | 4                  | 3                   | 2                              | 1                           | 0                   |  |
| 000h   | DATAR | Data Bits                                     |                         |                   |                    |                     |                                |                             |                     |  |
|        | AFIFO | Address Bits                                  |                         |                   |                    |                     |                                |                             |                     |  |
| 001h   | DSR   | Printer Status                                | ACK# Status             | PE Status         | SLCT Status        | ERR# Status         | RSVD                           |                             | EPP Timeout Status  |  |
| 002h   | DCR   | RSVD  |                         | Direction Control | Interrupt Enable   | PP Input Control    | Printer Initialization Control | Automatic Line Feed Control | Data Strobe Control |  |
| 003h   | ADDR  | EPP Device or Register Selection Address Bits |                         |                   |                    |                     |                                |                             |                     |  |
| 004h   | DATA0 | EPP Device or R/W Data                        |                         |                   |                    |                     |                                |                             |                     |  |
| 005h   | DATA1 | EPP Device or R/W Data                        |                         |                   |                    |                     |                                |                             |                     |  |
| 006h   | DATA2 | EPP Device or R/W Data                        |                         |                   |                    |                     |                                |                             |                     |  |
| 007h   | DATA3 | EPP Device or R/W Data                        |                         |                   |                    |                     |                                |                             |                     |  |
| 400h   | CFIFO | Data Bits                                     |                         |                   |                    |                     |                                |                             |                     |  |
| 400h   | DFIFO | Data Bits                                     |                         |                   |                    |                     |                                |                             |                     |  |
| 400h   | TFIFO | Data Bits                                     |                         |                   |                    |                     |                                |                             |                     |  |
| 400h   | CNFGA | RSVD  |                         |                   |                    | Bit 7 of PP Config0 | RSVD                           |                             |                     |  |
| 401h   | CNFGB | RSVD  | Interrupt Request Value | Interrupt Select  |                    |                     | RSVD                           | DMA Channel Select          |                     |  |
| 402h   | ECR   | ECP Mode Control                              |                         |                   | ECP Interrupt Mask | ECP DMA Enable      | ECP Interrupt Service          | FIFO Full                   | FIFO Empty          |  |
| 403h   | EIR   | RSVD  |                         |                   |                    | Second Level Offset |                                |                             |                     |  |
| 404h   | EDR   | Data Bits                                     |                         |                   |                    |                     |                                |                             |                     |  |
| 405h   | EAR   | FIFO Tag                                      | RSVD                    |                   |                    |                     |                                |                             |                     |  |

Table 5-36. Parallel Port Bit Map for Second Level Offset

| Offset | Name       | Bits              |                              |                        |                            |      |                            |                        |                            |
|--------|------------|-------------------|------------------------------|------------------------|----------------------------|------|----------------------------|------------------------|----------------------------|
|        |            | 7                 | 6                            | 5                      | 4                          | 3    | 2                          | 1                      | 0                          |
| 00h    | Control0   | RSVD              |                              | DCR Register Live      | Freeze Bit                 | RSVD |                            |                        | EPP Timeout Interrupt Mask |
| 02h    | Control2   | SPP Compatibility | Channel Address Enable       | RSVD                   | Revision 1.7 or 1.9 Select | RSVD |                            |                        |                            |
| 04h    | Control4   | RSVD              | PP DMA Request Inactive Time |                        |                            | RSVD | PP DMA Request Active Time |                        |                            |
| 05h    | PP Config0 | Bit 3 of CNFGA    | Demand DMA Enable            | ECP IRQ Channel Number |                            |      | PE Internal PU or PD       | ECP DMA Channel Number |                            |

## 5.8.2 UART Functionality (SP1 and SP2)

Both SP1 and SP2 provide UART functionality. The generic SP1 and SP2 support serial data communication with remote peripheral device or modem using a wired interface. The functional blocks can function as a standard 16450, 16550, or as an Extended UART.

### 5.8.2.1 UART Mode Register Bank Overview

Four register banks, each containing eight registers, control UART operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 5-18.

### 5.8.2.2 SP1 and SP2 Register and Bit Maps for UART Functionality

The tables in this subsection provide register and bit maps for Banks 0 through 3.

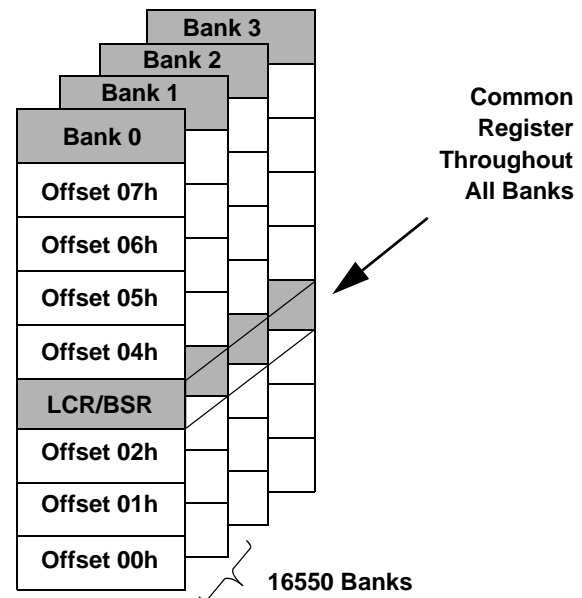


Figure 5-18. UART Mode Register Bank Architecture

Table 5-37. Bank 0 Register Map

| Offset | Type | Name   |
|--------|------|--|
| 00h    | RO   | <b>RXD.</b> Receiver Data Port                 |
|        | W    | <b>TXD.</b> Transmitter Data Port              |
| 01h    | R/W  | <b>IER.</b> Interrupt Enable                   |
| 02h    | RO   | <b>EIR.</b> Event Identification (Read Cycles) |
|        | R/W  | <b>FCR.</b> FIFO Control (Write Cycles)        |
| 03h    | W    | <b>LCR</b> <sup>1</sup> . Line Control         |
|        | R/W  | <b>BSR</b> <sup>1</sup> . Bank Select          |
| 04h    | R/W  | <b>MCR.</b> Modem/Mode Control                 |
| 05h    | R/W  | <b>LSR.</b> Link Status                        |
| 06h    | R/W  | <b>MSR.</b> Modem Status                       |
| 07h    | R/W  | <b>SPR.</b> Scratchpad                         |
|        | R/W  | <b>ASCR.</b> Auxiliary Status and Control      |

1. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-38.

Table 5-38. Bank Selection Encoding

| BSR Bits |   |   |   |   |   |   |   | Bank Selected |
|----------|---|---|---|---|---|---|---|---------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |               |
| 0        | x | x | x | x | x | x | x | 0             |
| 1        | 0 | x | x | x | x | x | x | 1             |
| 1        | 1 | x | x | x | x | 1 | x | 1             |
| 1        | 1 | x | x | x | x | x | 1 | 1             |
| 1        | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 2             |
| 1        | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 3             |

Table 5-39. Bank 1 Register Map

| Offset  | Type | Name  |
|---------|------|---|
| 00h     | R/W  | <b>LBGD(L)</b> . Legacy Baud Generator Divisor Port (Low Byte)  |
| 01h     | R/W  | <b>LBGD(H)</b> . Legacy Baud Generator Divisor Port (High Byte) |
| 02h     | ---  | <b>RSVD</b> . Reserved  |
| 03h     | W    | <b>LCR</b> <sup>1</sup> . Line Control                          |
|         | R/W  | <b>BSR</b> <sup>1</sup> . Bank Select                           |
| 04h-07h | ---  | <b>RSVD</b> . Reserved  |

1. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-38 on page 148.

Table 5-40. Bank 2 Register Map

| Offset | Type | Name  |
|--------|------|---|
| 00h    | R/W  | <b>BGD(L)</b> . Baud Generator Divisor Port (Low Byte)  |
| 01h    | R/W  | <b>BGD(H)</b> . Baud Generator Divisor Port (High Byte) |
| 02h    | R/W  | <b>EXCR1</b> . Extended Control 1                       |
| 03h    | R/W  | <b>BSR</b> . Bank Select                                |
| 04h    | R/W  | <b>EXCR2</b> . Extended Control 2                       |
| 05h    | ---  | <b>RSVD</b> . Reserved                                  |
| 06h    | RO   | <b>RXFLV</b> . RX_FIFO Level                            |
| 07h    | RO   | <b>TXFLV</b> . TX_FIFO Level                            |

Table 5-41. Bank 3 Register Map

| Offset  | Type | Name                                   |
|---------|------|--|
| 00h     | RO   | <b>MRID</b> . Module and Revision ID   |
| 01h     | RO   | <b>SH_LCR</b> . Shadow of LCR          |
| 02h     | RO   | <b>SH_FCR</b> . Shadow of FIFO Control |
| 03h     | R/W  | <b>BSR</b> . Bank Select               |
| 04h-07h | ---  | <b>RSVD</b> . Reserved                 |

Table 5-42. Bank 0 Bit Map

| Register |                   | Bits                             |                        |                    |  |                  |                      |          |          |
|----------|-------------------|----------------------------------|------------------------|--------------------|--|------------------|----------------------|----------|----------|
| Offset   | Name              | 7                                | 6                      | 5                  | 4  | 3                | 2                    | 1        | 0        |
| 00h      | RXD               | RXD[7:0] (Receiver Data Bits)    |                        |                    |  |                  |                      |          |          |
|          | TXD               | TXD[7:0] (Transmitter Data Bits) |                        |                    |  |                  |                      |          |          |
| 01h      | IER <sup>1</sup>  | RSVD                             |                        |                    |  | MS_IE            | LS_IE                | TXLDL_IE | RXHDL_IE |
|          | IER <sup>2</sup>  | RSVD                             |                        | TXEMP_IE           | RSVD <sup>3</sup> /<br>DMA_IE <sup>4</sup> | MS_IE            | LS_IE                | TXLDL_IE | RXHDL_IE |
| 02h      | EIR <sup>1</sup>  | FEN[1:0]                         |                        | RSVD               |  | RXFT             | IPR1                 | IPR0     | IPF      |
|          | EIR <sup>2</sup>  | RSVD                             |                        | TXEMP_EV           | RSVD <sup>3</sup> /<br>DMA_EV <sup>4</sup> | MS_EV            | LS_EV or<br>TXHLT_EV | TXLDL_EV | RXHDL_EV |
|          | FCR               | RXFTH[1:0]                       |                        | TXFTH[1:0]         |  | RSVD             | TXSR                 | RXSR     | FIFO_EN  |
| 03h      | LCR <sup>5</sup>  | BKSE                             | SBRK                   | STKP               | EPS  | PEN              | STB                  | WLS[1:0] |          |
|          | BSR <sup>5</sup>  | BKSE                             | BSR[6:0] (Bank Select) |                    |  |                  |                      |          |          |
| 04h      | MCR <sup>1</sup>  | RSVD                             |                        |                    | LOOP                                       | ISEN or<br>DCDLP | RILP                 | RTS      | DTR      |
|          | MCR <sup>2</sup>  | RSVD                             |                        |                    |  | TX_DFR           | RSVD                 | RTS      | DTR      |
| 05h      | LSR               | ER_INF                           | TXEMP                  | TXRDY              | BRK  | FE               | PE                   | OE       | RXDA     |
| 06h      | MSR               | DCD                              | RI                     | DSR                | CTS  | DDCD             | TERI                 | DDSR     | DCTS     |
| 07h      | SPR <sup>1</sup>  | Scratch Data                     |                        |                    |  |                  |                      |          |          |
|          | ASCR <sup>2</sup> | RSVD                             | TXUR <sup>4</sup>      | RXACT <sup>4</sup> | RXWDG <sup>4</sup>                         | RSVD             | S_OET <sup>4</sup>   | RSVD     | RXF_TOUT |

1. Non-Extended Mode.
2. Extended Mode.
3. In SP1 only.
4. In SP2 only.
5. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-38 on page 148.

Table 5-43. Bank 1 Bit Map

| Register |                  | Bits                   |                        |      |     |     |     |          |   |
|----------|------------------|------------------------|------------------------|------|-----|-----|-----|----------|---|
| Offset   | Name             | 7                      | 6                      | 5    | 4   | 3   | 2   | 1        | 0 |
| 00h      | LBGD(L)          | LBGD[7:0] (Low Byte)   |                        |      |     |     |     |          |   |
| 01h      | LBGD(H)          | LBGD[15:8] (High Byte) |                        |      |     |     |     |          |   |
| 02h      | RSVD             | Reserved               |                        |      |     |     |     |          |   |
| 03h      | LCR <sup>1</sup> | BKSE                   | SBRK                   | STKP | EPS | PEN | STB | WLS[1:0] |   |
|          | BSR <sup>1</sup> | BKSE                   | BSR[6:0] (Bank Select) |      |     |     |     |          |   |
| 04h-07h  | RSVD             | Reserved               |                        |      |     |     |     |          |   |

1. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-38 on page 148.

Table 5-44. Bank 2 Bit Map

| Register |        | Bits                   |                        |            |          |      |   |        |   |
|----------|--------|------------------------|------------------------|------------|----------|------|---|--------|---|
| Offset   | Name   | 7                      | 6                      | 5          | 4        | 3    | 2 | 1      | 0 |
| 00h      | BGD(L) | BGD[7:0] (Low Byte)    |                        |            |          |      |   |        |   |
| 01h      | BGD(H) | BGD [15:8] (High Byte) |                        |            |          |      |   |        |   |
| 02h      | EXCR1  | BTEST                  | RSVD                   | ETDLBK     | LOOP     | RSVD |   | EXT_SL |   |
| 03h      | BSR    | BKSE                   | BSR[6:0] (Bank Select) |            |          |      |   |        |   |
| 04h      | EXCR2  | LOCK                   | RSVD                   | PRESL[1:0] |          | RSVD |   |        |   |
| 05h      | RSVD   | Reserved               |                        |            |          |      |   |        |   |
| 06h      | RXFLV  | RSVD                   |                        |            | RFL[4:0] |      |   |        |   |
| 07h      | TXFLV  | RSVD                   |                        |            | TFL[4:0] |      |   |        |   |

Table 5-45. Bank 3 Bit Map

| Register |        | Bits       |                        |            |     |          |      |          |         |
|----------|--------|------------|------------------------|------------|-----|----------|------|----------|---------|
| Offset   | Name   | 7          | 6                      | 5          | 4   | 3        | 2    | 1        | 0       |
| 00h      | MRID   | MID[3:0]   |                        |            |     | RID[3:0] |      |          |         |
| 01h      | SH_LCR | BKSE       | SBRK                   | STKP       | EPS | PEN      | STB  | WLS[1:0] |         |
| 02h      | SH_FCR | RXFTH[1:0] |                        | TXFHT[1:0] |     | RSVD     | TXSR | RXSR     | FIFO_EN |
| 03h      | BSR    | BKSE       | BSR[6:0] (Bank Select) |            |     |          |      |          |         |
| 04h-07h  | RSVD   | RSVD       |                        |            |     |          |      |          |         |

### 5.8.3 IR Communications Port (IRCP) / Serial Port 3 (SP3) Functionality

This section describes the IRCP/SP3 support registers. The IRCP/SP3 functional block provides advanced, versatile serial communications features with IR capabilities.

The IRCP/SP3 also supports two DMA channels; the functional block can use either one or both of them. One channel is required for IR-based applications, since IR communication works in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex IR based applications.

The IRCP or Serial Port 3 is chosen via bit 6 of the PMR Register (see Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88).

#### 5.8.3.1 IR/SP3 Mode Register Bank Overview

Eight register banks, each containing eight registers, control IR/SP3 operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 5-19.

#### 5.8.3.2 IRCP/SP3 Register and Bit Maps

The tables in this subsection provide register and bit maps for Banks 0 through 7.

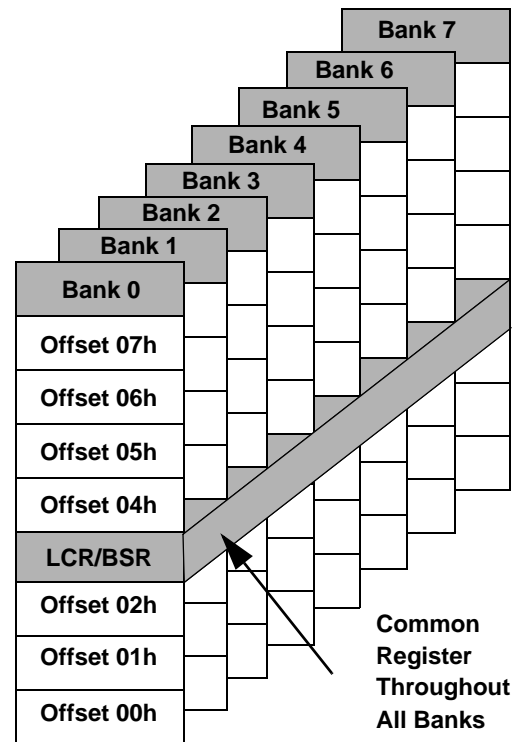


Figure 5-19. IRCP/SP3 Register Bank Architecture

Table 5-46. Bank 0 Register Map

| Offset | Type | Name                                      |
|--------|------|---|
| 00h    | RO   | <b>RXD.</b> Receive Data Port             |
|        | W    | <b>TXD.</b> Transmit Data Port            |
| 01h    | R/W  | <b>IER.</b> Interrupt Enable              |
| 02h    | RO   | <b>EIR.</b> Event Identification          |
|        | R/W  | <b>FCR.</b> FIFO Control                  |
| 03h    | W    | <b>LCR</b> <sup>1</sup> . Link Control    |
|        | R/W  | <b>BSR</b> <sup>1</sup> . Bank Select     |
| 04h    | R/W  | <b>MCR.</b> Modem/Mode Control            |
| 05h    | R/W  | <b>LSR.</b> Link Status                   |
| 06h    | R/W  | <b>MSR.</b> Modem Status                  |
| 07h    | R/W  | <b>SPR.</b> Scratchpad                    |
|        | R/W  | <b>ASCR.</b> Auxiliary Status and Control |

1. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-47.

Table 5-47. Bank Selection Encoding

| BSR Bits |   |   |   |   |   |   |   | Bank Selected | Functionality |
|----------|---|---|---|---|---|---|---|---------------|---------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |               |               |
| 0        | x | x | x | x | x | x | x | 0             | UART + IR     |
| 1        | 0 | x | x | x | x | x | x | 1             |               |
| 1        | 1 | x | x | x | x | 1 | x | 1             |               |
| 1        | 1 | x | x | x | x | x | 1 | 1             |               |
| 1        | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 2             |               |
| 1        | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 3             |               |
| 1        | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 4             | IR Only       |
| 1        | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 5             |               |
| 1        | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 6             |               |
| 1        | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 7             |               |

Table 5-48. Bank 1 Register Map

| Offset  | Type | Name  |
|---------|------|---|
| 00h     | R/W  | <b>LBGD(L)</b> . Legacy Baud Generator Divisor Port (Low Byte)  |
| 01h     | R/W  | <b>LBGD(H)</b> . Legacy Baud Generator Divisor Port (High Byte) |
| 02h     | ---  | <b>RSVD</b> . Reserved  |
| 03h     | W    | <b>LCR</b> <sup>1</sup> . Link Control                          |
|         | R/W  | <b>BSR</b> <sup>1</sup> . Bank Select                           |
| 04h-07h | ---  | <b>RSVD</b> . Reserved  |

1. When bit 7 of this register is set to 1, bits [6:0] of BSR select the bank, as shown in Table 5-47.

Table 5-49. Bank 2 Register Map

| Offset | Type | Name  |
|--------|------|---|
| 00h    | R/W  | <b>BGD(L)</b> . Baud Generator Divisor Port (Low Byte)  |
| 01h    | R/W  | <b>BGD(H)</b> . Baud Generator Divisor Port (High Byte) |
| 02h    | R/W  | <b>EXCR1</b> . Extended Control 1                       |
| 03h    | R/W  | <b>BSR</b> . Bank Select                                |
| 04h    | R/W  | <b>EXCR2</b> . Extended Control 2                       |
| 05h    | ---  | <b>RSVD</b> . Reserved                                  |
| 06h    | RO   | <b>TXFLV</b> . TX FIFO Level                            |
| 07h    | RO   | <b>RXFLV</b> . RX FIFO Level                            |



Table 5-50. Bank 3 Register Map

| Offset  | Type | Name   |
|---------|------|--|
| 00h     | RO   | <b>MID.</b> Module and Revision Identification |
| 01h     | RO   | <b>SH_LCR.</b> Link Control Shadow             |
| 02h     | RO   | <b>SH_FCR.</b> FIFO Control Shadow             |
| 03h     | R/W  | <b>BSR.</b> Bank Select                        |
| 04h-07h | ---  | <b>RSVD.</b> Reserved                          |

Table 5-51. Bank 4 Register Map

| Offset | Type | Name  |
|--------|------|---|
| 00h    | RO   | <b>TMR(L).</b> Timer (Low Byte)                             |
| 01h    | RO   | <b>TMR(H).</b> Timer (High Byte)                            |
| 02h    | R/W  | <b>IRCR1.</b> IR Control 1                                  |
| 03h    | R/W  | <b>BSR.</b> Bank Select                                     |
| 04h    | R/W  | <b>TFRL(L).</b> Transmission Frame Length (Low Byte)        |
|        | RO   | <b>TFRCC(L).</b> Transmission Current Count (Low Byte)      |
| 05h    | R/W  | <b>TFRL(H).</b> Transmission Frame Length (High Byte)       |
|        | RO   | <b>TFRCC(H).</b> Transmission Current Count (High Byte)     |
| 06h    | R/W  | <b>RFRML(L).</b> Reception Frame Maximum Length (Low Byte)  |
|        | RO   | <b>RFRCC(L).</b> Reception Frame Current Count (Low Byte)   |
| 07h    | R/W  | <b>RFRML(H).</b> Reception Frame Maximum Length (High Byte) |
|        | RO   | <b>RFRCC(H).</b> Reception Frame Current Count (High Byte)  |

Table 5-52. Bank 5 Register Map

| Offset | Type | Name  |
|--------|------|---|
| 00h    | R/W  | <b>SPR3.</b> Scratchpad 2                         |
| 01h    | R/W  | <b>SPR3.</b> Scratchpad 3                         |
| 02h    | R/W  | <b>RSVD.</b> Reserved                             |
| 03h    | R/W  | <b>BSR.</b> Bank Select                           |
| 04h    | R/W  | <b>IRCR2.</b> IR Control 2                        |
| 05h    | RO   | <b>FRM_ST.</b> Frame Status                       |
| 06h    | RO   | <b>RFRL(L).</b> Received Frame Length (Low Byte)  |
|        | RO   | <b>LSTFRC.</b> Lost Frame Count                   |
| 07h    | RO   | <b>RFRL(H).</b> Received Frame Length (High Byte) |

Table 5-53. Bank 6 Register Map

| Offset  | Type | Name   |
|---------|------|--|
| 00h     | R/W  | <b>IRCR3.</b> IR Control 3                   |
| 01h     | R/W  | <b>MIR_PW.</b> MIR Pulse Width               |
| 02h     | R/W  | <b>SIR_PW.</b> SIR Pulse Width               |
| 03h     | R/W  | <b>BSR.</b> Bank Select                      |
| 04h     | R/W  | <b>BFPL.</b> Beginning Flags/Preamble Length |
| 05h-07h | ---  | <b>RSVD.</b> Reserved                        |

Table 5-54. Bank 7 Register Map

| Offset  | Type | Name  |
|---------|------|---|
| 00h     | R/W  | <b>IRRXDC.</b> IR Receiver Demodulator Control  |
| 01h     | R/W  | <b>IRTXMC.</b> IR Transmitter Modulator Control |
| 02h     | R/W  | <b>RCCFG.</b> Consumer IR (CEIR) Configuration  |
| 03h     | R/W  | <b>BSR.</b> Bank Select                         |
| 04h     | R/W  | <b>IRCFG1.</b> IR Interface Configuration 1     |
| 05h-06h | ---  | <b>RSVD.</b> Reserved                           |
| 07h     | R/W  | <b>IRCFG4.</b> IR Interface Configuration 4     |

Table 5-55. Bank 0 Bit Map

| Register |                   | Bits                     |                        |                 |               |            |                |          |          |
|----------|-------------------|--------------------------|------------------------|-----------------|---------------|------------|----------------|----------|----------|
| Offset   | Name              | 7                        | 6                      | 5               | 4             | 3          | 2              | 1        | 0        |
| 00h      | RXD               | RXD[7:0] (Receive Data)  |                        |                 |               |            |                |          |          |
|          | TXD               | TXD[7:0] (Transmit Data) |                        |                 |               |            |                |          |          |
| 01h      | IER <sup>1</sup>  | RSVD                     |                        |                 |               | MS_IE      | LS_IE          | TXLDL_IE | RXHDL_IE |
|          | IER <sup>2</sup>  | TMR_IE                   | SFIF_IE                | TXEMP_IE/PLD_IE | DMA_IE        | MS_IE      | LS_IE          | TXLDL_IE | RXHDL_IE |
| 02h      | EIR <sup>1</sup>  | FEN[1:0]                 |                        | RSVD            |               | RXFT       | IPR[1:0]       |          | IPF      |
|          | EIR <sup>2</sup>  | TMR_EV                   | SFIF_EV                | TXEMP_EV/PLD_EV | DMA_EV        | MS_EV      | LS_EV/TXHLT_EV | TXLDL_EV | RXHDL_EV |
|          | FCR               | RXFTH[1:0]               |                        | TXFTH[1:0]      |               | RSVD       | TXSR           | RXSR     | FIFO_EN  |
| 03h      | LCR               | BKSE                     | SBRK                   | STKP            | EPS           | PEN        | STB            | WLS[1:0] |          |
|          | BSR               | BKSE                     | BSR[6:0] (Bank Select) |                 |               |            |                |          |          |
| 04h      | MCR <sup>1</sup>  | RSVD                     |                        |                 | LOOP          | ISEN/DCDLP | RILP           | RTS      | DTR      |
|          | MCR <sup>2</sup>  | MDSL[2:0]                |                        |                 | IR_PLS        | TX_DFR     | DMA_EN         | RTS      | DTR      |
| 05h      | LSR               | ER_INF/FR_END            | TXEMP                  | TXRDY           | BRK/MAX_LEN   | FE/PHY_ERR | PE/BAD_CRC     | OE       | RXDA     |
| 06h      | MSR               | DCD                      | RI                     | DSR             | CTS           | DDCD       | TERI           | DDSR     | DCTS     |
| 07h      | SPR <sup>1</sup>  | Scratch Data             |                        |                 |               |            |                |          |          |
|          | ASCR <sup>2</sup> | CTE/PLD                  | TXUR                   | RXACT/RXBSY     | RXWDG/LOST_FR | TXHFE      | S_EOT          | FEND_INF | RXF_TOUT |

1. Non-extended mode.

2. Extended mode.

Table 5-56. Bank 1 Bit Map

| Register |         | Bits                        |                        |      |     |     |     |          |   |
|----------|---------|-----------------------------|------------------------|------|-----|-----|-----|----------|---|
| Offset   | Name    | 7                           | 6                      | 5    | 4   | 3   | 2   | 1        | 0 |
| 00h      | LBGD(L) | LBGD[7:0] (Low Byte Data)   |                        |      |     |     |     |          |   |
| 01h      | LBGD(H) | LBGD[15:8] (High Byte Data) |                        |      |     |     |     |          |   |
| 02h      | RSVD    | RSVD                        |                        |      |     |     |     |          |   |
| 03h      | LCR     | BKSE                        | SBRK                   | STKP | EPS | PEN | STB | WLS[1:0] |   |
|          | BSR     | BKSE                        | BSR[6:0] (Bank Select) |      |     |     |     |          |   |
| 04h-07h  | RSVD    | RSVD                        |                        |      |     |     |     |          |   |

Table 5-57. Bank 2 Bit Map

| Register |        | Bits                       |                        |            |          |             |       |             |        |  |
|----------|--------|----------------------------|------------------------|------------|----------|-------------|-------|-------------|--------|--|
| Offset   | Name   | 7                          | 6                      | 5          | 4        | 3           | 2     | 1           | 0      |  |
| 00h      | BGD(L) | BGD[7:0] (Low Byte Data)   |                        |            |          |             |       |             |        |  |
| 01h      | BGD(H) | BGD[15:8] (High Byte Data) |                        |            |          |             |       |             |        |  |
| 02h      | EXCR1  | BTEST                      | RSVD                   | ETDLBK     | LOOP     | DMASWP      | DMATH | DMANF       | EXT_SL |  |
| 03h      | BSR    | BKSE                       | BSR[6:0] (Bank Select) |            |          |             |       |             |        |  |
| 04h      | EXCR2  | LOCK                       | RSVD                   | PRESL[1:0] |          | RF_SIZ[1:0] |       | TF_SIZ[1:0] |        |  |
| 05h      | RSVD   | RSVD                       |                        |            |          |             |       |             |        |  |
| 06h      | TXFLV  | RSVD                       |                        |            | TFL[5:0] |             |       |             |        |  |
| 07h      | RXFLV  | RSVD                       |                        |            | RFL[5:0] |             |       |             |        |  |

Table 5-58. Bank 3 Bit Map

| Register |                     | Bits       |                        |            |     |          |      |          |         |  |
|----------|---------------------|------------|------------------------|------------|-----|----------|------|----------|---------|--|
| Offset   | Name                | 7          | 6                      | 5          | 4   | 3        | 2    | 1        | 0       |  |
| 00h      | MID                 | MID[3:0]   |                        |            |     | RID[3:0] |      |          |         |  |
| 01h      | SH_LCR <sup>1</sup> | RSVD       | SBRK                   | STKP       | EPS | PEN      | STB  | WLS[1:0] |         |  |
| 02h      | SH_FCR <sup>2</sup> | RXFTH[1:0] |                        | TXFTH[1:0] |     | RSVD     | TXSR | RXSR     | FIFO_EN |  |
| 03h      | BSR                 | BKSE       | BSR[6:0] (Bank Select) |            |     |          |      |          |         |  |
| 04h-07h  | RSVD                | Reserved   |                        |            |     |          |      |          |         |  |

1. LCR Register Value
2. FCR Register Value

Table 5-59. Bank 4 Bit Map

| Register |                      | Bits                                   |                        |   |   |   |   |       |        |  |
|----------|----------------------|--|------------------------|---|---|---|---|-------|--------|--|
| Offset   | Name                 | 7                                      | 6                      | 5 | 4 | 3   | 2 | 1     | 0      |  |
| 00h      | TMR(L)               | TMR[7:0] (Low Byte Data)               |                        |   |   |   |   |       |        |  |
| 01h      | TMR(H)               | RSVD                                   |                        |   |   | TMR[11:8] (High Byte Data)                |   |       |        |  |
| 02h      | IRCR1                | RSVD                                   |                        |   |   | IR_SL[1:0]                                |   | CTEST | TMR_EN |  |
| 03h      | BSR                  | BKSE                                   | BSR[6:0] (Bank Select) |   |   |   |   |       |        |  |
| 04h      | TFRL(L)/<br>TFRCC(L) | TFRL[7:0] / TFRCC[7:0] (Low Byte Data) |                        |   |   |   |   |       |        |  |
| 05h      | TFRL(H)/<br>TFRCC(H) | RSVD                                   |                        |   |   | TFRL[12:8] / TFRCC[12:8] (High Byte Data) |   |       |        |  |

Table 5-59. Bank 4 Bit Map (Continued)

| Register |                       | Bits                                    |   |   |  |   |   |   |   |
|----------|-----------------------|---|---|---|--|---|---|---|---|
| Offset   | Name                  | 7                                       | 6 | 5 | 4  | 3 | 2 | 1 | 0 |
| 06h      | RFRML(L)/<br>RFRCC(L) | RFRML[7:0] / RFRCC[7:0] (Low Byte Data) |   |   |  |   |   |   |   |
| 07h      | RFRML(H)/<br>RFRCC(H) | RSVD                                    |   |   | RFRML[12:8] / RFRCC[12:8] (High Byte Data) |   |   |   |   |

Table 5-60. Bank 5 Bit Map

| Register |                    | Bits                                    |                        |         |          |         |         |        |          |
|----------|--------------------|---|------------------------|---------|----------|---------|---------|--------|----------|
| Offset   | Name               | 7                                       | 6                      | 5       | 4        | 3       | 2       | 1      | 0        |
| 00h      | SPR2               | Scratchpad 2                            |                        |         |          |         |         |        |          |
| 01h      | SPR3               | Scratchpad 2                            |                        |         |          |         |         |        |          |
| 02h      | RSVD               | RSVD                                    |                        |         |          |         |         |        |          |
| 03h      | BSR                | BKSE                                    | BSR[6:0] (Bank Select) |         |          |         |         |        |          |
| 04h      | IRCR2              | RSVD                                    | SFTSL                  | FEND_MD | AUX_IRRX | TX_MS   | MDRS    | IRMSSL | IR_FDPLX |
| 05h      | FRM_ST             | VLD                                     | LOST_FR                | RSVD    | MAX_LEN  | PHY_ERR | BAD_CRC | OVR1   | OVR2     |
| 06h      | RFRL(L)/<br>LSTFRC | RFRL[7:0] (Low Byte Data) / LSTFRC[7:0] |                        |         |          |         |         |        |          |
| 07h      | RFRL(H)            | RFRL[15:8] (High Byte Data)             |                        |         |          |         |         |        |          |

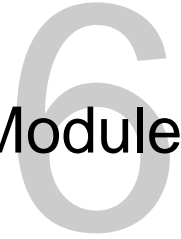
Table 5-61. Bank 6 Bit Map

| Register |        | Bits     |                        |         |         |          |           |          |      |
|----------|--------|----------|------------------------|---------|---------|----------|-----------|----------|------|
| Offset   | Name   | 7        | 6                      | 5       | 4       | 3        | 2         | 1        | 0    |
| 00h      | IRCR3  | SHDM_DS  | SHMD_DS                | FIR_CRC | MIR_CRC | RSVD     | TXCRC_INV | TXCRC_DS | RSVD |
| 01h      | MIR_PW | RSVD     |                        |         |         | MPW[3:0] |           |          |      |
| 02h      | SIR_PW | RSVD     |                        |         |         | SPW[3:0] |           |          |      |
| 03h      | BSR    | BKSE     | BSR[6:0] (Bank Select) |         |         |          |           |          |      |
| 04h      | BFPL   | MBF[3:0] |                        |         |         | FPL[3:0] |           |          |      |
| 05h-07h  | RSVD   | RSVD     |                        |         |         |          |           |          |      |

Table 5-62. Bank 7 Bit Map

| Register |        | Bits      |                        |          |           |           |           |             |   |
|----------|--------|-----------|------------------------|----------|-----------|-----------|-----------|-------------|---|
| Offset   | Name   | 7         | 6                      | 5        | 4         | 3         | 2         | 1           | 0 |
| 00h      | IRRXDC | DBW[2:0]  |                        |          | DFR[4:0]  |           |           |             |   |
| 01h      | IRTXMC | MCPW[2:0] |                        |          | MCFR[4:0] |           |           |             |   |
| 02h      | RCCFG  | R_LEN     | T_OV                   | RXHSC    | RCDM_DS   | RSVD      | TXHSC     | RC_MMD[1:0] |   |
| 03h      | BSR    | BKSE      | BSR[6:0] (Bank Select) |          |           |           |           |             |   |
| 04h      | IRCFG1 | STRV_MS   | SIRC[2:0]              |          |           | IRID3     | IRIC[2:0] |             |   |
| 05h-06h  | RSVD   | RSVD      |                        |          |           |           |           |             |   |
| 07h      | IRCFG4 | RSVD      | IRRX_MD                | IRSL0_DS | RXINV     | IRSL21_DS | RSVD      |             |   |

# Core Logic Module



The Core Logic module is an enhanced PCI-to-Sub-ISA bridge (South Bridge), this module is ACPI-compliant, and provides AT/Sub-ISA functionality. The Core Logic module also contains state-of-the-art power management. Two bus mastering IDE controllers are included for support of up to four ATA-compliant devices. A three-port Universal Serial Bus (USB) provides high speed, and Plug & Play expansion for a variety of new consumer peripheral devices.

## 6.1 Feature List

### Internal Fast-PCI Interface

The internal Fast-PCI bus interface is used to connect the Core Logic and GX1 modules of the SC3200. This interface includes the following features:

- PCI protocol for transfers on Fast-PCI bus
- Up to 66 MHz operation
- Subtractive decode handled internally in conjunction with external PCI bus

### Bus Mastering IDE Controllers

- Two controllers with support for up to four IDE devices
- Independent timing for master and slave devices for both channels
- PCI bus master burst reads and writes
- Multiword DMA support
- Programmed I/O (PIO) Modes 0-4 support

### Universal Serial Bus

- Three independent USB interfaces
- Open Host Controller Interface (OpenHCI) specification compliant

### PCI Interface

- PCI 2.1 compliant
- PCI master for AC97 and IDE controllers
- Subtractive agent for unclaimed transactions
- Supports PCI initiator-to-Sub-ISA cycle translations

- PCI-to-Sub-ISA interrupt mapper/translator
- External PCI bus
  - Devices internal to the Core Logic module (IDE, Audio, USB, Sub-ISA, etc.) cannot master to memory through the external PCI bus.
  - Legacy DMA is not supported to memory located on external PCI bus.
  - The Core Logic module does not transfer subtractively decoded I/O cycles originating from the external PCI bus.

### AT Compatibility

- 8259A-equivalent interrupt controllers
- 8254-equivalent timer
- 8237-equivalent DMA controllers
- Port A, B, and NMI logic
- Positive decode for AT I/O space

### Sub-ISA Interface

- Boot ROM chip select
- Extended ROM to 16 MB
- Two general-purpose chip selects
- NAND Flash support
- M-Systems DiskOnChip support
- Is not the subtractive decode agent

### Power Management

- Automated CPU 0V Suspend modulation
- I/O Traps and Idle Timers for peripheral power management
- Software SMI and Stop Clock for APM support
- ACPI-compliant timer and register set
- Up to 22 GPIOs of which all can generate Power Management Interrupts (PMEs)
- Three Dedicated GPWIOs powered by  $V_{SBL}$  and  $V_{SB}$
- Shadow register support for legacy controllers for 0V Suspend

### Integrated Audio

- AC97 Version 2.0 compliant interface to audio codecs
- Secondary codec support
- AMC97 codec support

### Video Processor Interface

- Synchronous serial interface to the Video Processor
- Translates video and clock control register accesses from PCI to serial interface
- Supports both reads and writes of Video Processor registers
- Retries Fast-PCI bus accesses until Core Logic completes the transfer over the serial interface

### Low Pin Count (LPC) Interface

- Based on Intel LPC Interface Specification Revision 1.0
- Serial IRQ support

## 6.2 Module Architecture

The Core Logic architecture provides the internal functional blocks shown in Figure 6-1.

- Fast-PCI interface to external PCI bus
- IDE controllers (UDMA-33)
- USB controllers
- Sub-ISA bus interface
- AT compatibility logic (legacy)
- ACPI compliant power management (includes GPIO interfaces, such as joystick)
- Integrated audio controller
- Low Pin Count (LPC) Interface

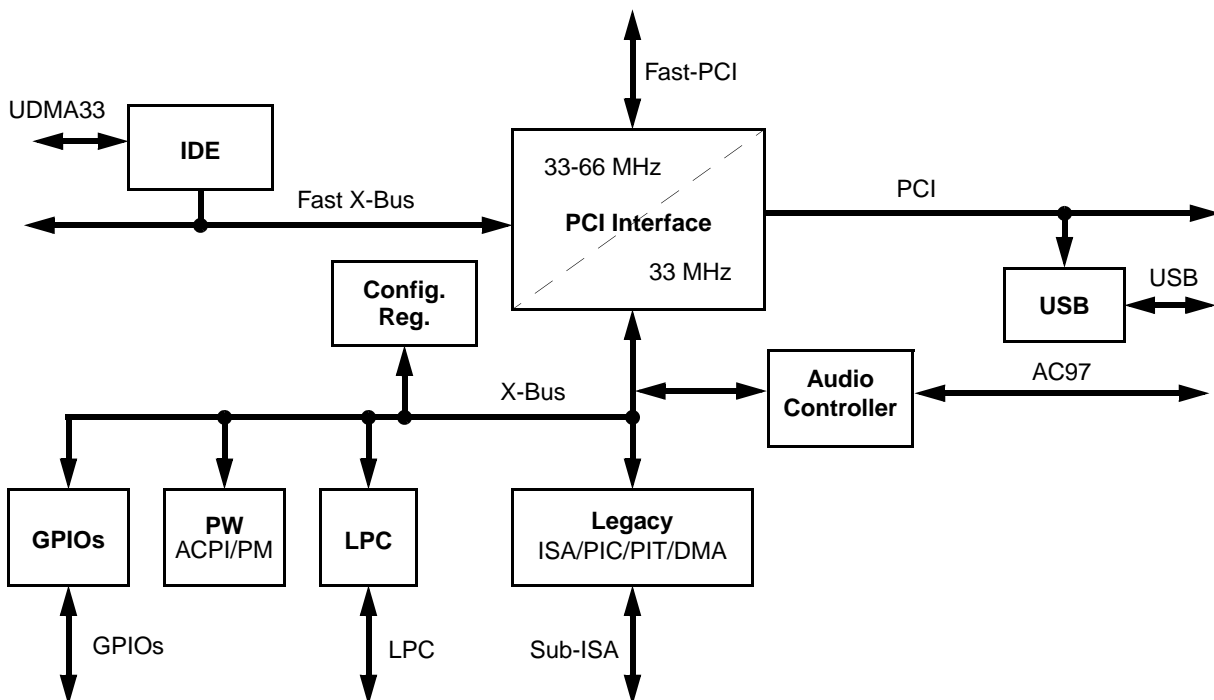


Figure 6-1. Core Logic Module Block Diagram

## 6.2.1 Fast-PCI Interface to External PCI Bus

The Core Logic module provides a PCI bus interface that is both a slave for PCI cycles initiated by the GX1 module or other PCI master devices, and a non-preemptive master for DMA transfer cycles. It is also a standard PCI master for the IDE controllers and audio I/O logic. The Core Logic supports positive decode for configurable memory and I/O regions, and implements a subtractive decode option for unclaimed PCI accesses. It also generates address and data parity, and performs parity checking. The arbiter for the Fast-PCI interface is located in the GX1 module.

Configuration registers are accessed through the PCI interface using the PCI Bus Type 1 configuration mechanism as described in the PCI Specification.

### 6.2.1.1 Processor Mastered Cycles

The Core Logic module acts on all processor initiated cycles according to PCI rules for active/subtractive decode using DEVSEL#. Memory writes are automatically posted. Reads are retried if they are *not* destined for actively decoded (i.e., positive decode) devices on the high speed X-Bus or the 33 MHz X-Bus. This means that reads to external PCI, LPC, or Sub-ISA devices are automatically treated as delayed transactions through the PCI retry mechanism. This allows the high bandwidth devices access to the Fast-PCI interface while the response from a slow device is accumulated.

Bursting from the host is not supported.

All types of configuration cycles are supported and handled appropriately according to the PCI specification.

### 6.2.1.2 External PCI Mastered Cycles

Memory cycles mastered by external PCI devices on the external PCI bus are actively taken if they are to the system memory address range. Memory cycles to system memory are forwarded to the Fast-PCI interface. Burst transfers are stopped on every cache line boundary to allow efficient buffering in the Fast-PCI interface block.

I/O and configuration cycles mastered by external PCI devices which are subtractively decoded by the Core Logic module, are not handled.

### 6.2.1.3 Core Logic Internal or Sub-ISA Mastered Cycles

Only memory cycles (not I/O cycles) are supported by the internal Sub-ISA or legacy DMA masters. These memory cycles are always forwarded to the Fast-PCI interface.

### 6.2.1.4 External PCI Bus

The external PCI bus is a fully-compliant PCI bus. PCI slots are connected to this bus. Support for up to two bus masters is provided. The arbiter is in the Core Logic module.

### 6.2.1.5 Bus Master Request Priority

The Fast-PCI bus supports seven bus masters. The requests (REQs) are fixed in priority. The seven bus masters in order of priority are:

- 1) VIP
- 2) IDE Channel 0
- 3) IDE Channel 1
- 4) Audio
- 5) USB
- 6) External REQ0#
- 7) External REQ1#

## 6.2.2 PSERIAL Interface

The majority of the system power management logic is implemented in the Core Logic module, but a minimal amount of logic is contained within the GX1 module to provide information that is not externally visible (e.g., graphics controller).

The GX1 module implements a simple serial communications mechanism to transmit the CPU status to the Core Logic module via internal signal PSERIAL. The GX1 module accumulates CPU events in an 8-bit register which it transmits serially every 1 to 10  $\mu$ s.

The packet transmitter holds the serial output internal signal (PSERIAL) low until the transmission interval counter has elapsed. Once the counter has elapsed, the PSERIAL signal is held high for two clocks to indicate the start of packet transmission. The contents of the Serial Packet register are then shifted out starting from bit 7 down to bit 0. The PSERIAL signal is held high for one clock to indicate the end of packet transmission and then remains low until the next transmission interval. After the packet transmission is complete, the GX1 module's Serial Packet register's contents are cleared.

The GX1 module's input clock is used as the clock reference for the serial packet transmitter.

Once a bit in the register is set, it remains set until the completion of the next packet transmission. Successive events of the same type that occur between packet transmissions are ignored. Multiple unique events between packet transmissions accumulate in this register. The GX1 module transmits the contents of the serial packet only when a bit in the Serial Packet register is set and the interval counter has elapsed.

The Core Logic module decodes the serial packet after each transmission and performs the power management tasks related to video retrace.

For more information on the Serial Packet register refer to the *AMD Geode™ GX1 Processor Data Book*.

### 6.2.2.1 Video Retrace Interrupt

Bit 7 of the “Serial Packet” can be used to generate an SMI whenever a video retrace occurs within the GX1 module. This function is normally not used for power management but for SoftVGA routines. Setting F0 Index 83h[2] = 1 enables this function. A read only status register located at F1BAR0+I/O Offset 00h[5] can be read to see if the SMI was caused by a video retrace event.

### 6.2.3 IDE Controller

The Core Logic module integrates a PCI bus mastering, ATA-4 compatible IDE controller. This controller supports UltraDMA, Multiword DMA and Programmed I/O (PIO) modes. Two devices are supported on the IDE controller. The data-transfer speed for each device can be independently programmed. This allows high-speed IDE peripherals to coexist on the same channel as lower speed devices.

The Core Logic module supports two IDE channels, a primary channel and a secondary channel.

The IDE interface provides a variety of features to optimize system performance, including 32-bit disk access, post write buffers, bus master, Multiword DMA, look-ahead read buffer, and prefetch mechanism for each channel respectively.

The IDE interface timing is completely programmable. Timing control covers the command active and recover pulse widths, and command block register accesses. The IDE data-transfer speed for each device on each channel can be independently programmed allowing high-speed IDE peripherals to coexist on the same channel as older, compatible devices.

The Core Logic module also provides a software accessible buffered reset signal to the IDE drive, F0 Index 44h[2]. The IDE\_RST# signal can be driven low or high as needed for device-power-off conditions. IDE\_RST# is not driven low by POR# (Power-On Reset).

#### 6.2.3.1 IDE Configuration Registers

Registers for configuring Channels 0 and 1 are located in the PCI register space designated as Function 2 (F2 Index 40h-5Ch). Table 6-35 on page 273 provides the bit formats for these registers. The IDE bus master configuration registers are accessed via F2 Index 20h which is Base Address Register 4 in Function 2 (F2BAR4). See Table 6-36 on page 277 for register/bit formats.

The following subsections discuss Core Logic operational/programming details concerning PIO, Bus Master, and UltraDMA/33 modes.

#### 6.2.3.2 PIO Mode

The IDE data port transaction latency consists of address latency, asserted latency and recovery latency. Address latency occurs when a PCI master cycle targeting the IDE data port is decoded, and the IDE\_ADDR[2:0] and IDE\_CS# lines are not set up. Address latency provides the setup time for the IDE\_ADDR[2:0] and IDE\_CS# lines prior to IDE\_IOR# and IDE\_IOW#.

Asserted latency consists of the I/O command strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back-to-back on the IDE interface without violating minimum cycle periods for the IDE interface.

If IDE\_IORDY is asserted when the initial sample point is reached, no wait states are added to the command strobe assertion length. If IDE\_IORDY is negated when the initial sample point is reached, additional wait states are added.

Recovery latency occurs after the IDE data port transactions have completed. It provides hold time on the IDE\_ADDR[2:0] and IDE\_CS# lines with respect to the read and write strobes (IDE\_IOR# and IDE\_IOW#).

The PIO portion of the IDE registers is enabled through:

- Channel 0 Drive 0 Programmed I/O Register (F2 Index 40h)
- Channel 0 Drive 1 Programmed I/O Register (F2 Index 48h)
- Channel 1 Drive 0 Programmed I/O Register (F2 Index 50h)
- Channel 1 Drive 1 Programmed I/O Register (F2 Index 58h)

The IDE channels and devices can be individually programmed to select the proper address setup time, asserted time, and recovery time.

The bit formats for these registers are shown in Table 6-35 on page 273. Note that there are different bit formats for each of the PIO programming registers depending on the operating format selected: Format 0 or Format 1:

- F2 Index 44h[31] (Channel 0 Drive 0 — DMA Control Register) sets the format of the PIO register.
  - If bit 31 = 0, Format 0 is used and it selects the slowest PIO mode (bits [19:16]) per channel for commands.
  - If bit 31 = 1, Format 1 is used and it allows independent control of command and data.

Also listed in the bit formats are recommended values for the different PIO modes. Note that these are only recommended settings and are not 100% tested.

When using independent control of command and data cycles the following algorithm should be used when two IDE devices are sharing the same channel:

- 1) The PIO data cycle timing for a particular device can be the timing value for the maximum PIO mode which that device reports it supports.
- 2) The PIO command cycle timing for a particular device must be the timing value for the lowest PIO mode for both devices on the channel.



For example, if a channel had one Mode 4 device and one Mode 0 device, then the Mode 4 device would have command timings for Mode 0 and data timing for Mode 4. The Mode 0 device would have both command and data timings for Mode 0. Note that for the Mode 0 case, the 32-bit timing value is listed because both data and command timings are the same mode. However, the actual timing value for the Mode 4 device would be constructed out of the Mode 4 data timing 16-bit value and the Mode 0 16-bit command timing value. Both 16-bit values are shown in the register description but not assembled together as they are mixed modes.

**6.2.3.3 Bus Master Mode**

Two IDE bus masters are provided to perform the data transfers for the primary and secondary channels. The IDE controller of the Core Logic module off-loads the CPU and improves system performance in multitasking environments.

The bus master mode programming interface is an extension of the standard IDE programming model. This means that devices can always be dealt with using the standard IDE programming model, with the master mode functionality used when the appropriate driver and devices are present. Master operation is designed to work with any IDE device that supports DMA transfers on the IDE bus. Devices that work in PIO mode can only use the standard IDE programming model.

The IDE bus masters use a simple scatter/gather mechanism allowing large transfer blocks to be scattered to or gathered from memory. This cuts down on the number of interrupts to and interactions with the CPU.

**Physical Region Descriptor Table Address**

Before the controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This pointer sets the starting memory location of the Physical Region Descriptors (PRDs). The PRDs describe the areas of memory that are used in the data transfer. The PRDs must be aligned on a 4-byte boundary and the table cannot cross a 64 KB boundary in memory.

**Primary and Secondary IDE Bus Master Registers**

The IDE Bus Master Registers for each channel (primary and secondary) have an IDE Bus Master Command register and Bus Master Status register. These registers and bit formats are described in Table 6-36 on page 277.

**Physical Region Descriptor Format**

Each physical memory region to be transferred is described by a Physical Region Descriptor (PRD) as illustrated in Table 6-1. When the bus master is enabled (Command register bit 0 = 1), data transfer proceeds until each PRD in the PRD table has been transferred. The bus master does not cache PRDs.

The PRD table consists of two DWORDs. The first DWORD contains a 32-bit pointer to a buffer to be transferred. The second DWORD contains the size (16 bits) of the buffer and the EOT flag. The EOT bit (bit 31) must be set to indicate the last PRD in the PRD table.

**Programming Model**

The following steps explain how to initiate and maintain a bus master transfer between memory and an IDE device.

- 1) Software creates a PRD table in system memory. Each PRD entry is 8 bytes long, consisting of a base address pointer and buffer size. The maximum data that can be transferred from a PRD entry is 64 KB. A PRD table must be aligned on a 4-byte boundary. The last PRD in a PRD table must have the EOT bit set.
- 2) Software loads the starting address of the PRD table by programming the PRD Table Address register.
- 3) Software must fill the buffers pointed to by the PRDs with IDE data.
- 4) Write 1 to the Bus Master Interrupt bit and Bus Master Error (Status register bits 2 and 1) to clear the bits.
- 5) Set the correct direction to the Read or Write Control bit (Command register bit 3).

Engage the bus master by writing a “1” to the Bus Master Control bit (Command register bit 0).

The bus master reads the PRD entry pointed to by the PRD Table Address register and increments the address by 08h to point to the next PRD. The transfer begins.

- 6) The bus master transfers data to/from memory responding to bus master requests from the IDE device. At the completion of each PRD, the bus master’s next response depends on the settings of the EOT flag in the PRD. If the EOT bit is set, then the IDE bus master clears the Bus Master Active bit (Status register bit 0) and stop. If any errors occurred during the transfer, the bus master sets the Bus Master Error bit Status register bit 1).

**Table 6-1. Physical Region Descriptor Format**

| DWORD | Byte 3   |    |    |          |    |    |    |    | Byte 2 |    |    |    |    |    |    |    | Byte 1 |             |    |    |    |    |   |   | Byte 0 |   |   |   |   |   |   |   |
|-------|--|----|----|----------|----|----|----|----|--------|----|----|----|----|----|----|----|--------|-------------|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
|       | 31   | 31 | 29 | 28       | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14          | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0     | Memory Region Physical Base Address [31:1] (IDE Data Buffer) |    |    |          |    |    |    |    |        |    |    |    |    |    |    |    |        |             |    |    |    |    |   |   |        |   |   |   |   |   |   | 0 |
| 1     | E  | O  | T  | Reserved |    |    |    |    |        |    |    |    |    |    |    |    |        | Size [15:1] |    |    |    |    |   |   |        |   |   |   |   |   |   | 0 |

### 6.2.3.4 UltraDMA/33 Mode

The IDE controller of the Core Logic module supports UltraDMA/33. It utilizes the standard IDE Bus Master functionality to interface, initiate and control the transfer. UltraDMA/33 definition also incorporates a Cyclic Redundancy Checking (CRC) error checking protocol to detect errors.

The UltraDMA/33 protocol requires no extra signal pins on the IDE connector. The IDE controller redefines three standard IDE control signals when in UltraDMA/33 mode. These definitions are shown in Table 6-2.

**Table 6-2. UltraDMA/33 Signal Definitions**

| IDE Controller Channel Signal | UltraDMA/33 Read Cycle | UltraDMA/33 Write Cycle |
|-------------------------------|------------------------|-------------------------|
| IDE_IOW#                      | STOP                   | STOP                    |
| IDE_IOR#                      | DMARDY#                | STROBE                  |
| IDE_IORDY                     | STROBE                 | DMARDY#                 |

All other signals on the IDE connector retain their functional definitions during the UltraDMA/33 operation.

IDE\_IOW# is defined as STOP for both read and write transfers to request to stop a transaction.

IDE\_IOR# is redefined as DMARDY# for transferring data from the IDE device to the IDE controller. It is used by the IDE controller to signal when it is ready to transfer data and to add wait states to the current transaction. IDE\_IOR# signal is defined as STROBE for transferring data from the IDE controller to the IDE device. It is the data strobe signal driven by the IDE controller on which data is transferred during each rising and falling edge transition.

IDE\_IORDY is redefined as STROBE for transferring data from the IDE device to the IDE controller during a read cycle. It is the data strobe signal driven by the IDE device on which data is transferred during each rising and falling edge transition. IDE\_IORDY is defined as DMARDY# during a write cycle for transferring data from the IDE controller to the IDE device. It is used by the IDE device to signal when it is ready to transfer data and to add wait states to the current transaction.

UltraDMA/33 data transfer consists of three phases, a startup phase, a data transfer phase and a burst termination phase.

The IDE device begins the startup phase by asserting IDE\_DREQ. When ready to begin the transfer, the IDE controller asserts IDE\_DACK#. When IDE\_DACK# is asserted, the IDE controller drives IDE\_CS0# and IDE\_CS1# asserted, and IDE\_ADDR[2:0] low. For write cycles, the IDE controller negates STOP, waits for the IDE device to assert DMARDY#, and then drives the first data WORD and STROBE signal. For read cycles, the IDE controller negates STOP, and asserts DMARDY#. The IDE device then sends the first data WORD and asserts STROBE.

The data transfer phase continues the burst transfers with the Core Logic and the IDE via providing data, toggling STROBE and DMARDY#. The IDE\_DATA[15:0] is latched by receiver on each rising and falling edge of STROBE. The transmitter can pause the burst cycle by holding STROBE high or low, and resume the burst cycle by again toggling STROBE. The receiver can pause the burst cycle by negating DMARDY# and resumes the burst cycle by asserting DMARDY#.

The current burst cycle can be terminated by either the transmitter or the receiver. A burst cycle must first be paused as described above before it can be terminated. The IDE controller can then stop the burst cycle by asserting STOP, with the IDE device acknowledging by negating IDE\_DREQ. The IDE device then stops the burst cycle by negating IDE\_DREQ and the IDE controller acknowledges by asserting STOP. The transmitter then drives the STROBE signal to a high level. The IDE controller then puts the result of the CRC calculation onto the IDE\_DATA[15:0] while de-asserting IDE\_DACK#. The IDE device latches the CRC value on the rising edge of IDE\_DACK#.

The CRC value is used for error checking on UltraDMA/33 transfers. The CRC value is calculated for all data by both the IDE controller and the IDE device during the UltraDMA/33 burst transfer cycles. This result of the CRC calculation is defined as all data transferred with a valid STROBE edge while IDE\_DACK# is asserted. At the end of the burst transfer, the IDE controller drives the result of the CRC calculation onto IDE\_DATA[15:0] which is then strobed by the de-assertion of IDE\_DACK#. The IDE device compares the CRC result of the IDE controller to its own and reports an error if there is a mismatch.

The timings for UltraDMA/33 are programmed into the DMA control registers:

- Channel 0 Drive 0 DMA Control Register (F2 Index 44h)
- Channel 0 Drive 1 DMA Control Register (F2 Index 4Ch)
- Channel 1 Drive 0 DMA Control Register (F2 Index 54h)
- Channel 1 Drive 1 DMA Control Register (F2 Index 5Ch)

The bit formats for these registers are described in Table 6-35 on page 273. Note that F2 Index 44h[20] is used to select either Multiword or UltraDMA mode. Bit 20 = 0 selects Multiword DMA mode. If bit 20 = 1, then UltraDMA/33 mode is selected. Once mode selection is made using this bit, the remaining DMA Control registers also operate in the selected mode.

Also listed in the bit formats are recommended values for both Multiword DMA Modes 0-2 and UltraDMA/33 Modes 0-2. Note that these are only recommended settings and are not 100% tested.

### 6.2.4 Universal Serial Bus

The Core Logic module provides three complete, independent USB ports. Each port has a Data "Negative" and a Data "Positive" signal.

The USB ports are Open Host Controller Interface (OpenHCI) compliant. The OpenHCI specification provides a register-level description for a host controller, as well as common industry hardware/software interface and drivers.

### 6.2.5 Sub-ISA Bus Interface

The Sub-ISA interface of the Core Logic module is an ISA-like bus interface that is used by SC3200 to interface with Boot Flash, M-Systems DiskOnChip or NAND EEPROM and other I/O devices. The Core Logic module is the default subtractive decoding agent and forwards all unclaimed memory and I/O cycles to the ISA bus. However, the Core Logic module can be configured to ignore either I/O, memory, or all unclaimed cycles (subtractive decode disabled).

**Note:** The external Sub-ISA bus is a positive decode bus. Unclaimed memory and I/O cycles will not appear on the Sub-ISA interface.

The Core Logic module does not support Sub-ISA refresh cycles. The refresh toggle bit in Port B still exists for software compatibility reasons.

The Sub-ISA interface includes the followings signals in addition to the signals used for an ISA interface:

- IOCS0#/IOCS1#
  - Asserted on I/O read/write transactions from/to a programmable address range.
- DOCCS#
  - Asserted on memory read/write transactions from/to a programmable window.
- ROMCS#
  - Asserted on memory read/write to upper 16 MB of address space. Configurable via the ROM Mask register (F0 Index 6Ch).
- DOCR#
  - DOCR# is asserted on memory read transactions from DOCCS# window (i.e., when both DOCCS# and MEMR# are active, DOCR# is active; otherwise, it is inactive).

- DOCW
  - DOCW# is asserted on memory write transactions to DOCCS# window (i.e., when both DOCCS# and MEMW# are active, DOCW# is active; otherwise, it is inactive).
- RD#, WR#
  - The signals IOR#, IOW#, MEMR#, and MEMW# are combined into two signals: RD# is asserted on I/O read or memory read; WR# is asserted on I/O write or memory write.

Memory devices that use ROMCS# or DOCCS# as their chip select signal can be configured to support an 8-bit or 16-bit data bus via bits 3 and 6 of the MCR register. Such devices can also be configured as zero wait states devices (regardless of the data bus width) via bits 9 and 10 of the MCR register. For MCR register bit descriptions, see Table 4-2 on page 88.

I/O peripherals that use IOCS0# or IOCS1# as their chip select signal can be configured to support an 8-bit or 16-bit data bus via bits 7 and 8 of the MCR register. Such devices can also be configured as zero wait state devices (for 8-bit peripherals) via bits 11 and 12 of the MCR register. For MCR register bit descriptions, see Table 4-2 on page 88.

Other memory devices and I/O peripherals must be 8-bit devices; their transactions can not be with zero wait states

The Boot Flash supported by the SC3200 can be up to 16 MB. It is supported with the ROMCS# signal.

All unclaimed memory and I/O cycles are forwarded to the Internal ISA bus if subtractive decode is enabled.

The DiskOnChip chip select signal (DOCCS#) is asserted on any memory read or memory write transaction from/to a programmable address range. The address range is programmable via the DOCCS# Base Address and Control registers (F0 Index 78h and 7Ch). The base address must be on an address boundary, the size of the range.

Signal DOCCS# can also be used to interface to NAND Flash devices together with signals DOCW# and DOCR#. See application note *AMD Geode™ SC1200/SC2200/SC3200 Processors: External NAND Flash Memory Circuit* for details.

**6.2.5.1 Sub-ISA Bus Cycles**

The ISA bus controller issues multiple ISA cycles to satisfy PCI transactions that are larger than 16 bits. A full 32-bit read or write results in two 16-bit ISA transactions or four 8-bit ISA transactions. The ISA controller gathers the data from multiple ISA read cycles and returns TRDY# to the PCI bus.

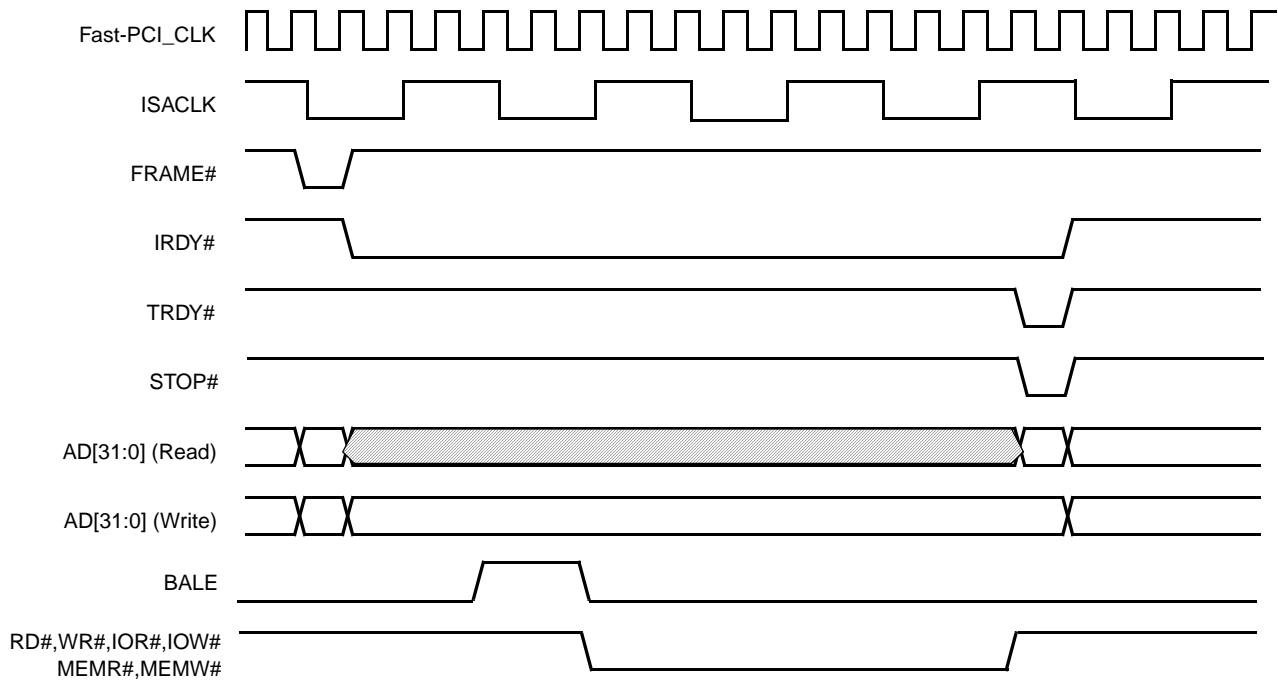
SA[23:0] are a concatenation of ISA LA[23:17] and SA[19:0] and perform equivalent functionality at a reduced pin count.

Figure 6-2 shows the relationship between a PCI cycle and the corresponding ISA cycle generated.

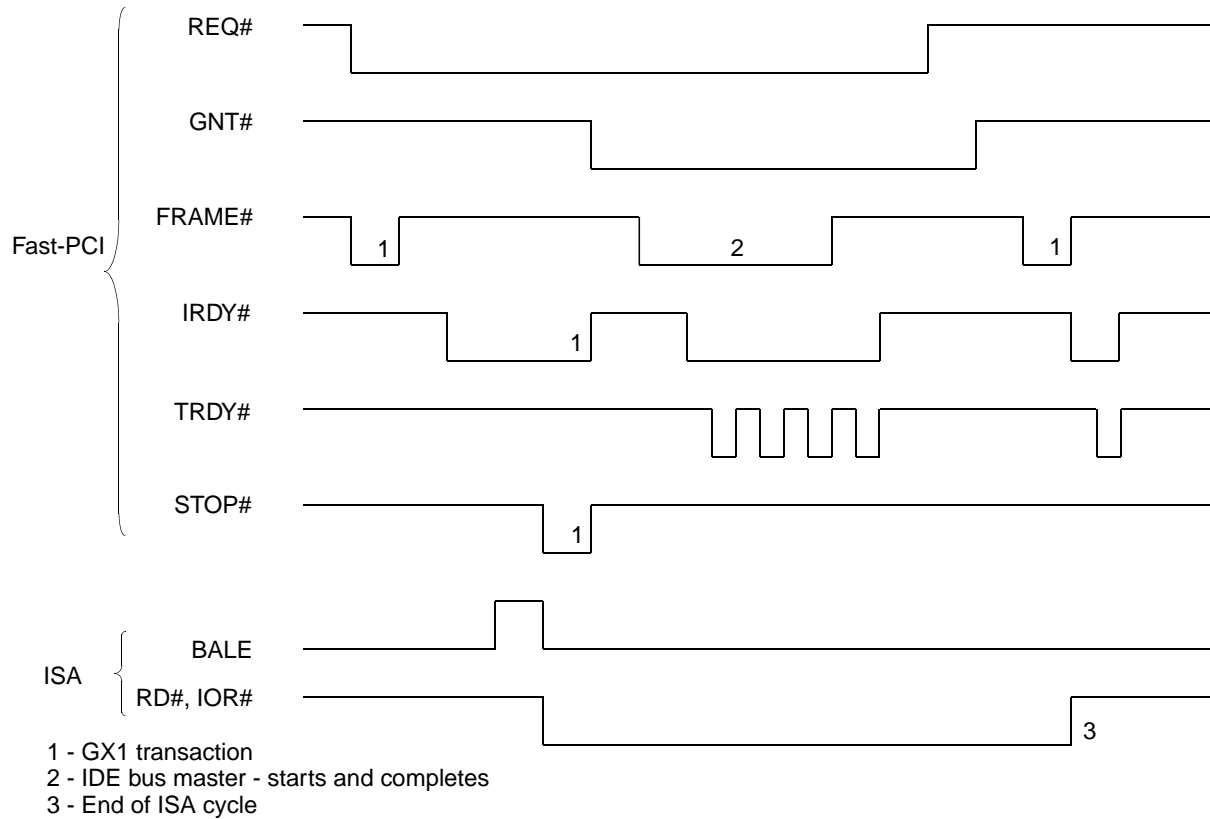
**Note:** Not all signals described in Figure 6-2 are available externally. See Section 3.4.7 "Sub-ISA Interface Signals" on page 73 for more information about which Sub-ISA signals are externally available on the SC3200.

**6.2.5.2 Sub-ISA Support of Delayed PCI Transactions**

Multiple PCI cycles occur for every slower ISA cycle. This prevents slow PCI cycles from occupying too much bandwidth and allows access to other PCI traffic. Figure 6-3 on page 165 shows the relationship of PCI cycles to an ISA cycle with PCI delayed transactions enabled.



**Figure 6-2. Non-Posted Fast-PCI to ISA Access**



**Figure 6-3. PCI to ISA Cycles with Delayed Transaction Enabled**

### 6.2.5.3 Sub-ISA Bus Data Steering

The Core Logic module performs all of the required data steering from SD[7:0] to SD[15:0] during normal 8-bit ISA cycles, as well as during DMA and ISA master cycles. It handles data transfers between the 32-bit PCI data bus and the ISA bus. 8/16-bit devices can reside on the ISA bus. Various PC-compatible I/O registers, DMA controller registers, interrupt controller registers, and counter/timer registers lie on the on-chip I/O data bus. Either the PCI bus master or the DMA controllers can become the bus owner.

When the PCI bus master is the bus owner, the Core Logic module data steering logic provides data conversion necessary for 8/16/32-bit transfers to and from 8/16-bit devices on either the Sub-ISA bus or the 8-bit registers on the on-chip I/O data bus. When PCI data bus drivers of the Core Logic module are in TRI-STATE, data transfers between the PCI bus master and PCI bus devices are handled directly via the PCI data bus.

When the DMA requestor is the bus owner, the Core Logic module allows 8/16-bit data transfer between the Sub-ISA bus and the PCI data bus.

### 6.2.5.4 I/O Recovery Delays

In normal operation, the Core Logic module inserts a delay between back-to-back ISA I/O cycles that originate on the PCI bus. The default delay is four ISACLK cycles. Thus, the second of consecutive I/O cycles is held in the ISA bus controller until this delay count has expired. The delay is measured between the rising edge of IOR#/IOW# and the falling edge of BALE. This delay can be adjusted to a greater delay through the ISA I/O Recovery Control register (F0 Index 51h).

**Note:** This delay is not inserted for a 16-bit Sub-ISA I/O access that is split into two 8-bit I/O accesses.

**6.2.5.5 ISA DMA**

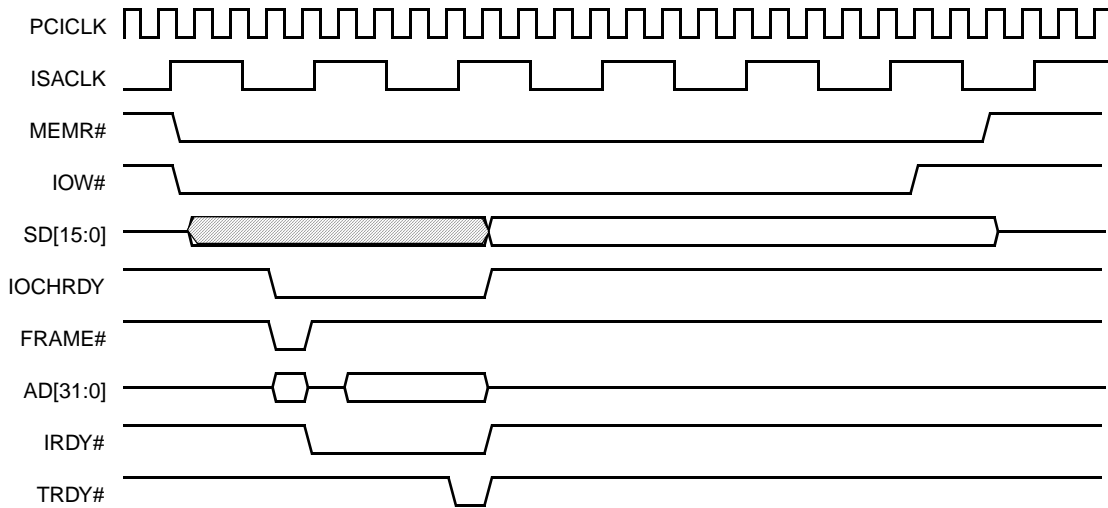
DMA transfers occur between ISA I/O peripherals and system memory (i.e., not available externally). The data width can be either 8 or 16 bits. Out of the seven DMA channels available, four are used for 8-bit transfers while the remaining three are used for 16-bit transfers. One byte or WORD is transferred in each DMA cycle.

**Note:** The Core Logic module does not support DMA transfers to ISA memory.

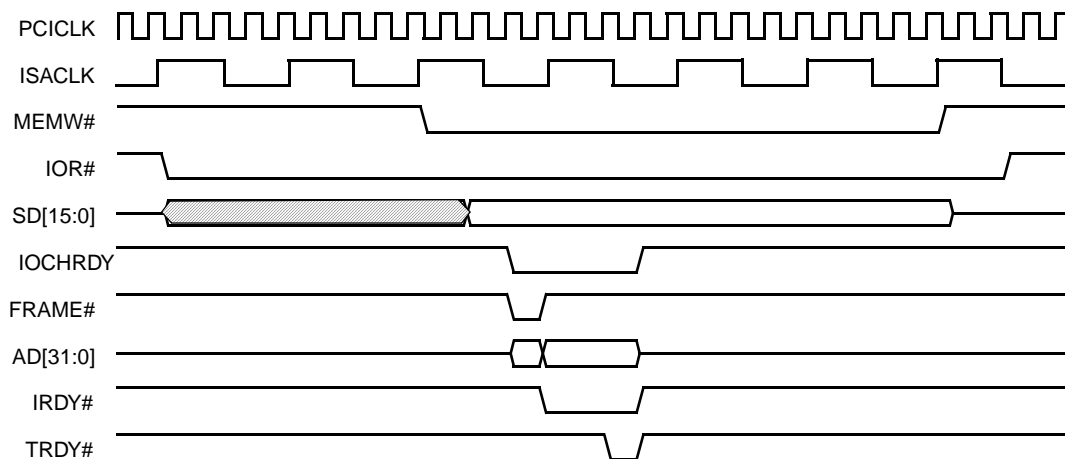
The ISA DMA device initiates a DMA request by asserting one of the DRQ[7:5, 3:0] signals. When the Core Logic module receives this request, it sends a bus grant request

to the PCI arbiter. After the PCI bus has been granted, the respective DACK# is driven active.

The Core Logic module generates PCI memory read or write cycles in response to a DMA cycle. Figure 6-4 and Figure 6-5 are examples of DMA memory read and memory write cycles. Upon detection of the DMA controller's MEMR# or MEMW# active, the Core Logic module starts the PCI cycle, asserts FRAME#, and negates an internal IOCHRDY. This assures the DMA cycle does not complete before the PCI cycle has provided or accepted the data. IOCHRDY is internally asserted when IRDY# and TRDY# are sampled active.



**Figure 6-4. ISA DMA Read from PCI Memory**



**Figure 6-5. ISA DMA Write to PCI Memory**

### 6.2.5.6 ROM Interface

The Core Logic module positively decodes memory addresses 000F0000h-000FFFFFh (64 KB) and FFFC0000h-FFFFFFFh (256 KB) at reset. These memory cycles cause the Core Logic module to claim the cycle, and generate an ISA bus memory cycle with ROMCS# asserted. The Core Logic module can also be configured to respond to memory addresses FF000000h-FFFFFFFh (16 MB) and 000E0000h-000FFFFFh (128 KB).

8- or 16-bit wide ROM is supported. BOOT16 strap determines the width after reset. MCR[14,3] (Offset 34h) in the General Configuration Block (see Table 4-2 on page 88 for bit details) allows program control of the width.

Flash ROM is supported in the Core Logic module by enabling the ROMCS# signal on write accesses to the ROM region. Normally only read cycles are passed to the ISA bus, and the ROMCS# signal is suppressed for write cycles. When the ROM Write Enable bit (F0 Index 52h[1]) is set, a write access to the ROM address region causes a write cycle to occur with MEMW#, WR# and ROMCS# asserted.

### 6.2.5.7 PCI and Sub-ISA Signal Cycle Multiplexing

The SC3200 multiplexes most PCI and Sub-ISA signals on the balls listed in Table 6-3, in order to reduce the number of balls on the device. Cycle multiplexing is on a bus-cycle by bus-cycle basis (see Figure 6-6 on page 168), where the internal Core Logic PCI bridge arbitrates between PCI cycles and Sub-ISA cycles. Other PCI and Sub-ISA signals remain non-shared, however, some Sub-ISA signals may be muxed with GPIO.

Sub-ISA cycles are only generated as a result of GX1 module accesses to the following addresses or conditions:

- ROMCS# address range.
- DOCCS# address range.
- IOCS0# address range.
- IOCS1# address range.
- An I/O write to address 80h or to 84h.
- Internal ISA is programmed to be the subtractive decode agent and no other agents claim the cycle.

If the Sub-ISA and PCI bus have more than four components, the Sub-ISA components can be buffered using 74HCT245 or 74FCT245 type transceivers. The RD# (an AND of IOR#, MEMR#) signal can be used as DIR control while TRDE# is used as enable control.

**Table 6-3. Cycle Multiplexed PCI / Sub-ISA Balls**

| PCI     | Sub-ISA | Ball No. |        |
|---------|---------|----------|--------|
|         |         | EBGA     | TEPBGA |
| AD0     | A0      | A17      | U1     |
| AD1     | A1      | D16      | P3     |
| AD2     | A2      | A18      | U3     |
| AD3     | A3      | A15      | N1     |
| AD4     | A4      | A16      | P1     |
| AD5     | A5      | A14      | N3     |
| AD6     | A6      | C15      | N2     |
| AD7     | A7      | B14      | M2     |
| AD8     | A8      | C14      | M4     |
| AD9     | A9      | B13      | L2     |
| AD10    | A10     | C13      | L3     |
| AD11    | A11     | C12      | K1     |
| AD12    | A12     | A12      | L4     |
| AD13    | A13     | C11      | J1     |
| AD14    | A14     | A11      | K4     |
| AD15    | A15     | B10      | J3     |
| AD16    | A16     | A7       | E1     |
| AD17    | A17     | C7       | F4     |
| AD18    | A18     | D7       | E3     |
| AD19    | A19     | A6       | E2     |
| AD20    | A20     | D6       | D3     |
| AD21    | A21     | C6       | D1     |
| AD22    | A22     | A5       | D2     |
| AD23    | A23     | F4       | B6     |
| AD24    | D0      | C5       | C2     |
| AD25    | D1      | D5       | C4     |
| AD26    | D2      | A4       | C1     |
| AD27    | D3      | B4       | D4     |
| AD28    | D4      | C4       | B4     |
| AD29    | D5      | A3       | B3     |
| AD30    | D6      | C2       | A3     |
| AD31    | D7      | B3       | D5     |
| C/BE0#  | D8      | A13      | L1     |
| C/BE1#  | D9      | A10      | J2     |
| C/BE2#  | D10     | D8       | F3     |
| C/BE3#  | D11     | A8       | H4     |
| PAR     | D12     | C10      | J4     |
| TRDY#   | D13     | B8       | F1     |
| IRDY#   | D14     | C8       | F2     |
| STOP#   | D15     | D9       | G1     |
| DEVSEL# | BHE#    | B5       | E4     |

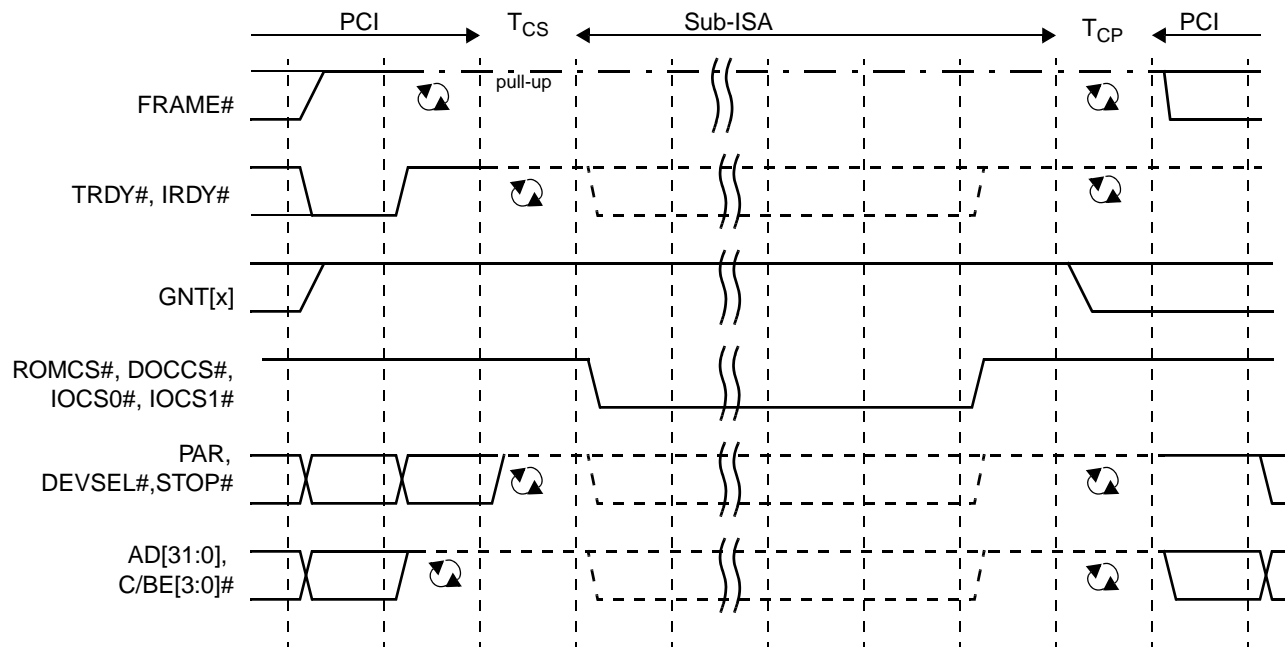


Figure 6-6. PCI Change to Sub-ISA and Back

### 6.2.6 AT Compatibility Logic

The Core Logic module integrates:

- Two 8237-equivalent DMA controllers with full 32-bit addressing
- Two 8259A-equivalent interrupt controllers providing 13 individually programmable external interrupts
- An 8254-equivalent timer for refresh, timer, and speaker logic
- NMI control and generation for PCI system errors and all parity errors
- Support for standard AT keyboard controllers
- Positive decode for the AT I/O register space
- Reset control

#### 6.2.6.1 DMA Controller

The Core Logic module supports industry standard DMA architecture using two 8237-compatible DMA controllers in cascaded configuration. The DMA functions supported by the Core Logic module include:

- Standard seven-channel DMA support (Channels 5 through 7 are not supported)
- 32-bit address range support via high page registers
- IOCHRDY extended cycles for compatible timing transfers
- Internal Sub-ISA bus master device support using cascade mode

- NMI control and generation for PCI system errors and all parity errors.

**Note:** DMA interface signals are not available externally.

#### DMA Channels

The Core Logic module supports seven DMA channels using two standard 8237-equivalent controllers. DMA Controller 1 contains Channels 0 through 3 and supports 8-bit I/O adapters. These channels are used to transfer data between 8-bit peripherals and PCI memory or 8/16-bit ISA memory. Using the high and low page address registers, a full 32-bit PCI address is output for each channel so they can all transfer data throughout the entire 4 GB system address space. Each channel can transfer data in 64 KB pages. Software initiated DMA requests are not supported.

DMA Controller 2 contains Channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. Using the high and low page address registers, a full 32-bit PCI address is output for each channel so they can all transfer data throughout the entire 4 GB system address space. Each channel can transfer data in 128 KB pages. Channels 5, 6, and 7 transfer 16-bit WORDs on even byte boundaries only. Channels 5 through 7 are not supported.



### DMA Transfer Modes

Each DMA channel can be programmed for *single*, *block*, *demand* or *cascade* transfer modes. In the most commonly used mode, *single* transfer mode, one DMA cycle occurs per DRQ and the PCI bus is released after every cycle. This allows the Core Logic module to timeshare the PCI bus with the GX1 module. This is imperative, especially in cases involving large data transfers, because the GX1 module gets locked out for too long.

In *block* transfer mode, the DMA controller executes all of its transfers consecutively without releasing the PCI bus.

In *demand* transfer mode, DMA transfer cycles continue to occur as long as DRQ is high or terminal count is not reached. In this mode, the DMA controller continues to execute transfer cycles until the I/O device drops DRQ to indicate its inability to continue providing data. For this case, the PCI bus is held by the Core Logic module until a break in the transfers occurs.

In *cascade* mode, the channel is connected to another DMA controller or to an ISA bus master, rather than to an I/O device. In the Core Logic module, one of the 8237 controllers is designated as the master and the other as the slave. The HOLD output of the slave is tied to the DRQ0 input of the master (Channel 4), and the master's DACK0# output is tied to the slave's HLDA input.

In each of these modes, the DMA controller can be programmed for *read*, *write*, or *verify* transfers.

Both DMA controllers are reset at power-on reset (POR) to *fixed* priority. Since master Channel 0 is actually connected to the slave DMA controller, the slave's four DMA channels have the highest priority, with Channel 0 as highest and Channel 3 as the lowest. Immediately following slave Channel 3, master Channel 1 (Channel 5) is the next highest, followed by Channels 6 and 7.

### DMA Controller Registers

The DMA controller can be programmed with standard I/O cycles to the standard register space for DMA. The I/O addresses for the DMA controller registers are listed Table 6-43 on page 313.

When writing to a channel's address or WORD Count register, the data is written into both the base register and the current register simultaneously. When reading a channel address or WORD Count register, only the current address or WORD Count can be read. The base address and base WORD Count are not accessible for reading.

### DMA Transfer Types

Each of the seven DMA channels may be programmed to perform one of three types of transfers: *read*, *write*, or *verify*. The transfer type selected defines the method used to transfer a byte or WORD during one DMA bus cycle.

For *read* transfer types, the Core Logic module reads data from memory and write it to the I/O device associated with the DMA channel.

For *write* transfer types, the Core Logic module reads data from the I/O device associated with the DMA channel and write to the memory.

The *verify* transfer type causes the Core Logic module to execute DMA transfer bus cycles, including generation of memory addresses, but neither the READ nor WRITE command lines are activated. This transfer type was used by DMA Channel 0 to implement DRAM refresh in the original IBM PC and XT.

### DMA Priority

The DMA controller may be programmed for two types of priority schemes: *fixed* and *rotate* (I/O Ports 008h[4] and 0D0h[4] - see Table 6-43 on page 313).

In *fixed* priority, the channels are fixed in priority order based on the descending values of their numbers. Thus, Channel 0 has the highest priority. In *rotate* priority, the last channel to get service becomes the lowest-priority channel with the priority of the others rotating accordingly. This prevents a channel from dominating the system.

The address and WORD Count registers for each channel are 16-bit registers. The value on the data bus is written into the upper byte or lower byte, depending on the state of the internal addressing byte pointer. This pointer can be cleared by the Clear Byte Pointer command. After this command, the first read/write to an address or WORD-count register reads or writes to the low byte of the 16-bit register and the byte pointer points to the high byte. The next read/write to an address or WORD-count register reads or writes to the high byte of the 16-bit register and the byte pointer points back to the low byte.

When programming the 16-bit channels (Channels 5, 6, and 7), the address which is written to the base address register must be the real address divided by two. Also, the base WORD Count for the 16-bit channels is the number of 16-bit WORDs to be transferred, not the number of bytes as is the case for the 8-bit channels.

The DMA controller allows the user to program the active level (low or high) of the DRQ and DACK# signals. Since the two controllers are cascaded together internally on the chip, these signals should always be programmed with the DRQ signal active high and the DACK# signal active low.

### DMA Shadow Registers

The Core Logic module contains a shadow register located at F0 Index B8h (Table 6-29 on page 206) for reading the configuration of the DMA controllers. This read only register can sequence to read through all of the DMA registers.

### DMA Addressing Capability

DMA transfers occur over the entire 32-bit address range of the PCI bus. This is accomplished by using the DMA controller's 16-bit memory address registers in conjunction with an 8-bit DMA Low Page register and an 8-bit DMA High Page register. These registers, associated with each channel, provide the 32-bit memory address capability. A write to the Low Page register clears the High Page register, for backward compatibility with the PC/AT standard. The starting address for the DMA transfer must be programmed into the DMA controller registers and the channel's respective Low and High Page registers prior to beginning the DMA transfer.

### DMA Page Registers and Extended Addressing

The DMA Page registers provide the upper address bits during DMA cycles. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8-bit channels (Channels 0 through 3) are every 64 KB and page boundaries for the 16-bit channels (Channels 5, 6, and 7) are every 128 KB.

Before any DMA operations are performed, the Page registers must be written at the I/O Port addresses in the DMA controller registers to select the correct page for each DMA channel. The other address locations between 080h and 08Fh and 480h and 48Fh are not used by the DMA channels, but can be read or written by a PCI bus master. These registers are reset to zero at POR. A write to the Low Page register clears the High Page register, for backward compatibility with the PC/AT standard.

For most DMA transfers, the High Page register is set to zeros and is driven onto PCI address bits AD[31:24] during DMA cycles. This mode is backward compatible with the PC/AT standard. For DMA extended transfers, the High Page register is programmed and the values are driven onto the PCI addresses AD[31:24] during DMA cycles to allow access to the full 4 GB PCI address space.

### DMA Address Generation

The DMA addresses are formed such that there is an upper address, a middle address, and a lower address portion.

The upper address portion, which selects a specific page, is generated by the Page registers. The Page registers for each channel must be set up by the system before a DMA operation. The DMA Page register values are driven on PCI address bits AD[31:16] for 8-bit channels and AD[31:17] for 16-bit channels.

The middle address portion, which selects a block within the page, is generated by the DMA controller at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for 8-bit channels (Channels 0 through 3) and 512 bytes for 16-bit channels (Channels 5, 6, and 7). The middle address bits are driven on PCI address bits AD[15:8] for 8-bit channels and AD[16:9] for 16-bit channels.

The lower address portion is generated directly by the DMA controller during DMA operations. The lower address bits are output on PCI address bits AD[7:0] for 8-bit channels and AD[8:1] for 16-bit channels.

BHE# is configured as an output during all DMA operations. It is driven as the inversion of AD0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

#### 6.2.6.2 Programmable Interval Timer

The Core Logic module contains an 8254-equivalent Programmable Interval Timer (PIT) configured as shown in Figure 6-7. The PIT has three timers/counters, each with an input frequency of 1.19318 MHz (OSC divided by 12), and individually programmable to different modes.

The gates of Counter 0 and 1 are usually enabled, however, they can be controlled via F0 Index 50h. The gate of Counter 2 is connected to I/O Port 061h[0]. The output of Counter 0 is connected internally to IRQ0. This timer is typically configured in Mode 3 (square wave output), and used to generate IRQ0 at a periodic rate to be used as a system timer function. The output of Counter 1 is connected to I/O Port 061h[4]. The reset state of I/O Port 061h[4] is 0 and every falling edge of Counter 1 output causes I/O Port 061h[4] to flip states. The output of Counter 2 is brought out to the PC\_BEEP output. This output is gated with I/O Port 061h[1].

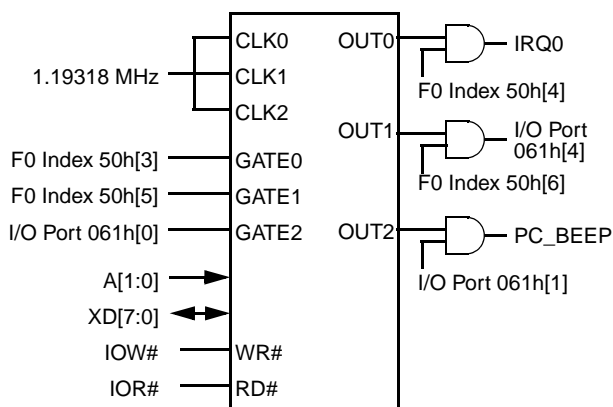


Figure 6-7. PIT Timer

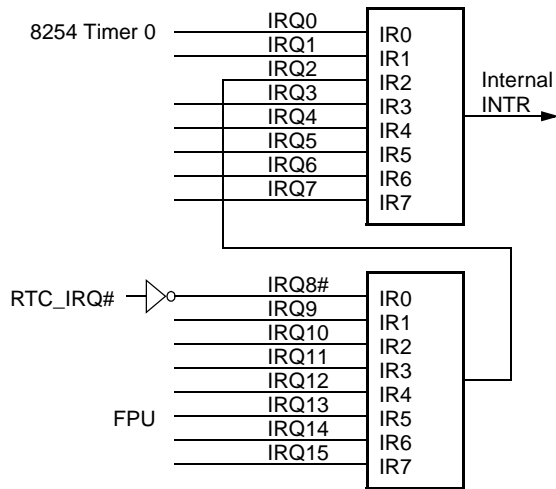
#### PIT Shadow Register

The PIT registers are shadowed to allow for 0V Suspend to save/restore the PIT state by reading the PIT's counter and *write only* registers. The read sequence for the shadow register is listed in F0 Index BAh (see Table 6-29 on page 206).

### 6.2.6.3 Programmable Interrupt Controller

The Core Logic module contains two 8259A-equivalent programmable interrupt controllers, with eight interrupt request lines each, for a total of 16 interrupts. The PCI device supports all x86 modes of operation except Special Fully Nested mode. The two controllers are cascaded internally, and two of the interrupt request inputs are connected to the internal circuitry. This allows a total of 13 externally available interrupt requests. See Figure 6-9.

Each Core Logic IRQ signal can be individually selected to as edge- or level-sensitive. The four PCI interrupt signals may be routed internally to any PIC IRQ.



**Figure 6-8. PIC Interrupt Controllers**

Three interrupts are available externally depending upon selected ball multiplexing:

- 1) IRQ15 (muxed with GPIO11+RI2#),
- 2) IRQ14 (muxed with TFTD1), and
- 3) IRQ9 (muxed with IDE\_DATA6)

More of the IRQs are available through the use of SERIRQ (muxed with GPIO39) function. See Table 6-4.

**Table 6-4. PIC Interrupt Mapping**

| Master IRQ | Mapping  |
|------------|--|
| IRQ0       | Connected to the OUT0 (system timer) of the internal 8254 PIT. |
| IRQ2       | Connected to the slave's INTR for a cascaded configuration.    |
| IRQ8#      | Connected to internal RTC.                                     |
| IRQ13      | Connected to the FPU interface of the GX1 module.              |
| IRQ15      | Interrupts available to other functions                        |
| IRQ14      |  |
| IRQ12      |  |
| IRQ11      |  |
| IRQ10      |  |
| IRQ9       |  |
| IRQ7       |  |
| IRQ6       |  |
| IRQ5       |  |
| IRQ4       |  |
| IRQ3       |  |
| IRQ1       |  |

The Core Logic module allows PCI interrupt signals INTA#, INTB#, INTC# (muxed with GPIO19+IOCHRDY) and INTD# (muxed with IDE\_DATA7) to be routed internally to any IRQ signal. The routing can be modified through Core Logic module's configuration registers. If this is done, the IRQ input must be configured to be level- rather than edge-sensitive. IRQ inputs may be individually programmed to be level-sensitive with the Interrupt Sensitivity configuration registers at I/O address space 4D0h and 4D1h. PCI interrupt configuration is discussed in further detail in "PCI Compatible Interrupts" on page 172.

### PIC Interrupt Sequence

A typical AT-compatible interrupt sequence is as follows. Any unmasked interrupt generates the internal INTR signal to the CPU. The interrupt controller then responds to the interrupt acknowledge (INTA) cycles from the CPU. On the first INTA cycle the cascading priority is resolved to determine which of the two 8259A controllers output the interrupt vector onto the data bus. On the second INTA cycle the appropriate 8259A controller drives the data bus with the correct interrupt vector for the highest priority interrupt.

By default, the Core Logic module responds to PCI INTA cycles because the system interrupt controller is located within the Core Logic module. This may be disabled with F0 Index 40h[0]. When the Core Logic module responds to a PCI INTA cycle, it holds the PCI bus and internally generates the two INTA cycles to obtain the correct interrupt vector. It then asserts TRDY# and returns the interrupt vector.

### PIC I/O Registers

Each PIC contains registers located in the standard I/O address locations, as shown in Table 6-46 "Programmable Interrupt Controller Registers" on page 321.

An initialization sequence must be followed to program the interrupt controllers. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the controller expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW) can be written after initialization. The PIC must be programmed before operation begins.

Since the controllers are operating in cascade mode, ICW3 of the master controller should be programmed with a value indicating that the IRQ2 input of the master interrupt controller is connected to the slave interrupt controller rather than an I/O device as part of the system initialization code. In addition, ICW3 of the slave interrupt controller should be programmed with the value 02h (slave ID) and corresponds to the input on the master controller.

### PIC Shadow Register

The PIC registers are shadowed to allow for 0V Suspend to save/restore the PIC state by reading the PICs *write only* registers. A write to this register resets the read sequence to the first register. The read sequence for the shadow register is listed in F0 Index B9h.

### PCI Compatible Interrupts

The Core Logic module allows the PCI interrupt signals INTA#, INTB#, INTC#, and INTD# (also known in industry terms as PIRQx#) to be mapped internally to any IRQ signal with the PCI Interrupt Steering registers 1 and 2, F0 Index 5Ch and 5Dh.

PCI interrupts are low-level sensitive, whereas PC/AT interrupts are positive-edge sensitive; therefore, the PCI interrupts are inverted before being connected to the 8259A.

Although the controllers default to the PC/AT-compatible mode (positive-edge sensitive), each IRQ may be individually programmed to be edge or level sensitive using the Interrupt Edge/Level Sensitivity registers in I/O Port 4D0h and 4D1h. However, if the controllers are programmed to be level-sensitive via ICW1, all interrupts must be level-sensitive. Figure 6-9 shows the PCI interrupt mapping for the master/slave 8259A interrupt controller.

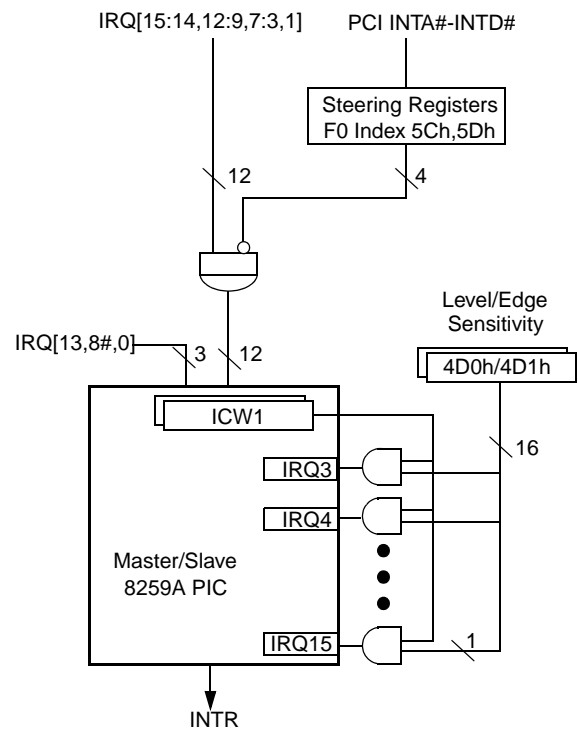


Figure 6-9. PCI and IRQ Interrupt Mapping

### 6.2.7 I/O Ports 092h and 061h System Control

The Core Logic module supports control functions of I/O Ports 092h (Port A) and 061h (Port B) for PS/2 compatibility. I/O Port 092h allows a fast assertion of the A20M# or CPU\_RST. (CPU\_RST is an internal signal that resets the CPU. It is asserted for 100  $\mu$ s after the negation of POR#.) I/O Port 061h controls NMI generation and reports system status. The Core Logic module generates an SMI for every internal change of the A20M# state and the SMI handler sets the A20M# state inside the GX1 module. This method is used for both the Port 092h (PS/2) and Port 061h (keyboard) methods of controlling A20M#.

### 6.2.7.1 I/O Port 092h System Control

I/O Port 092h allows for a fast keyboard assertion of an A20# SMI and a fast keyboard CPU reset. Decoding for this register may be disabled via F0 Index 52h[3].

The assertion of a fast keyboard A20# SMI is controlled by either I/O Port 092h or by monitoring for the keyboard command sequence (see Section 6.2.8.1 "Fast Keyboard Gate Address 20 and CPU Reset" on page 173). If bit 1 of I/O Port 092h is cleared, the Core Logic module internally asserts an A20M#, which in turn causes an SMI to the GX1 module. If bit 1 is set, A20M# is internally de-asserted, again causing an SMI.

The assertion of a fast keyboard reset (WM\_RST SMI) is controlled by bit 0 in I/O Port 092h or by monitoring for the keyboard command sequence (write data = FEh to I/O port 64h). If bit 0 is changed from 0 to 1, the Core Logic module generates a reset to the GX1 module by generating a WM\_RST SMI. When the WM\_RST SMI occurs, the BIOS jumps to the Warm Reset vector. Note that Warm Reset is not a pin, it is under SMI control.

### 6.2.7.2 I/O Port 061h System Control

Through I/O Port 061h, the speaker output can be enabled, the status of IOCHK# and SERR# can be read, and the state of the speaker data (Timer2 output) and refresh toggle (Timer1 output) can be read back. Note that NMI is under SMI control. Even though the hardware is present, the IOCHK# ball does not exist. Therefore, an NMI from IOCHK# can not happen.

### 6.2.7.3 SMI Generation for NMI

Figure 6-10 shows how the Core Logic module can generate an SMI for an NMI. Note that NMI is not a ball.

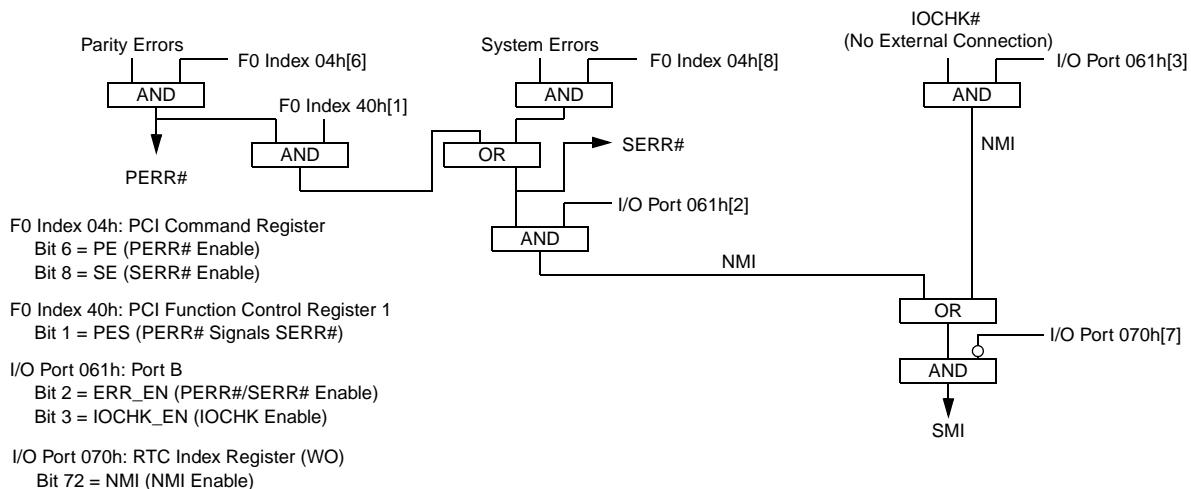


Figure 6-10. SMI Generation for NMI

### 6.2.8 Keyboard Support

The Core Logic module can actively decode the keyboard controller I/O Ports 060h, 062h, 064h and 066h, and generate an LPC bus cycle. Keyboard positive decoding can be disabled if F0 Index 5Ah[1] is cleared (i.e., subtractive decoding enabled).

#### 6.2.8.1 Fast Keyboard Gate Address 20 and CPU Reset

The Core Logic module monitors the keyboard I/O Ports 064h and 060h for the fast keyboard A20M# and CPU reset control sequences. If a write to I/O Port 060h[1] = 1 after a write takes place to I/O Port 064h with data of D1h, then the Core Logic module asserts the A20M# signal. A20M# remains asserted until cleared by any one of the following:

- A write to bit 1 of I/O Port 092h.
- A CPU reset of some kind.
- A write to I/O Port 060h[1] = 0 following a write to I/O Port 064h with data of D1h.

The fast keyboard A20M# and CPU reset can be disabled through F0 Index 52h[7]. By default, bit 7 is set, and the fast keyboard A20M# and CPU reset monitor logic is active. If bit 7 is clear, the Core Logic module forwards the commands to the keyboard controller.

By default, the Core Logic module forces the de-assertion of A20M# during a warm reset. This action may be disabled if F0 Index 52h[4] is cleared.

## 6.2.9 Power Management Logic

The Core Logic module integrates advanced power management features including idle timers for common system peripherals, address trap registers for programmable address ranges for I/O or memory accesses, four programmable general purpose external inputs, clock throttling with automatic speedup for the GX1 clock, software GX1 stop clock, 0V Suspend/Resume with peripheral shadow registers, and a dedicated serial bus to/from the GX1 module providing power management status.

The Core Logic module is ACPI (Advanced Configuration Power Interface) compliant. An ACPI-compliant system is one whose underlying BIOS, device drivers, chipset and peripherals conform to revision 1.0 of the ACPI specification. The Core Logic also supports Advanced Power Management (APM).

The SC3200 provides the following support of ACPI states:

- CPU States: C0, C1, and C3.
- Sleep States:
  - SL1/SL2 - ACPI S1 equivalent.
  - SL3 - ACPI S3 equivalent.
  - SL4 - ACPI S4 equivalent.
  - SL5 - ACPI S5 equivalent.
- General Purpose Events: Fully programmable GPE0 Event Block registers.
- Wakeup Events: Supported through GPWIO[2:0] which are powered by standby voltage and generate SMIs. See registers at F1BAR1+I/O Offset 0Ah and F1BAR1+I/O Offset 12h. Also see Section 5.6 "System Wakeup Control (SWC)" on page 132 and Table 6-5 "Wakeup Events Capability" on page 175.

SC3200 device power management is highly tuned for low power systems. It allows the system designer to implement a wide range of power saving modes using a wide range of capabilities and configuration options.

SC3200 controls the following functions directly:

- The system clocks.
- Core processor power states.
- Wakeup/resume event detection, including general purpose events.
- Power supply and power planes.

It also supports systems with an external micro controller that is used as a power management controller.

### 6.2.9.1 CPU States

The SC3200 supports three CPU states: C0, C1 and C3 (the Core Logic C2 CPU state is not supported). These states are fully compliant with the ACPI specification, revision 1.0. These states occur in the Working state only (S0/G0). They have no meaning when the system transitions into a Sleep state. For details on the various Sleep states, see Section 6.2.9.2 "Sleep States" on page 175.

#### C0 Power State - On

In this state the GX1 module executes code. This state has two sub-states: Full Speed or Throttling; selected via the THT\_EN bit (F1BAR1+I/O Offset 00h[4]).

#### C1 Power State - Active Idle

The SC3200 enters the C1 state, when the Halt Instruction (HLT) is executed. It exits this state back to the C0 state upon an NMI, an unmasked interrupt, or an SMI. The Halt instruction stops program execution and generates a special Halt bus cycle. (See "Usage Hints" on page 177.)

Bus masters are supported in the C1 state and the SC3200 will temporarily exit C1 to perform a bus master transaction.

#### C2 Power State

The SC3200 does not support the C2 power state. All relevant registers and bit fields in the Core Logic are reserved.

#### C3 Power State

The SC3200 enters the C3 state, when the P\_LVL3 register (F1BAR1+I/O Offset 05h) is read. It exits this state back to the C0 state (Full Speed or Throttling, depending on the THT\_EN bit) upon:

- An NMI, an unmasked interrupt, or an SMI.
- A bus master request, if enabled via the BM\_RLD bit (F1BAR1+I/O Offset 0Ch[1]).

In this state, the GX1 module is in Suspend Refresh mode (for details, see the Power Management section of the *AMD Geode™ GX1 Processor Data Book*, and Section 6.2.9.5 "Usage Hints" on page 177).

PCI arbitration should be disabled prior entering the C3 state via the ARB\_DIS bit in the PM2\_CNT register (F1BAR1+I/O Offset 20h[0]) because a PCI arbitration event could start after P\_LVL3 has been read. After wakeup ARB\_DIS needs to be cleared.

### 6.2.9.2 Sleep States

The SC3200 supports four Sleep states (SL1-SL3) and the Soft Off state (G2/S5). These states are fully compliant with the ACPI specification, revision 1.0.

When the SLP\_EN bit (F1BAR1+I/O Offset 0Ch[13]) is set to 1, the SC3200 enters an SLx state according to the SLP\_TYPx field (F1BAR1+I/O Offset 0Ch[12:10]). It exits the Sleep state back to the S0 state (C0 state - Full Speed or Throttling, depending on the THT\_EN bit) upon an enabled power management event. Table 6-5 on page 175 lists wakeup events from the various Sleep states.

#### SL1 Sleep State (ACPI S1)

In this state the core processor is in 3V Suspend mode (all its clocks are stopped, including the memory controller and the display controller). The SDRAM is placed in self-refresh mode. All other SC3200 system clocks and PLLs are running. All devices are powered up (PWRCNT[2:1] and ONCTL# are all asserted). See Section 6.2.9.5 "Usage Hints" on page 177.

No reset is performed, when exiting this state. The SC3200 keeps all context in this state. This state corresponds to ACPI Sleep state S1.

#### SL2 Sleep State (ACPI S1)

In this state, all of the SC3200 clocks are stopped including the PLLs. Selected clocks from the PLLs can be kept running under program control (F0 Index 60h). An exception to this is the CLK32 output signal which keeps toggling and the 32 KHz oscillator itself. The SDRAM is placed in self-refresh mode. The PWRCNT1 pin is de-asserted. The SC3200 itself is powered up. The system designer can

decide which other system devices to power off with the PWRCNT1 pin.

No reset is performed, when exiting this state. The SC3200 keeps all context in this state. This state corresponds to ACPI sleep state S1, with lower power and longer wake time than in SL1.

#### SL3 Sleep State (ACPI S3)

In this state, the SDRAM is placed in self-refresh mode, and PWRCNT[2:1] are de-asserted. PWRCNT[2:1] should be used to power off most of the system (except for the SDRAM). If the Save-to-RAM feature is used, external circuitry in the SDRAM interface is required to guarantee data integrity. All SC3200 signals powered by V<sub>SB</sub>, V<sub>SBL</sub> or V<sub>BAT</sub> are still functional to allow wakeup and to keep the RTC.

The power-up sequence is performed, when exiting this state. This state corresponds to ACPI Sleep state S3.

#### SL4 and SL5 Sleep States (ACPI S4 and S5)

The SL4 and SL5 states are similar from the hardware perspective. In these states, the SC3200 de-asserts PWRCNT[2:1] and ONCTL#. PWRCNT[2:1] and ONCTL# should be used to power off the system. All signals powered by V<sub>SB</sub>, V<sub>SBL</sub> or V<sub>BAT</sub> are still functional to allow wakeup and to keep the RTC.

While in this state, LED# can be toggled to give visual notification of this state. ACPI Function Control register (F1BAR1+I/O Offset 07h[7:6]) is used to control LED#.

The power-up sequence is performed when exiting this state. This state corresponds to ACPI Sleep states S4 and S5.

**Table 6-5. Wakeup Events Capability**

| Event                      | S0/C1            | S0/C3 | SL1 | SL2 | SL3 | SL4, SL5 |
|----------------------------|------------------|-------|-----|-----|-----|----------|
| Enabled Interrupts         | Yes              | Yes   | Yes | -   | -   | -        |
| SMI according to Table 6-8 | Yes              | Yes   | Yes | -   | -   | -        |
| SCI according to Table 6-8 | Yes              | Yes   | Yes | -   | -   | -        |
| GPIO[47:32], GPIO[15:0]    | Yes              | Yes   | Yes | -   | -   | -        |
| Power Button               | Yes              | Yes   | Yes | Yes | Yes | Yes      |
| Power Button Override      | Yes              | Yes   | Yes | Yes | Yes | Yes      |
| Bus Master Request         | Yes <sup>1</sup> | Yes   | Yes | -   | -   | -        |
| Thermal Monitoring         | Yes              | Yes   | Yes | Yes | Yes | Yes      |
| USB                        | Yes              | Yes   | Yes | Yes | -   | -        |
| SDATA_IN2 (AC97)           | Yes              | Yes   | Yes | Yes | -   | -        |
| IRRX1 (Infrared)           | Yes              | Yes   | Yes | Yes | -   | -        |
| GPWIO[2:0]                 | Yes              | Yes   | Yes | Yes | Yes | Yes      |
| RI2# (UART2)               | Yes              | Yes   | Yes | Yes | -   | -        |
| RTC                        | Yes              | Yes   | Yes | Yes | Yes | Yes      |

1. Temporarily exits state.

### 6.2.9.3 Power Planes Control

The SC3200 supports up to three power planes. Three signals are used to control these power planes. Table 6-6 describes the signals and when each is asserted.

**Table 6-6. Power Planes Control Signals vs. Sleep States**

| Signal  | S0 | SL1 | SL2 | SL3 | SL4 and SL5 |
|---------|----|-----|-----|-----|-------------|
| PWRCNT1 | 1  | 1   | 0   | 0   | 0           |
| PWRCNT2 | 1  | 1   | 1   | 0   | 0           |
| ONCTL#  | 0  | 0   | 0   | 0   | 1           |

These signals allow control of the power of system devices and the SC3200 itself. Table 6-7 describes the SC3200 power planes with respect to the different Sleep and Global states.

**Table 6-7. Power Planes vs. Sleep/Global States**

| Sleep/Global State | $V_{CORE}$ , $V_{I/O}$ , $V_{PLL}$ | $V_{SB}$ , $V_{SBL}$ | $V_{BAT}$ |
|--------------------|------------------------------------|----------------------|-----------|
| S0, SL1 and SL2    | On                                 | On                   | On or Off |
| SL3, SL4 and SL5   | Off                                | On                   | On or Off |
| G3                 | Off                                | Off                  | On        |
| No Power           | Off                                | Off                  | Off       |
| Illegal            | On                                 | Off                  | On or Off |

The SC3200 power planes are controlled externally by the three signals (i.e., the system designer should make sure the system design is such that Table 6-7 is met) for all supported Sleep states.

$V_{SB}$  and  $V_{BAT}$  are not controlled by any control signal.  $V_{SB}$  exists as long as the AC power is plugged in (for desktop systems) or the main battery is charged (for mobile systems).  $V_{BAT}$  exists as long as the RTC battery is charged.

The case in which  $V_{SB}$  does not exist is called Mechanical Off (G3).

### 6.2.9.4 Power Management Events

The SC3200 supports power management events that can manage:

- Transition of the system from a Sleep state to a Work state. This is done by the hardware. These events are defined as wakeup events.
- Enabled wakeup events to set the WAK\_STS bit (F1BAR1+I/O Offset 08h[15]) to 1, when transitioning the system back to the working state.
- Generation of an interrupt. This invokes the relevant software driver. The interrupt can either be an SMI or SCI (selected by the SCI\_EN bit, F1BAR1+I/O Offset 0Ch[0]). These events are defined as interrupt events.

Table 6-8 lists the power management events that can generate an SCI or SMI.

**Table 6-8. Power Management Events**

| Event                 | SCI | SMI |
|-----------------------|-----|-----|
| Power Button          | Yes | Yes |
| Power Button Override | Yes | -   |
| Bus Master Request    | Yes | -   |
| Thermal Monitoring    | Yes | Yes |
| USB                   | Yes | Yes |
| RTC                   | Yes | Yes |
| ACPI Timer            | Yes | Yes |
| GPIO                  | Yes | Yes |
| SDATA_IN2 (AC97)      | Yes | Yes |
| IRRX1                 | Yes | Yes |
| RI2#                  | Yes | Yes |
| GPWIO                 | Yes | Yes |
| Internal SMI signal   | Yes | -   |



## Power Button

The power button (PWRBTN#) input provides two events: a wake request, and a sleep request. For both these events, the PWRBTN# signal is debounced (i.e., the signal state is transferred only after 14 to 16 ms without transitions, to ensure that the signal is no longer bouncing).

ACPI is non-functional and all ACPI outputs are undefined when the power-up sequence does not include using the power button. SUSP# is an internal signal generated from the ACPI block. Without an ACPI reset, SUSP# can be permanently asserted. If the USE\_SUSP bit in CCR2 of GX1 module is enabled (Index C2h[7] = 1), the CPU will stop.

If ACPI functionality is desired, or the situation described above avoided, the power button must be toggled. This can be done externally or internally. GPIO63 is internally connected to PWRBTN#. To toggle the power button with software, GPIO63 must be programmed as an output using the normal GPIO programming protocol (see Section 6.4.1.1 "GPIO Support Registers" on page 240). GPIO63 must be pulsed low for at least 16 ms and not more than 4 sec.

Asserting POR# has no effect on ACPI. If POR# is asserted and ACPI was active prior to POR#, then ACPI will remain active after POR#. Therefore, BIOS must ensure that ACPI is inactive before GPIO63 is pulsed low.

**Power Button Wake Event** - Detection of a high-to-low transition on the debounced PWRBTN# input signal when in SL1 to SL5 Sleep states. The system is considered in the Sleep state, only after it actually transitioned into the state and not only according to the SLP\_TYP field.

In reaction to this event, the PWRBTN\_STS bit (F1BAR1+I/O Offset 08h[8]) is set to 1 and a wakeup event or an interrupt is generated (note that this is regardless of the PWRBTN\_EN bit, F1BAR1+I/O Offset 0Ah[8]).

**Power Button Sleep Event** - Detection of a high-to-low transition on the debounced PWRBTN# input signal, when in the Working state (S0).

In reaction to this event, the PWRBTN\_STS bit is set to 1.

- When both the PWRBTN\_STS bit and the PWRBTN\_EN bit are set to 1, an SCI interrupt is generated.
- When SCI\_EN bit is 0, ONCTL# and PWRCNT[2:1] are de-asserted immediately regardless of the PWRBTN\_EN bit.

## Power Button Override

When PWRBTN# is 0 for more than four seconds, ONCTL# and PWRCNT[2:1] are de-asserted (i.e., the system transitions to the SL5 state, "Soft Off"). This power management event is called the power button override event.

In reaction to this event, the PWRBTN\_STS bit is cleared to 0 and the PWRBTNOR\_STS bit (F1BAR1+I/O Offset 08h[11]) is set to 1.

## Thermal Monitoring

The thermal monitoring event (THRM#) enables control of ACPI-OS Control.

When the THRM# signal transitions from high-to-low, the THRM\_STS bit (F1BAR1+I/O Offset 10h[5]) is set to 1. If the THRM\_EN bit (F1BAR1+I/O Offset 12h[5]) is also set to 1, an interrupt is generated.

## SDATA\_IN2, IRRX1, RI2#

Section 5.4.1 "SIO Control and Configuration Registers" on page 113 for control and operation.

### 6.2.9.5 Usage Hints

- During initialization, the BIOS should:
  - Clear the SUSP\_HLT bit in CCR2 (GX1 module, Index C2h[3]) to 0. This is needed for compliance with C0 definition of ACPI, when the Halt Instruction (HLT) is executed.
  - Disable the SUSP\_3V option in C3 power state (F0 Index 60h[2]).
  - Disable the SUSP\_3V option in SL1 sleep state (F0 Index 60h[1]).
- SMM code should clear the CLK\_STP bit in the PM Clock Stop Control register (GX\_BASE+Memory Offset 8500h[0]) to 0 when entering C3 state.
- SMM code should correctly set the CLK\_STP bit in the PM Clock Stop Control register (GX\_BASE+Memory Offset 8500h[0]) when entering the SL1, SL2, and SL3 states.

### 6.2.10 Power Management Programming

The power management resources provided by a combined GX1 module and Core Logic module based system supports a high efficiency power management implementation. The following explanations pertain to a full-featured "notebook" power management system. The extent to which these resources are employed depends on the application and on the discretion of the system designer.

Power management resources can be grouped according to the function they enable or support. The major functions are as follows:

- APM Support
- CPU Power Management
  - Suspend Modulation
  - 3V Suspend
  - Save-to-Disk
- Peripheral Power Management
  - Device Idle Timers and Traps
  - General Purpose Timers
  - ACPI Timer Register
  - Power Management SMI Status Reporting Registers

Included in the following subsections are details regarding the registers used for configuring power management features. The majority of these registers are directly accessed through the PCI configuration register space designated as Function 0 (F0). However, included in the discussions are references to F1BARx+I/O Offset xxh. This refers to registers accessed through base address registers in Function 1 (F1) at Index 10h (F1BAR0) and Index 40h (F1BAR1).

#### 6.2.10.1 APM Support

Many notebook computers rely solely on an Advanced Power Management (APM) driver for enabling the operating system to power-manage the CPU. APM provides several services which enhance the system power management; but in its current form, APM is imperfect for the following reasons:

- APM is an OS-specific driver, and may not be available for some operating systems.
- Application support is inconsistent. Some applications in foreground may prevent Idle calls.
- APM does not help with Suspend determination or peripheral power management.

The Core Logic module provides two entry points for APM support:

- Software CPU Suspend control via the CPU Suspend Command register (F0 Index AEh)
- Software SMI entry via the Software SMI register (F0 Index D0h). This allows the APM BIOS to be part of the SMI handler.

#### 6.2.10.2 CPU Power Management

The three greatest power consumers in a system are the display, the hard drive, and the CPU. The power management of the first two is relatively straightforward and is discussed in Section 6.2.10.3 "Peripheral Power Management" on page 180.

APM, if available, is used primarily by CPU power management since the operating system is most capable of reporting the Idle condition. Additional resources provided by the Core Logic module supplement APM by monitoring external activity and power managing the CPU based on the system demands. The two processes for power managing the CPU are Suspend Modulation and 3V Suspend.

#### Suspend Modulation

Suspend Modulation works by asserting and de-asserting the internal SUSP# signal to the GX1 module for configurable durations. When SUSP# is asserted to the GX1 module, it enters an Idle state during which time the power consumption is significantly reduced. Even though the PCI clock is still running, the GX1 module stops the clocks to its core when SUSP# is asserted. By modulating SUSP# a reduced frequency of operation is achieved.

The Suspend Modulation feature works by assuming that the GX1 module is Idle unless external activity indicates otherwise. This approach effectively slows down the GX1 module until external activity indicates a need to run at full speed, thereby reducing power consumption. This approach is the opposite of that taken by most power management schemes in the industry, which run the system at full speed until a period of inactivity is detected, and then slows down. Suspend Modulation, the more aggressive approach, yields lower power consumption.

Suspend Modulation serves as the primary CPU power management mechanism when APM is not present. It also acts as a backup for situations where APM does not correctly detect an Idle condition in the system.

To provide high-speed performance when needed, SUSP# modulation is temporarily disabled any time system activity is detected. When this happens, the GX1 module is "instantly" converted to full speed for a programmed duration. System activities in the Core Logic module are asserted as: any unmasked IRQ, accessing Port 061h, any asserted SMI, and/or accessing the Video Processor module interface.

The graphics controller is integrated in the GX1 module. Therefore, the indication of video activity is sent to the Core Logic module via the serial link (see Section 6.2.2 "PSE-RIAL Interface" on page 159 for more information on serial link) and is automatically decoded. Video activity is defined as any access to the VGA register space, the VGA frame buffer, the graphics accelerator control registers and the configured graphics frame buffer.

The automatic speedup events (video and IRQ) for Suspend Modulation should be used together with software-controlled speedup registers for major I/O events such as any access to the FDC, HDD, or parallel/serial ports, since these are indications of major system activities. When major I/O events occur, Suspend Modulation should be temporarily disabled using the procedures described in the Power Management registers in the following subsections.

If a bus master (UltraDMA/33, Audio, USB) request occurs, the GX1 module automatically de-asserts SUSPA# and grants the bus to the requesting bus master. When the bus master de-asserts REQ#, SUSPA# reasserts. This does not directly affect the Suspend Modulation programming.

**Configuring Suspend Modulation:** Control of the Suspend Modulation feature is accomplished using the Suspend Modulation and Suspend Configuration registers (F0 Index 94h and 96h, respectively).

The Suspend Configuration register contains the global power management enable bit, as well as the enables for the individual activity speedup timers. The global power management bit must be enabled for Suspend Modulation and all other power management resources to function.

Bit 0 of the Suspend Configuration register enables Suspend Modulation. Bit 1 controls how SMI events affect Suspend Modulation. In general this bit should be set to 1, which causes SMIs to disable Suspend Modulation until it is re-enabled by the SMI handler.

The Suspend Modulation register controls two 8-bit counters that represent the number of 32  $\mu$ s intervals that the internal SUSP# signal is asserted and then de-asserted to the GX1 module. These counters define a ratio which is the effective frequency of operation of the system while Suspend Modulation is enabled.

$$F_{\text{eff}} = F_{\text{GX1}} \times \frac{\text{Asserted Count}}{\text{Asserted Count} + \text{De-asserted Count}}$$

The IRQ and Video Speedup Timer Count registers (F0 Index 8Ch and 8Dh) configure the amount of time which Suspend Modulation is disabled when the respective events occur.

**SMI Speedup Disable:** If the Suspend Modulation feature is being used for CPU power management, the occurrence of an SMI disables Suspend Modulation so that the system operates at full speed while in SMM. There are two methods used to invoke this via bit 1 of the Suspend Configuration register.

- 1) If F0 Index 96h[1] = 0: Use the IRQ Speedup Timer (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs.
- 2) If F0 Index 96h[1] = 1: Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable register (F1BAR0+I/O Offset 08h).

The SMI Speedup Disable register prevents VSA software from entering Suspend Modulation while operating in SMM. The data read from this register can be ignored. If the Suspend Modulation feature is disabled, reading this I/O location has no effect.

### 3 Volt Suspend

The Core Logic module supports the stopping of the CPU and system clocks for a 3V Suspend state. If appropriately configured, via the Clock Stop Control register (F0 Index BCh), the Core Logic module asserts internal SUSP\_3V after it has gone through the SUSP#/SUSPA# handshake. SUSP\_3V is a state indicator, indicating that the system is in a low-activity state and Suspend Modulation is active. This indicator can be used to put the system into a low-power state (the system clock can be turned off).

Internal SUSP\_3V is connected to the enable control of the clock generators, so that the clocks to the CPU and the Core Logic module (and most other system devices) are stopped. The Core Logic module continues to decrement all of its device timers and respond to external SMI interrupts after the input clock has been stopped, as long as the 32 KHz clock continues to oscillate. Any SMI event or unmasked interrupt causes the Core Logic module to de-assert SUSP\_3V, restarting the system clocks. As the CPU or other device might include a PLL, the Core Logic module holds SUSP# active for a pre-programmed period of delay (the PLL re-sync delay) that varies from 0 to 15 ms. After this period has expired, the Core Logic module de-asserts SUSP#, stopping Suspend. SMI# is held active for the entire period, so that the CPU reenters SMM when the clocks are restarted.

### Save-to-Disk

Save-to-Disk is supported by the Core Logic module. In this state, the power is typically removed from the Core Logic module and from the entire SC3200, causing the state of the legacy peripheral devices to be lost. Shadow registers are provided for devices which allow their state to be saved prior to removing power. This is necessary because the legacy AT peripheral devices used several write only registers. To restore the exact state of these devices on resume, the write only register values are "shadowed" so that the values can be saved by the power management software.

The PC/AT compatible keyboard controller (KBC) and floppy port (FDC) do not exist in the SC3200. However, it is possible that one is attached on the ISA bus or the LPC bus (e.g., in a SuperI/O device). Some of the KBC and FDC registers are shadowed because they cannot be safely read. Additional shadow registers for other functions are described in Table 6-29 "F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support" on page 206.

### 6.2.10.3 Peripheral Power Management

The Core Logic module provides peripheral power management using a combination of device idle timers, address traps, and general purpose I/O pins. Idle timers are used in conjunction with traps to support powering down peripheral devices.

#### Device Idle Timers and Traps

Idle timers are used to power manage a peripheral by determining when the peripheral has been inactive for a specified period of time, and removing power from the peripheral at the end of that time period.

Idle timers are provided for the commonly-used peripherals (FDC, IDE, Parallel/Serial Ports, and Mouse/Keyboard). In addition, there are three user-defined timers that can be configured for either I/O or memory ranges.

The idle timers are 16-bit countdown timers with a one second timebase or prescaler, providing a timeout range of 1 to 65536 seconds (1092 minutes) (18 hours). The input clock is 32 KHz. Very small count values have some error since the prescaler is free-running. (See the next subsection "General Purpose Timers" for further discussion on prescaler value limitations.)

When the idle timer count registers are loaded with a non-zero value and enabled, the timers decrement until one of two possibilities happens: a bus cycle occurs at that I/O or memory range, or the timer decrements to zero.

If a bus cycle occurs, the timer is reloaded and begins decrementing again. If the timer decrements to zero, and power management is enabled (F0 Index 80h[0] = 1), the timer generates an SMI.

When an idle timer generates an SMI, the SMI handler manages the peripheral power, disables the timer, and enables the trap. The next time an event occurs, the trap generates an SMI. This time, the SMI handler applies power to the peripheral, resets the timer, and disables the trap.

Relevant registers for controlling Device Idle Timers are: F0 Index 80h, 81h, 82h, 93h, 98h-9Eh, and ACh.

Relevant registers for controlling User Defined Device Idle Timers are: F0 Index 81h, 82h, A0h, A2h, A4h, C0h, C4h, C8h, CCh, CDh, and CEh.

Although not considered as device idle timers, two additional timers are provided by the Core Logic module. The Video Idle Timer used for Suspend-determination and the VGA Timer used for SoftVGA.

The programming bits for these timers are:

- F0 Index 81h[7], Video Access Idle Timer Enable
- F0 Index 82h[7], Video Access Trap Enable
- F0 Index A6h[15:0], Video Timer Count
- F0 Index 83h[3], VGA Timer Enable
- F0 Index 8Bh[6], VGA Timer Base
- F0 Index 8Eh[7:0], VGA Timer Count

### General Purpose Timers

The Core Logic module contains two general purpose idle timers, General Purpose Timer 1 (F0 Index 88h) and General Purpose Timer 2 (F0 Index 8Ah). These two timers are similar to the Device Idle Timers in that they count down to zero unless re-triggered, and generate an SMI when they reach zero. However, these are 8-bit timers instead of 16 bits, they have a programmable timebase, and the events which reload these timers are configurable. These timers are typically used for an indication of system inactivity for Suspend determination.

General Purpose Timer 1 can be re-triggered by activity to any of the configured User Defined Devices, Keyboard and Mouse, Parallel and Serial, Floppy disk, or Hard disk.

General Purpose Timer 2 can be re-triggered by a transition on the GPIO7 signal (if GPIO7 is properly configured).

When a General Purpose Timer is enabled or when an event reloads the timer, the timer is loaded with the configured count value. Upon expiration of the timer an SMI is generated and a status flag is set. Once expired, this counter must be re-initialized by disabling and enabling it.

The timebase or prescaler for both General Purpose Timers can be configured as either 1 second (default) or 1 millisecond. The 32 KHz clock feeds the prescaler. The registers at F0 Index 89h and 8Bh are the control registers for the General Purpose Timers.

The prescaler (1 millisecond or 1 second) that feeds the timers is free-running; meaning that the first count decrement will not be correct. The decrement time can be as short as 0 or as long as the prescaler. The actual time for the decrement to occur can not be determined since the current prescaler value can not be read. A periodic timer can be achieved after the first timer SMI, because when retriggered, the prescaler will be at or very nearly at the maximum value. Any software using these timers must understand this limitation. Small count values have the most error with a value of 1 having the largest error.

#### ACPI Timer Register

The ACPI Timer register (F1BAR0+I/O Offset 1Ch or at F1BAR1+I/O Offset 1Ch) provides the ACPI counter. The counter counts at 14.31818/4 MHz (3.579545 MHz). If SMI generation is enabled (F0 Index 83h[5] = 1), an SMI or SCI is generated when bit 23 toggles.

**Power Management SMI Status Reporting Registers**

The Core Logic module updates status registers to reflect the SMI sources. Power management SMI sources are the device idle timers, address traps, and general purpose I/O pins.

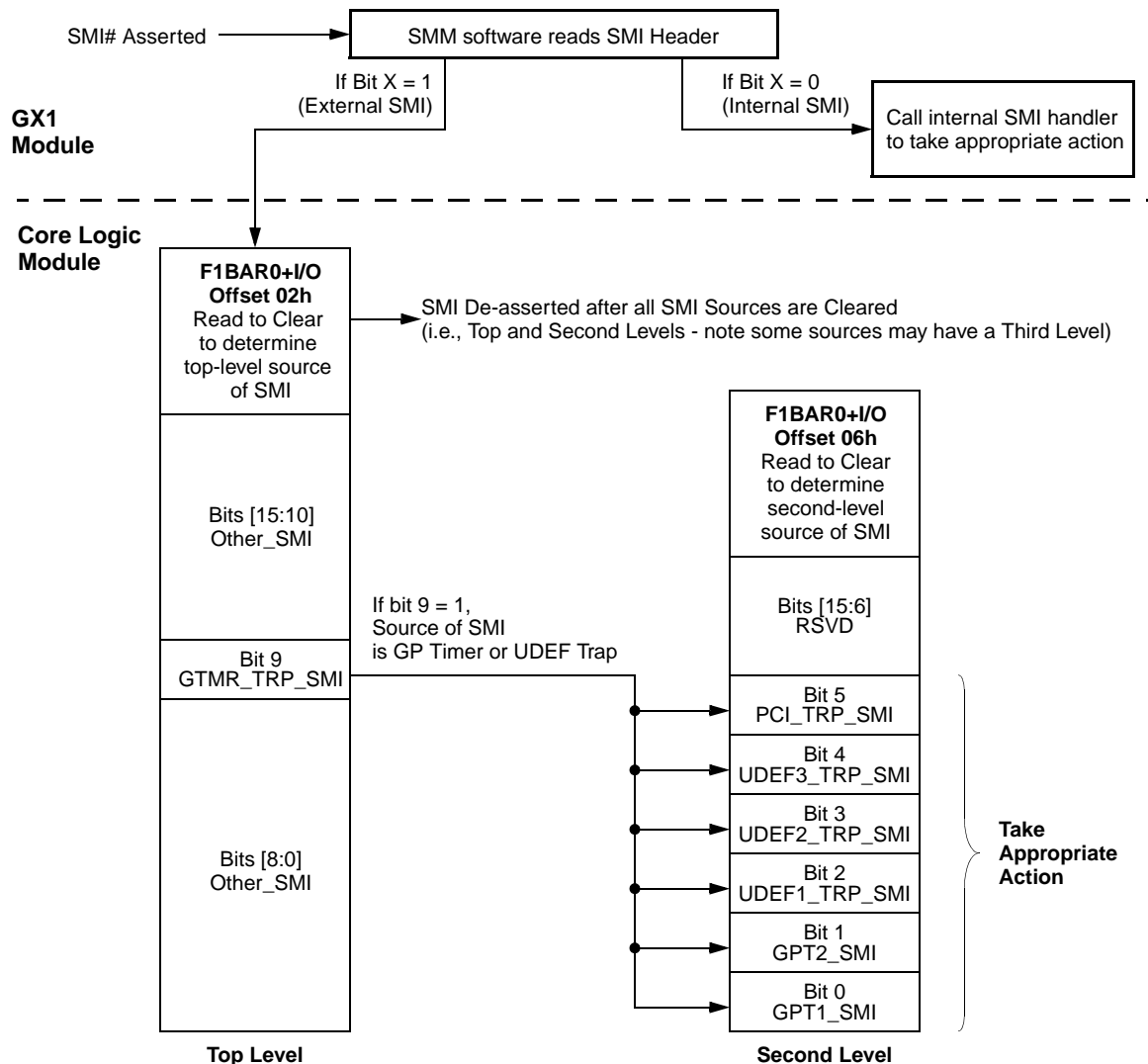
Power management events are reported to the GX1 module through the active low SMI# signal. When an SMI is initiated, the SMI# signal is asserted low and is held low until all SMI sources are cleared. At that time, SMI# is deasserted.

All SMI sources report to the Top Level SMI Status register (F1BAR0+I/O Offset 02h) and the Top Level SMI Status Mirror register (F1BAR0+I/O Offset 00h). The Top SMI Status and Status Mirror registers are the top level of hierarchy for the SMI Handler in determining the source of an SMI.

These two registers are identical except that reading the register at F1BAR0+I/O Offset 02h clears the status.

Since all SMI sources report to the Top Level SMI Status register, many of its bits combine a large number of events requiring a second level of SMI status reporting. The second level of SMI status reporting is set up very much like the top level. There are two status reporting registers, one “read only” (mirror) and one “read to clear”. The data returned by reading either offset is the same, the difference between the two being that the SMI can not be cleared by reading the mirror register.

Figure 6-11 on page 181 shows an example SMI tree for checking and clearing the source of General Purpose Timers and the User Defined Trap generated SMI.



**Figure 6-11. General Purpose Timer and UDEF Trap SMI Tree Example**

**6.2.10.4 Power Management Programming Summary**

Table 6-9 provides a programming register summary for the power management timers, traps, and functions. For

complete bit information regarding the registers listed in Table 6-9, refer to Section 6.4.1 "Bridge, GPIO, and LPC Registers - Function 0" on page 206.

**Table 6-9. Device Power Management Programming Summary**

| Device Power Management Resource | Located at F0 Index xxh Unless Otherwise Noted |                                |                                  |                                    |
|----------------------------------|--|--------------------------------|----------------------------------|------------------------------------|
|                                  | Enable   | Configuration                  | Second Level SMI Status/No Clear | Second Level SMI Status/With Clear |
| Global Timer Enable              | 80h[0]   | N/A                            | N/A                              | N/A                                |
| Keyboard / Mouse Idle Timer      | 81h[3]   | 93h[1:0]                       | 85h[3]                           | F5h[3]                             |
| Parallel / Serial Idle Timer     | 81h[2]   | 93h[1:0]                       | 85h[2]                           | F5h[2]                             |
| Floppy Disk Idle Timer           | 81h[1]   | 9Ah[15:0], 93h[7]              | 85h[1]                           | F5h[1]                             |
| Video Idle Timer <sup>1</sup>    | 81h[7]   | A6h[15:0]                      | 85h[7]                           | F5h[7]                             |
| VGA Timer <sup>2</sup>           | 83h[3]   | 8Eh[7:0]                       | F1BAR0+I/O Offset 00h[6]         | F1BAR0+I/O Offset 02h[6]           |
| Primary Hard Disk Idle Timer     | 81h[0]   | 98h[15:0], 93h[5]              | 85h[0]                           | F5h[0]                             |
| Secondary Hard Disk Idle Timer   | 83h[7]   | ACh[15:0], 93h[4]              | 86h[4]                           | F6h[4]                             |
| User Defined Device 1 Idle Timer | 81h[4]   | A0h[15:0], C0h[31:0], CCh[7:0] | 85h[4]                           | F5h[4]                             |
| User Defined Device 2 Idle Timer | 81h[5]   | A2h[15:0], C4h[31:0], CDh[7:0] | 85h[5]                           | F5h[5]                             |
| User Defined Device 3 Idle Timer | 81h[6]   | A4h[15:0], C8h[31:0], CEh[7:0] | 85h[6]                           | F5h[6]                             |
| Global Trap Enable               | 80h[2]   | N/A                            | N/A                              | N/A                                |
| Keyboard / Mouse Trap            | 82h[3]   | 9Eh[15:0] 93h[1:0]             | 86h[3]                           | F6h[3]                             |
| Parallel / Serial Trap           | 82h[2]   | 9Ch[15:0], 93h[1:0]            | 86h[2]                           | F6h[2]                             |
| Floppy Disk Trap                 | 82h[1]   | 93h[7]                         | 86h[1]                           | F6h[1]                             |
| Video Access Trap                | 82h[7]   | N/A                            | 86h[7]                           | F6h[7]                             |
| Primary Hard Disk Trap           | 82h[0]   | 93h[5]                         | 86h[0]                           | F6h[0]                             |
| Secondary Hard Disk Trap         | 83h[6]   | 93h[4]                         | 86h[5]                           | F6h[5]                             |
| User Defined Device 1 Trap       | 82h[4]   | C0h[31:0], CCh[7:0]            | F1BAR0+I/O Offset 04h[2]         | F1BAR0+I/O Offset 06h[2]           |
| User Defined Device 2 Trap       | 82h[5]   | C4h[31:0], CDh[7:0]            | F1BAR0+I/O Offset 04h[3]         | F1BAR0+I/O Offset 06h[3]           |
| User Defined Device 3 Trap       | 82h[6]   | C8h[31:0], CEh[7:0]            | F1BAR0+I/O Offset 04h[4]         | F1BAR0+I/O Offset 06h[4]           |
| General Purpose Timer 1          | 83h[0]   | 88h[7:0], 89h[7:0], 8Bh[4]     | F1BAR0+I/O Offset 04h[0]         | F1BAR0+I/O Offset 06h[0]           |
| General Purpose Timer 2          | 83h[1]   | 8Ah[7:0], 8Bh[5,3,2]           | F1BAR0+I/O Offset 04h[1]         | F1BAR0+I/O Offset 06h[1]           |
| Suspend Modulation               | 96h[0]   | 94h[15:0], 96h[2:0]            | N/A                              | N/A                                |
| Video Speedup                    | 80h[4]   | 8Dh[7:0], A8h[15:0]            | N/A                              | N/A                                |
| IRQ Speedup                      | 80h[3]   | 8Ch[7:0]                       | N/A                              | N/A                                |

1. This function is used for Suspend determination.
2. This function is used for SoftVGA.

### 6.2.11 GPIO Interface

Up to 64 GPIOs in the in the Core Logic module are provided for system control. For further information, see Section 4.2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88 and Table 6-30 "F0BAR0+I/O Offset: GPIO Configuration Registers" on page 240.

**Note:** Not all GPIOs are available on SC3200 balls. GPIOs [63:42], [31:21], and [5:2] are reserved.

### 6.2.12 Integrated Audio

The Core Logic module provides hardware support for the Virtual (soft) Audio subsystem as part of the Virtual System Architecture<sup>®</sup> (VSA<sup>™</sup>) technology for capture and playback of audio using an external codec. This eliminates much of the hardware traditionally associated with audio functions.

This hardware support includes:

- Six-channel buffered PCI bus mastering interface.
- AC97 version 2.0 compatible interface to the codec. Any codec, which supports an independent input and output sample rate conversion interface, can be used with the Core Logic module.

Additional hardware provides the necessary functionality for VSA. This hardware includes the ability to:

- Generate an SMI to alert software to update required data. An SMI is generated when either audio buffer is half empty or full. If the buffers become completely empty or full, the Empty bit is asserted.
- Generate an SMI on I/O traps.
- Trap accesses for sound card compatibility at either I/O Port 220h-22Fh, 240h-24Fh, 260h-26Fh, or 280h-28Fh.
- Trap accesses for FM compatibility at I/O Port 388h-38Bh.

- Trap accesses for MIDI UART interface at I/O Port 300h-301h or 330h-331h.
- Trap accesses for serial input and output at COM2 (I/O Port 2F8h-2FFh) or COM4 (I/O Port 2E8h-2EFh).
- Support trapping for low (I/O Port 00h-0Fh) and/or high (I/O Port C0h-DFh) DMA accesses.
- Support hardware status register reads in Core Logic module, minimizing SMI overhead.
- Support is provided for software-generated IRQs on IRQ 2, 3, 5, 7, 10, 11, 12, 13, 14, and 15.

The following subsections include details of the registers used for configuring the audio interface. The registers are accessed through F3 Index 10h, the Base Address Register (F3BAR0) in Function 3. F3BAR0 sets the base address for the audio support registers as shown in Table 6-37 "F3: PCI Header Registers for Audio Configuration" on page 279.

#### 6.2.12.1 Data Transport Hardware

The data transport hardware can be broadly divided into two sections: bus mastering and the codec interface.

##### Audio Bus Masters

The Core Logic module audio hardware includes six PCI bus masters (three for input and three for output) for transferring digitized audio between memory and the external codec. With these bus master engines, the Core Logic module off-loads the CPU and improves system performance.

The programming interface defines a simple scatter/gather mechanism allowing large transfer blocks to be scattered to or gathered from memory. This cuts down on the number of interrupts to and interactions with the CPU.

The six bus masters that directly drive specific slots on the AC97 interface are described in Table 6-10.

**Table 6-10. Bus Masters That Drive Specific Slots of the AC97 Interface**

| Audio Bus Master # | Slots   | Description   |
|--------------------|---------|---|
| 0                  | 3 and 4 | 32-Bit output to codec. Left and right channels.                                    |
| 1                  | 3 and 4 | 32-Bit input from codec. Left and right channels.                                   |
| 2                  | 5       | 16-Bit output to codec.   |
| 3                  | 5       | 16-Bit input from codec.  |
| 4                  | 6 or 11 | 16-Bit output to codec. Slot in use is determined by F3BAR0+Memory Offset 08h[19].  |
| 5                  | 6 or 11 | 16-Bit input from codec. Slot in use is determined by F3BAR0+Memory Offset 08h[20]. |

**Physical Region Descriptor Table Address**

Before the bus master starts a master transfer it must be programmed with a pointer (PRD Table Address register) to a Physical Region Descriptor Table. This pointer sets the starting memory location of the Physical Region Descriptors (PRDs). The PRDs describe the areas of memory that are used in the data transfer. The descriptor table entries must be aligned on a 32-byte boundary and the table cannot cross a 64 KB boundary in memory.

**Physical Region Descriptor Format**

Each physical memory region to be transferred is described by a Physical Region Descriptor (PRD) as illustrated in Table 6-11. When the bus master is enabled (Command register bit 0 = 1), data transfer proceeds until each PRD in the PRD table has been transferred. The bus master does not cache PRDs.

The PRD table consists of two DWORDs. The first DWORD contains a 32-bit pointer to a buffer to be transferred. The second DWORD contains the size (16 bits) of the buffer and flags (EOT, EOP, JMP). The description of the flags are as follows:

- EOT bit - If set in a PRD, this bit indicates the last entry in the PRD table (bit 31). The last entry in a PRD table must have either the EOT bit or the JMP bit set. A PRD can not have both the JMP and EOT bits set.
- EOP bit - If set in a PRD and the bus master has completed the PRD's transfer, the End of Page bit is set (Status register bit 0 = 1) and an SMI is generated. If a second EOP is reached due to the completion of another PRD before the End of Page bit is cleared, the Bus Master Error bit is set (Status register bit 1 = 1) and the bus master pauses. In this paused condition, reading the Status register clears both the Bus Master Error and the End of Page bits and the bus master continues.
- JMP bit - This PRD is special. If set, the Memory Region Physical Base Address is now the target address of the JMP. The target address must be on a 32-byte boundary so bits[4:0] must be written to 0. There is no data transfer with this PRD. This PRD allows the creation of a

looping mechanism. If a PRD table is created with the JMP bit set in the last PRD, the PRD table does not need a PRD with the EOT bit set. A PRD can not have both the JMP and EOT bits set.

**Programming Model**

The following discussion explains, in steps, how to initiate and maintain a bus master transfer between memory and an audio slave device.

In the steps listed below, the reference to "Example" refers to Figure 6-12 "PRD Table Example" on page 185.

- 1) Software creates a PRD table in system memory. Each PRD entry is 8 bytes long; consisting of a base address pointer and buffer size. The maximum data that can be transferred from a PRD entry is 64 KB. A PRD table must be aligned on a 32-byte boundary. The last PRD in a PRD table must have the EOT or JMP bit set.

**Example** - Assume the data is outbound. There are three PRDs in the example PRD table. The first two PRDs (PRD\_1, PRD\_2) have only the EOP bit set. The last PRD (PRD\_3) has only the JMP bit set. This example creates a PRD loop.

- 2) Software loads the starting address of the PRD table by programming the PRD Table Address register.

**Example** - Program the PRD Table Address register with Address\_3.

- 3) Software must fill the buffers pointed to by the PRDs with audio data. It is not absolutely necessary to fill the buffers; however, the buffer filling process must stay ahead of the buffer emptying. The simplest way to do this is by using the EOP flags to generate an SMI when a PRD is empty.

Example - Fill Audio Buffer\_1 and Audio Buffer\_2. The SMI generated by the EOP from the first PRD allows the software to refill Audio Buffer\_1. The second SMI refills Audio Buffer\_2. The third SMI refills Audio Buffer\_1 and so on.

**Table 6-11. Physical Region Descriptor Format**

| DWORD | Byte 3  |    |    |          |    |    |    |    | Byte 2 |    |    |    |    |    |    |    | Byte 1      |    |    |    |    |    |   |   | Byte 0 |   |   |   |   |   |   |   |
|-------|---|----|----|----------|----|----|----|----|--------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
|       | 31  | 30 | 29 | 28       | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0     | Memory Region Base Address [31:1] (Audio Data Buffer) |    |    |          |    |    |    |    |        |    |    |    |    |    |    |    | 0           |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
| 1     | E   | E  | J  | Reserved |    |    |    |    |        |    |    |    |    |    |    |    | Size [15:1] |    |    |    |    |    |   |   | 0      |   |   |   |   |   |   |   |
|       | O   | O  | M  |          |    |    |    |    |        |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|       | T   | P  | P  |          |    |    |    |    |        |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |



- 4) Read the SMI Status register to clear the Bus Master Error and End of Page bits (bits 1 and 0).

Set the correct direction to the Read or Write Control bit (Command register bit 3). Note that the direction of the data transfer of a particular bus master is fixed and therefore the direction bit must be programmed accordingly. It is assumed that the codec has been properly programmed to receive the audio data.

Engage the bus master by writing a “1” to the Bus Master Control bit (Command register bit 0).

The bus master reads the PRD entry pointed to by the PRD Table Address register and increments the address by 08h to point to the next PRD. The transfer begins.

**Example** - The bus master is now properly programmed to transfer Audio Buffer\_1 to a specific slot(s) in the AC97 interface.

- 5) The bus master transfers data to/from memory responding to bus master requests from the AC97 interface. At the completion of each PRD, the bus master’s next response depends on the settings of the flags in the PRD.

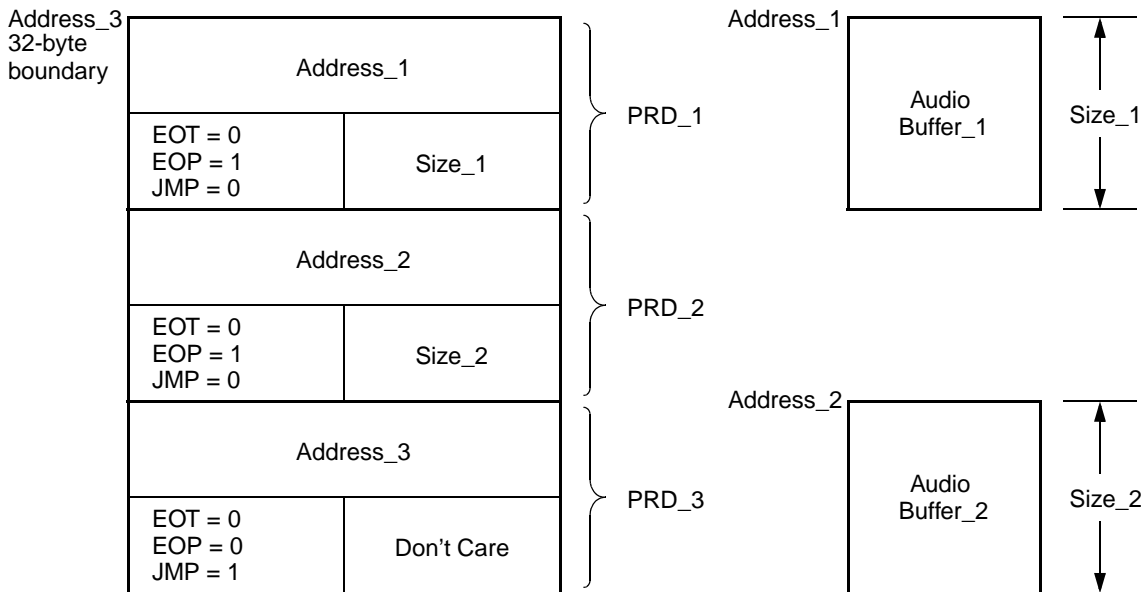
**Example** - At the completion of PRD\_1 an SMI is generated because the EOP bit is set while the bus master continues on to PRD\_2. The address in the PRD

Table Address register is incremented by 08h and is now pointing to PRD\_3. The SMI Status register is read to clear the End of Page status flag. Since Audio Buffer\_1 is now empty, the software can refill it.

At the completion of PRD\_2 an SMI is generated because the EOP bit is set. The bus master then continues on to PRD\_3. The address in the PRD Table Address register is incremented by 08h. The DMA SMI Status register is read to clear the End of Page status flag. Since Audio Buffer\_2 is now empty, the software can refill it. Audio Buffer\_1 has been refilled from the previous SMI.

PRD\_3 has the JMP bit set. This means the bus master uses the address stored in PRD\_3 (Address\_3) to locate the next PRD. It does not use the address in the PRD Table Address register to get the next PRD. Since Address\_3 is the location of PRD\_1, the bus master has looped the PRD table.

Stopping the bus master can be accomplished by not reading the SMI Status register End of Page status flag. This leads to a second EOP which causes a Bus Master Error and pauses the bus master. In effect, once a bus master has been enabled it never has to be disabled, just paused. The bus master cannot be disabled unless the bus master has been paused or has reached an EOT.



**Figure 6-12. PRD Table Example**

**6.2.12.2 AC97 Codec Interface**

The AC97 codec (e.g., LM4548) is the master of the serial interface and generates the clocks to Core Logic module. Figure 6-13 shows the signal connections between two codecs and the SC3200:

- Codec1 can be AC97 Rev. 1.3 or higher compliant.
- Codec2 is optional, but must be compliant with AC97 2.0 or higher. (For specifics on the serial interface, refer to the appropriate codec manufacturer's data book.)
  - SDATA\_IN2 has wakeup capability. (See Section 5.6 "System Wakeup Control (SWC)" on page 132.)
  - If SDATA\_IN2 is not used it must be connected to V<sub>SS</sub>.
  - If an AMC97 codec is used (as Codec2), it should be connected to SDATA\_IN2 and SDATA\_IN should be connected to V<sub>SS</sub>.
- For PC speaker synthesis, the Core Logic module outputs the PC speaker signal on the PC\_BEEP pin which is connected to the PC\_BEEP input of the AC97 codec. Note that PC\_BEEP is muxed with GPIO16 and must be programmed via PMR[0] (see Table 4-2 on page 88.)

**Codec Configuration/Control Registers**

The codec 32-bit related registers:

- GPIO Status and Control Registers
  - Codec GPIO Status Register (F3BAR0+Memory Offset 00h)
  - Codec GPIO Control Register (F3BAR0+Memory Offset 04h)
- Codec Status Register (F3BAR0+Memory Offset 08h)
- Codec Command Register (F3BAR0+Memory Offset 0Ch)

**Codec GPIO Status and Control Registers:**

The Codec GPIO Status and Control registers are used for codec GPIO related tasks such as enabling a codec GPIO interrupt to cause an SMI.

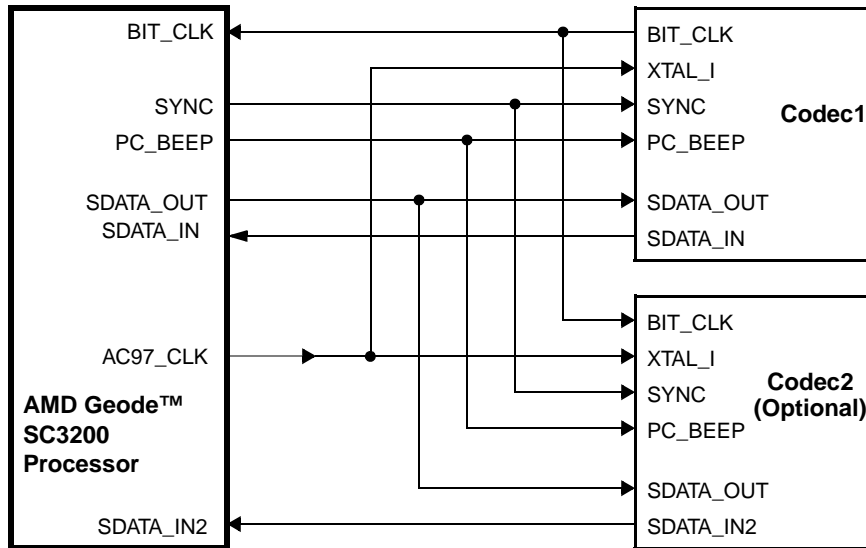
**Codec Status Register:**

The Codec Status register stores the codec status WORD. It is updated every valid Status Word slot.

**Codec Command Register:**

The Codec Command register writes the control WORD to the codec. By writing the appropriate control WORDs to this port, the features of the codec can be controlled. The contents of this register are written to the codec during the Control Word slot.

The bit formats for these registers are given in Table 6-38 "F3BAR0+Memory Offset: Audio Configuration Registers" on page 280.



**Figure 6-13. AC97 V2.0 Codec Signal Connections**

### 6.2.12.3 VSA Technology Support Hardware

The Core Logic module incorporates the required hardware in order to support the Virtual System Architecture® (VSA) technology for capture and playback of audio using an external codec. This eliminates much of the hardware traditionally associated with industry standard audio functions.

#### VSA Technology

VSA technology provides a framework to enable software implementation of traditionally hardware-only components. VSA software executes in System Management Mode (SMM), enabling it to execute transparently to the operating system, drivers and applications.

The VSA design is based upon a simple model for replacing hardware components with software. Hardware to be virtualized is merely replaced with simple access detection circuitry which asserts the SMI# (System Management Interrupt) internal signal when hardware accesses are detected. The current execution stream is immediately preempted, and the processor enters SMM. The SMM system software then saves the processor state, initializes the VSA execution environment, decodes the SMI source and dispatches handler routines which have registered requests to service the decoded SMI source. Once all handler routines have completed, the processor state is restored and normal execution resumes. In this manner, hardware accesses are transparently replaced with the execution of SMM handler software.

Historically, SMM software was used primarily for the single purpose of facilitating active power management for notebook designs. That software's only function was to manage the power up and down of devices to save power. With high performance processors now available, it is feasible to implement, primarily in SMM software, PC capabilities traditionally provided by hardware. In contrast to power management code, this virtualization software generally has strict performance requirements to prevent application performance from being significantly impacted.

#### Audio SMI Related Registers

The SMI related registers consist of:

- Audio SMI Status Reporting Registers:
  - Top Level SMI Mirror and Status Registers (F1BAR0+Memory Offset 00h/02h)
  - Second Level SMI Status Registers (F3BAR0+Memory Offset 10h/12h)
- I/O Trap SMI and Fast Write Status Register (F3BAR0+Memory Offset 14h)
- I/O Trap SMI Enable Register (F3BAR0+Memory Offset 18h)

#### Audio SMI Status Reporting Registers:

The Top SMI Status Mirror and Status registers are the top level of hierarchy for the SMI Handler in determining the source of an SMI. These two registers are at F1BAR0+Memory Offset 00h (Status Mirror) and 02h (Status). The registers are identical except that reading the register at F1BAR0+Memory Offset 02h clears the status.

The second level of audio SMI status reporting is set up very much like the top level. There are two status reporting registers, one "read only" (mirror) and one "read to clear". The data returned by reading either offset is the same (i.e., SMI was caused by an audio related event). The difference between F3BAR0+Memory Offset 10h (Status Mirror) and 12h (Status) is in the ability to clear the SMI source at 12h.

Figure 6-14 on page 188 shows an SMI tree for checking and clearing the source of an audio SMI. Only the audio SMI bit is detailed here. For details regarding the remaining bits in the Top SMI Status Mirror and Status registers refer to Table 6-33 "F1BAR0+I/O Offset: SMI Status Registers" on page 253.

#### I/O Trap SMI and Fast Write Status Register:

This 32-bit read-only register (F3BAR0+Memory Offset 14h) not only indicates if the enabled I/O trap generated an SMI, but also contains Fast Path Write related bits.

#### I/O Trap SMI Enable Register:

The I/O Trap SMI Enable register (F3BAR0+Memory Offset 18h) allows traps for specified I/O addresses and configures generation for I/O events. It also contains the enabling bit for Fast Path Read/Write features.

#### Status Fast Path Read/Write

Status Fast Path Read – If enabled, the Core Logic module intercepts and responds to reads to several status registers. This speeds up operations, and prevents SMI generation for reads to these registers. This process is called Status Fast Path Read. Status Fast Path Read is enabled via F3BAR0+Memory Offset 18h[4].

In Status Fast Path Read the Core Logic module responds to reads of the following addresses:

388h-38Bh, 2x0h, 2x1h, 2x2h, 2x3h, 2x8h and 2x9h

Note that if neither sound card or FM I/O mapping is enabled, then status read trapping is not possible.

Fast Path Write – If enabled, the Core Logic module captures certain writes to several I/O locations. This feature prevents two SMIs from being asserted for write operations that are known to take two accesses (the first access is an index and the second is data). This process is called Fast Path Write. Fast Path Write is enabled in via F3BAR0+Memory Offset 18h[11].

Fast Path Write captures the data and address bit 1 (A1) of the first access, but does not generate an SMI. A1 is stored in F3BAR0+Memory Offset 14h[15]. The second access causes an SMI, and the data and address are captured as in a normal trapped I/O.

In Fast Path Write, the Core Logic module responds to writes to the following addresses: 388h, 38Ah, 38Bh, 2x0h, 2x2h, and 2x8h.

Table 6-38 on page 280 shows the bit formats of the second level SMI status reporting registers and the Fast Path Read/Write programming bits.

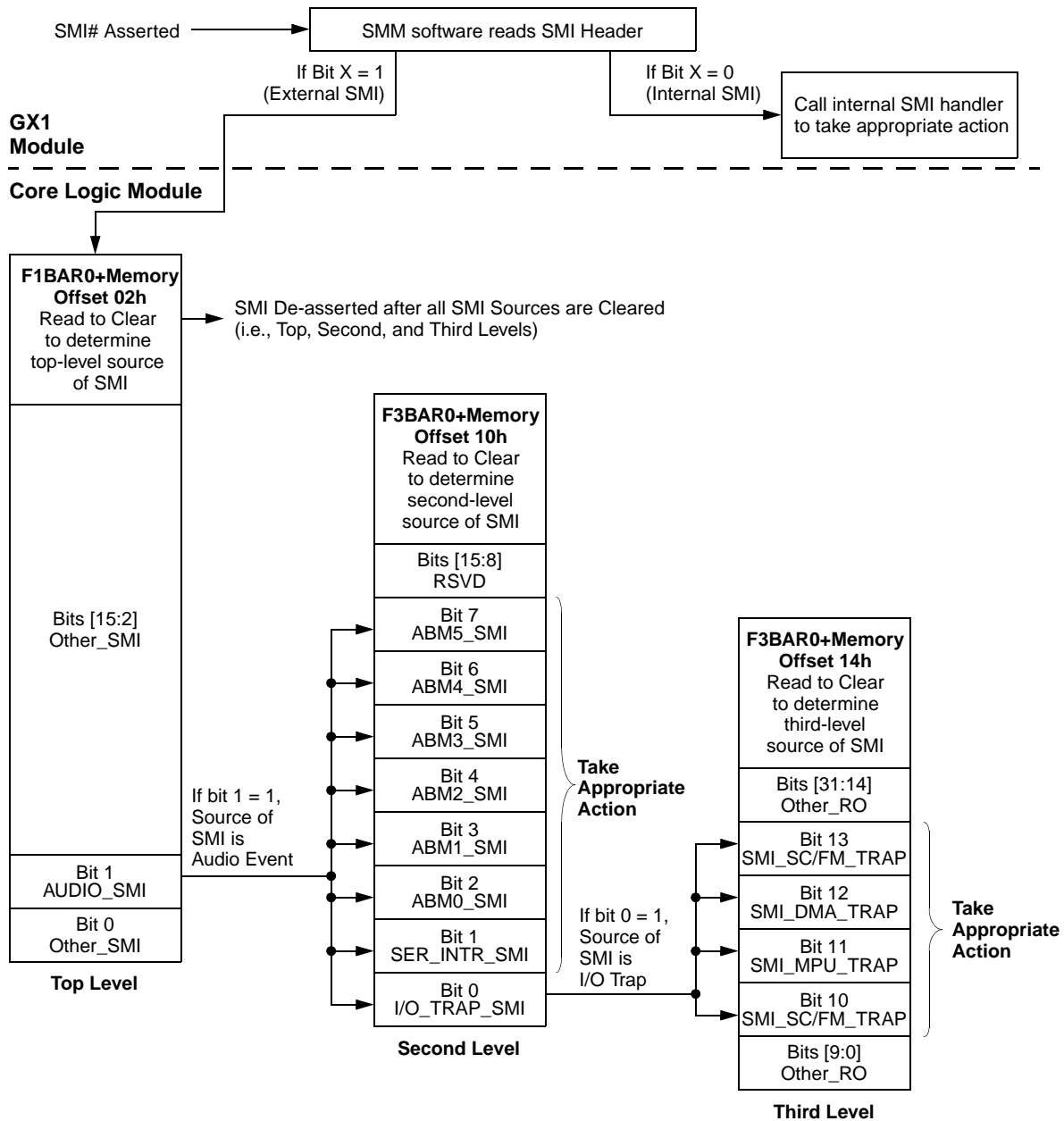


Figure 6-14. Audio SMI Tree Example

#### 6.2.12.4 IRQ Configuration Registers

The Core Logic module provides the ability to set and clear IRQs internally through software control. If the IRQs are configured for software control, they do not respond to external hardware. There are two registers provided for this feature:

- Internal IRQ Enable Register (F3BAR0+Memory Offset 1Ah)
- Internal IRQ Control Register (F3BAR0+Memory Offset 1Ch)

##### Internal IRQ Enable Register

The Internal IRQ Enable register configures the IRQs as internal (software) interrupts or external (hardware) interrupts. Any IRQ used as an internal software driven source must be configured as internal.

##### Internal IRQ Control Register

The Internal IRQ Control register allows individual software assertion/de-assertion of the IRQs that are enabled as internal. These bits are used as masks when attempting to write a particular IRQ bit. If the mask bit is set, it can then be asserted/de-asserted according to the value in the low-order 16 bits. Otherwise the assertion/de-assertion values of the particular IRQ can not be changed.

#### 6.2.12.5 LPC Interface

The LPC interface of the Core Logic module is based on the Intel® Low Pin Count (LPC) Interface specification, revision 1.0. In addition to the requirement pins that are specified in the Intel LPC Interface specification, the Core Logic module also supports three optional pins: LDRQ#, SERIRQ, and LPCPD#.

The following subsections briefly describe some sections of the specification. However, for full details refer to the LPC specification directly.

The goals of the LPC interface are to:

- Enable a system without an ISA bus.
- Reduce the cost of traditional ISA bus devices.
- Use on a motherboard only.
- Perform the same cycle types as the ISA bus: memory, I/O, DMA, and Bus Master.
- Increase the memory space from 16 MB to 4 GB to allow BIOS sizes much greater.
- Provide synchronous design. Much of the challenge of an ISA design is meeting the different, and in some cases conflicting, ISA timings. Make the timings synchronous to a reference well known to component designers, such as PCI.
- Support software transparency: do not require special drivers or configuration for this interface. The motherboard BIOS should be able to configure all devices at boot.

- Support desktop and mobile implementations.
- Enable support of a variable number of wait states.
- Enable I/O memory cycle retries in SMM handler.
- Enable support of wakeup and other power state transitions.

Assumptions and functionality requirements of the LPC interface are:

- Only the following class of devices may be connected to the LPC interface:
  - SuperI/O (FDC, SP, PP, IR, KBC) - I/O slave, DMA, bus master (for IR, PP).
  - Audio, including AC97 style design - I/O slave, DMA, bus master.
  - Generic Memory, including BIOS - Memory slave.
  - System Management Controller - I/O slave, bus master.
- Interrupts are communicated with the serial interrupt (SERIRQ) protocol.
- The LPC interface does not need to support high-speed buses (such as CardBus, 1394, etc.) downstream, nor does it need to support low-latency buses such as USB.

Figure 6-15 shows a typical setup. In this setup, the LPC is connected through the Core Logic module to a PCI or host bus.

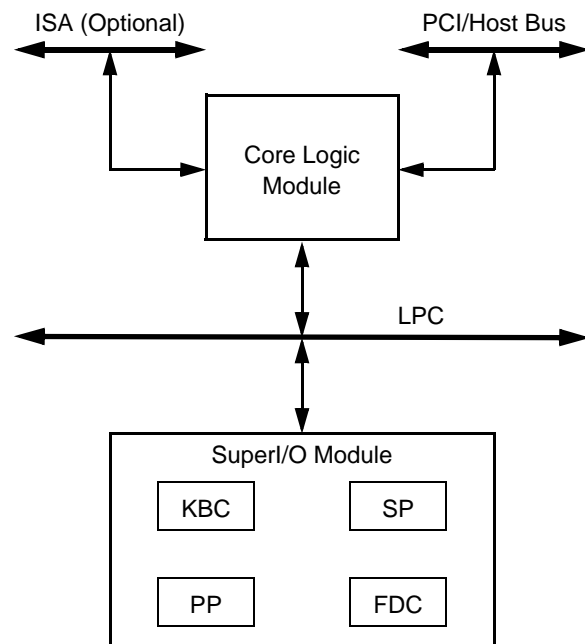


Figure 6-15. Typical Setup

### 6.2.12.6 LPC Interface Signal Definitions

The LPC specification lists seven required and six optional signals for supporting the LPC interface. Many of the signals are the same signals found on the PCI interface and do not require any new pins on the host. Required signals must be implemented by both hosts and peripherals. Optional signals may or may not be present on particular hosts or peripherals.

The Core Logic module incorporates all the required LPC interface signals and two of the optional signals:

- Required LPC signals:
  - LAD[3:0] - Multiplexed Command, Address and Data.
  - LFRAME# - Frame: Indicates start of a new cycle, termination of broken cycle.
  - LRESET# - Reset: This signal is not available. Use PCI Reset signal PCIRST# instead.
  - LCLK - Clock: This signal is not available. Use PCI 33 MHz clock signal PCICLK instead.
- Core Logic module optional LPC signals:
  - LDRQ# - Encoded DMA/Bus Master Request: Only needed by peripheral that need DMA or bus mastering. Peripherals may not share the LDRQ# signal.
  - SERIRQ - Serialized IRQ: Only needed by peripherals that need interrupt support.
  - LPCPD# - Power Down: Indicates that the peripheral should prepare for power to the LPC interface to be shut down. Optional for the host.

### 6.2.12.7 Cycle Types

Table 6-12 shows the various types of cycles that are supported by the Core Logic module.

**Table 6-12. Cycle Types**

| Cycle Type              | Supported Sizes (Bytes) |
|-------------------------|-------------------------|
| Memory Read             | 1                       |
| Memory Write            | 1                       |
| I/O Read                | 1                       |
| I/O Write               | 1                       |
| DMA Read                | 1 or 2                  |
| DMA Write               | 1 or 2                  |
| Bus Master Memory Read  | 1, 2, or 4              |
| Bus Master Memory Write | 1, 2, or 4              |

### 6.2.12.8 LPC Interface Support

The LPC interface supports all the features described in the LPC Bus Interface specification, revision 1.0, with the following exceptions:

- Only 8- or 16-bit DMA, depending on channel number. Does not support the optional larger transfer sizes.
- Only one external DRQ pin.

## 6.3 Register Descriptions

The Core Logic module is a multi-function module. Its register space can be broadly divided into three categories in which specific types of registers are located:

- 1) Chipset Register Space (F0-F5) (Note that F4 is for Video Processor support, see Section 7.3.1 on page 345 for register descriptions): Comprised of six separate functions, each with its own register space, consisting of PCI header registers and configuration registers.  
  
The PCI header is a 256-byte region used for configuring a PCI device or function. The first 64 bytes are the same for all PCI devices and are predefined by the PCI specification. These registers are used to configure the PCI for the device. The rest of the 256-byte region is used to configure the device or function itself.
- 2) USB Controller Register Space (PCIUSB): Consists of the standard PCI header registers. The USB controller supports three ports and is OpenHCI compliant.
- 3) ISA Legacy Register Space (I/O Ports): Contains all the legacy compatibility I/O ports that are internal, trapped, shadowed, or snooped.

The following subsections provide:

- A brief discussion on how to access the registers located in PCI Configuration Space.
- Core Logic module register summaries.
- Bit formats for Core Logic module registers.

### 6.3.1 PCI Configuration Space and Access Methods

Configuration cycles are generated in the processor. All configuration registers in the Core Logic module are accessed through the PCI interface using the PCI Type One Configuration Mechanism. This mechanism uses two DWORD I/O locations at 0CF8h and 0CFCh. The first location (0CF8h) references the Configuration Address register. The second location (0CFCh) references the Configuration Data Register (CDR).

To access PCI configuration space, write the Configuration Address (0CF8h) Register with data that specifies the Core Logic module as the device on PCI being accessed, along with the configuration register offset. On the following cycle, a read or write to the Configuration Data Register (CDR) causes a PCI configuration cycle to the Core Logic module. Byte, WORD, or DWORD accesses are allowed to CDR at 0CFCh, 0CFDh, 0CFEh, or 0CFHh.

The Core Logic module has seven PCI configuration register sets, one for each function (F0-F5) and USB (PCIUSB). Base Address Registers (BARx) in F0-F5 and PCIUSB set the base addresses for additional I/O or memory mapped configuration registers for each function.

Table 6-13 shows the PCI Configuration Address Register (0CF8h) and how to access the PCI header registers.

**Table 6-13. PCI Configuration Address Register (0CF8h)**

| 31  | 30 | 24              | 23 | 16                | 15 | 11                     | 10 | 8               | 7 | 2            | 1 | 0               |
|---|----|-----------------|----|-------------------|----|------------------------|----|-----------------|---|--------------|---|-----------------|
| <b>Configuration Space Mapping</b>  |    | <b>Reserved</b> |    | <b>Bus Number</b> |    | <b>Device Number</b>   |    | <b>Function</b> |   | <b>Index</b> |   | <b>DWORD 00</b> |
| 1 (Enable)  |    | 000 000         |    | 0000 0000         |    | xxxx x ( <b>Note</b> ) |    | xxx             |   | xxxx xx      |   | 00 (Always)     |
| <b>Function 0 (F0): Bridge Configuration, GPIO and LPC Configuration Register Space</b>   |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 000                    |    |                 |   |              |   | Index           |
| <b>Function 1 (F1): SMI Status and ACPI Timer Configuration Register Space</b>  |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 001                    |    |                 |   |              |   | Index           |
| <b>Function 2 (F2): IDE Controller Configuration Register Space</b>   |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 010                    |    |                 |   |              |   | Index           |
| <b>Function 3 (F3): Audio Configuration Register Space</b>  |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 011                    |    |                 |   |              |   | Index           |
| <b>Function 4 (F4): Video Processor Configuration Register Space</b>  |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 100                    |    |                 |   |              |   | Index           |
| <b>Function 5 (F5): X-Bus Expansion Configuration Register Space</b>  |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 0 or 1000 0  |    | 101                    |    |                 |   |              |   | Index           |
| <b>PCIUSB: USB Controller Configuration Register Space</b>  |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |
| 80h   |    | 0000 0000       |    | 1001 1 or 1000 1  |    | 000                    |    |                 |   |              |   | Index           |
| <b>Note:</b> The device number depends upon the IDSEL Strap Override bit (F5BAR0+I/O Offset 04h[0]). This bit allows selection of the address lines to be used as the IDSEL. By Default: IDSEL = AD28 (1001 0) for F0-F5, AD29 (1001 1) for PCIUSB. |    |                 |    |                   |    |                        |    |                 |   |              |   |                 |

### 6.3.2 Register Summary

The tables in this subsection summarize the registers of the Core Logic module. Included in the tables are the register's reset values and page references where the bit formats are found.

**Note:** Function 4 (F4) is for Video Processor support (although accessed through the Core Logic PCI configuration registers). Refer to Section 7.3.1 "Register Summary" on page 345 for details.

**Table 6-14. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support Summary**

| F0 Index | Width (Bits) | Type | Name   | Reset Value | Reference (Table 6-29) |
|----------|--------------|------|--|-------------|------------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register   | 100Bh       | Page 206               |
| 02h-03h  | 16           | RO   | Device Identification Register   | 0500h       | Page 206               |
| 04h-05h  | 16           | R/W  | PCI Command Register   | 000Fh       | Page 206               |
| 06h-07h  | 16           | R/W  | PCI Status Register  | 0280h       | Page 207               |
| 08h      | 8            | RO   | Device Revision ID Register  | 00h         | Page 208               |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register  | 060100h     | Page 208               |
| 0Ch      | 8            | R/W  | PCI Cache Line Size Register   | 00h         | Page 208               |
| 0Dh      | 8            | R/W  | PCI Latency Timer Register   | 00h         | Page 208               |
| 0Eh      | 8            | RO   | PCI Header Type Register   | 80h         | Page 208               |
| 0Fh      | 8            | RO   | PCI BIST Register  | 00h         | Page 208               |
| 10h-13h  | 32           | R/W  | Base Address Register 0 (F0BAR0) — Sets the base address for the I/O mapped GPIO Runtime and Configuration Registers (summarized in Table 6-15). | 00000001h   | Page 208               |
| 14h-17h  | 32           | R/W  | Base Address Register 1 (F0BAR1) — Sets the base address for the I/O mapped LPC Configuration Registers (summarized in Table 6-16)               | 00000001h   | Page 208               |
| 18h-2Bh  | ---          | ---  | Reserved   | 00h         | Page 208               |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID  | 100Bh       | Page 208               |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID   | 0500h       | Page 208               |
| 30h-3Fh  | ---          | ---  | Reserved   | 00h         | Page 208               |
| 40h      | 8            | R/W  | PCI Function Control Register 1  | 39h         | Page 209               |
| 41h      | 8            | R/W  | PCI Function Control Register 2  | 00h         | Page 209               |
| 42h      | ---          | ---  | Reserved   | 00h         | Page 210               |
| 43h      | 8            | R/W  | PIT Delayed Transactions Register  | 02h         | Page 210               |
| 44h      | 8            | R/W  | Reset Control Register   | 01h         | Page 210               |
| 45h      | ---          | ---  | Reserved   | 00h         | Page 211               |
| 46h      | 8            | R/W  | PCI Functions Enable Register  | FEh         | Page 211               |
| 47h      | 8            | R/W  | Miscellaneous Enable Register  | 00h         | Page 211               |
| 48h-4Bh  | ---          | ---  | Reserved   | 00h         | Page 211               |
| 4Ch-4Fh  | 32           | R/W  | Top of System Memory   | FFFFFFFFh   | Page 212               |
| 50h      | 8            | R/W  | PIT Control/ISA CLK Divider  | 7Bh         | Page 212               |
| 51h      | 8            | R/W  | ISA I/O Recovery Control Register  | 40h         | Page 212               |
| 52h      | 8            | R/W  | ROM/AT Logic Control Register  | 98h         | Page 213               |
| 53h      | 8            | R/W  | Alternate CPU Support Register   | 00h         | Page 213               |
| 54h-59h  | ---          | ---  | Reserved   | 00h         | Page 214               |
| 5Ah      | 8            | R/W  | Decode Control Register 1  | 01h         | Page 214               |
| 5Bh      | 8            | R/W  | Decode Control Register 2  | 20h         | Page 214               |
| 5Ch      | 8            | R/W  | PCI Interrupt Steering Register 1  | 00h         | Page 215               |
| 5Dh      | 8            | R/W  | PCI Interrupt Steering Register 2  | 00h         | Page 215               |
| 5Eh-5Fh  | ---          | ---  | Reserved   | 00h         | Page 215               |
| 60h-63h  | 32           | R/W  | ACPI Control Register  | 00000000h   | Page 216               |
| 64h-6Bh  | ---          | ---  | Reserved   | 00h         | Page 216               |



**Table 6-14. F0: PCI Header/Bridge Configuration Registers  
for GPIO and LPC Support Summary (Continued)**

| F0 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 6-29) |
|----------|--------------|------|---|-------------|------------------------|
| 6Ch-6Fh  | 32           | R/W  | ROM Mask Register                                       | 0000FFF0h   | Page 216               |
| 70h-71h  | 16           | R/W  | IOCS1# Base Address Register                            | 0000h       | Page 217               |
| 72h      | 8            | R/W  | IOCS1# Control Register                                 | 00h         | Page 217               |
| 73h      | 8            | ---  | Reserved  | 00h         | Page 217               |
| 74h-75h  | 16           | R/W  | IOCS0 Base Address Register                             | 0000h       | Page 217               |
| 76h      | 8            | R/W  | IOCS0 Control Register                                  | 00h         | Page 217               |
| 77h      | ---          | ---  | Reserved  | 00h         | Page 217               |
| 78h-7Bh  | 32           | R/W  | DOCCS Base Address Register                             | 00000000h   | Page 218               |
| 7Ch-7Fh  | 32           | R/W  | DOCCS Control Register                                  | 00000000h   | Page 218               |
| 80h      | 8            | R/W  | Power Management Enable Register 1                      | 00h         | Page 218               |
| 81h      | 8            | R/W  | Power Management Enable Register 2                      | 00h         | Page 219               |
| 82h      | 8            | R/W  | Power Management Enable Register 3                      | 00h         | Page 221               |
| 83h      | 8            | R/W  | Power Management Enable Register 4                      | 00h         | Page 222               |
| 84h      | 8            | RO   | Second Level PME/SMI Status Mirror Register 1           | 00h         | Page 223               |
| 85h      | 8            | RO   | Second Level PME/SMI Status Mirror Register 2           | 00h         | Page 224               |
| 86h      | 8            | RO   | Second Level PME/SMI Status Mirror Register 3           | 00h         | Page 225               |
| 87h      | 8            | RO   | Second Level PME/SMI Status Mirror Register 4           | 00h         | Page 226               |
| 88h      | 8            | R/W  | General Purpose Timer 1 Count Register                  | 00h         | Page 226               |
| 89h      | 8            | R/W  | General Purpose Timer 1 Control Register                | 00h         | Page 227               |
| 8Ah      | 8            | R/W  | General Purpose Timer 2 Count Register                  | 00h         | Page 228               |
| 8Bh      | 8            | R/W  | General Purpose Timer 2 Control Register                | 00h         | Page 228               |
| 8Ch      | 8            | R/W  | IRQ Speedup Timer Count Register                        | 00h         | Page 228               |
| 8Dh      | 8            | R/W  | Video Speedup Timer Count Register                      | 00h         | Page 228               |
| 8Eh      | 8            | R/W  | VGA Timer Count Register                                | 00h         | Page 229               |
| 8Fh-92h  | ---          | ---  | Reserved  | 00h         | Page 229               |
| 93h      | 8            | R/W  | Miscellaneous Device Control Register                   | 00h         | Page 229               |
| 94h-95h  | 16           | R/W  | Suspend Modulation Register                             | 0000h       | Page 229               |
| 96h      | 8            | R/W  | Suspend Configuration Register                          | 00h         | Page 230               |
| 97h      | ---          | ---  | Reserved  | 00h         | Page 230               |
| 98h-99h  | 16           | R/W  | Hard Disk Idle Timer Count Register — Primary Channel   | 0000h       | Page 230               |
| 9Ah-9Bh  | 16           | R/W  | Floppy Disk Idle Timer Count Register                   | 0000h       | Page 230               |
| 9Ch-9Dh  | 16           | R/W  | Parallel / Serial Idle Timer Count Register             | 0000h       | Page 230               |
| 9Eh-9Fh  | 16           | R/W  | Keyboard / Mouse Idle Timer Count Register              | 0000h       | Page 231               |
| A0h-A1h  | 16           | R/W  | User Defined Device 1 Idle Timer Count Register         | 0000h       | Page 231               |
| A2h-A3h  | 16           | R/W  | User Defined Device 2 Idle Timer Count Register         | 0000h       | Page 231               |
| A4h-A5h  | 16           | R/W  | User Defined Device 3 Idle Timer Count Register         | 0000h       | Page 231               |
| A6h-A7h  | 16           | R/W  | Video Idle Timer Count Register                         | 0000h       | Page 231               |
| A8h-A9h  | 16           | R/W  | Video Overflow Count Register                           | 0000h       | Page 231               |
| AAh-ABh  | ---          | ---  | Reserved  | 00h         | Page 231               |
| ACh-ADh  | 16           | R/W  | Hard Disk Idle Timer Count Register — Secondary Channel | 0000h       | Page 232               |
| AEh      | 8            | WO   | CPU Suspend Command Register                            | 00h         | Page 232               |
| AFh      | 8            | WO   | Suspend Notebook Command Register                       | 00h         | Page 232               |
| B0h-B3h  | ---          | ---  | Reserved  | 00h         | Page 232               |
| B4h      | 8            | RO   | Floppy Port 3F2h Shadow Register                        | xxh         | Page 232               |
| B5h      | 8            | RO   | Floppy Port 3F7h Shadow Register                        | xxh         | Page 232               |
| B6h      | 8            | RO   | Floppy Port 1F2h Shadow Register                        | xxh         | Page 232               |
| B7h      | 8            | RO   | Floppy Port 1F7h Shadow Register                        | xxh         | Page 232               |

**Table 6-14. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support Summary (Continued)**

| F0 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 6-29) |
|----------|--------------|------|---|-------------|------------------------|
| B8h      | 8            | RO   | DMA Shadow Register                         | xxh         | Page 233               |
| B9h      | 8            | RO   | PIC Shadow Register                         | xxh         | Page 233               |
| BAh      | 8            | RO   | PIT Shadow Register                         | xxh         | Page 233               |
| BBh      | 8            | RO   | RTC Index Shadow Register                   | xxh         | Page 234               |
| BCh      | 8            | R/W  | Clock Stop Control Register                 | 00h         | Page 234               |
| BDh-BFh  | ---          | ---  | Reserved                                    | 00h         | Page 234               |
| C0h-C3h  | 32           | R/W  | User Defined Device 1 Base Address Register | 00000000h   | Page 234               |
| C4h-C7h  | 32           | R/W  | User Defined Device 2 Base Address Register | 00000000h   | Page 234               |
| C8h-CBh  | 32           | R/W  | User Defined Device 3 Base Address Register | 00000000h   | Page 234               |
| CCh      | 8            | R/W  | User Defined Device 1 Control Register      | 00h         | Page 235               |
| CDh      | 8            | R/W  | User Defined Device 2 Control Register      | 00h         | Page 235               |
| CEh      | 8            | R/W  | User Defined Device 3 Control Register      | 00h         | Page 235               |
| CFh      | ---          | ---  | Reserved                                    | 00h         | Page 235               |
| D0h      | 8            | WO   | Software SMI Register                       | 00h         | Page 235               |
| D1h-EBh  | 16           | ---  | Reserved                                    | 00h         | Page 235               |
| ECh      | 8            | R/W  | Timer Test Register                         | 00h         | Page 236               |
| EDh-F3h  | ---          | ---  | Reserved                                    | 00h         | Page 236               |
| F4h      | 8            | RC   | Second Level PME/SMI Status Register 1      | 00h         | Page 236               |
| F5h      | 8            | RC   | Second Level PME/SMI Status Register 2      | 00h         | Page 236               |
| F6h      | 8            | RC   | Second Level PME/SMI Status Register 3      | 00h         | Page 237               |
| F7h      | 8            | RC   | Second Level PME/SMI Status Register 4      | 00h         | Page 238               |
| F8h-FFh  | ---          | ---  | Reserved                                    | 00h         | Page 239               |

Table 6-15. F0BAR0: GPIO Support Registers Summary

| F0BAR0+<br>I/O Offset | Width<br>(Bits) | Type  | Name                                      | Reset<br>Value | Reference<br>(Table 6-30) |
|-----------------------|-----------------|-------|---|----------------|---------------------------|
| 00h-03h               | 32              | R/W   | GPDO0 — GPIO Data Out 0 Register          | FFFFFFFFh      | Page 240                  |
| 04h-07h               | 32              | RO    | GPDI0 — GPIO Data In 0 Register           | FFFFFFFFh      | Page 240                  |
| 08h-0Bh               | 32              | R/W   | GPIEN0 — GPIO Interrupt Enable 0 Register | 00000000h      | Page 240                  |
| 0Ch-0Fh               | 32              | R/W1C | GPST0 — GPIO Status 0 Register            | 00000000h      | Page 240                  |
| 10h-13h               | 32              | R/W   | GPDO1 — GPIO Data Out 1 Register          | FFFFFFFFh      | Page 241                  |
| 14h-17h               | 32              | RO    | GPDI1 — GPIO Data In 1 Register           | FFFFFFFFh      | Page 241                  |
| 18h-1Bh               | 32              | R/W   | GPIEN1 — GPIO Interrupt Enable 1 Register | 00000000h      | Page 241                  |
| 1Ch-1Fh               | 32              | R/W1C | GPST1 — GPIO Status 1 Register            | 00000000h      | Page 241                  |
| 20h-23h               | 32              | R/W   | GPIO Signal Configuration Select Register | 00000000h      | Page 241                  |
| 24h-27h               | 32              | R/W   | GPIO Signal Configuration Access Register | 00000044h      | Page 242                  |
| 28h-2Bh               | 32              | R/W   | GPIO Reset Control Register               | 00000000h      | Page 243                  |

Table 6-16. F0BAR1: LPC Support Registers Summary

| F0BAR1+<br>I/O Offset | Width<br>(Bits) | Type | Name   | Reset<br>Value | Reference<br>(Table 6-31) |
|-----------------------|-----------------|------|--|----------------|---------------------------|
| 00h-03h               | 32              | R/W  | SERIRQ_SRC — Serial IRQ Source Register        | 00000000h      | Page 244                  |
| 04h-07h               | 32              | R/W  | SERIRQ_LVL — Serial IRQ Level Control Register | 00000000h      | Page 245                  |
| 08h-0Bh               | 32              | R/W  | SERIRQ_CNT — Serial IRQ Control Register       | 00000000h      | Page 247                  |
| 0Ch-0Fh               | 32              | R/W  | DRQ_SRC — DRQ Source Register                  | 00000000h      | Page 247                  |
| 10h-13h               | 32              | R/W  | LAD_EN — LPC Address Enable Register           | 00000000h      | Page 248                  |
| 14h-17h               | 32              | R/W  | LAD_D0 — LPC Address Decode 0 Register         | 00080020h      | Page 249                  |
| 18h-1Bh               | 32              | R/W  | LAD_D1 — LPC Address Decode 1 Register         | 00000000h      | Page 250                  |
| 1Ch-1Fh               | 32              | R/W  | LPC_ERR_SMI — LPC Error SMI Register           | 00000080h      | Page 250                  |
| 20h-23h               | 32              | RO   | LPC_ERR_ADD — LPC Error Address Register       | 00000000h      | Page 251                  |

**Table 6-17. F1: PCI Header Registers for SMI Status and ACPI Support Summary**

| F1 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 6-32) |
|----------|--------------|------|---|-------------|------------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register  | 100Bh       | Page 252               |
| 02h-03h  | 16           | RO   | Device Identification Register  | 0501h       | Page 252               |
| 04h-05h  | 16           | R/W  | PCI Command Register  | 0000h       | Page 252               |
| 06h-07h  | 16           | RO   | PCI Status Register   | 0280h       | Page 252               |
| 08h      | 8            | RO   | Device Revision ID Register   | 00h         | Page 252               |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register   | 068000h     | Page 252               |
| 0Ch      | 8            | RO   | PCI Cache Line Size Register  | 00h         | Page 252               |
| 0Dh      | 8            | RO   | PCI Latency Timer Register  | 00h         | Page 252               |
| 0Eh      | 8            | RO   | PCI Header Type Register  | 00h         | Page 252               |
| 0Fh      | 8            | RO   | PCI BIST Register   | 00h         | Page 252               |
| 10h-13h  | 32           | R/W  | Base Address Register 0 (F1BAR0) — Sets the base address for the I/O mapped SMI Status Registers (summarized in Table 6-18).  | 00000001h   | Page 252               |
| 14h-2Bh  | ---          | ---  | Reserved  | 00h         | Page 252               |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID   | 100Bh       | Page 252               |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID  | 0501h       | Page 252               |
| 30h-3Fh  | ---          | ---  | Reserved  | 00h         | Page 252               |
| 40h-43h  | 32           | R/W  | Base Address Register 1 (F1BAR1) — Sets the base address for the I/O mapped ACPI Support Registers (summarized in Table 6-19) | 00000001h   | Page 252               |
| 44h-FFh  | ---          | ---  | Reserved  | 00h         | Page 252               |

**Table 6-18. F1BAR0: SMI Status Registers Summary**

| F1BAR0+ I/O Offset | Width (Bits) | Type           | Name   | Reset Value | Reference (Table 6-33) |
|--------------------|--------------|----------------|--|-------------|------------------------|
| 00h-01h            | 16           | RO             | Top Level PME/SMI Status Mirror Register   | 0000h       | Page 253               |
| 02h-03h            | 16           | RO/RC          | Top Level PME/SMI Status Register  | 0000h       | Page 254               |
| 04h-05h            | 16           | RO             | Second Level General Traps & Timers PME/SMI Status Mirror Register   | 0000h       | Page 256               |
| 06h-07h            | 16           | RC             | Second Level General Traps & Timers PME/SMI Status Register  | 0000h       | Page 257               |
| 08h-09h            | 16           | Read to Enable | SMI Speedup Disable Register   | 0000h       | Page 258               |
| 0Ah-1Bh            | ---          | ---            | Reserved   | 00h         | Page 258               |
| 1Ch-1Fh            | 32           | RO             | ACPI Timer Register  | xxxxxxxxh   | Page 258               |
| 20h-21h            | 16           | RO             | Second Level ACPI PME/SMI Status Mirror Register   | 0000h       | Page 258               |
| 22h-23h            | 16           | RC             | Second Level ACPI PME/SMI Status Register  | 0000h       | Page 259               |
| 24h-27h            | 32           | R/W            | External SMI Register  | 00000000h   | Page 259               |
| 28h-4Fh            | ---          | ---            | Not Used   | 00h         | Page 262               |
| 50h-FFh            | ---          | ---            | The I/O mapped registers located here (F1BAR0+I/O Offset 50h-FFh) are also accessible at F0 Index 50h-FFh. The preferred method is to program these registers through the F0 register space. |             |                        |

Table 6-19. F1BAR1: ACPI Support Registers Summary

| F1BAR1+ I/O Offset | Width (Bits) | Type | Name   | Reset Value | Reference (Table 6-34) |
|--------------------|--------------|------|--|-------------|------------------------|
| 00h-03h            | 32           | R/W  | P_CNT — Processor Control Register                 | 00000000h   | Page 263               |
| 04h                | 8            | RO   | Reserved, do not read                              | 00h         | Page 263               |
| 05h                | 8            | RO   | P_LVL3 — Enter C3 Power State Register             | xxh         | Page 263               |
| 06h                | 8            | R/W  | SMI_CMD — OS/BIOS Requests Register                | 00h         | Page 263               |
| 07h                | 8            | R/W  | ACPI_FUN_CNT — ACPI Function Control Register      | 00h         | Page 263               |
| 08h-09h            | 16           | R/W  | PM1A_STS — PM1A Status Register                    | 0000h       | Page 264               |
| 0Ah-0Bh            | 16           | R/W  | PM1A_EN — PM1A Enable Register                     | 0000h       | Page 265               |
| 0Ch-0Dh            | 16           | R/W  | PM1A_CNT — PM1A Control Register                   | 0000h       | Page 265               |
| 0Eh                | 8            | R/W  | ACPI_BIOS_STS Register                             | 00h         | Page 266               |
| 0Fh                | 8            | R/W  | ACPI_BIOS_EN Register                              | 00h         | Page 267               |
| 10h-11h            | 16           | R/W  | GPE0_STS — General Purpose Event 0 Status Register | xxxxh       | Page 267               |
| 12h-13h            | 16           | R/W  | GPE0_EN — General Purpose Event 0 Enable Register  | 0000h       | Page 269               |
| 14h                | 8            | R/W  | GPWIO Control Register 1                           | 00h         | Page 270               |
| 15h                | 8            | R/W  | GPWIO Control Register 2                           | 00h         | Page 270               |
| 16h                | 8            | R/W  | GPWIO Data Register                                | 00h         | Page 271               |
| 17h                | ---          | ---  | Reserved   | 00h         | Page 271               |
| 18h-1Bh            | 32           | R/W  | ACPI_SCI_ROUTING Register                          | 0000F00h    | Page 271               |
| 1Ch-1Fh            | 32           | RO   | PM_TMR — PM Timer Register                         | xxxxxxxxh   | Page 272               |
| 20h                | 8            | R/W  | PM2_CNT — PM2 Control Register                     | 00h         | Page 272               |
| 21h-FFh            | ---          | ---  | Not Used   | 00h         | Page 272               |

Table 6-20. F2: PCI Header Registers for IDE Controller Support Summary

| F2 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 6-35) |
|----------|--------------|------|---|-------------|------------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register  | 100Bh       | Page 273               |
| 02h-03h  | 16           | RO   | Device Identification Register  | 0502h       | Page 273               |
| 04h-05h  | 16           | R/W  | PCI Command Register  | 0000h       | Page 273               |
| 06h-07h  | 16           | RO   | PCI Status Register   | 0280h       | Page 273               |
| 08h      | 8            | RO   | Device Revision ID Register   | 01h         | Page 273               |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register   | 010180h     | Page 273               |
| 0Ch      | 8            | RO   | PCI Cache Line Size Register  | 00h         | Page 273               |
| 0Dh      | 8            | RO   | PCI Latency Timer Register  | 00h         | Page 273               |
| 0Eh      | 8            | RO   | PCI Header Type Register  | 00h         | Page 273               |
| 0Fh      | 8            | RO   | PCI BIST Register   | 00h         | Page 273               |
| 10h-13h  | 32           | RO   | Base Address Register 0 (F2BAR0) — Reserved for possible future use by the Core Logic module.                                   | 00000000h   | Page 273               |
| 14h-17h  | 32           | RO   | Base Address Register 1 (F2BAR1) — Reserved for possible future use by the Core Logic module.                                   | 00000000h   | Page 273               |
| 18h-1Bh  | 32           | RO   | Base Address Register 2 (F2BAR2) — Reserved for possible future use by the Core Logic module.                                   | 00000000h   | Page 273               |
| 1Ch-1Fh  | 32           | RO   | Base Address Register 3 (F2BAR3) — Reserved for possible future use by the Core Logic module.                                   | 00000000h   | Page 273               |
| 20h-23h  | 32           | R/W  | Base Address Register 4 (F2BAR4) — Sets the base address for the I/O mapped Bus Master IDE Registers (summarized in Table 6-21) | 00000001h   | Page 273               |
| 24h-2Bh  | ---          | ---  | Reserved  | 00h         | Page 273               |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID   | 100Bh       | Page 273               |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID  | 0502h       | Page 273               |
| 30h-3Fh  | ---          | ---  | Reserved  | 00h         | Page 274               |
| 40h-43h  | 32           | R/W  | Channel 0 Drive 0 PIO Register  | 00009172h   | Page 274               |
| 44h-47h  | 32           | R/W  | Channel 0 Drive 0 DMA Control Register  | 00077771h   | Page 275               |
| 48h-4Bh  | 32           | R/W  | Channel 0 Drive 1 PIO Register  | 00009172h   | Page 275               |
| 4Ch-4Fh  | 32           | R/W  | Channel 0 Drive 1 DMA Control Register  | 00077771h   | Page 275               |
| 50h-53h  | 32           | R/W  | Channel 1 Drive 0 PIO Register  | 00009172h   | Page 276               |
| 54h-57h  | 32           | R/W  | Channel 1 Drive 0 DMA Control Register  | 00077771h   | Page 276               |
| 58h-5Bh  | 32           | R/W  | Channel 1 Drive 1 PIO Register  | 00009172h   | Page 276               |
| 5Ch-5Fh  | 32           | R/W  | Channel 1 Drive 1 DMA Control Register  | 00077771h   | Page 276               |
| 60h-FFh  | ---          | ---  | Reserved  | 00h         | Page 276               |

**Table 6-21. F2BAR4: IDE Controller Support Registers Summary**

| F2BAR4+ I/O Offset | Width (Bits) | Type | Name   | Reset Value | Reference (Table 6-36) |
|--------------------|--------------|------|--|-------------|------------------------|
| 00h                | 8            | R/W  | IDE Bus Master 0 Command Register — Primary    | 00h         | Page 277               |
| 01h                | ---          | ---  | Not Used                                       | ---         | Page 277               |
| 02h                | 8            | R/W  | IDE Bus Master 0 Status Register — Primary     | 00h         | Page 277               |
| 03h                | ---          | ---  | Not Used                                       | ---         | Page 277               |
| 04h-07h            | 32           | R/W  | IDE Bus Master 0 PRD Table Address — Primary   | 00000000h   | Page 277               |
| 08h                | 8            | R/W  | IDE Bus Master 1 Command Register — Secondary  | 00h         | Page 278               |
| 09h                | ---          | ---  | Not Used                                       | ---         | Page 278               |
| 0Ah                | 8            | R/W  | IDE Bus Master 1 Status Register — Secondary   | 00h         | Page 278               |
| 0Bh                | ---          | ---  | Not Used                                       | ---         | Page 278               |
| 0Ch-0Fh            | 32           | R/W  | IDE Bus Master 1 PRD Table Address — Secondary | 00000000h   | Page 278               |

**Table 6-22. F3: PCI Header Registers for Audio Support Summary**

| F3 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 6-37) |
|----------|--------------|------|---|-------------|------------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register  | 100Bh       | Page 279               |
| 02h-03h  | 16           | RO   | Device Identification Register  | 0503h       | Page 279               |
| 04h-05h  | 16           | R/W  | PCI Command Register  | 0000h       | Page 279               |
| 06h-07h  | 16           | RO   | PCI Status Register   | 0280h       | Page 279               |
| 08h      | 8            | RO   | Device Revision ID Register   | 00h         | Page 279               |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register   | 040100h     | Page 279               |
| 0Ch      | 8            | RO   | PCI Cache Line Size Register  | 00h         | Page 279               |
| 0Dh      | 8            | RO   | PCI Latency Timer Register  | 00h         | Page 279               |
| 0Eh      | 8            | RO   | PCI Header Type Register  | 00h         | Page 279               |
| 0Fh      | 8            | RO   | PCI BIST Register   | 00h         | Page 279               |
| 10h-13h  | 32           | R/W  | Base Address Register 0 (F3BAR0) — Sets the base address for the memory mapped VSA audio interface control register block (summarized in Table 6-23). | 00000000h   | Page 279               |
| 14h-2Bh  | ---          | ---  | Reserved  | 00h         | Page 279               |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID   | 100Bh       | Page 279               |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID  | 0503h       | Page 279               |
| 30h-FFh  | ---          | ---  | Reserved  | 00h         | Page 279               |

Table 6-23. F3BAR0: Audio Support Registers Summary

| F3BAR0+<br>Memory<br>Offset | Width<br>(Bits) | Type | Name  | Reset<br>Value | Reference<br>(Table 6-38) |
|-----------------------------|-----------------|------|---|----------------|---------------------------|
| 00h-03h                     | 32              | R/W  | Codec GPIO Status Register                    | 00000000h      | Page 280                  |
| 04h-07h                     | 32              | R/W  | Codec GPIO Control Register                   | 00000000h      | Page 280                  |
| 08h-0Bh                     | 32              | R/W  | Codec Status Register                         | 00000000h      | Page 280                  |
| 0Ch-0Fh                     | 32              | R/W  | Codec Command Register                        | 00000000h      | Page 281                  |
| 10h-11h                     | 16              | RC   | Second Level Audio SMI Status Register        | 0000h          | Page 281                  |
| 12h-13h                     | 16              | RO   | Second Level Audio SMI Status Mirror Register | 0000h          | Page 282                  |
| 14h-17h                     | 32              | RO   | I/O Trap SMI and Fast Write Status Register   | 00000000h      | Page 283                  |
| 18h-19h                     | 16              | R/W  | I/O Trap SMI Enable Register                  | 0000h          | Page 284                  |
| 1Ah-1Bh                     | 16              | R/W  | Internal IRQ Enable Register                  | 0000h          | Page 285                  |
| 1Ch-1Fh                     | 32              | R/W  | Internal IRQ Control Register                 | 00000000h      | Page 286                  |
| 20h                         | 8               | R/W  | Audio Bus Master 0 Command Register           | 00h            | Page 288                  |
| 21h                         | 8               | RC   | Audio Bus Master 0 SMI Status Register        | 00h            | Page 288                  |
| 22h-23h                     | ----            | ---  | Not Used                                      | ---            | Page 288                  |
| 24h-27h                     | 32              | R/W  | Audio Bus Master 0 PRD Table Address          | 00000000h      | Page 288                  |
| 28h                         | 8               | R/W  | Audio Bus Master 1 Command Register           | 00h            | Page 289                  |
| 29h                         | 8               | RC   | Audio Bus Master 1 SMI Status Register        | 00h            | Page 289                  |
| 2Ah-2Bh                     | ---             | ---  | Not Used                                      | ---            | Page 289                  |
| 2Ch-2Fh                     | 32              | R/W  | Audio Bus Master 1 PRD Table Address          | 00000000h      | Page 289                  |
| 30h                         | 8               | R/W  | Audio Bus Master 2 Command Register           | 00h            | Page 290                  |
| 31h                         | 8               | RC   | Audio Bus Master 2 SMI Status Register        | 00h            | Page 290                  |
| 32h-33h                     | ---             | ---  | Not Used                                      | 00h            | Page 290                  |
| 34h-37h                     | 32              | R/W  | Audio Bus Master 2 PRD Table Address          | 00000000h      | Page 290                  |
| 38h                         | 8               | R/W  | Audio Bus Master 3 Command Register           | 00h            | Page 291                  |
| 39h                         | 8               | RC   | Audio Bus Master 3 SMI Status Register        | 00h            | Page 291                  |
| 3Ah-3Bh                     | ---             | ---  | Not Used                                      | ---            | Page 291                  |
| 3Ch-3Fh                     | 32              | R/W  | Audio Bus Master 3 PRD Table Address          | 00000000h      | Page 291                  |
| 40h                         | 8               | R/W  | Audio Bus Master 4 Command Register           | 00h            | Page 292                  |
| 41h                         | 8               | RC   | Audio Bus Master 4 SMI Status Register        | 00h            | Page 292                  |
| 42h-43h                     | ---             | ---  | Not Used                                      | ---            | Page 292                  |
| 44h-47h                     | 32              | R/W  | Audio Bus Master 4 PRD Table Address          | 00000000h      | Page 292                  |
| 48h                         | 8               | R/W  | Audio Bus Master 5 Command Register           | 00h            | Page 293                  |
| 49h                         | 8               | RC   | Audio Bus Master 5 SMI Status Register        | 00h            | Page 293                  |
| 4Ah-4Bh                     | ---             | ---  | Not Used                                      | ---            | Page 293                  |
| 4Ch-4Fh                     | 32              | R/W  | Audio Bus Master 5 PRD Table Address          | 00000000h      | Page 293                  |



**Table 6-24. F5: PCI Header Registers for X-Bus Expansion Support Summary**

| F5 Index | Width (Bits) | Type | Name   | Reset Value | Reference (Table 6-39) |
|----------|--------------|------|--|-------------|------------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register   | 100Bh       | Page 294               |
| 02h-03h  | 16           | RO   | Device Identification Register   | 0505h       | Page 294               |
| 04h-05h  | 16           | R/W  | PCI Command Register   | 0000h       | Page 294               |
| 06h-07h  | 16           | RO   | PCI Status Register  | 0280h       | Page 294               |
| 08h      | 8            | RO   | Device Revision ID Register  | 00h         | Page 294               |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register  | 068000h     | Page 294               |
| 0Ch      | 8            | RO   | PCI Cache Line Size Register   | 00h         | Page 294               |
| 0Dh      | 8            | RO   | PCI Latency Timer Register   | 00h         | Page 294               |
| 0Eh      | 8            | RO   | PCI Header Type Register   | 00h         | Page 294               |
| 0Fh      | 8            | RO   | PCI BIST Register  | 00h         | Page 294               |
| 10h-13h  | 32           | R/W  | Base Address Register 0 (F5BAR0) — Sets the base address for the X-Bus Expansion support registers (summarized in Table 6-25.) | 00000000h   | Page 294               |
| 14h-17h  | 32           | R/W  | Base Address Register 1 (F5BAR1) — Reserved for possible future use by the Core Logic module.                                  | 00000000h   | Page 294               |
| 18h-1Bh  | 32           | R/W  | Base Address Register 2 (F5BAR2) — Reserved for possible future use by the Core Logic module.                                  | 00000000h   | Page 294               |
| 1Ch-1Fh  | 32           | R/W  | Base Address Register 3 (F5BAR3) — Reserved for possible future use by the Core Logic module.                                  | 00000000h   | Page 295               |
| 20h-23h  | 32           | R/W  | Base Address Register 4 (F5BAR4) — Reserved for possible future use by the Core Logic module.                                  | 00000000h   | Page 295               |
| 24h-27h  | 32           | R/W  | Base Address Register 5 (F5BAR5) — Reserved for possible future use by the Core Logic module.                                  | 00000000h   | Page 295               |
| 28h-2Bh  | ---          | ---  | Reserved   | 00h         | Page 295               |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID  | 100Bh       | Page 295               |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID   | 0505h       | Page 295               |
| 30h-3Fh  | ---          | ---  | Reserved   | 00h         | Page 295               |
| 40h-43h  | 32           | R/W  | F5BAR0 Base Address Register Mask  | FFFFFFC1h   | Page 295               |
| 44h-47h  | 32           | R/W  | F5BAR1 Base Address Register Mask  | 00000000h   | Page 296               |
| 48h-4Bh  | 32           | R/W  | F5BAR2 Base Address Register Mask  | 00000000h   | Page 296               |
| 4Ch-4Fh  | 32           | R/W  | F5BAR3 Base Address Register Mask  | 00000000h   | Page 296               |
| 50h-53h  | 32           | R/W  | F5BAR4 Base Address Register Mask  | 00000000h   | Page 296               |
| 54h-57h  | 32           | R/W  | F5BAR5 Base Address Register Mask  | 00000000h   | Page 296               |
| 58h      | 8            | R/W  | F5BARx Initialized Register  | 00h         | Page 296               |
| 59h-FFh  | ---          | ---  | Reserved   | xxh         | Page 296               |
| 60h-63h  | 32           | R/W  | Scratchpad for Chip Number   | 00000000h   | Page 296               |
| 64h-67h  | 32           | R/W  | Scratchpad for Configuration Block Address   | 00000000h   | Page 297               |
| 68h-FFh  | ---          | ---  | Reserved   | 00h         | Page 297               |

**Table 6-25. F5BAR0: I/O Control Support Registers Summary**

| F5BAR0+ I/O Offset | Width (Bits) | Type | Name                   | Reset Value | Reference (Table 6-40) |
|--------------------|--------------|------|------------------------|-------------|------------------------|
| 00h-03h            | 32           | R/W  | I/O Control Register 1 | 010C0007h   | Page 298               |
| 04h-07h            | 32           | R/W  | I/O Control Register 2 | 00000002h   | Page 299               |
| 08h-0Bh            | 32           | R/W  | I/O Control Register 3 | 00009000h   | Page 299               |

Table 6-26. PCIUSB: USB PCI Configuration Register Summary

| PCIUSB Index | Width (Bits) | Type | Name                           | Reset Value | Reference (Table 6-41) |
|--------------|--------------|------|--------------------------------|-------------|------------------------|
| 00h-01h      | 16           | RO   | Vendor Identification          | 0E11h       | Page 300               |
| 02h-03h      | 16           | RO   | Device Identification          | A0F8h       | Page 300               |
| 04h-05h      | 16           | R/W  | Command Register               | 00h         | Page 300               |
| 06h-07h      | 16           | R/W  | Status Register                | 0280h       | Page 301               |
| 08h          | 8            | RO   | Device Revision ID             | 08h         | Page 301               |
| 09h-0Bh      | 24           | RO   | Class Code                     | 0C0310h     | Page 301               |
| 0Ch          | 8            | R/W  | Cache Line Size                | 00h         | Page 301               |
| 0Dh          | 8            | R/W  | Latency Timer                  | 00h         | Page 301               |
| 0Eh          | 8            | RO   | Header Type                    | 00h         | Page 301               |
| 0Fh          | 8            | RO   | BIST Register                  | 00h         | Page 301               |
| 10h-13h      | 32           | R/W  | Base Address 0                 | 00000000h   | Page 301               |
| 14h-2Bh      | ---          | ---  | Reserved                       | 00h         | Page 302               |
| 2Ch-2Dh      | 16           | RO   | Subsystem Vendor ID            | 0E11h       | Page 302               |
| 2Eh-2Fh      | 16           | RO   | Subsystem ID                   | A0F8h       | Page 302               |
| 30h-3Bh      | ---          | ---  | Reserved                       | 00h         | Page 302               |
| 3Ch          | 8            | R/W  | Interrupt Line Register        | 00h         | Page 302               |
| 3Dh          | 8            | R/W  | Interrupt Pin Register         | 01h         | Page 302               |
| 3Eh          | 8            | RO   | Min. Grant Register            | 00h         | Page 302               |
| 3Fh          | 8            | RO   | Max. Latency Register          | 50h         | Page 302               |
| 40h-43h      | 32           | R/W  | ASIC Test Mode Enable Register | 000F0000h   | Page 302               |
| 44h          | 8            | R/W  | ASIC Operational Mode Enable   | 00h         | Page 302               |
| 45h-FFh      | ---          | ---  | Reserved                       | 00h         | Page 302               |

Table 6-27. USB\_BAR: USB Controller Registers Summary

| USB_BAR0<br>+Memory<br>Offset | Width<br>(Bits) | Type | Name               | Reset Value | Reference<br>(Table 6-42) |
|-------------------------------|-----------------|------|--------------------|-------------|---------------------------|
| 00h-03h                       | 32              | R/W  | HcRevision         | 00000110h   | Page 303                  |
| 04h-07h                       | 32              | R/W  | HcControl          | 00000000h   | Page 303                  |
| 08h-0Bh                       | 32              | R/W  | HcCommandStatus    | 00000000h   | Page 303                  |
| 0Ch-0Fh                       | 32              | R/W  | HcInterruptStatus  | 00000000h   | Page 303                  |
| 10h-13h                       | 32              | R/W  | HcInterruptEnable  | 00000000h   | Page 304                  |
| 14h-17h                       | 32              | R/W  | HcInterruptDisable | 00000000h   | Page 304                  |
| 18h-1Bh                       | 32              | R/W  | HcHCCA             | 00000000h   | Page 305                  |
| 1Ch-1Fh                       | 32              | R/W  | HcPeriodCurrentED  | 00000000h   | Page 305                  |
| 20h-23h                       | 32              | R/W  | HcControlHeadED    | 00000000h   | Page 305                  |
| 24h-27h                       | 32              | R/W  | HcControlCurrentED | 00000000h   | Page 305                  |
| 28h-2Bh                       | 32              | R/W  | HcBulkHeadED       | 00000000h   | Page 305                  |
| 2Ch-2Fh                       | 32              | R/W  | HcBulkCurrentED    | 00000000h   | Page 305                  |
| 30h-33h                       | 32              | R/W  | HcDoneHead         | 00000000h   | Page 305                  |
| 34h-37h                       | 32              | R/W  | HcFmInterval       | 00002EDFh   | Page 306                  |
| 38h-3Bh                       | 32              | RO   | HcFrameRemaining   | 00000000h   | Page 306                  |
| 3Ch-3Fh                       | 32              | RO   | HcFmNumber         | 00000000h   | Page 306                  |
| 40h-43h                       | 32              | R/W  | HcPeriodicStart    | 00000000h   | Page 306                  |
| 44h-47h                       | 32              | R/W  | HcLSThreshold      | 00000628h   | Page 306                  |
| 48h-4Bh                       | 32              | R/W  | HcRhDescriptorA    | 01000003h   | Page 306                  |
| 4Ch-4Fh                       | 32              | R/W  | HcRhDescriptorB    | 00000000h   | Page 307                  |
| 50h-53h                       | 32              | R/W  | HcRhStatus         | 00000000h   | Page 307                  |
| 54h-57h                       | 32              | R/W  | HcRhPortStatus[1]  | 00000000h   | Page 308                  |
| 58h-5Bh                       | 32              | R/W  | HcRhPortStatus[2]  | 00000000h   | Page 309                  |
| 5Ch-5Fh                       | 32              | R/W  | HcRhPortStatus[3]  | 00000000h   | Page 310                  |
| 60h-9Fh                       | ---             | ---  | Reserved           | xxxxxxxh    | Page 311                  |
| 100h-103h                     | 32              | R/W  | HceControl         | 00000000h   | Page 311                  |
| 104h-107h                     | 32              | R/W  | HceInput           | 000000xxh   | Page 312                  |
| 108h-10Dh                     | 32              | R/W  | HceOutput          | 000000xxh   | Page 312                  |
| 10Ch-10Fh                     | 32              | R/W  | HceStatus          | 00000000h   | Page 312                  |

Table 6-28. ISA Legacy I/O Register Summary

| I/O Port  | Type  | Name   | Reference |
|---|-------|--|-----------|
| <b>DMA Channel Control Registers (Table 6-43)</b> |       |  |           |
| 000h  | R/W   | DMA Channel 0 Address Register                   | Page 313  |
| 001h  | R/W   | DMA Channel 0 Transfer Count Register            | Page 313  |
| 002h  | R/W   | DMA Channel 1 Address Register                   | Page 313  |
| 003h  | R/W   | DMA Channel 1 Transfer Count Register            | Page 313  |
| 004h  | R/W   | DMA Channel 2 Address Register                   | Page 313  |
| 005h  | R/W   | DMA Channel 2 Transfer Count Register            | Page 313  |
| 006h  | R/W   | DMA Channel 3 Address Register                   | Page 313  |
| 007h  | R/W   | DMA Channel 3 Transfer Count Register            | Page 313  |
| 008h  | Read  | DMA Status Register, Channels 3:0                | Page 313  |
|   | Write | DMA Command Register, Channels 3:0               | Page 314  |
| 009h  | WO    | Software DMA Request Register, Channels 3:0      | Page 314  |
| 00Ah  | W     | DMA Channel Mask Register, Channels 3:0          | Page 314  |
| 00Bh  | WO    | DMA Channel Mode Register, Channels 3:0          | Page 315  |
| 00Ch  | WO    | DMA Clear Byte Pointer Command, Channels 3:0     | Page 315  |
| 00Dh  | WO    | DMA Master Clear Command, Channels 3:0           | Page 315  |
| 00Eh  | WO    | DMA Clear Mask Register Command, Channels 3:0    | Page 315  |
| 00Fh  | WO    | DMA Write Mask Register Command, Channels 3:0    | Page 315  |
| 0C0h  | R/W   | DMA Channel 4 Address Register (Not used)        | Page 315  |
| 0C2h  | R/W   | DMA Channel 4 Transfer Count Register (Not Used) | Page 315  |
| 0C4h  | R/W   | DMA Channel 5 Address Register                   | Page 315  |
| 0C6h  | R/W   | DMA Channel 5 Transfer Count Register            | Page 315  |
| 0C8h  | R/W   | DMA Channel 6 Address Register                   | Page 315  |
| 0CAh  | R/W   | DMA Channel 6 Transfer Count Register            | Page 315  |
| 0CCh  | R/W   | DMA Channel 7 Address Register                   | Page 315  |
| 0CEh  | R/W   | DMA Channel 7 Transfer Count Register            | Page 315  |
| 0D0h  | Read  | DMA Status Register, Channels 7:4                | Page 316  |
|   | Write | DMA Command Register, Channels 7:4               | Page 316  |
| 0D2h  | WO    | Software DMA Request Register, Channels 7:4      | Page 317  |
| 0D4h  | W     | DMA Channel Mask Register, Channels 7:4          | Page 317  |
| 0D6h  | WO    | DMA Channel Mode Register, Channels 7:4          | Page 317  |
| 0D8h  | WO    | DMA Clear Byte Pointer Command, Channels 7:4     | Page 317  |
| 0DAh  | WO    | DMA Master Clear Command, Channels 7:4           | Page 317  |
| 0DCh  | WO    | DMA Clear Mask Register Command, Channels 7:4    | Page 317  |
| 0DEh  | WO    | DMA Write Mask Register Command, Channels 7:4    | Page 318  |
| <b>DMA Page Registers (Table 6-44)</b>            |       |  |           |
| 081h  | R/W   | DMA Channel 2 Low Page Register                  | Page 318  |
| 082h  | R/W   | DMA Channel 3 Low Page Register                  | Page 318  |
| 083h  | R/W   | DMA Channel 1 Low Page Register                  | Page 318  |
| 087h  | R/W   | DMA Channel 0 Low Page Register                  | Page 318  |
| 089h  | R/W   | DMA Channel 6 Low Page Register                  | Page 318  |
| 08Ah  | R/W   | DMA Channel 7 Low Page Register                  | Page 318  |
| 08Bh  | R/W   | DMA Channel 5 Low Page Register                  | Page 318  |
| 08Fh  | R/W   | Sub-ISA Refresh Low Page Register                | Page 318  |
| 481h  | R/W   | DMA Channel 2 High Page Register                 | Page 318  |
| 482h  | R/W   | DMA Channel 3 High Page Register                 | Page 318  |
| 483h  | R/W   | DMA Channel 1 High Page Register                 | Page 318  |

Table 6-28. ISA Legacy I/O Register Summary (Continued)

| I/O Port  | Type | Name   | Reference |
|---|------|--|-----------|
| 487h  | R/W  | DMA Channel 0 High Page Register   | Page 318  |
| 489h  | R/W  | DMA Channel 6 High Page Register   | Page 318  |
| 48Ah  | R/W  | DMA Channel 7 High Page Register   | Page 318  |
| 48Bh  | R/W  | DMA Channel 5 High Page Register   | Page 318  |
| <b>Programmable Interval Timer Registers (Table 6-45)</b>       |      |  |           |
| 040h  | W    | PIT Timer 0 Counter  | Page 319  |
|   | R    | PIT Timer 0 Status   | Page 319  |
| 041h  | W    | PIT Timer 1 Counter (Refresh)  | Page 319  |
|   | R    | PIT Timer 1 Status (Refresh)   | Page 319  |
| 042h  | W    | PIT Timer 2 Counter (Speaker)  | Page 320  |
|   | R    | PIT Timer 2 Status (Speaker)   | Page 320  |
| 043h  | R/W  | PIT Mode Control Word Register   | Page 320  |
|   |      | Read Status Command  |           |
|   |      | Counter Latch Command  |           |
| <b>Programmable Interrupt Controller Registers (Table 6-46)</b> |      |  |           |
| 020h / 0A0h   | WO   | Master / Slave PCI ICW1  | Page 321  |
| 021h / 0A1h   | WO   | Master / Slave PIC ICW2  | Page 321  |
| 021h / 0A1h   | WO   | Master / Slave PIC ICW3  | Page 321  |
| 021h / 0A1h   | WO   | Master / Slave PIC ICW4  | Page 321  |
| 021h / 0A1h   | R/W  | Master / Slave PIC OCW1  | Page 321  |
| 020h / 0A0h   | WO   | Master / Slave PIC OCW2  | Page 322  |
| 020h / 0A0h   | WO   | Master / Slave PIC OCW3  | Page 322  |
| 020h / 0A0h   | RO   | Master / Slave PIC Interrupt Request and Service Registers for OCW3 Commands | Page 322  |
| <b>Keyboard Controller Registers (Table 6-47)</b>               |      |  |           |
| 060h  | R/W  | External Keyboard Controller Data Register                                   | Page 324  |
| 061h  | R/W  | Port B Control Register  | Page 324  |
| 062h  | R/W  | External Keyboard Controller Mailbox Register                                | Page 324  |
| 064h  | R/W  | External Keyboard Controller Command Register                                | Page 324  |
| 066h  | R/W  | External Keyboard Controller Mailbox Register                                | Page 324  |
| 092h  | R/W  | Port A Control Register  | Page 324  |
| <b>Real-Time Clock Registers (Table 6-48)</b>                   |      |  |           |
| 070h  | WO   | RTC Address Register   | Page 325  |
| 071h  | R/W  | RTC Data Register  | Page 325  |
| 072h  | WO   | RTC Extended Address Register  | Page 325  |
| 073h  | R/W  | RTC Extended Data Register   | Page 325  |
| <b>Miscellaneous Registers (Table 6-49)</b>                     |      |  |           |
| 0F0h, 0F1h  | WO   | Coprocessor Error Register   | Page 325  |
| 170h-177h/<br>376h-377h   | R/W  | Secondary IDE Registers  | Page 325  |
| 1F0-1F7h/<br>3F6h-3F7h  | R/W  | Primary IDE Registers  | Page 325  |
| 4D0h  | R/W  | Interrupt Edge/Level Select Register 1                                       | Page 325  |
| 4D1h  | R/W  | Interrupt Edge/Level Select Register 2                                       | Page 326  |

## 6.4 Chipset Register Space

The Chipset Register Space of the Core Logic module is comprised of six separate functions (F0-F5), each with its own register space. Base Address Registers (BARs) in each PCI header register space set the base address for the configuration registers for each respective function. The configuration registers accessed through BARs are I/O or memory mapped. The PCI header registers in all functions are very similar.

- 1) Function 0 (F0): PCI Header/Bridge Configuration Registers for GPIO, and LPC Support (see Section 6.4.1).
- 2) Function 1 (F1): PCI Header Registers for SMI Status and ACPI Support (see Section 6.4.2 on page 252).
- 3) Function 2 (F2): PCI Header/Channel 0 and 1 Configuration Registers for IDE Controller Support (see Section 6.4.3 on page 273).
- 4) Function 3 (F3): PCI Header Registers for audio support (see Section 6.4.4 on page 279).
- 5) Function 4 (F4): PCI Header Registers Video Processor Support (see Section 7.3 on page 345).
- 6) Function 5 (F5): PCI Header Registers for X-Bus Expansion Support (see Section 6.4.5 on page 294).

Function 5 contain six BARs in their standard PCI header locations (i.e., Index 10h, 14h, 18h, 1Ch, 20h, and 24h). In addition there are six mask registers that allow the six BARs to be fully programmable from 4 GB to 16 bytes for memory and from 4 GB to 4 bytes for I/O

### General Remarks:

- Reserved bits that are defined as "must be set to 0 or 1" should be written with that value.
- Reserved bits that are not defined as "must be set to 0 or 1" should be written with a value that is read from them.
- "Read to Clear" registers that are wider than one byte should be read in one read operation. If they are read a byte at a time, status bits may be lost, or not cleared.

### 6.4.1 Bridge, GPIO, and LPC Registers - Function 0

The register space designated as Function 0 (F0) is used to configure Bridge features and functionality unique to the Core Logic module. In addition, it configures the PCI portion of support hardware for the GPIO and LPC support registers. The bit formats for the PCI Header and Bridge Configuration registers are given in Table 6-29.

**Note:** The registers at F0 Index 50h-FFh can also be accessed at F1BAR0+I/O Offset 50h-FFh. However, the preferred method is to program these registers through the F0 register space.

Located in the PCI Header registers of F0, are two Base Address Registers (FOBARx) used for pointing to the register spaces designated for GPIO and LPC configuration (described in Section 6.4.1.1 "GPIO Support Registers" on page 240 and Section 6.4.1.2 "LPC Support Registers" on page 244).

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support**

| Bit                  | Description  |
|----------------------|--|
| <b>Index 00h-01h</b> | <b>Vendor Identification Register (RO)</b> <span style="float: right;"><b>Reset Value: 100Bh</b></span>  |
| <b>Index 02h-03h</b> | <b>Device Identification Register (RO)</b> <span style="float: right;"><b>Reset Value: 0500h</b></span>  |
| <b>Index 04h-05h</b> | <b>PCI Command Register (R/W)</b> <span style="float: right;"><b>Reset Value: 000Fh</b></span>   |
| 15:10                | <b>Reserved.</b> Must be set to 0.   |
| 9                    | <b>Fast Back-to-Back Enable.</b> This function is not supported when the Core Logic module is a master. It must always be disabled (i.e., must be set to 0).   |
| 8                    | <b>SERR#.</b> Allow SERR# assertion on detection of special errors.<br>0: Disable. (Default)<br>1: Enable.   |
| 7                    | <b>Wait Cycle Control (Read Only).</b> This function is not supported in the Core Logic module. It is always disabled (always reads 0, hardwired).   |
| 6                    | <b>Parity Error.</b> Allow the Core Logic module to check for parity errors on PCI cycles for which it is a target and to assert PERR# when a parity error is detected.<br>0: Disable. (Default)<br>1: Enable. |
| 5                    | <b>VGA Palette Snoop Enable. (Read Only)</b> This function is not supported in the Core Logic module. It is always disabled (always reads 0, hardwired).   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit                              | Description   |
|----------------------------------|---|
| 4                                | <b>Memory Write and Invalidate.</b> Allow the Core Logic module to do memory write and invalidate cycles, if the PCI Cache Line register (F0 Index 0Ch) is set to 32 bytes (08h).<br>0: Disable. (Default)<br>1: Enable.  |
| 3                                | <b>Special Cycles.</b> Allow the Core Logic module to respond to special cycles.<br>0: Disable.<br>1: Enable. (Default)<br>This bit must be enabled to allow an SMI to be generated from a CPU Shutdown cycle.  |
| 2                                | <b>Bus Master.</b> Allow the Core Logic module bus mastering capabilities.<br>0: Disable.<br>1: Enable. (Default)<br>This bit must be set to 1.   |
| 1                                | <b>Memory Space.</b> Allow the Core Logic module to respond to memory cycles from the PCI bus.<br>0: Disable.<br>1: Enable. (Default)   |
| 0                                | <b>I/O Space.</b> Allow the Core Logic module to respond to I/O cycles from the PCI bus:<br>0: Disable.<br>1: Enable. (Default)<br>This bit must be set to 1 to access I/O offsets through F0BAR0 and F0BAR1 (see F0 Index 10h and 14h).                                |
| <b>Index 06h-07h</b>             |   |
| <b>PCI Status Register (R/W)</b> |   |
| <b>Reset Value: 0280h</b>        |   |
| 15                               | <b>Detected Parity Error.</b> This bit is set whenever a parity error is detected.<br>Write 1 to clear.   |
| 14                               | <b>Signaled System Error.</b> This bit is set whenever the Core Logic module asserts SERR# active.<br>Write 1 to clear.   |
| 13                               | <b>Received Master Abort.</b> This bit is set whenever a master abort cycle occurs. A master abort occurs when a PCI cycle is not claimed, except for special cycles.<br>Write 1 to clear.  |
| 12                               | <b>Received Target Abort.</b> This bit is set whenever a target abort is received while the Core Logic module is the master for the PCI cycle.<br>Write 1 to clear.   |
| 11                               | <b>Signaled Target Abort.</b> This bit is set whenever the Core Logic module signals a target abort. This occurs when an address parity error occurs for an address that hits in the active address decode space of the Core Logic module.<br>Write 1 to clear.         |
| 10:9                             | <b>DEVSEL# Timing. (Read Only)</b> These bits are always 01, as the Core Logic module always responds to cycles for which it is an active target with medium DEVSEL# timing.<br>00: Fast<br>01: Medium<br>10: Slow<br>11: Reserved.                                     |
| 8                                | <b>Data Parity Detected.</b> This bit is set when:<br>1) The Core Logic module asserts PERR# or observed PERR# asserted.<br>2) The Core Logic module is the master for the cycle in which the PERR# occurred, and PE is set (F0 Index 04h[6] = 1).<br>Write 1 to clear. |
| 7                                | <b>Fast Back-to-Back Capable. (Read Only)</b> Enables the Core Logic module, as a target, to accept fast back-to-back transactions.<br>0: Disable.<br>1: Enable.<br>This bit is always set to 1.  |
| 6:0                              | <b>Reserved. (Read Only)</b> Must be set to 0 for future use.   |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit  | Description  |                        |
|--|--|------------------------|
| Index 08h  | Device Revision ID Register (RO)   | Reset Value: 00h       |
| Index 09h-0Bh  | PCI Class Code Register (RO)   | Reset Value: 060100h   |
| Index 0Ch  | PCI Cache Line Size Register (R/W)   | Reset Value: 00h       |
| 7:0  | <b>PCI Cache Line Size Register.</b> This register sets the size of the PCI cache line, in increments of four bytes. For memory write and invalidate cycles, the PCI cache line size must be set to 32 bytes (08h) and the Memory Write and Invalidate bit (F0 Index 04h[4]) must be set to 1.   |                        |
| Index 0Dh  | PCI Latency Timer Register (R/W)   | Reset Value: 00h       |
| 7:4  | <b>Reserved.</b> Must be set to 0.   |                        |
| 3:0  | <b>PCI Latency Timer Value.</b> The PCI Latency Timer register prevents system lockup when a slave does not respond to a cycle that the Core Logic module masters.<br>If the value is set to 00h (default), the timer is disabled.<br>If the timer is written with any other value, bits [3:0] become the four most significant bits in a timer that counts PCI clocks for slave response.<br>The timer is reset on each valid data transfer. If the counter expires before the next assertion of TRDY# is received, the Core Logic module stops the transaction with a master abort and asserts SERR#, if enabled to do so (via F0 Index 04h[8]). |                        |
| Index 0Eh  | PCI Header Type (RO)   | Reset Value: 80h       |
| 7:0  | <b>PCI Header Type Register.</b> This register defines the format of this header. This header has a format of type 0. (For more information about this format, see the PCI Local Bus specification, revision 2.2.)<br>Additionally, bit 7 of this register defines whether this PCI device is a multifunction device (bit 7 = 1) or not (bit 7 = 0).   |                        |
| Index 0Fh  | PCI BIST Register (RO)   | Reset Value: 00h       |
| This register indicates various information about the PCI Built-In Self-Test (BIST) mechanism.<br><b>Note:</b> This mechanism is not supported in the Core Logic module in the SC3200.   |  |                        |
| 7  | <b>BIST Capable.</b> Indicates if the device can run a Built-In Self-Test (BIST).<br>0: The device has no BIST functionality.<br>1: The device can run a BIST.   |                        |
| 6  | <b>Start BIST.</b> Setting this bit to 1 starts up a BIST on the device. The device resets this bit when the BIST is completed. (Not supported.)   |                        |
| 5:4  | <b>Reserved.</b>   |                        |
| 3:0  | <b>BIST Completion Code.</b> Upon completion of the BIST, the completion code is stored in these bits. A completion code of 0000 indicates that the BIST was successfully completed. Any other value indicates a BIST failure.   |                        |
| Index 10h-13h  | Base Address Register 0 - F0BAR0 (R/W)   | Reset Value: 00000001h |
| This register allows access to I/O mapped GPIO runtime and configuration Registers. Bits [5:0] are read only (000001), indicating a 64-byte aligned I/O address space. Refer to Table 6-30 on page 240 for the GPIO register bit formats and reset values. |  |                        |
| 31:6   | <b>GPIO Base Address.</b>  |                        |
| 5:0  | <b>Address Range. (Read Only)</b>  |                        |
| Index 14h-17h  | Base Address Register 1 - F0BAR1 (R/W)   | Reset Value: 00000001h |
| This register allows access to I/O mapped LPC configuration registers. Bits [5:0] are read only (000001), indicating a 64-byte aligned I/O address space. Refer to Table 6-31 on page 244 for the bit formats and reset values of the LPC registers.       |  |                        |
| 31:6   | <b>LPC Base Address.</b>   |                        |
| 5:0  | <b>Address Range. (Read Only)</b>  |                        |
| Index 18h-2Bh  | Reserved   | Reset Value: 00h       |
| Index 2Ch-2Dh  | Subsystem Vendor ID (RO)   | Reset Value: 100Bh     |
| Index 2Eh-2Fh  | Subsystem ID (RO)  | Reset Value: 0500h     |
| Index 30h-3Fh  | Reserved   | Reset Value: 00h       |



Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description   |
|---|---|
| <b>Index 40h</b> <span style="float:right"><b>PCI Function Control Register 1 (R/W)</b></span> <span style="float:right"><b>Reset Value: 39h</b></span> |   |
| 7:6   | <b>Reserved.</b> Must be set to 0.  |
| 5   | <b>Reserved.</b> Must be set to 0.  |
| 4   | <b>PCI Subtractive Decode.</b><br>0: Disable transfer of subtractive decode address to external PCI bus. External PCI bus is not usable.<br>1: Enable transfer of subtractive decode address to external PCI bus. Recommended setting.  |
| 3   | <b>Reserved.</b> Must be set to 1.  |
| 2   | <b>Reserved.</b> Must be set to 0.  |
| 1   | <b>PERR# Signals SERR#.</b> Assert SERR# when PERR# is asserted or detected as active by the Core Logic module (allows PERR# assertion to be cascaded to NMI (SMI) generation in the system).<br>0: Disable.<br>1: Enable.  |
| 0   | <b>PCI Interrupt Acknowledge Cycle Response.</b> The Core Logic module responds to PCI interrupt acknowledge cycles.<br>0: Disable.<br>1: Enable.   |
| <b>Index 41h</b> <span style="float:right"><b>PCI Function Control Register 2 (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span> |   |
| 7:6   | <b>Reserved.</b> Must be set to 0.  |
| 5   | <b>X-Bus Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 5 (F5) register space, an SMI is generated. Writes are trapped; access to the register is denied. Reads are snooped; access to the register is allowed.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5]. |
| 4   | <b>Video Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 4 (F4) register space, an SMI is generated. Writes are trapped; access to the register is denied. Reads are snooped; access to the register is allowed.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5]. |
| 3   | <b>Audio Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 3 (F3) register space, an SMI is generated. Writes are trapped; access to the register is denied. Reads are snooped; access to the register is allowed.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5]. |
| 2   | <b>IDE Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 2 (F2) register space, an SMI is generated. Writes are trapped; access to the register is denied. Reads are snooped; access to the register is allowed.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5].   |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit  | Description   |
|--|---|
| 1  | <p><b>Power Management Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 1 (F1) register space, an SMI is generated. Writes are trapped; access to the register is denied. Reads are snooped; access to the register is allowed.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5].</p> |
| 0  | <p><b>Legacy Configuration Trap.</b> If this bit is set to 1 and an access occurs to one of the configuration registers in PCI Function 0 (F0), an SMI is generated. Reads and writes are snooped; access to the register is allowed.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[5].</p>   |
| <b>Index 42h</b>                           |   |
| <b>Reserved</b>                            |   |
| <b>Reset Value: 00h</b>                    |   |
| <b>Index 43h</b>                           |   |
| <b>Delayed Transactions Register (R/W)</b> |   |
| <b>Reset Value: 02h</b>                    |   |
| 7:6  | <b>Reserved.</b> Must be set to 0.  |
| 5  | <b>Reserved.</b> Must be set to 1.  |
| 4  | <p><b>Enable PCI Delayed Transactions for Access to I/O Address 170h-177h (Secondary IDE Channel).</b> PIO mode uses repeated I/O transactions that are faster when non-delayed transactions are used.</p> <p>0: I/O addresses complete as fast as possible on PCI. (Default)<br/>1: Accesses to Secondary IDE channel I/O addresses are delayed transactions on PCI.</p> <p>For best performance of VIP, this bit should be set to 1 unless PIO mode 3 or 4 are used.</p>                        |
| 3  | <p><b>Enable PCI Delayed Transactions for Access to I/O Address 1F0h-1F7h (Primary IDE Channel).</b> PIO mode uses repeated I/O transactions that are faster when non-delayed transactions are used.</p> <p>0: I/O addresses complete as fast as possible on PCI. (Default)<br/>1: Accesses to Primary IDE channel I/O addresses are delayed transactions on PCI.</p> <p>For best performance of VIP, this bit should be set to 1 unless PIO mode 3 or 4 are used.</p>                            |
| 2  | <p><b>Enable PCI Delayed Transactions for AT Legacy PIC I/O Addresses.</b> Some PIC status reads are long. Enabling delayed transactions help reduce DMA latency for high bandwidth devices like VIP.</p> <p>0: PIC I/O addresses complete as fast as possible on PCI. (Default)<br/>1: Accesses to PIC I/O addresses are delayed transactions on PCI.</p> <p>For best performance of VIP, this bit should be set to 1.</p>   |
| 1  | <p><b>Enable PCI Delayed Transactions for AT Legacy PIT I/O Addresses.</b> Some x86 programs (certain benchmarks/diagnostics) assume a particular latency for PIT accesses; this bit allows that code to work.</p> <p>0: PIT I/O addresses complete as fast as possible on PCI.<br/>1: Accesses to PIT I/O addresses are delayed transactions on PCI. (Default)</p> <p>For best performance (e.g., when running Microsoft Windows®), this bit should be set to 0.</p>                             |
| 0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Index 44h</b>                           |   |
| <b>Reset Control Register (R/W)</b>        |   |
| <b>Reset Value: 01h</b>                    |   |
| 7  | <p><b>AC97 Soft Reset.</b> Active low reset for the AC97 codec interface.</p> <p>0: AC97_RST# is driven high. (Default)<br/>1: AC97_RST# is driven low.</p>   |
| 6:4  | <b>Reserved.</b> Must be set to 0.  |
| 3  | <p><b>IDE Controller Reset.</b> Reset the IDE controller.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Write 0 to clear. This bit is level-sensitive and must be cleared after the reset is enabled.</p>  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit  | Description  |
|--|--|
| 2  | <p><b>IDE Reset.</b> Reset IDE bus.</p> <p>0: Disable.</p> <p>1: Enable (drive IDE_RST# low).</p> <p>Write 0 to clear. This bit is level-sensitive and must be cleared after the reset is enabled.</p> <p><b>Note:</b> When X-Bus Warm Start is enabled (bit 0 = 1) or during POR#, IDE_RST# is put into TRI-STATE mode. To properly reset the IDE bus, after POR# the boot code must cause IDE_RST# to activate.</p>                                    |
| 1  | <p><b>PCI Reset.</b> Reset PCI bus.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>When this bit is set to 1, the Core Logic module output signal PCIRST# is asserted and all devices on the PCI bus (including PCIUSB) are reset. No other function within the Core Logic module is affected by this bit.</p> <p>Write 0 to clear this bit. This bit is level-sensitive and must be cleared after the reset is enabled.</p>                                |
| 0  | <p><b>X-Bus Warm Start.</b> Writing and reading this bit each have different meanings.</p> <p>When reading this bit, it indicates whether or not a warm start occurred since power-up:</p> <p>0: A warm start occurred.</p> <p>1: No warm start has occurred.</p> <p>When writing this bit, it can be used to trigger a system-wide reset:</p> <p>0: No effect.</p> <p>1: Execute system-wide reset (used only for clock configuration at power-up).</p> |
| <b>Index 45h</b>                           |  |
| <b>Reserved</b>                            |  |
| <b>Reset Value: 00h</b>                    |  |
| <b>Index 46h</b>                           |  |
| <b>PCI Functions Enable Register (R/W)</b> |  |
| <b>Reset Value: FEh</b>                    |  |
| 7:6  | <b>Reserved.</b> Resets to 11.   |
| 5  | <b>F5 (PCI Function 5).</b> When asserted (set to 1), enables the register space designated as F5. This bit must always be set to 1. (Default)   |
| 4  | <b>F4 (PCI Function 4).</b> When asserted (set to 1), enables the register space designated as F4. This bit must always be set to 1. (Default)   |
| 3  | <b>F3 (PCI Function 3).</b> When asserted (set to 1), enables the register space designated as F3. This bit must always be set to 1. (Default)   |
| 2  | <b>F2 (PCI Function 2).</b> When asserted (set to 1), enables the register space designated as F2. This bit must always be set to 1. (Default)   |
| 1  | <b>F1 (PCI Function 1).</b> When asserted (set to 1), enables the register space designated as F1. This bit must always be set to 1. (Default)   |
| 0  | <b>Reserved.</b> Must be set to 0.   |
| <b>Index 47h</b>                           |  |
| <b>Miscellaneous Enable Register (R/W)</b> |  |
| <b>Reset Value: 00h</b>                    |  |
| 7:3  | <b>Reserved.</b> Must be set to 0.   |
| 2  | <b>F0BAR1 (PCI Function 0, Base Address Register 1).</b> F0BAR1, pointer to I/O mapped LPC configuration registers.<br>0: Disable.<br>1: Enable.   |
| 1  | <b>F0BAR0 (PCI Function 0, Base Address Register 0).</b> F0BAR0, pointer to I/O mapped GPIO configuration registers.<br>0: Disable.<br>1: Enable.  |
| 0  | <b>Reserved.</b> Must be set to 0.   |
| <b>Index 48h-4Bh</b>                       |  |
| <b>Reserved</b>                            |  |
| <b>Reset Value: 00h</b>                    |  |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description  |                  |                  |                  |                  |                  |                  |                  |                  |
|---|--|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| <b>Index 4Ch-4Fh</b> <span style="float:right"><b>Top of System Memory (R/W)</b></span> <span style="float:right"><b>Reset Value: FFFFFFFh</b></span>     |  |                  |                  |                  |                  |                  |                  |                  |                  |
| 31:0  | <p><b>Top of System Memory.</b> Highest address in system used to determine active decode for external PCI mastered memory cycles.</p> <p>If an external PCI master requests a memory address below the value programmed in this register, the cycle is transferred from the external PCI bus interface to the Fast-PCI interface for servicing by the GX1 module.</p> <p><b>Note:</b> The four least significant bits must be set to 1100.</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| <b>Index 50h</b> <span style="float:right"><b>PIT Control/ISA CLK Divider (R/W)</b></span> <span style="float:right"><b>Reset Value: 7Bh</b></span>       |  |                  |                  |                  |                  |                  |                  |                  |                  |
| 7   | <p><b>PIT Software Reset.</b></p> <p>0: Disable.<br/>1: Enable.</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| 6   | <p><b>PIT Counter 1.</b></p> <p>0: Forces Counter 1 output (OUT1) to zero.<br/>1: Allows Counter 1 output (OUT1) to pass to the Port 061h[4].</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| 5   | <p><b>PIT Counter 1 Enable.</b></p> <p>0: Sets GATE1 input low.<br/>1: Sets GATE1 input high.</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| 4   | <p><b>PIT Counter 0.</b></p> <p>0: Forces Counter 0 output (OUT0) to zero.<br/>1: Allows Counter 0 output (OUT0) to pass to IRQ0.</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| 3   | <p><b>PIT Counter 0 Enable.</b></p> <p>0: Sets GATE0 input low.<br/>1: Sets GATE0 input high.</p>  |                  |                  |                  |                  |                  |                  |                  |                  |
| 2:0   | <p><b>ISA Clock Divisor.</b> Determines the divisor of the PCI clock used to make the ISA clock, which is typically programmed for approximately 8 MHz:</p> <table style="width:100%; border:none;"> <tr> <td>000: Divide by 1</td> <td>100: Divide by 5</td> </tr> <tr> <td>001: Divide by 2</td> <td>101: Divide by 6</td> </tr> <tr> <td>010: Divide by 3</td> <td>110: Divide by 7</td> </tr> <tr> <td>011: Divide by 4</td> <td>111: Divide by 8</td> </tr> </table> <p>If PCI clock = 25 MHz, use setting of 010 (divide by 3).<br/>If PCI clock = 30 or 33 MHz, use a setting of 011 (divide by 4).</p> | 000: Divide by 1 | 100: Divide by 5 | 001: Divide by 2 | 101: Divide by 6 | 010: Divide by 3 | 110: Divide by 7 | 011: Divide by 4 | 111: Divide by 8 |
| 000: Divide by 1  | 100: Divide by 5   |                  |                  |                  |                  |                  |                  |                  |                  |
| 001: Divide by 2  | 101: Divide by 6   |                  |                  |                  |                  |                  |                  |                  |                  |
| 010: Divide by 3  | 110: Divide by 7   |                  |                  |                  |                  |                  |                  |                  |                  |
| 011: Divide by 4  | 111: Divide by 8   |                  |                  |                  |                  |                  |                  |                  |                  |
| <b>Index 51h</b> <span style="float:right"><b>ISA I/O Recovery Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 40h</b></span> |  |                  |                  |                  |                  |                  |                  |                  |                  |
| 7:4   | <p><b>8-Bit I/O Recovery.</b> These bits determine the number of ISA bus clocks between back-to-back 8-bit I/O read cycles. This count is in addition to a preset one-clock delay built into the controller.</p> <p>0000: 1 PCI clock<br/>0001: 2 PCI clocks<br/>:::<br/>:::<br/>:::<br/>1111: 16 PCI clocks</p>   |                  |                  |                  |                  |                  |                  |                  |                  |
| 3:0   | <p><b>16-Bit I/O Recovery.</b> These bits determine the number of ISA bus clocks between back-to-back 16-bit I/O cycles. This count is in addition to a preset one-clock delay built into the controller.</p> <p>0000: 1 PCI clock<br/>0001: 2 PCI clocks<br/>:::<br/>:::<br/>:::<br/>1111: 16 PCI clocks</p>  |                  |                  |                  |                  |                  |                  |                  |                  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit  | Description   |
|--|---|
| <b>Index 52h</b> <span style="float:right"><b>ROM/AT Logic Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 98h</b></span>  |   |
| 7  | <b>Snoop Fast Keyboard Gate A20 and Fast Reset.</b> Enables the snoop logic associated with keyboard commands for A20 Mask and Reset.<br>0: Disable snooping. The keyboard controller handles the commands.<br>1: Enable snooping.  |
| 6:5  | <b>Reserved.</b> Must be set to 0.  |
| 4  | <b>Enable A20M# De-assertion on Warm Reset.</b> Force A20M# high during a Warm Reset (guarantees that A20M# is de-asserted regardless of the state of A20).<br>0: Disable.<br>1: Enable.  |
| 3  | <b>Enable Port 092h (Port A).</b> Port 092h decode and the logical functions.<br>0: Disable.<br>1: Enable.  |
| 2  | <b>Upper ROM Size.</b> Selects upper ROM addressing size.<br>0: 256K (FFFC0000h-FFFFFFFFh).<br>1: Use ROM Mask register (F0 Index 6Ch).<br>ROMCS# goes active for the above ranges whether strapped for ISA or LPC. (Refer to F0BAR1+I/O Offset 10h[15] for further strapping/programming details.)<br>The selected range can then be either positively or subtractively decoded through F0 Index 5Bh[5].   |
| 1  | <b>ROM Write Enable.</b> When asserted, enables writes to ROM space, allowing Flash programming.<br>If strapped for ISA and this bit is set to 1, writes to the configured ROM space asserts ROMCS#, enabling the write cycle to the Flash device on the ISA bus. Otherwise, ROMCS# is inhibited for writes.<br>If strapped for LPC and this bit is set to 1, the cycle runs on the LPC bus. Otherwise, the LPC bus cycle is inhibited for writes.<br>Refer to F0BAR1+I/O Offset 10h[15] for further strapping/programming details. |
| 0  | <b>Lower ROM Size.</b> Selects lower ROM addressing size in which ROMCS# goes active.<br>0: Lower ROM access are 000F0000h-000FFFFFFh (64 KB). (Default)<br>1: Lower ROM accesses are 000E0000h-000FFFFFFh (128 KB).<br>ROMCS# goes active for the above ranges whether strapped for ISA or LPC. (Refer to F0BAR1+I/O Offset 10h[15] for further strapping/programming details.)<br>The selected range can then be either positively or subtractively decoded through F0 Index 5Bh[5].  |
| <b>Index 53h</b> <span style="float:right"><b>Alternate CPU Support Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span> |   |
| 7:6  | <b>Reserved.</b> Must be set to 0.  |
| 5  | <b>Bidirectional SMI Enable.</b><br>0: Disable.<br>1: Enable.<br>This bit must be set to 0.   |
| 4:3  | <b>Reserved.</b> Must be set to 0.  |
| 2  | <b>Reserved.</b> Must be set to 0.  |
| 1  | <b>IRQ13 Function Selection.</b> Selects function of the internal IRQ13/FERR# signal.<br>0: FERR#.<br>1: IRQ13.<br>This bit must be set to 1.   |
| 0  | <b>Generate SMI on A20M# Toggle.</b><br>0: Disable.<br>1: Enable.<br>This bit must be set to 1.<br>SMI status is reported at F1BAR0+I/O Offset 00h/02h[7].  |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit  | Description   |
|--|---|
| <b>Index 54h-59h</b> <span style="float: right;"><b>Reset Value: 00h</b></span>  |   |
| <b>Reserved</b>  |   |
| <b>Index 5Ah</b> <span style="float: right;"><b>Reset Value: 01h</b></span>  |   |
| <b>Decode Control Register 1 (R/W)</b>   |   |
| Indicates PCI positive or negative decoding for various I/O ports on the ISA bus.  |   |
| <b>Note:</b> Positive decoding by the Core Logic module speeds up I/O cycle time. The I/O ports mentioned in the bit descriptions below, do not exist in the Core Logic module. It is assumed that if positive decode is enabled for a port, the port exists on the ISA bus.         |   |
| 7  | <b>Secondary Floppy Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 372h-375h and 377h.<br>0: Subtractive.<br>1: Positive.  |
| 6  | <b>Primary Floppy Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 3F2h-3F5h and 3F7h.<br>0: Subtractive.<br>1: Positive.  |
| 5  | <b>COM4 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 2E8h-2EFh.<br>0: Subtractive.<br>1: Positive.   |
| 4  | <b>COM3 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 3E8h-3EFh.<br>0: Subtractive.<br>1: Positive.   |
| 3  | <b>COM2 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 2F8h-2FFh.<br>0: Subtractive.<br>1: Positive.   |
| 2  | <b>COM1 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 3F8h-3FFh.<br>0: Subtractive.<br>1: Positive.   |
| 1  | <b>Keyboard Controller Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O Ports 060h and 064h (as well as 062h and 066h, if enabled - F4 Index 5Bh[7] = 1).<br>0: Subtractive.<br>1: Positive.<br><b>Note:</b> If F0BAR1+I/O Offset 10h bits 10 = 0 and 16 = 1, then this bit must be written 0. |
| 0  | <b>Real-Time Clock Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O Ports 070h-073h.<br>0: Subtractive.<br>1: Positive.  |
| <b>Index 5Bh</b> <span style="float: right;"><b>Reset Value: 20h</b></span>  |   |
| <b>Decode Control Register 2 (R/W)</b>   |   |
| <b>Note:</b> Positive decoding by the Core Logic module speeds up the I/O cycle time. The Keyboard, LPT3, LPT2, and LPT1 I/O ports do not exist in the Core Logic module. It is assumed that if positive decoding is enabled for any of these ports, the port exists on the ISA bus. |   |
| 7  | <b>Keyboard I/O Port 062h/066h Positive Decode.</b> This alternate port to the keyboard controller is provided in support of power management features.<br>0: Disable.<br>1: Enable.  |
| 6  | <b>Reserved.</b> Must be set to 0.  |
| 5  | <b>BIOS ROM Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to the configured ROM space.<br>0: Subtractive.<br>1: Positive.<br>ROM configuration is at F0 Index 52h[2:0].  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description   |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
|---|---|----------------|----------------|----------------|-------------|------------|------------|------------|----------------|----------------|------------|-------------|-------------|------------|------------|-------------|-------------|
| 4   | <p><b>Secondary IDE Controller Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 170h-177h and 376h-377h (excluding writes to 377h).</p> <p>0: Subtractive. Subtractively decoded IDE addresses are forwarded to the PCI slot bus. If a master abort occurs, they are then forwarded to ISA.</p> <p>1: Positive. Positively decoded IDE addresses are forwarded to the internal IDE controller and then to the IDE bus.</p>                               |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 3   | <p><b>Primary IDE Controller Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 1F0h-1F7h and 3F6h-3F7h (excluding writes to 3F7h).</p> <p>0: Subtractive. Subtractively decoded IDE addresses are forwarded to the PCI slot bus. If a master abort occurs, they are then forwarded to ISA.</p> <p>1: Positive. Positively decoded IDE addresses are forwarded to the internal IDE controller and then to the IDE bus.</p>                                 |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 2   | <p><b>LPT3 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 278h-27Fh.</p> <p>0: Subtractive.</p> <p>1: Positive.</p>  |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 1   | <p><b>LPT2 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 378h-37Fh.</p> <p>0: Subtractive.</p> <p>1: Positive.</p>  |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0   | <p><b>LPT1 Positive Decode.</b> Selects PCI positive or subtractive decoding for accesses to I/O ports 3BCh-3BFh.</p> <p>0: Subtractive.</p> <p>1: Positive.</p>  |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Index 5Ch PCI Interrupt Steering Register 1 (R/W) Reset Value: 00h</b></p> <p>Indicates target interrupts for signals INTB# and INTA#.</p> <p><b>Note:</b> The target interrupt must first be configured as level sensitive via I/O Ports 4D0h and 4D1h in order to maintain PCI interrupt compatibility.</p>   |   |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 7:4   | <p><b>INTB# (EBGA Ball AF1 / TEPBGA Ball C26) Target Interrupt.</b></p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: Reserved</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: Reserved</td> </tr> <tr> <td>0010: Reserved</td> <td>0110: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0111: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table> | 0000: Disable  | 0100: IRQ4     | 1000: Reserved | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: Reserved | 0010: Reserved | 0110: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0111: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable   | 0100: IRQ4  | 1000: Reserved | 1100: IRQ12    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0001: IRQ1  | 0101: IRQ5  | 1001: IRQ9     | 1101: Reserved |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0010: Reserved  | 0110: IRQ6  | 1010: IRQ10    | 1110: IRQ14    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0011: IRQ3  | 0111: IRQ7  | 1011: IRQ11    | 1111: IRQ15    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 3:0   | <p><b>INTA# (EBGA Ball AE3 / TEPBGA Ball D26) Target Interrupt.</b></p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: Reserved</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: Reserved</td> </tr> <tr> <td>0010: Reserved</td> <td>0110: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0111: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table> | 0000: Disable  | 0100: IRQ4     | 1000: Reserved | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: Reserved | 0010: Reserved | 0110: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0111: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable   | 0100: IRQ4  | 1000: Reserved | 1100: IRQ12    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0001: IRQ1  | 0101: IRQ5  | 1001: IRQ9     | 1101: Reserved |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0010: Reserved  | 0110: IRQ6  | 1010: IRQ10    | 1110: IRQ14    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0011: IRQ3  | 0111: IRQ7  | 1011: IRQ11    | 1111: IRQ15    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Index 5Dh PCI Interrupt Steering Register 2 (R/W) Reset Value: 00h</b></p> <p>Indicates target interrupts for signals INTD# and INTC#. Note that INTD# is muxed with IDE_DATA7 (selection made via PMR[24]) and INTC# is muxed with GPIO19+IOCHRDY (selection made via PMR[9,4]). See Table 4-2 on page 88 for PMR bit descriptions.</p> <p><b>Note:</b> The target interrupt must first be configured as level sensitive via I/O Ports 4D0h and 4D1h in order to maintain PCI interrupt compatibility.</p> |   |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 7:4   | <p><b>INTD# (EBGA Ball B22 / TEPBGA Ball AA2) Target Interrupt.</b></p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: Reserved</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: Reserved</td> </tr> <tr> <td>0010: Reserved</td> <td>0110: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0111: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table> | 0000: Disable  | 0100: IRQ4     | 1000: Reserved | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: Reserved | 0010: Reserved | 0110: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0111: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable   | 0100: IRQ4  | 1000: Reserved | 1100: IRQ12    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0001: IRQ1  | 0101: IRQ5  | 1001: IRQ9     | 1101: Reserved |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0010: Reserved  | 0110: IRQ6  | 1010: IRQ10    | 1110: IRQ14    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0011: IRQ3  | 0111: IRQ7  | 1011: IRQ11    | 1111: IRQ15    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 3:0   | <p><b>INTC# (EBGA Ball H4 / TEPBGA Ball C9) Target Interrupt.</b></p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: Reserved</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: Reserved</td> </tr> <tr> <td>0010: Reserved</td> <td>0110: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0111: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table>   | 0000: Disable  | 0100: IRQ4     | 1000: Reserved | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: Reserved | 0010: Reserved | 0110: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0111: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable   | 0100: IRQ4  | 1000: Reserved | 1100: IRQ12    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0001: IRQ1  | 0101: IRQ5  | 1001: IRQ9     | 1101: Reserved |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0010: Reserved  | 0110: IRQ6  | 1010: IRQ10    | 1110: IRQ14    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| 0011: IRQ3  | 0111: IRQ7  | 1011: IRQ11    | 1111: IRQ15    |                |             |            |            |            |                |                |            |             |             |            |            |             |             |
| <p><b>Index 5Eh-5Fh Reserved Reset Value: 00h</b></p>   |   |                |                |                |             |            |            |            |                |                |            |             |             |            |            |             |             |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description  |
|---|--|
| <b>Index 60h-63h</b> <b>ACPI Control Register (R/W)</b> <b>Reset Value: 00000000h</b> |  |
| 31:8  | <b>Reserved.</b> Must be set to 0.   |
| 7   | <b>SUSP_3V Shut Down PLL5.</b> Allow internal SUSP_3V to shut down PLL5.<br>0: Clock generator is stopped when internal SUSP_3V is active.<br>1: Clock generator continues working when internal SUSP_3V is active.  |
| 6   | <b>SUSP_3V Shut Down PLL4.</b> Allow internal SUSP_3V to shut down PLL4<br>0: Clock generator is stopped when internal SUSP_3V is active.<br>1: Clock generator continues working when internal SUSP_3V is active.   |
| 5   | <b>SUSP_3V Shut Down PLL3.</b> Allow internal SUSP_3V to shut down PLL3.<br>0: Clock generator is stopped when internal SUSP_3V is active.<br>1: Clock generator continues working when internal SUSP_3V is active.  |
| 4   | <b>SUSP_3V Shut Down PLL2.</b> Allow internal SUSP_3V to shut down PLL2.<br>0: Clock generator is stopped when internal SUSP_3V is active.<br>1: Clock generator continues working when internal SUSP_3V is active.  |
| 3   | <b>SUSP_3V Shut Down PLL6.</b> Allow internal SUSP_3V to shut down PLL6.<br>0: Clock generator is stopped when internal SUSP_3V is active.<br>1: Clock generator continues working when internal SUSP_3V is active.  |
| 2   | <b>ACPI C3 SUSP_3V Enable.</b> Allow internal SUSP_3V to be active during C3 state.<br>0: Disable.<br>1: Enable.   |
| 1   | <b>ACPI SL1 SUSP_3V Enable.</b> Allow internal SUSP_3V to be active during SL1 sleep state.<br>0: Disable.<br>1: Enable.   |
| 0   | <b>ACPI C3 Support Enable.</b> Allow support of C3 states.<br>0: Disable.<br>1: Enable.  |
| <b>Index 64h-6Bh</b> <b>Reserved</b> <b>Reset Value: 00h</b>                          |  |
| <b>Index 6Ch-6Fh</b> <b>ROM Mask Register (R/W)</b> <b>Reset Value: 0000FFF0h</b>     |  |
| <b>Note:</b> Register must be read/written as a DWORD.                                |  |
| 31:16   | <b>Reserved.</b> Must be written to 0.   |
| 15:8  | <b>Reserved.</b> Must be written to FFh.   |
| 7:4   | <b>ROM Size.</b> If F0 Index 52h[2] = 1:<br>0000: 16 MB = FF000000h-FFFFFFFFh<br>1000: 8 MB = FF800000h-FFFFFFFFh<br>1100: 4 MB = FFC00000h-FFFFFFFFh<br>1110: 2 MB = FFE00000h-FFFFFFFFh<br>1111: 1 MB = FFF00000h-FFFFFFFFh<br>All other settings for these bits are reserved. |
| 3:0   | <b>Reserved.</b> Must be set to 0.   |



**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description   |
|---|---|
| <b>Index 70h-71h</b> <b>IOCS1# Base Address Register (R/W)</b> <b>Reset Value: 0000h</b>  |   |
| 15:0  | <b>I/O Chip Select 1 Base Address.</b> This 16-bit value represents the I/O base address used to enable assertion of IOCS1# (EBGA ball H2 or AL12 / TEPBGA ball D10 or N30 - see PMR[23] in Table 4-2 on page 88).<br>This register is used in conjunction with F0 Index 72h (IOCS1# Control register). |
| <b>Index 72h</b> <b>IOCS1# Control Register (R/W)</b> <b>Reset Value: 00h</b><br>This register is used in conjunction with F0 Index 70h (IOCS1# Base Address register). |   |
| 7   | <b>I/O Chip Select 1 Positive Decode (IOCS1#).</b><br>0: Disable.<br>1: Enable.   |
| 6   | <b>Writes Result in Chip Select.</b> When this bit is set to 1, writes to configured I/O address (base address configured in F0 Index 70h; range configured in bits [4:0]) cause IOCS1# to be asserted.<br>0: Disable.<br>1: Enable.  |
| 5   | <b>Reads Result in Chip Select.</b> When this bit is set to 1, reads from configured I/O address (base address configured in F0 Index 70h; range configured in bits [4:0]) cause IOCS1# to be asserted.<br>0: Disable.<br>1: Enable.  |
| 4:0   | <b>IOCS1# I/O Address Range.</b> This 5-bit field is used to select the range of IOCS1#.<br>00000: 1 Byte<br>00001: 2 Bytes<br>00011: 4 Bytes<br>00111: 8 Bytes<br>01111: 16 Bytes<br>11111: 32 Bytes<br>All other combinations are reserved.   |
| <b>Index 73h</b> <b>Reserved</b> <b>Reset Value: 00h</b>  |   |
| <b>Index 74h-75h</b> <b>IOCS0# Base Address Register (R/W)</b> <b>Reset Value: 0000h</b>  |   |
| 15:0  | <b>I/O Chip Select 0 Base Address.</b> This 16-bit value represents the I/O base address used to enable the assertion of IOCS0# (EBGA ball J4 / TEPBGA ball A10 - see PMR[23] in Table 4-2 on page 88).<br>This register is used in conjunction with F0 Index 76h (IOCS0# Control register).            |
| <b>Index 76h</b> <b>IOCS0# Control Register (R/W)</b> <b>Reset Value: 00h</b><br>This register is used in conjunction with F0 Index 74h (IOCS0# Base Address register). |   |
| 7   | <b>I/O Chip Select 0 Positive Decode (IOCS0#).</b><br>0: Disable.<br>1: Enable.   |
| 6   | <b>Writes Result in Chip Select.</b> When this bit is set to 1, writes to configured I/O address (base address configured in F0 Index 74h; range configured in bits [4:0]) cause IOCS0# to be asserted.<br>0: Disable.<br>1: Enable.  |
| 5   | <b>Reads Result in Chip Select.</b> When this bit is set to 1, reads from configured I/O address (base address configured in F0 Index 74h; range configured in bits [4:0]) cause IOCS0# to be asserted.<br>0: Disable.<br>1: Enable.  |
| 4:0   | <b>IOCS0# I/O Address Range.</b> This 5-bit field is used to select the range of IOCS0#.<br>00000: 1 Byte<br>00001: 2 Bytes<br>00011: 4 Bytes<br>00111: 8 Bytes<br>01111: 16 Bytes<br>11111: 32 Bytes<br>All other combinations are reserved.   |
| <b>Index 77h</b> <b>Reserved</b> <b>Reset Value: 00h</b>  |   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description  |
|---|--|
| <b>Index 78h-7Bh DOCCS# Base Address Register (R/W) Reset Value: 00000000h</b>  |  |
| 31:0  | <b>DiskOnChip Chip Select Base Address.</b> This 32-bit value represents the memory base address used to enable assertion of DOCCS# (EBGA ball H3 or AJ13 / TEPBGA ball A9 or N31, see PMR[23] in Table 4-2 on page 88).<br>This register is used in conjunction with F0 Index 7Ch (DOCCS# Control register).  |
| <b>Index 7Ch-7Fh DOCCS# Control Register (R/W) Reset Value: 00000000h</b><br>This register is used in conjunction with F0 Index 78h (DOCCS# Base Address register). |  |
| 31:27   | <b>Reserved.</b> Must be set to 0.   |
| 26  | <b>DiskOnChip Chip Select Positive Decode (DOCCS#).</b><br>0: Disable.<br>1: Enable.   |
| 25  | <b>Writes Result in Chip Select.</b> When this bit is set to 1, writes to configured memory address (base address configured in F0 Index 78h; range configured in bits [18:0]) cause DOCCS# to be asserted.<br>0: Disable.<br>1: Enable.   |
| 24  | <b>Reads Result in Chip Select.</b> When this bit is set to 1, reads from configured memory address (base address configured in F0 Index 78h; range configured in bits [18:0]) cause DOCCS# to be asserted.<br>0: Disable.<br>1: Enable.   |
| 23:19   | <b>Reserved.</b> Must be set to 0.   |
| 18:0  | <b>DOCCS# Memory Address Range.</b> This 19-bit mask is used to qualify accesses on which DOCCS# is asserted by masking the upper 19 bits of the incoming PCI address (AD[31:13]).   |
| <b>Index 80h Power Management Enable Register 1 (R/W) Reset Value: 00h</b>  |  |
| 7:6   | <b>Reserved.</b> Must be set to 0.   |
| 5   | <b>Codec SDATA_IN SMI.</b> When set to 1, this bit allows an SMI to be generated in response to an AC97 codec producing a positive edge on SDATA_IN.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br>Second level SMI status is reported at F0 Index 87h/F7h[2].  |
| 4   | <b>Video Speedup.</b> Any video activity, as decoded from the serial connection (P SERIAL) from the GX1 module disables clock throttling (via internal SUSP#/SUSPA# handshake) for a configurable duration when system is power-managed using CPU Suspend modulation.<br>0: Disable.<br>1: Enable.<br>The duration of the speedup is configured in the Video Speedup Timer Count Register (F0 Index 8Dh). Detection of an external VGA access (3Bx, 3Cx, 3Dx and A000h-B7FFh) on the PCI bus is also supported. This configuration is non-standard, but it does allow the power management routines to support an external VGA chip. |
| 3   | <b>IRQ Speedup.</b> Any unmasked IRQ (per I/O Ports 021h/0A1h) or SMI disables clock throttling (via internal SUSP#/SUSPA# handshake) for a configurable duration when system is power-managed using CPU Suspend modulation.<br>0: Disable.<br>1: Enable.<br>The duration of the speedup is configured in the IRQ Speedup Timer Count Register (F0 Index 8Ch).   |
| 2   | <b>Traps.</b> Globally enable all power management I/O traps.<br>0: Disable.<br>1: Enable.<br>This excludes the audio I/O traps, which are enabled via F3BAR0+Memory Offset 18h.   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description   |
|---|---|
| 1   | <p><b>Idle Timers.</b> Device idle timers.</p> <p>0: Disable.<br/>1: Enable.</p> <p><b>Note:</b> Disable at this level does not reload the timers on the enable. The timers are disabled at their current counts. This bit has no affect on the Suspend Modulation register (F0 Index 94h). Only applicable when in APM mode (F1BAR1+I/O Offset 0Ch[0] = 0) and not ACPI mode.</p>  |
| 0   | <p><b>Power Management.</b> Global power management.</p> <p>0: Disable.<br/>1: Enable.</p> <p>This bit must be set to 1 immediately after POST for power management resources to function.</p>  |
| <b>Index 81h</b>                                |   |
| <b>Power Management Enable Register 2 (R/W)</b> |   |
| <b>Reset Value: 00h</b>                         |   |
| 7   | <p><b>Video Access Idle Timer Enable.</b> Turn on Video Idle Timer Count Register (F0 Index A6h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the video address range (sets bit 0 of the GX1 module's P SERIAL register) the timer is reloaded with the programmed count.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[7].</p>   |
| 6   | <p><b>User Defined Device 3 (UDEF3) Idle Timer Enable.</b> Turn on UDEF3 Idle Timer Count Register (F0 Index A4h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the programmed address range, the timer is reloaded with the programmed count.</p> <p>UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register).</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[6].</p> |
| 5   | <p><b>User Defined Device 2 (UDEF2) Idle Timer Enable.</b> Turn on UDEF2 Idle Timer Count Register (F0 Index A2h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the programmed address range, the timer is reloaded with the programmed count.</p> <p>UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register).</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[5].</p> |
| 4   | <p><b>User Defined Device 1 (UDEF1) Idle Timer Enable.</b> Turn on UDEF1 Idle Timer Count Register (F0 Index A0h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the programmed address range, the timer is reloaded with the programmed count.</p> <p>UDEF1 address programming is at F0 Index C0h (base address register) and CCh (control register).</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[4].</p> |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit | Description  |
|-----|--|
| 3   | <p><b>Keyboard/Mouse Idle Timer Enable.</b> Turn on Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the address ranges listed below, the timer is reloaded with the programmed count:</p> <ul style="list-style-type: none"> <li>— Keyboard Controller: I/O Ports 060h/064h.</li> <li>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included).</li> <li>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included).</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[3].</p>   |
| 2   | <p><b>Parallel/Serial Idle Timer Enable.</b> Turn on Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the address ranges listed below, the timer is reloaded with the programmed count.</p> <ul style="list-style-type: none"> <li>— LPT1: I/O Port 3BCh-3BEh.</li> <li>— LPT2: I/O Port 378h-37Fh.</li> <li>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded).</li> <li>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded).</li> <li>— COM3: I/O Port 3E8h-3EFh.</li> <li>— COM4: I/O Port 2E8h-2EFh.</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[2].</p> |
| 1   | <p><b>Floppy Disk Idle Timer Enable.</b> Turn on Floppy Disk Idle Timer Count Register (F0 Index 9Ah) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the address ranges (listed below, the timer is reloaded with the programmed count.</p> <ul style="list-style-type: none"> <li>— Primary floppy disk: I/O Port 3F2h-3F5h, 3F7h.</li> <li>— Secondary floppy disk: I/O Port 372h-375h, 377h.</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[1].</p>   |
| 0   | <p><b>Primary Hard Disk Idle Timer Enable.</b> Turn on Primary Hard Disk Idle Timer Count Register (F0 Index 98h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the address ranges selected in F0 Index 93h[5], the timer is reloaded with the programmed count.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[0].</p>  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit              | Description  |
|------------------|--|
| <b>Index 82h</b> | <b>Power Management Enable Register 3 (R/W)</b> <span style="float: right;"><b>Reset Value: 00h</b></span>   |
| 7                | <p><b>Video Access Trap.</b> If this bit is enabled and an access occurs in the video address range (sets bit 0 of the GX1 module's PSERIAL register), an SMI is generated.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[7].</p>   |
| 6                | <p><b>User Defined Device 3 (UDE3) Access Trap.</b> If this bit is enabled and an access occurs in the programmed address range, an SMI is generated. UDEF3 address programming is at F0 Index C8h (Base Address register) and CEh (Control register).</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[4].</p>   |
| 5                | <p><b>User Defined Device 2 (UDE2) Access Trap.</b> If this bit is enabled and an access occurs in the programmed address range, an SMI is generated. UDEF2 address programming is at F0 Index C4h (Base Address register) and CDh (Control register).</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[3].</p>   |
| 4                | <p><b>User Defined Device 1 (UDE1) Access Trap.</b> If this bit is enabled and an access occurs in the programmed address range, an SMI is generated. UDEF1 address programming is at F0 Index C0h (base address register), and CCh (control register).</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[2].</p>  |
| 3                | <p><b>Keyboard/Mouse Access Trap.</b></p> <p>0: Disable.<br/>1: Enable.</p> <p>If this bit is enabled and an access occurs in the address ranges listed below, an SMI is generated.</p> <ul style="list-style-type: none"> <li>— Keyboard Controller: I/O Ports 060h/064h.</li> <li>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included).</li> <li>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included).</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[3].</p>   |
| 2                | <p><b>Parallel/Serial Access Trap.</b></p> <p>0: Disable.<br/>1: Enable.</p> <p>If this bit is enabled and an access occurs in the address ranges listed below, an SMI is generated.</p> <ul style="list-style-type: none"> <li>— LPT1: I/O Port 3BCh-3BEh.</li> <li>— LPT2: I/O Port 378h-37Fh.</li> <li>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded).</li> <li>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded).</li> <li>— COM3: I/O Port 3E8h-3EFh.</li> <li>— COM4: I/O Port 2E8h-2EFh.</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[2].</p> |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit              | Description  |
|------------------|--|
| 1                | <p><b>Floppy Disk Access Trap.</b></p> <p>0: Disable.<br/>1: Enable.</p> <p>If this bit is enabled and an access occurs in the address ranges listed below, an SMI is generated.</p> <ul style="list-style-type: none"> <li>— Primary floppy disk: I/O Port 3F2h-3F5h, 3F7h.</li> <li>— Secondary floppy disk: I/O Port 372h-375h, 377h.</li> </ul> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[1].</p> |
| 0                | <p><b>Primary Hard Disk Access Trap.</b></p> <p>0: Disable.<br/>1: Enable.</p> <p>If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[5], an SMI is generated.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[0].</p>   |
| <b>Index 83h</b> | <b>Power Management Enable Register 4 (R/W)</b>  |
|                  | <b>Reset Value: 00h</b>  |
| 7                | <p><b>Secondary Hard Disk Idle Timer Enable.</b> Turn on Secondary Hard Disk Idle Timer Count Register (F0 Index ACh) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the address ranges selected in F0 Index 93h[4], the timer is reloaded with the programmed count.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[4].</p>              |
| 6                | <p><b>Secondary Hard Disk Access Trap.</b> If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[4], an SMI is generated.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 86h/F6h[5].</p>  |
| 5                | <p><b>ACPI Timer SMI.</b> Allow SMI generation for MSB toggles on the ACPI Timer (F1BAR0+I/O Offset 1Ch or F1BAR1+I/O Offset 1Ch).</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 87h/F7h[0].</p>  |
| 4                | <p><b>THRM# SMI.</b> Allow SMI generation on assertion of THRM#.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 87h/F7h[6].</p>  |
| 3                | <p><b>VGA Timer Enable.</b> Turn on VGA Timer Count Register (F0 Index 8Eh) and generate an SMI when the timer reaches 0.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If an access occurs in the programmed address range, the timer is reloaded with the programmed count. F0 Index 8Bh[6] selects the timebase for the VGA Timer.</p> <p>SMI status is reported at F1BAR0+I/O Offset 00h/02h[6] (top level only).</p>   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description   |
|---|---|
| 2   | <p><b>Video Retrace Interrupt SMI.</b> Allow SMI generation whenever video retrace occurs.</p> <p>0: Disable.<br/>1: Enable.</p> <p>This information is decoded from the serial connection (P SERIAL register, bit 7) from the GX1 module. This function is normally not used for power management but for soft (VSA) VGA routines.</p> <p>SMI status reporting is at F1BAR0+I/O Offset 00h/02h[5] (top level only).</p>  |
| 1   | <p><b>General Purpose Timer 2 Enable.</b> Turn on GP Timer 2 Count Register (F0 Index 8Ah) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>This idle timer is reloaded from the assertion of GPIO7 (if programmed to do so). GP Timer 2 programming is at F0 Index 8Bh[5,3,2].</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[1].</p>                           |
| 0   | <p><b>General Purpose Timer 1 Enable.</b> Turn on GP Timer 1 Count Register (F0 Index 88h) and generate an SMI when the timer expires.</p> <p>0: Disable.<br/>1: Enable.</p> <p>This idle timer's load is multi-sourced and gets reloaded any time an enabled event (F0 Index 89h[6:0]) occurs. GP Timer 1 programming is at F0 Index 8Bh[4].</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[0].</p> |
| <p><b>Index 84h</b> <b>Second Level PME/SMI Status Mirror Register 1 (RO)</b> <b>Reset Value: 00h</b></p> <p>The bits in this register are used for the second level of status reporting. The top level is reported at F1BAR0+I/O Offset 00h/02h[0].</p> <p>This register is called a "mirror" register since an identical register exists at F0 Index F4h. Reading this register does not clear the status, while reading its counterpart at F0 Index F4h clears the status at both the second and the top levels.</p> |   |
| 7:3   | <b>Reserved.</b> Reads as 0.  |
| 2   | <p><b>GPWIO2 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO2 pin.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation:<br/>1) Ensure that GPWIO2 is enabled as an input: F1BAR1+I/O Offset 15h[2] = 0.<br/>2) Set F1BAR1+I/O Offset 15h[6] to 1.</p>   |
| 1   | <p><b>GPWIO1 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO1 pin.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation:<br/>1) Ensure that GPWIO1 is enabled as an input: F1BAR1+I/O Offset 15h[1] = 0.<br/>2) Set F1BAR1+I/O Offset 15h[5] to 1.</p>   |
| 0   | <p><b>GPWIO0 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO0 pin.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation:<br/>1) Ensure that GPWIO0 is enabled as an input: F1BAR1+I/O Offset 15h[0] = 0.<br/>2) Set F1BAR1+I/O Offset 15h[4] to 1.</p>   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit              | Description   |
|------------------|---|
| <b>Index 85h</b> | <b>Second Level PME/SMI Status Mirror Register 2 (RO)</b> <span style="float: right;"><b>Reset Value: 00h</b></span><br>The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br>This register is called a "Mirror" register since an identical register exists at F0 Index F5h. Reading this register does not clear the status, while reading its counterpart at F0 Index F5h clears the status at both the second and top levels. |
| 7                | <b>Video Idle Timer Timeout.</b> Indicates whether or not an SMI was caused by expiration of Video Idle Timer Count Register (F0 Index A6h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[7] to 1.  |
| 6                | <b>User Defined Device Idle Timer 3 Timeout.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 3 Idle Timer Count Register (F0 Index A4h).<br>0: No<br>1: Yes<br>To enable SMI generation, set F0 Index 81h[6] to 1.  |
| 5                | <b>User Defined Device Idle Timer 2 Timeout.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 2 Idle Timer Count Register (F0 Index A2h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[5] to 1.  |
| 4                | <b>User Defined Device Idle Timer 1 Timeout.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 1 Idle Timer Count Register (F0 Index A0h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[4] to 1.  |
| 3                | <b>Keyboard/Mouse Idle Timer Timeout.</b> Indicates whether or not an SMI was caused by expiration of Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[3] to 1.  |
| 2                | <b>Parallel/Serial Idle Timer Timeout.</b> Indicates whether or not an SMI was caused by expiration of Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[2] to 1.   |
| 1                | <b>Floppy Disk Idle Timer Timeout.</b> Indicates whether or not an SMI was caused by expiration of Floppy Disk Idle Timer Count Register (F0 Index 9Ah).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[1] to 1.  |
| 0                | <b>Primary Hard Disk Idle Timer Timeout.</b> Indicates whether or not an SMI was caused by expiration of Primary Hard Disk Idle Timer Count Register (F0 Index 98h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[0] to 1.  |



**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit              | Description   |
|------------------|---|
| <b>Index 86h</b> | <b>Second Level PME/SMI Status Mirror Register 3 (RO)</b> <span style="float: right;"><b>Reset Value: 00h</b></span><br>The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br>This register is called a "Mirror" register since an identical register exists at F0 Index F6h. Reading this register does not clear the status, while reading its counterpart at F0 Index F6h clears the status at both the second and top levels. |
| 7                | <b>Video Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the Video I/O Trap.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[7] to 1.  |
| 6                | <b>Reserved.</b>  |
| 5                | <b>Secondary Hard Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the secondary hard disk.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[6] to 1.   |
| 4                | <b>Secondary Hard Disk Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Secondary Hard Disk Idle Timer Count register (F0 Index ACh).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[7] to 1.   |
| 3                | <b>Keyboard/Mouse Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by an trapped I/O access to the keyboard or mouse.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[3] to 1.   |
| 2                | <b>Parallel/Serial Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to either the serial or parallel ports.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[2] to 1.   |
| 1                | <b>Floppy Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the floppy disk.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[1] to 1.   |
| 0                | <b>Primary Hard Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the primary hard disk.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[0] to 1.   |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit              | Description  |
|------------------|--|
| <b>Index 87h</b> | <b>Second Level PME/SMI Status Mirror Register 4 (RO)</b> <span style="float: right;"><b>Reset Value: 00h</b></span><br>The bits in this register contain second level status reporting. Top level status is reported at F1BAR0+I/O Offset 00h/02h[0].<br>This register is called a "Mirror" register since an identical register exists at F0 Index F7h. Reading this register does not clear the status, while reading its counterpart at F0 Index F7h clears the status at both the second and top levels except for bit 7 which has a third level of SMI status reporting at F0BAR0+I/O 0Ch/1Ch.   |
| 7                | <b>GPIO Event SMI Status.</b> Indicates whether or not an SMI was caused by a transition of any of the GPIOs (GPIO47-GPIO32 and GPIO15-GPIO0).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[0] to 0.<br>F0BAR0+I/O Offset 08h/18h selects which GPIOs are enabled to generate a PME and setting F1BAR1+I/O Offset 0Ch[0] = 0 enables the PME to generate an SMI. In addition, the selected GPIO must be enabled as an input (F0BAR0+I/O Offset 20h and 24h).<br>The next level (third level) of SMI status is at F0BAR0+I/O 0Ch/1Ch[15:0].  |
| 6                | <b>Thermal Override SMI Status.</b> Indicates whether or not an SMI was caused by the assertion of THRM#.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[4] to 1.  |
| 5:4              | <b>Reserved.</b> Always reads 0.   |
| 3                | <b>SIO PWUREQ SMI Status.</b> Indicates whether or not an SMI was caused by a power-up event from the SIO.<br>0: No.<br>1: Yes.<br>A power-up event is defined as any of the following events/activities:<br>— RI2#<br>— SDATA_IN2<br>— IRRX1 (CEIR)<br>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[0] to 0.   |
| 2                | <b>Codec SDATA_IN SMI Status.</b> Indicates whether or not an SMI was caused by AC97 Codec producing a positive edge on SDATA_IN.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 80h[5] to 1.  |
| 1                | <b>RTC Alarm (IRQ8#) SMI Status.</b> Indicates whether or not an SMI was caused by an RTC interrupt.<br>0: No.<br>1: Yes.<br>This SMI event can only occur while in 3V Suspend and an RTC interrupt occurs with F1BAR1+I/O Offset 0Ch[0] = 0.  |
| 0                | <b>ACPI Timer SMI Status.</b> Indicates whether or not an SMI was caused by an ACPI Timer (F1BAR0+I/O Offset 1Ch or F1BAR1+I/O Offset 1Ch) MSB toggle.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[5] to 1.   |
| <b>Index 88h</b> | <b>General Purpose Timer 1 Count Register (R/W)</b> <span style="float: right;"><b>Reset Value: 00h</b></span>   |
| 7:0              | <b>GPT1_COUNT.</b> This field represents the load value for General Purpose Timer 1. This value can represent either an 8-bit counter or a 16-bit counter (selected in F0 Index 8Bh[4]). It is loaded into the counter when the timer is enabled (F0 Index 83h[0] = 1). Once enabled, an enabled event (configured in F0 Index 89h[6:0]) reloads the timer.<br>The counter is decremented with each clock of the configured timebase (1 ms or 1 sec selected at F0 Index 89h[7]). Upon expiration of the counter, an SMI is generated, and the top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[9]. The second level SMI status is reported at F1BAR0+I/O Offset 04h/06h[0]. Once expired, this counter must be re-initialized by either disabling and enabling it, or writing a new count value in this register. See Section 6.2.10.3 "Peripheral Power Management" on page 180 for a discussion on the limitations of producing count error with small values. |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit              | Description   |
|------------------|---|
| <b>Index 89h</b> | <b>General Purpose Timer 1 Control Register (R/W)</b> <span style="float: right;"><b>Reset Value: 00h</b></span>  |
| 7                | <b>General Purpose Timer 1 Timebase.</b> Selects timebase for General Purpose Timer 1 (F0 Index 88h).<br>0: 1 second.<br>1: 1 millisecond.  |
| 6                | <b>Re-trigger General Purpose Timer 1 on User Defined Device 3 (UDEF3) Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the configured (memory or I/O) address range for UDEF3 (configured in F0 Index C8h and CEh) reloads General Purpose Timer 1.   |
| 5                | <b>Re-trigger General Purpose Timer 1 on User Defined Device 2 (UDEF2) Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the configured (memory or I/O) address range for UDEF2 (configured in F0 Index C4h and CDh) reloads General Purpose Timer 1.   |
| 4                | <b>Re-trigger General Purpose Timer 1 on User Defined Device 1 (UDEF1) Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the configured (memory or I/O) address range for UDEF1 (configured in F0 Index C0h and CCh) reloads General Purpose Timer 1.   |
| 3                | <b>Re-trigger General Purpose Timer 1 on Keyboard or Mouse Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the keyboard or mouse I/O address range listed below reloads General Purpose Timer 1:<br>— Keyboard Controller: I/O Ports 060h/064h.<br>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included).<br>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included).   |
| 2                | <b>Re-trigger General Purpose Timer 1 on Parallel/Serial Port Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the parallel or serial port I/O address range listed below reloads the General Purpose Timer 1:<br>— LPT1: I/O Port 3BCh-3BEh.<br>— LPT2: I/O Port 378h-37Fh.<br>— COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded).<br>— COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded).<br>— COM3: I/O Port 3E8h-3EFh.<br>— COM4: I/O Port 2E8h-2EFh. |
| 1                | <b>Re-trigger General Purpose Timer 1 on Floppy Disk Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the floppy disk drive address ranges listed below reloads General Purpose Timer 1:<br>— Primary floppy disk: I/O Port 3F2h-3F5h, 3F7h<br>— Secondary floppy disk: I/O Port 372h-375h, 377h<br>The active floppy disk drive is configured via F0 Index 93h[7].  |
| 0                | <b>Re-trigger General Purpose Timer 1 on Primary Hard Disk Activity.</b><br>0: Disable.<br>1: Enable.<br>Any access to the primary hard disk address range selected in F0 Index 93h[5], reloads General Purpose Timer 1.  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit  | Description  |
|--|--|
| <b>Index 8Ah</b> <b>General Purpose Timer 2 Count Register (R/W)</b> <b>Reset Value: 00h</b>   |  |
| 7:0  | <p><b>GPT2_COUNT.</b> This field represents the load value for General Purpose Timer 2. This value can represent either an 8-bit or 16-bit counter (configured in F0 Index 8Bh[5]). It is loaded into the counter when the timer is enabled (F0 Index 83h[1] = 1). Once the timer is enabled and a transition occurs on GPIO7, the timer is re-loaded.</p> <p>The counter is decremented with each clock of the configured timebase (1 ms or 1 sec selected at F0 Index 8Bh[3]). Upon expiration of the counter, an SMI is generated and the top level of status is F1BAR0+I/O Offset 00h/02h[9]. The second level of status is reported at F1BAR0+I/O Offset 04h/06h[1]). Once expired, this counter must be re-initialized by either disabling and enabling it, or by writing a new count value in this register. Section 6.2.10.3 "Peripheral Power Management" on page 180 for a discussion on the limitations of producing count error with small values.</p> <p>For GPIO7 to act as the reload for this counter, it must be enabled as such (F0 Index 8Bh[2]) and be configured as an input. (GPIO pin programming is at F0BAR0+I/O Offset 20h and 24h.)</p> |
| <b>Index 8Bh</b> <b>General Purpose Timer 2 Control Register (R/W)</b> <b>Reset Value: 00h</b> |  |
| 7  | <p><b>Re-trigger General Purpose Timer 1 (GP Timer 1) on Secondary Hard Disk Activity.</b></p> <p>0: Disable.<br/>1: Enable.</p> <p>Any access to the secondary hard disk address range selected in F0 Index 93h[4] reloads GP Timer 1.</p>  |
| 6  | <p><b>VGA Timer Base.</b> Selects timebase for VGA Timer Register (F0 Index 8Eh).</p> <p>0: 1 millisecond.<br/>1: 32 microseconds.</p>   |
| 5  | <p><b>General Purpose Timer 2 (GP Timer 2) Shift.</b> GP Timer 2 is treated as an 8-bit or 16-bit timer.</p> <p>0: 8-bit. The count value is loaded into GP Timer 2 Count Register (F0 Index 8Ah).<br/>1: 16-bit. The value loaded into GP Timer 2 Count Register is shifted left by eight bits, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 2.</p>  |
| 4  | <p><b>General Purpose Timer 1 (GP Timer 1) Shift.</b> GP Timer 1 is treated as an 8-bit or 16-bit timer.</p> <p>0: 8-bit. The count value is that loaded into GP Timer 1 Count Register (F0 Index 88h).<br/>1: 16-bit. The value loaded into GP Timer 1 Count Register is shifted left by eight bit, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 1.</p>  |
| 3  | <p><b>General Purpose Timer 2 (GP Timer 2) Timebase.</b> Selects timebase for GP Timer 2 (F0 Index 8Ah).</p> <p>0: 1 second.<br/>1: 1 millisecond.</p>   |
| 2  | <p><b>Re-trigger Timer on GPIO7 Pin Transition.</b> A rising-edge transition on the GPIO7 pin reloads GP Timer 2 (F0 Index 8Ah).</p> <p>0: Disable.<br/>1: Enable.</p> <p>For GPIO7 to work here, it must first be configured as an input. (GPIO pin programming is at F0BAR0+I/O Offset 20h and 24h.)</p>   |
| 1:0  | <b>Reserved.</b> Set to 0.   |
| <b>Index 8Ch</b> <b>IRQ Speedup Timer Count Register (R/W)</b> <b>Reset Value: 00h</b>         |  |
| 7:0  | <p><b>IRQ Speedup Timer Load Value.</b> This field represents the load value for the IRQ speedup timer. It is loaded into the counter when Suspend Modulation is enabled (F0 Index 96h[0] = 1) and an INTR or an access to I/O Port 061h occurs. When the event occurs, the Suspend Modulation logic is inhibited, permitting full performance operation of the GX1 module. Upon expiration, no SMI is generated; the Suspend Modulation begins again. The IRQ speedup timer's timebase is 1 ms.</p> <p>This speedup mechanism allows instantaneous response to system interrupts for full-speed interrupt processing. A typical value here would be 2 to 4 ms.</p>  |
| <b>Index 8Dh</b> <b>Video Speedup Timer Count Register (R/W)</b> <b>Reset Value: 00h</b>       |  |
| 7:0  | <p><b>Video Speedup Timer Load Value.</b> This field represents the load value for the Video speedup timer. It is loaded into the counter when Suspend Modulation is enabled (F0 Index 96[0] = 1) and any access to the graphics controller occurs. When a video access occurs, the Suspend Modulation logic is inhibited, permitting full-performance operation of the GX1 module. Upon expiration, no SMI is generated, and Suspend Modulation begins again. The video speedup timer's timebase is 1 ms.</p> <p>This speedup mechanism allows instantaneous response to video activity for full speed during video processing calculations. A typical value here would be 50 ms to 100 ms.</p>   |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description  |
|---|--|
| <b>Index 8Eh</b> <span style="float:right"><b>VGA Timer Count Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>              |  |
| 7:0   | <p><b>VGA Timer Load Value.</b> This field represents the load value for VGA Timer. It is loaded into the counter when the timer is enabled (F0 Index 83h[3] = 1). The counter is decremented with each clock of the configured timebase (F0 Index 8Bh[6]). Upon expiration of the counter, an SMI is generated and the status is reported at F1BAR0+I/O Offset 00h/02h[6] (only). Once expired, this counter must be re-initialized by either disabling and enabling it, or by writing a new count value in this register.</p> <p><b>Note:</b> Although grouped with the power management Idle Timers, the VGA Timer is not a power management function. It is not affected by the Global Power Management Enable setting at F0 Index 80h[0].</p> |
| <b>Index 8Fh-92h</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>                                |  |
| <b>Index 93h</b> <span style="float:right"><b>Miscellaneous Device Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span> |  |
| 7   | <p><b>Floppy Drive Port Select.</b> Indicates whether all system resources used to power manage the floppy drive use the primary, or secondary FDC addresses for decode.</p> <p>0: Secondary.<br/>1: Primary.</p>  |
| 6   | <b>Reserved.</b> Must be set to 1.   |
| 5   | <p><b>Partial Primary Hard Disk Decode.</b> This bit is used to restrict the addresses which are decoded as primary hard disk accesses.</p> <p>0: Power management monitors all reads and writes to I/O Port 1F0h-1F7h, 3F6h-3F7h (excludes writes to 3F7h), and 170h-177h, 376h-377h (excludes writes to 377h).<br/>1: Power management monitors only writes to I/O Port 1F6h and 1F7h.</p>   |
| 4   | <p><b>Partial Secondary Hard Disk Decode.</b> This bit is used to restrict the addresses which are decoded as secondary hard disk accesses.</p> <p>0: Power management monitors all reads and writes to I/O Port 170h-177h, 376h-377h (excludes writes to 377h).<br/>1: Power management monitors only writes to I/O Port 176h and 177h.</p>   |
| 3:2   | <b>Reserved.</b> Must be set to 0.   |
| 1   | <p><b>Mouse on Serial Enable.</b> Mouse is present on a Serial Port.</p> <p>0: No.<br/>1: Yes.</p> <p>If a mouse is attached to a serial port (i.e., this bit is set to 1), that port is removed from the serial device list being used to monitor serial port access for power management purposes and added to the keyboard/mouse decode. This is done because a mouse, along with the keyboard, is considered an input device and is used only to determine when to blank the screen.</p> <p>This bit and bit 0 of this register determine the decode used for the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) as well as the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch).</p>                                    |
| 0   | <p><b>Mouse Port Select.</b> Selects which serial port the mouse is attached to:</p> <p>0: COM1<br/>1: COM2.</p> <p>For more information see the description of bit 1 in this register (above).</p>  |
| <b>Index 94h-95h</b> <span style="float:right"><b>Suspend Modulation Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000h</b></span>     |  |
| 15:8  | <p><b>Suspend Signal Asserted Counter.</b> This 8-bit counter represents the number of 32 <math>\mu</math>s intervals that the internal SUSP# signal is asserted to the GX1 module. Together with bits [7:0], perform the Suspend Modulation function for CPU power management. The ratio of SUSP# asserted-to-de-asserted sets up an effective (emulated) clock frequency, allowing the power manager to reduce GX1 module power consumption.</p> <p>This counter is prematurely reset if an enabled speedup event occurs (i.e., IRQ and video speedups).</p>   |
| 7:0   | <p><b>Suspend Signal De-asserted Counter.</b> This 8-bit counter represents the number of 32 <math>\mu</math>s intervals that the internal SUSP# signal is de-asserted to the GX1 module. Together with bits [15:8], perform the Suspend Modulation function for CPU power management. The ratio of SUSP# asserted-to-de-asserted sets up an effective (emulated) clock frequency, allowing the power manager to reduce GX1 module power consumption.</p> <p>This counter is prematurely reset if an enabled speedup event occurs (i.e., IRQ and video speedups).</p>  |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description   |
|---|---|
| <b>Index 96h</b> <span style="float:right"><b>Suspend Configuration Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>                                      |   |
| 7:3   | <b>Reserved.</b> Must be set to 0.  |
| 2   | <b>Suspend Mode Configuration.</b> Special 3V Suspend mode to support powering down the GX1 module during Suspend.<br>0: Disable.<br>1: Enable.   |
| 1   | <b>SMI Speedup Configuration.</b> Selects how the Suspend Modulation function should react when an SMI occurs.<br>0: Use the IRQ Speedup Timer Count Register (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs.<br>1: Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable Register (F1BAR0+I/O Offset 08h).<br><br>The purpose of this bit is to disable Suspend Modulation while the GX1 module is in the System Management Mode so that VSA and Power Management operations occur at full speed. Two methods for accomplishing this are:<br>Map the SMI into the IRQ Speedup Timer Count Register (F0 Index 8Ch).<br>- or -<br>Have the SMI disable Suspend Modulation until the SMI handler reads the SMI Speedup Disable Register (F1BAR0+I/O Offset 08h). This the preferred method.<br><br>This bit has no affect if the Suspend Modulation feature is disabled (bit 0 = 0). |
| 0   | <b>Suspend Modulation Feature Enable.</b> This bit is used to enable/disable the Suspend Modulation feature.<br>0: Disable.<br>1: Enable.<br><br>When enabled, the internal SUSP# signal is asserted and de-asserted for the durations programmed in the Suspend Modulation register (F0 Index 94h).<br><br>The setting of this bit is mirrored in the Top Level PME/SMI Status register (F1BAR0+I/O Offset 00h/02h[15]). It is used by the SMI handler to determine if the SMI Speedup Disable register (F1BAR0+I/O Offset 08h) must be cleared on exit.   |
| <b>Index 97h</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>  |   |
| <b>Index 98h-99h</b> <span style="float:right"><b>Primary Hard Disk Idle Timer Count Register (Primary Channel) (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000h</b></span> |   |
| 15:0  | <b>Primary Hard Disk Idle Timer Count.</b> This idle timer is used to determine when the primary hard disk is not in use so that it can be powered down. The 16-bit value programmed here represents the period of hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured hard disk's data port (I/O port 1F0h or 3F6h).<br><br>This counter uses a 1 second timebase. To enable this timer, set F0 Index 81h[0] = 1.<br><br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br>Second level SMI status is reported at F0 Index 85h/F5h[0].  |
| <b>Index 9Ah-9Bh</b> <span style="float:right"><b>Floppy Disk Idle Timer Count Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000h</b></span>                         |   |
| 15:0  | <b>Floppy Disk Idle Timer Count.</b> This idle timer is used to determine when the floppy disk drive is not in use so that it can be powered down. The 16-bit value programmed here represents the period of floppy disk drive inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured floppy drive's data port (I/O port 3F5h or 375h).<br><br>This counter uses a 1 second time base. To enable this timer, set F0 Index 81h[1] = 1.<br><br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br>Second level SMI status is reported at F0 Index 85h/F5h[1].  |
| <b>Index 9Ch-9Dh</b> <span style="float:right"><b>Parallel / Serial Idle Timer Count Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000h</b></span>                   |   |
| 15:0  | <b>Parallel / Serial Idle Timer Count.</b> This idle timer is used to determine when the parallel and serial ports are not in use so that the ports can be power managed. The 16-bit value programmed in this register represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the parallel (LPT) or serial (COM) I/O address spaces. If the mouse is enabled on a serial port, that port is not considered here.<br><br>This counter uses a 1 second timebase. To enable this timer, set F0 Index 81h[2] = 1.<br><br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br>Second level SMI status is reported at F0 Index 85h/F5h[2].  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description  |
|---|--|
| <b>Index 9Eh-9Fh Keyboard / Mouse Idle Timer Count Register (R/W) Reset Value: 0000h</b>      |  |
| 15:0  | <p><b>Keyboard / Mouse Idle Timer Count.</b> This idle timer determines when the keyboard and mouse are not in use so that the LCD screen can be blanked. The 16-bit value programmed in this register represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to either the keyboard or mouse I/O address spaces (including the mouse serial port address space when a mouse is enabled on a serial port.)</p> <p>This counter uses a 1 second time base. To enable this timer, set F0 Index 81h[3] = 1.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[3].</p>  |
| <b>Index A0h-A1h User Defined Device 1 Idle Timer Count Register (R/W) Reset Value: 0000h</b> |  |
| 15:0  | <p><b>User Defined Device 1 (UDEF1) Idle Timer Count.</b> This idle timer determines when the device configured as User Defined Device 1 (UDEF1) is not in use so that it can be power managed. The 16-bit value programmed in this register represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured in the F0 Index C0h (Base Address register) and F0 Index CCh (Control register).</p> <p>This counter uses a 1 second time base. To enable this timer, set F0 Index 81h[4] = 1.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[4].</p>  |
| <b>Index A2h-A3h User Defined Device 2 Idle Timer Count Register (R/W) Reset Value: 0000h</b> |  |
| 15:0  | <p><b>User Defined Device 2 (UDEF2) Idle Timer Count.</b> This idle timer determines when the device configured as UDEF2 is not in use so that it can be power managed. The 16-bit value programmed in this register represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured in the F0 Index C4h (Base Address register) and F0 Index CDh (Control register).</p> <p>This counter uses a 1 second timebase. To enable this timer, set F0 Index 81h[5] = 1.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[5].</p>   |
| <b>Index A4h-A5h User Defined Device 3 Idle Timer Count Register (R/W) Reset Value: 0000h</b> |  |
| 15:0  | <p><b>User Defined Device 3 (UDEF3) Idle Timer Count.</b> This idle timer determines when the device configured as UDEF3 is not in use so that it can be power managed. The 16-bit value programmed in this register represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured in the UDEF3 Base Address Register (F0 Index C8h) and UDEF3 Control Register (F0 Index CEh).</p> <p>This counter uses a 1 second timebase. To enable this timer, set F0 Index 81h[6] = 1.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[6].</p>   |
| <b>Index A6h-A7h Video Idle Timer Count Register (R/W) Reset Value: 0000h</b>                 |  |
| 15:0  | <p><b>Video Idle Timer Count.</b> This idle timer determines when the graphics subsystem has been idle as part of the Suspend-determination algorithm. The 16-bit value programmed in this register represents the period of video inactivity after which the system is alerted via an SMI. The count in this timer is automatically reset at any access to the graphics controller space.</p> <p>This counter uses a 1 second timebase. To enable this timer, set F0 Index 81h[7] = 1.</p> <p>Since the graphics controller is embedded in the GX1 module, video activity is communicated to the Core Logic module via the serial connection (PSERIAL register, bit 0). The Core Logic module also detects accesses to standard VGA space on PCI (3Bxh, 3Cxh, 3Dxh and A000h-B7FFh) if an external VGA controller is being used.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>Second level SMI status is reported at F0 Index 85h/F5h[7].</p> |
| <b>Index A8h-A9h Video Overflow Count Register (R/W) Reset Value: 0000h</b>                   |  |
| 15:0  | <p><b>Video Overflow Count.</b> Each time the video speedup counter is triggered, a 100 ms timer is started. If the 100 ms timer expires before the video speedup counter lapses, the Video Overflow Count register increments and the 100 ms timer re-triggers. Software clears the overflow register when new evaluations are to begin. The count contained in this register can be combined with other data to determine the type of video accesses present in the system.</p>  |
| <b>Index AAh-ABh Reserved Reset Value: 00h</b>  |  |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description   |
|---|---|
| <b>Index ACh-ADh Secondary Hard Disk Idle Timer Count Register (R/W) Reset Value: 0000h</b> |   |
| 15:0  | <p><b>Secondary Hard Disk Idle Timer Count.</b> This idle timer is used to determine when the secondary hard disk is not in use so that it can be powered down. The 16-bit value programmed in this register represents the period of hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured hard disk's data port (I/O port 1F0h or 170h).</p> <p>This counter uses a 1 second timebase. To enable this timer, set F0 Index 83h[7] = 1.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[0].</p> <p>Second level SMI status is reported at F0 Index 86h/F6h[4].</p>                                 |
| <b>Index AEh CPU Suspend Command Register (WO) Reset Value: 00h</b>                         |   |
| 7:0   | <p><b>Software CPU Suspend Command.</b> If bit 0 in the Clock Stop Control register is set low (F0 Index BCh[0] = 0), a write to this register causes an internal SUSP#/SUSPA# handshake with the GX1 module, placing the GX1 module in a low-power state. The actual data written is irrelevant. Once in this state, any unmasked IRQ or SMI releases the GX1 module halt condition.</p> <p>If F0 Index BCh[0] = 1, writing to this register invokes a full system Suspend. In this case, the internal SUSP_3V signal is asserted after the SUSP#/SUSPA# halt. Upon a Resume event, the PLL delay programmed in the F0 Index BCh[7:4] is invoked, allowing the clock chip and GX1 module PLL to stabilize before de-asserting SUSP#.</p> |
| <b>Index AFh Suspend Notebook Command Register (WO) Reset Value: 00h</b>                    |   |
| 7:0   | <p><b>Software CPU Stop Clock Suspend.</b> A write to this register causes a SUSP#/SUSPA# handshake with the CPU, placing the GX1 module in a low-power state. Following this handshake, the SUSP_3V signal is asserted. The SUSP_3V signal is intended to be used to stop all system clocks.</p> <p>Upon a Resume event, the internal SUSP_3V signal is de-asserted. After a slight delay, the Core Logic module de-asserts the SUSP# signal. Once the clocks are stable, the GX1 module de-asserts SUSPA# and system operation resumes.</p>   |
| <b>Index B0h-B3h Reserved Reset Value: 00h</b>  |   |
| <b>Index B4h Floppy Port 3F2h Shadow Register (RO) Reset Value: xxh</b>                     |   |
| 7:0   | <p><b>Floppy Port 3F2h Shadow.</b> Last written value of I/O Port 3F2h. Required for support of FDC power On/Off and 0V Suspend/Resume coherency.</p> <p>This register is a copy of an I/O register which cannot safely be directly read. The value in this register is not deterministic of when the register is being read. It is provided here to assist in a Suspend-to-Disk operation.</p>   |
| <b>Index B5h Floppy Port 3F7h Shadow Register (RO) Reset Value: xxh</b>                     |   |
| 7:0   | <p><b>Floppy Port 3F7h Shadow.</b> Last written value of I/O Port 3F7h. Required for support of FDC power On/Off and 0V Suspend/Resume coherency.</p> <p>This register is a copy of an I/O register which cannot safely be directly read. The value in this register is not deterministic of when the register is being read. It is provided here to assist in a Suspend-to-Disk operation.</p>   |
| <b>Index B6h Floppy Port 372h Shadow Register (RO) Reset Value: xxh</b>                     |   |
| 7:0   | <p><b>Floppy Port 372h Shadow.</b> Last written value of I/O Port 372h. Required for support of FDC power On/Off and 0V Suspend/Resume coherency.</p> <p>This register is a copy of an I/O register which cannot safely be directly read. The value in this register is not deterministic of when the register is being read. It is provided here to assist in a Suspend-to-Disk operation.</p>   |
| <b>Index B7h Floppy Port 377h Shadow Register (RO) Reset Value: xxh</b>                     |   |
| 7:0   | <p><b>Floppy Port 377h Shadow.</b> Last written value of I/O Port 377h. Required for support of FDC power On/Off and 0V Suspend/Resume coherency.</p> <p>This register is a copy of an I/O register which cannot safely be directly read. The value in this register is not deterministic of when the register is being read. It is provided here to assist in a Suspend-to-Disk operation.</p>   |



Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit  | Description   |
|--|---|
| <b>Index B8h</b> <span style="float: right;"><b>DMA Shadow Register (RO)</b></span> <span style="float: right;"><b>Reset Value: xxh</b></span> |   |
| 7:0  | <p><b>DMA Shadow.</b> This 8-bit port sequences through the following list of shadowed DMA Controller registers. At power on, a pointer starts at the first register in the list and continuing through the other registers in subsequent reads according to the read sequence. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location.</p> <p>The read sequence for this register is:</p> <ol style="list-style-type: none"> <li>1. DMA Channel 0 Mode Register</li> <li>2. DMA Channel 1 Mode Register</li> <li>3. DMA Channel 2 Mode Register</li> <li>4. DMA Channel 3 Mode Register</li> <li>5. DMA Channel 4 Mode Register</li> <li>6. DMA Channel 5 Mode Register</li> <li>7. DMA Channel 6 Mode Register</li> <li>8. DMA Channel 7 Mode Register</li> <li>9. DMA Channel Mask Register (bit 0 is channel 0 mask, etc.)</li> <li>10. DMA Busy Register (bit 0 or 1 means a DMA occurred within last 1 ms, all other bits are 0)</li> </ol>  |
| <b>Index B9h</b> <span style="float: right;"><b>PIC Shadow Register (RO)</b></span> <span style="float: right;"><b>Reset Value: xxh</b></span> |   |
| 7:0  | <p><b>PIC Shadow.</b> This 8-bit port sequences through the following list of shadowed Interrupt Controller registers. At power on, a pointer starts at the first register in the list and continuing through the other registers in subsequent reads according to the read sequence. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location.</p> <p>The read sequence for this register is:</p> <ol style="list-style-type: none"> <li>1. PIC1 ICW1</li> <li>2. PIC1 ICW2</li> <li>3. PIC1 ICW3</li> <li>4. PIC1 ICW4 - Bits [7:5] of ICW4 are always 0.</li> <li>5. PIC1 OCW2 - Bits [6:3] of OCW2 are always 0 (See Note).</li> <li>6. PIC1 OCW3 - Bits [7:4] are 0 and bits [6:3] are 1.</li> <li>7. PIC2 ICW1</li> <li>8. PIC2 ICW2</li> <li>9. PIC2 ICW3</li> <li>10. PIC2 ICW4 - Bits [7:5] of ICW4 are always 0.</li> <li>11. PIC2 OCW2 - Bits [6:3] of OCW2 are always 0 (See Note).</li> <li>12. PIC2 OCW3 - Bits [7:4] are 0 and bits [6:3] are 1.</li> </ol> <p><b>Note:</b> To restore OCW2 to the shadow register value, write the appropriate address twice. First with the shadow register value, then with the shadow register value ORed with C0h.</p> |
| <b>Index BAh</b> <span style="float: right;"><b>PIT Shadow Register (RO)</b></span> <span style="float: right;"><b>Reset Value: xxh</b></span> |   |
| 7:0  | <p><b>PIT Shadow.</b> This 8-bit port sequences through the following list of shadowed Programmable Interval Timer registers. At power on, a pointer starts at the first register in the list and continuing through the other registers in subsequent reads according to the read sequence. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location.</p> <p>The read sequence for this register is:</p> <ol style="list-style-type: none"> <li>1. Counter 0 LSB (least significant byte)</li> <li>2. Counter 0 MSB</li> <li>3. Counter 1 LSB</li> <li>4. Counter 1 MSB</li> <li>5. Counter 2 LSB</li> <li>6. Counter 2 MSB</li> <li>7. Counter 0 Command Word</li> <li>8. Counter 1 Command Word</li> <li>9. Counter 2 Command Word</li> </ol> <p><b>Note:</b> The LSB/MSB of the count is the Counter base value, not the current value. Bits [7:6] of the command words are not used.</p>  |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit   | Description  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
|---|--|-------------|-------------|------------|-------------|------------|------------|------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|
| <b>Index BBh</b> <span style="float:right"><b>RTC Index Shadow Register (RO)</b></span> <span style="float:right"><b>Reset Value: xxh</b></span>  |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 7:0   | <b>RTC Index Shadow.</b> The RTC Shadow register contains the last written value of the RTC Index register (I/O Port 070h).  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <b>Index BCh</b> <span style="float:right"><b>Clock Stop Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>   |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 7:4   | <p><b>PLL Delay.</b> The programmed value in this field sets the delay (in milliseconds) after a break event occurs before the internal SUSP# signal is de-asserted to the GX1 module. This delay is designed to allow the clock chip and CPU PLL to stabilize before starting execution. This delay is only invoked if the STP_CLK bit was set.</p> <p>The 4-bit field allows values from 0 to 15 ms.</p> <table style="width:100%; border:none;"> <tr> <td style="width:25%;">0000: 0 ms</td> <td style="width:25%;">0100: 4 ms</td> <td style="width:25%;">1000: 8 ms</td> <td style="width:25%;">1100: 12 ms</td> </tr> <tr> <td>0001: 1 ms</td> <td>0101: 5 ms</td> <td>1001: 9 ms</td> <td>1101: 13 ms</td> </tr> <tr> <td>0010: 2 ms</td> <td>0110: 6 ms</td> <td>1010: 10 ms</td> <td>1110: 14 ms</td> </tr> <tr> <td>0011: 3 ms</td> <td>0111: 7 ms</td> <td>1011: 11 ms</td> <td>1111: 15 ms</td> </tr> </table> | 0000: 0 ms  | 0100: 4 ms  | 1000: 8 ms | 1100: 12 ms | 0001: 1 ms | 0101: 5 ms | 1001: 9 ms | 1101: 13 ms | 0010: 2 ms | 0110: 6 ms | 1010: 10 ms | 1110: 14 ms | 0011: 3 ms | 0111: 7 ms | 1011: 11 ms | 1111: 15 ms |
| 0000: 0 ms  | 0100: 4 ms   | 1000: 8 ms  | 1100: 12 ms |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 0001: 1 ms  | 0101: 5 ms   | 1001: 9 ms  | 1101: 13 ms |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 0010: 2 ms  | 0110: 6 ms   | 1010: 10 ms | 1110: 14 ms |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 0011: 3 ms  | 0111: 7 ms   | 1011: 11 ms | 1111: 15 ms |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 3:1   | <b>Reserved.</b> Set to 0.   |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 0   | <p><b>CPU Clock Stop.</b></p> <p>0: Normal internal SUSP#/SUSPA# handshake.</p> <p>1: Full system Suspend.</p>   |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <p><b>Note:</b> This register configures the Core Logic module to support a 3V Suspend mode. Setting bit 0 causes the SUSP_3V signal to assert after the appropriate conditions, stopping the system clocks. A delay of 0-15 ms is programmable (bits [7:4]) to allow for a delay for the clock chip and CPU PLL to stabilize when an event Resumes the system.</p> <p>A write to the CPU Suspend Command register (F0 Index AEh) with bit 0 written as:</p> <p>0: Internal SUSP#/SUSPA# handshake occurs. The GX1 module is put into a low-power state, and the system clocks are not stopped. When a break/resume event occurs, it releases the CPU halt condition.</p> <p>1: Internal SUSP#/SUSPA# handshake occurs and the SUSP_3V signal is asserted, thus invoking a full system Suspend (both GX1 module and system clocks are stopped). When a break event occurs, the SUSP_3V signal is de-asserted, the PLL delay programmed in bits [7:4] are invoked which allows the clock chip and GX1 module PLL to stabilize before de-asserting the internal SUSP# signal.</p> |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <b>Index BDh-BFh</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00h</b></span>  |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <b>Index C0h-C3h</b> <span style="float:right"><b>User Defined Device 1 Base Address Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span>  |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 31:0  | <p><b>User Defined Device 1 Base Address.</b> This 32-bit register supports power management (Trap and Idle timer resources) for a PCMCIA slot or some other device in the system. The value in this register is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CCh).</p> <p>The Core Logic module cannot snoop addresses on the Fast-PCI bus unless it actually claims the cycle. Therefore, Traps and Idle timers cannot support power management of devices on the Fast-PCI bus.</p>  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <b>Index C4h-C7h</b> <span style="float:right"><b>User Defined Device 2 Base Address Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span>  |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 31:0  | <p><b>User Defined Device 2 Base Address.</b> This 32-bit register supports power management (Trap and Idle timer resources) for a PCMCIA slot or some other device in the system. The value in this register is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CDh).</p> <p>The Core Logic module cannot snoop addresses on the Fast-PCI bus unless it actually claims the cycle. Therefore, Traps and Idle timers cannot support power management of devices on the Fast-PCI bus.</p>  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| <b>Index C8h-CBh</b> <span style="float:right"><b>User Defined Device 3 Base Address Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span>  |  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |
| 31:0  | <p><b>User Defined Device 3 Base Address.</b> This 32-bit register supports power management (Trap and Idle timer resources) for a PCMCIA slot or some other device in the system. The value in this register is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CEh).</p> <p>The Core Logic module cannot snoop addresses on the Fast-PCI bus unless the it actually claims the cycle. Therefore, Traps and Idle timers cannot support power management of devices on the Fast-PCI bus.</p>  |             |             |            |             |            |            |            |             |            |            |             |             |            |            |             |             |

Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)

| Bit  | Description   |
|--|---|
| <b>Index CCh</b> <b>User Defined Device 1 Control Register (R/W)</b> <b>Reset Value: 00h</b> |   |
| 7  | <b>Memory or I/O Mapped.</b> Determines how User Defined Device 1 is mapped.<br>0: I/O.<br>1: Memory.   |
| 6:0  | <b>Mask.</b><br>If bit 7 = 0 (I/O):<br>Bit 6    0: Disable write cycle tracking<br>1: Enable write cycle tracking<br>Bit 5    0: Disable read cycle tracking<br>1: Enable read cycle tracking<br>Bits [4:0] Mask for address bits A[4:0]<br>If bit 7 = 1 (Memory):<br>Bits [6:0] Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) A[8:0] are ignored.<br><b>Note:</b> A "1" in a mask bit means that the address bit is ignored for comparison. |
| <b>Index CDh</b> <b>User Defined Device 2 Control Register (R/W)</b> <b>Reset Value: 00h</b> |   |
| 7  | <b>Memory or I/O Mapped.</b> determines how User Defined Device 2 is mapped.<br>0: I/O<br>1: Memory   |
| 6:0  | <b>Mask.</b><br>If bit 7 = 0 (I/O):<br>Bit 6    0: Disable write cycle tracking<br>1: Enable write cycle tracking<br>Bit 5    0: Disable read cycle tracking<br>1: Enable read cycle tracking<br>Bits [4:0] Mask for address bits A[4:0]<br>If bit 7 = 1 (Memory):<br>Bits [6:0] Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) A[8:0] are ignored.<br><b>Note:</b> A "1" in a mask bit means that the address bit is ignored for comparison. |
| <b>Index CEh</b> <b>User Defined Device 3 Control Register (R/W)</b> <b>Reset Value: 00h</b> |   |
| 7  | <b>Memory or I/O Mapped.</b> Determines how User Defined Device 3 is mapped.<br>0: I/O.<br>1: Memory.   |
| 6:0  | <b>Mask.</b><br>If bit 7 = 0 (I/O):<br>Bit 6    0: Disable write cycle tracking<br>1: Enable write cycle tracking<br>Bit 5    0: Disable read cycle tracking<br>1: Enable read cycle tracking<br>Bits [4:0] Mask for address bits A[4:0]<br>If bit 7 = 1 (Memory):<br>Bits [6:0] Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) A[8:0] are ignored.<br><b>Note:</b> A "1" in a mask bit means that the address bit is ignored for comparison. |
| <b>Index CFh</b> <b>Reserved</b> <b>Reset Value: 00h</b>                                     |   |
| <b>Index D0h</b> <b>Software SMI Register (WO)</b> <b>Reset Value: 00h</b>                   |   |
| 7:0  | <b>Software SMI.</b> A write to this location generates an SMI. The data written is irrelevant. This register allows software entry into SMM via normal bus access instructions.  |
| <b>Index D1h-EBh</b> <b>Reserved</b> <b>Reset Value: 00h</b>                                 |   |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit  | Description   |
|--|---|
| <b>Index ECh</b> <b>Timer Test Register (R/W)</b> <b>Reset Value: 00h</b>  |   |
| 7:0  | <b>Timer Test Value.</b> The Timer Test register is intended only for test and debug purposes. It is not intended for setting operational timebases. For normal operation, never write to this register.  |
| <b>Index EDh-F3h</b> <b>Reserved</b> <b>Reset Value: 00h</b>   |   |
| <b>Index F4h</b> <b>Second Level PME/SMI Status Register 1 (RC)</b> <b>Reset Value: 00h</b>  |   |
| The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br>Reading this register clears the status at both the second and top levels.<br>A read-only "Mirror" version of this register exists at F0 Index 84h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F0 Index 84h can be read instead. |   |
| 7:3  | <b>Reserved.</b> Reads as 0.  |
| 2  | <b>GPWIO2 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO2 pin.<br>0: No.<br>1: Yes.<br>To enable SMI generation:<br>1) Ensure that GPWIO2 is enabled as an input: F1BAR1+I/O Offset 15h[2] = 0.<br>2) Set F1BAR1+I/O Offset 15h[6] = 1 to allow SMI generation.  |
| 1  | <b>GPWIO1 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO1 pin.<br>0: No.<br>1: Yes.<br>To enable SMI generation:<br>1) Ensure that GPWIO1 is enabled as an input: F1BAR1+I/O Offset 15h[1] = 0.<br>2) Set F1BAR1+I/O Offset 15h[5] to 1 to allow SMI generation. |
| 0  | <b>GPWIO0 SMI Status.</b> Indicates whether or not an SMI was caused by a transition on the GPWIO0 pin.<br>0: No<br>1: Yes<br>To enable SMI generation:<br>1) Ensure that GPWIO0 is enabled as an input: F1BAR1+I/O Offset 15h[0] = 0.<br>2) Set F1BAR1+I/O Offset 15h[4] to 1 to allow SMI generation.   |
| <b>Index F5h</b> <b>Second Level PME/SMI Status Register 2 (RC)</b> <b>Reset Value: 00h</b>  |   |
| The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br>Reading this register clears the status at both the second and top levels.<br>A read-only "Mirror" version of this register exists at F0 Index 85h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F0 Index 85h can be read instead. |   |
| 7  | <b>Video Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Video Idle Timer Count Register, (F0 Index A6h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[7] = 1.   |
| 6  | <b>User Defined Device Idle Timer 3 (UDEF3) SMI Status.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 3 (UDEF3) Idle Timer Count Register (F0 Index A4h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[6] = 1.                                |
| 5  | <b>User Defined Device Idle Timer 2 (UDEF2) SMI Status.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 2 (UDEF2) Idle Timer Count Register (F0 Index A2h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[5] = 1.                                |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit   | Description  |
|---|--|
| 4   | <b>User Defined Device Idle Timer 1 (UDEF1) SMI Status.</b> Indicates whether or not an SMI was caused by expiration of User Defined Device 1 (UDEF1) Idle Timer Count Register (F0 Index A0h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[4] = 1. |
| 3   | <b>Keyboard/Mouse Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Keyboard/ Mouse Idle Timer Count Register (F0 Index 9Eh).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[3] = 1.                              |
| 2   | <b>Parallel/Serial Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[2] = 1.                        |
| 1   | <b>Floppy Disk Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Floppy Disk Idle Timer Count Register (F0 Index 9Ah).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[1] = 1.                                     |
| 0   | <b>Hard Disk Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Hard Disk Idle Timer Count Register (F0 Index 98h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 81h[0] = 1.   |
| <b>Index F6h</b> <b>Second Level PME/SMI Status Register 3 (RC)</b> <b>Reset Value: 00h</b><br>The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br>Reading this register clears the status at both the second and top levels.<br>A read-only "Mirror" version of this register exists at F0 Index 86h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F0 Index 86h can be read instead. |  |
| 7   | <b>Video Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the Video I/O Trap.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[7] = 1.  |
| 6   | <b>Reserved.</b> Reads as 0.   |
| 5   | <b>Secondary Hard Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the secondary hard disk.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[6] = 1.   |
| 4   | <b>Secondary Hard Disk Idle Timer SMI Status.</b> Indicates whether or not an SMI was caused by expiration of Secondary Hard Disk Idle Timer Count register (F0 Index ACh).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[7] = 1.                     |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit  | Description   |
|--|---|
| 3  | <p><b>Keyboard/Mouse Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the keyboard or mouse.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[3] = 1.</p>   |
| 2  | <p><b>Parallel/Serial Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to either the serial or parallel ports.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[2] = 1.</p>  |
| 1  | <p><b>Floppy Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the floppy disk.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[1] = 1.</p>  |
| 0  | <p><b>Primary Hard Disk Access Trap SMI Status.</b> Indicates whether or not an SMI was caused by a trapped I/O access to the primary hard disk.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[0] = 1.</p>  |
| <p><b>Index F7h</b> <b>Second Level PME/SMI Status Register 4 (RC)</b> <b>Reset Value: 00h</b></p> <p>The bits in this register contain second level status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[0].<br/>Reading this register clears the status at both the second and top levels except for bit 7 which has a third level of status reporting at F0BAR0+I/O 0Ch/1Ch.</p> <p>A read-only "Mirror" version of this register exists at F0 Index 87h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F0 Index 87h can be read instead.</p> |   |
| 7  | <p><b>GPIO Event SMI Status (Read Only, Read does not Clear).</b> Indicates whether or not an SMI was caused by a transition of any of the GPIOs (GPIO47-GPIO32 and GPIO15-GPIO0).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[0] = 0.</p> <p>F0BAR0+I/O Offset 08h/18h selects which GPIOs are enabled to generate a PME and setting F1BAR1+I/O Offset 0Ch[0] = 0 enables the PME to generate an SMI. In addition, the selected GPIO must be enabled as an input (F0BAR0+I/O Offset 20h and 24h).</p> <p>The next level (third level) of SMI status is at F0BAR0+I/O 0Ch/1Ch.</p> |
| 6  | <p><b>Thermal Override SMI Status.</b> Indicates whether or not an SMI was caused by an assertion of the THRM#.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation set F0 Index 83h[4] = 1.</p>  |
| 5:4  | <b>Reserved.</b> Read as 0.   |
| 3  | <p><b>SIO PWUREQ SMI Status.</b> Indicates whether or not an SMI was caused by a power-up event from the SIO.</p> <p>0: No.<br/>1: Yes.</p> <p>A power-up event is defined as any of the following events/activities:</p> <ul style="list-style-type: none"> <li>— RI2#</li> <li>— SDATA_IN2</li> <li>— IRRX1 (CEIR)</li> </ul> <p>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[0] = 0.</p>  |

**Table 6-29. F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support (Continued)**

| Bit                     | Description  |
|-------------------------|--|
| 2                       | <p><b>Codec SDATA_IN SMI Status.</b> Indicates whether or not an SMI was caused by AC97 Codec producing a positive edge on SDATA_IN.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 80h[5] = 1.</p>                                 |
| 1                       | <p><b>RTC Alarm (IRQ8#) SMI Status.</b> Indicates whether or not an SMI was caused by an RTC interrupt.</p> <p>0: No.<br/>1: Yes.</p> <p>This SMI event can only occur while in 3V Suspend and an RTC interrupt occurs and F1BAR1+I/O Offset 0Ch[0] = 0.</p> |
| 0                       | <p><b>ACPI Timer SMI Status.</b> Indicates whether or not an SMI was caused by an ACPI Timer (F1BAR0+I/O Offset 1Ch or F1BAR1+I/O Offset 1Ch) MSB toggle.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 83h[5] = 1.</p>            |
| <b>Index F8h-FFh</b>    |  |
| <b>Reserved</b>         |  |
| <b>Reset Value: 00h</b> |  |

### 6.4.1.1 GPIO Support Registers

F0 Index 10h, Base Address Register 0 (F0BAR0) points to the base address of where the GPIO runtime and configuration registers are located. Table 6-29 gives the bit formats of I/O mapped registers accessed through F0BAR0.

**Table 6-30. F0BAR0+I/O Offset: GPIO Configuration Registers**

| Bit   | Description   |
|---|---|
| <b>Offset 00h-03h</b> <b>GPDO0 — GPIO Data Out 0 Register (R/W)</b> <b>Reset Value: FFFFFFFh</b>          |   |
| 31:0  | <p><b>GPIO Data Out.</b> Bits [31:0] of this register correspond to GPIO31-GPIO0 signals, respectively. The value of each bit determines the value driven on the corresponding GPIO signal when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPIO Configuration register Lock bit (F0BAR0+I/O Offset 24h[3]). Reading the bit returns the value, regardless of the signal value and configuration.</p> <p>0: Corresponding GPIO signal is driven to low when output enabled.<br/>1: Corresponding GPIO signal is driven or released to high (according to buffer type and static pull-up selection) when output is enabled.</p>  |
| <b>Offset 04h-07h</b> <b>GPDI0 — GPIO Data In 0 Register (RO)</b> <b>Reset Value: FFFFFFFh</b>            |   |
| 31:0  | <p><b>GPIO Data In.</b> Bits [31:0] of this register correspond to GPIO31-GPIO0 signals, respectively. Reading each bit returns the value of the corresponding GPIO signal, regardless of the signal configuration and the GPDO0 register (F0BAR0+I/O Offset 00h) value.</p> <p>Writes to this register are ignored.</p> <p>0: Corresponding GPIO signal level is low.<br/>1: Corresponding GPIO signal level is high.</p>  |
| <b>Offset 08h-0Bh</b> <b>GPIEN0 — GPIO Interrupt Enable 0 Register (R/W)</b> <b>Reset Value: 0000000h</b> |   |
| 31:16   | <b>Reserved.</b> Must be set to 0.  |
| 15:0  | <p><b>GPIO Power Management Event (PME) Enable.</b> Bits [15:0] correspond to GPIO15-GPIO0 signals, respectively. Each bit allows PME generation by the corresponding GPIO signal.</p> <p>0: Disable PME generation.<br/>1: Enable PME generation.</p> <p><b>Notes:</b> 1) All of the enabled GPIO PMEs are always reported at F1BAR1+I/O Offset 10h[3].<br/>2) Any enabled GPIO PME can be selected to generate an SCI or SMI at F1BAR1+I/O Offset 0Ch[0].<br/>If SCI is selected, then the individually selected GPIO PMEs are globally enabled for SCI generation at F1BAR1+I/O Offset 12h[3] and the status is reported at F1BAR1+I/O Offset 10h[3].<br/>If SMI is selected, the individually selected GPIO PMEs generate an SMI and the status is reported at F1BAR0+I/O Offset 00h/02h[0].</p>  |
| <b>Offset 0Ch-0Fh</b> <b>GPST0 — GPIO Status 0 Register (R/W1C)</b> <b>Reset Value: 0000000h</b>          |   |
| 31:16   | <b>Reserved.</b> Must be set to 0.  |
| 15:0  | <p><b>GPIO Status.</b> Bits [15:0] correspond to GPIO15-GPIO0 signals, respectively. Each bit reports a 1 when hardware detects the edge (rising/falling on the GPIO signal) that is programmed in F0BAR0+I/O Offset 24h[5]. If the corresponding bit in F0BAR0+I/O Offset 08h is set, this edge generates a PME.</p> <p>0: No active edge detected since the bit was last cleared.<br/>1: Active edge detected.</p> <p>Writing 1 to the a Status bit clears it to 0.</p> <p>This is the third level of SMI status reporting to the second level at F0 Index 87h/F7h[7] and the top level at F1BAR0+I/O Offset 00h/02h[0]. Clearing the third level also clears the second and top levels.</p> <p>This is the second level of SCI status reporting to the top level at F1BAR1+Offset 10h[3]. The status must be cleared at both the this level and the top level (i.e., the top level is not automatically cleared when a bit in this register is cleared).</p> |



Table 6-30. F0BAR0+I/O Offset: GPIO Configuration Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 10h-13h</b> <b>GPDO1 — GPIO Data Out 1 Register (R/W)</b> <b>Reset Value: FFFFFFFFh</b>         |   |
| 31:0  | <p><b>GPIO Data Out.</b> Bits [31:0] of this register correspond to GPIO63-GPIO32 signals, respectively. The value of each bit determines the value driven on the corresponding GPIO signal when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPIO Configuration register Lock bit (F0BAR0+I/O Offset 24h[3]). Reading the bit returns the value, regardless of the signal value and configuration.</p> <p>0: Corresponding GPIO signal driven to low when output enabled.</p> <p>1: Corresponding GPIO signal driven or released to high (according to buffer type and static pull-up selection) when output enabled.</p>   |
| <b>Offset 14h-17h</b> <b>GPDI1 — GPIO Data In 1 Register (RO)</b> <b>Reset Value: FFFFFFFFh</b>           |   |
| 31:0  | <p><b>GPIO Data In.</b> Bits [31:0] of this register correspond to GPIO63-GPIO32 signals, respectively. Reading each bit returns the value of the corresponding GPIO signal, regardless of the signal configuration and the GPDO1 register (F0BAR0+I/O Offset 10h) value. Writes to this register are ignored.</p> <p>0: Corresponding GPIO signal level low.</p> <p>1: Corresponding GPIO signal level high.</p>   |
| <b>Offset 18h-1Bh</b> <b>GPIEN1 — GPIO Interrupt Enable 1 Register (R/W)</b> <b>Reset Value: 0000000h</b> |   |
| 31:16   | <b>Reserved.</b> Must be set to 0.  |
| 15:0  | <p><b>GPIO Power Management Event (PME) Enable.</b> Bits [15:0] of this register correspond to GPIO47-GPIO32 signals, respectively. Each bit allows PME generation by the corresponding GPIO signal.</p> <p>0: Disable PME generation.</p> <p>1: Enable PME generation.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1) All of the enabled GPIO PMEs are always reported at F1BAR1+I/O Offset 10h[3].</li> <li>2) Any enabled GPIO PME can be selected to generate an SCI or SMI at F1BAR1+I/O Offset 0Ch[0].</li> </ol> <p>If SCI is selected, the individually selected GPIO PMEs are globally enabled for SCI generation at F1BAR1+I/O Offset 12h[3] and the status is reported at F1BAR1+I/O Offset 10h[3].</p> <p>If SMI is selected, the individually selected GPIO PMEs generate an SMI and the status is reported at F1BAR0+I/O Offset 00h/02h[0].</p>   |
| <b>Offset 1Ch-1Fh</b> <b>GPST1 — GPIO Status 1 Register (R/W1C)</b> <b>Reset Value: 0000000h</b>          |   |
| 31:16   | <b>Reserved.</b> Must be set to 0.  |
| 15:0  | <p><b>GPIO Status.</b> Bits [15:0] correspond to GPIO47-GPIO32 signals, respectively. Each bit reports a 1 when hardware detects the edge (rising/falling on the GPIO signal) that is programmed in F0BAR0+I/O Offset 24h[5]. If the corresponding bit in F0BAR0+I/O Offset 18h is set, this edge generates a PME.</p> <p>0: No active edge detected since the bit was last cleared.</p> <p>1: Active edge detected.</p> <p>Writing 1 to the a Status bit clears it to 0.</p> <p>This is the third level of SMI status reporting to the second level at F0 Index 87h/F7h[7] and the top level at F1BAR0+I/O Offset 00h/02h[0]. Clearing the third level also clears the second and top levels.</p> <p>This is the second level of SCI status reporting to the top level at F1BAR1+Offset 10h[3]. The status must be cleared at both the this level and the top level (i.e., the top level is not automatically cleared when a bit in this register is cleared).</p> |
| <b>Offset 20h-23h</b> <b>GPIO Signal Configuration Select Register (R/W)</b> <b>Reset Value: 0000000h</b> |   |
| 31:6  | <b>Reserved.</b> Must be set to 0.  |

**Table 6-30. F0BAR0+I/O Offset: GPIO Configuration Registers (Continued)**

| Bit  | Description   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
|--|---|---|--|--|--|----------------|---|----------------|---|----------------|--|----------------|-----------------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|---|-----------------|---|-----------------|--|-----------------|--|-----------------|---|-----------------|---|-----------------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|---|-----------------|---|-----------------|---|-----------------|---|-----------------|--|-----------------|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|
| 5:0  | <p><b>Signal Select.</b> Selects the GPIO signal to be configured in the Bank selected via bit 5 setting (i.e., Bank 0 or Bank 1). See Table 4-2 on page 88 for GPIO ball muxing options. GPIOs without an associated ball number are not available externally.</p> <p><b>Bank 0</b></p> <table> <tbody> <tr> <td>000000 = GPIO0 (EBGA: H1 / TEPBGA: D11)</td> <td>010000 = GPIO16 (EBGA: AL15 / TEPBGA: V31)</td> </tr> <tr> <td>000001 = GPIO1 (EBGA: H2, AL12 / TEPBGA: D10, N30)</td> <td>010001 = GPIO17 (EBGA: J4 / TEPBGA: A10)</td> </tr> <tr> <td>000010 = GPIO2</td> <td>010010 = GPIO18 (EBGA: A28 / TEPBGA: AG1)</td> </tr> <tr> <td>000011 = GPIO3</td> <td>010011 = GPIO19 (EBGA: H4 / TEPBGA: C9)</td> </tr> <tr> <td>000100 = GPIO4</td> <td>010100 = GPIO20 (EBGA: H3, AJ13 / TEPBGA: A9, N31)</td> </tr> <tr> <td>000101 = GPIO5</td> <td>010101 = GPIO21</td> </tr> <tr> <td>000110 = GPIO6 (EBGA: AH3 / TEPBGA: D28)</td> <td>010110 = GPIO22</td> </tr> <tr> <td>000111 = GPIO7 (EBGA: AH4 / TEPBGA: C30)</td> <td>010111 = GPIO23</td> </tr> <tr> <td>001000 = GPIO8 (EBGA: AJ2 / TEPBGA: C31)</td> <td>011000 = GPIO24</td> </tr> <tr> <td>001001 = GPIO9 (EBGA: AG4 / TEPBGA: C28)</td> <td>011001 = GPIO25</td> </tr> <tr> <td>001010 = GPIO10 (EBGA: AJ1 / TEPBGA: B29)</td> <td>011010 = GPIO26</td> </tr> <tr> <td>001011 = GPIO11 (EBGA: H30 / TEPBGA: AJ8)</td> <td>011011 = GPIO27</td> </tr> <tr> <td>001100 = GPIO12 (EBGA: AJ12 / TEPBGA: N29)</td> <td>011100 = GPIO28</td> </tr> <tr> <td>001101 = GPIO13 (EBGA: AL11 / TEPBGA: M29)</td> <td>011101 = GPIO29</td> </tr> <tr> <td>001110 = GPIO14 (EBGA: F1 / TEPBGA: D9)</td> <td>011110 = GPIO30</td> </tr> <tr> <td>001111 = GPIO15 (EBGA: G3 / TEPBGA: A8)</td> <td>011111 = GPIO31</td> </tr> </tbody> </table> <p><b>Bank 1</b></p> <table> <tbody> <tr> <td>100000 = GPIO32 (EBGA: AJ11 / TEPBGA: M28)</td> <td>110000 = GPIO48</td> </tr> <tr> <td>100001 = GPIO33 (EBGA: AL10 / TEPBGA: L31)</td> <td>110001 = GPIO49</td> </tr> <tr> <td>100010 = GPIO34 (EBGA: AK10 / TEPBGA: L30)</td> <td>110010 = GPIO50</td> </tr> <tr> <td>100011 = GPIO35 (EBGA: AJ10 / TEPBGA: L29)</td> <td>110011 = GPIO51</td> </tr> <tr> <td>100100 = GPIO36 (EBGA: AL9 / TEPBGA: L28)</td> <td>110100 = GPIO52</td> </tr> <tr> <td>100101 = GPIO37 (EBGA: AK9 / TEPBGA: K31)</td> <td>110101 = GPIO53</td> </tr> <tr> <td>100110 = GPIO38 (EBGA: AJ9 / TEPBGA: K28)</td> <td>110110 = GPIO54</td> </tr> <tr> <td>100111 = GPIO39 (EBGA: AL8 / TEPBGA: J31)</td> <td>110111 = GPIO55</td> </tr> <tr> <td>101000 = GPIO40 (EBGA: A21 / TEPBGA: Y3)</td> <td>111000 = GPIO56</td> </tr> <tr> <td>101001 = GPIO41 (EBGA: C19 / TEPBGA: W4)</td> <td>111001 = GPIO57</td> </tr> <tr> <td>101010 = GPIO42</td> <td>111010 = GPIO58</td> </tr> <tr> <td>101011 = GPIO43</td> <td>111011 = GPIO59</td> </tr> <tr> <td>101100 = GPIO44</td> <td>111100 = GPIO60</td> </tr> <tr> <td>101101 = GPIO45</td> <td>111101 = GPIO61</td> </tr> <tr> <td>101110 = GPIO46</td> <td>111110 = GPIO62</td> </tr> <tr> <td>101111 = GPIO47</td> <td>111111 = GPIO63 (Note)</td> </tr> </tbody> </table> <p><b>Note:</b> GPIO63 can be used to generate the PWRBTN# input signal. See PWRBTN# signal description in Section 3.4.15 "Power Management Interface Signals" on page 80.</p> | 000000 = GPIO0 (EBGA: H1 / TEPBGA: D11) | 010000 = GPIO16 (EBGA: AL15 / TEPBGA: V31) | 000001 = GPIO1 (EBGA: H2, AL12 / TEPBGA: D10, N30) | 010001 = GPIO17 (EBGA: J4 / TEPBGA: A10) | 000010 = GPIO2 | 010010 = GPIO18 (EBGA: A28 / TEPBGA: AG1) | 000011 = GPIO3 | 010011 = GPIO19 (EBGA: H4 / TEPBGA: C9) | 000100 = GPIO4 | 010100 = GPIO20 (EBGA: H3, AJ13 / TEPBGA: A9, N31) | 000101 = GPIO5 | 010101 = GPIO21 | 000110 = GPIO6 (EBGA: AH3 / TEPBGA: D28) | 010110 = GPIO22 | 000111 = GPIO7 (EBGA: AH4 / TEPBGA: C30) | 010111 = GPIO23 | 001000 = GPIO8 (EBGA: AJ2 / TEPBGA: C31) | 011000 = GPIO24 | 001001 = GPIO9 (EBGA: AG4 / TEPBGA: C28) | 011001 = GPIO25 | 001010 = GPIO10 (EBGA: AJ1 / TEPBGA: B29) | 011010 = GPIO26 | 001011 = GPIO11 (EBGA: H30 / TEPBGA: AJ8) | 011011 = GPIO27 | 001100 = GPIO12 (EBGA: AJ12 / TEPBGA: N29) | 011100 = GPIO28 | 001101 = GPIO13 (EBGA: AL11 / TEPBGA: M29) | 011101 = GPIO29 | 001110 = GPIO14 (EBGA: F1 / TEPBGA: D9) | 011110 = GPIO30 | 001111 = GPIO15 (EBGA: G3 / TEPBGA: A8) | 011111 = GPIO31 | 100000 = GPIO32 (EBGA: AJ11 / TEPBGA: M28) | 110000 = GPIO48 | 100001 = GPIO33 (EBGA: AL10 / TEPBGA: L31) | 110001 = GPIO49 | 100010 = GPIO34 (EBGA: AK10 / TEPBGA: L30) | 110010 = GPIO50 | 100011 = GPIO35 (EBGA: AJ10 / TEPBGA: L29) | 110011 = GPIO51 | 100100 = GPIO36 (EBGA: AL9 / TEPBGA: L28) | 110100 = GPIO52 | 100101 = GPIO37 (EBGA: AK9 / TEPBGA: K31) | 110101 = GPIO53 | 100110 = GPIO38 (EBGA: AJ9 / TEPBGA: K28) | 110110 = GPIO54 | 100111 = GPIO39 (EBGA: AL8 / TEPBGA: J31) | 110111 = GPIO55 | 101000 = GPIO40 (EBGA: A21 / TEPBGA: Y3) | 111000 = GPIO56 | 101001 = GPIO41 (EBGA: C19 / TEPBGA: W4) | 111001 = GPIO57 | 101010 = GPIO42 | 111010 = GPIO58 | 101011 = GPIO43 | 111011 = GPIO59 | 101100 = GPIO44 | 111100 = GPIO60 | 101101 = GPIO45 | 111101 = GPIO61 | 101110 = GPIO46 | 111110 = GPIO62 | 101111 = GPIO47 | 111111 = GPIO63 (Note) |
| 000000 = GPIO0 (EBGA: H1 / TEPBGA: D11)            | 010000 = GPIO16 (EBGA: AL15 / TEPBGA: V31)  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000001 = GPIO1 (EBGA: H2, AL12 / TEPBGA: D10, N30) | 010001 = GPIO17 (EBGA: J4 / TEPBGA: A10)  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000010 = GPIO2                                     | 010010 = GPIO18 (EBGA: A28 / TEPBGA: AG1)   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000011 = GPIO3                                     | 010011 = GPIO19 (EBGA: H4 / TEPBGA: C9)   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000100 = GPIO4                                     | 010100 = GPIO20 (EBGA: H3, AJ13 / TEPBGA: A9, N31)  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000101 = GPIO5                                     | 010101 = GPIO21   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000110 = GPIO6 (EBGA: AH3 / TEPBGA: D28)           | 010110 = GPIO22   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 000111 = GPIO7 (EBGA: AH4 / TEPBGA: C30)           | 010111 = GPIO23   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001000 = GPIO8 (EBGA: AJ2 / TEPBGA: C31)           | 011000 = GPIO24   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001001 = GPIO9 (EBGA: AG4 / TEPBGA: C28)           | 011001 = GPIO25   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001010 = GPIO10 (EBGA: AJ1 / TEPBGA: B29)          | 011010 = GPIO26   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001011 = GPIO11 (EBGA: H30 / TEPBGA: AJ8)          | 011011 = GPIO27   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001100 = GPIO12 (EBGA: AJ12 / TEPBGA: N29)         | 011100 = GPIO28   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001101 = GPIO13 (EBGA: AL11 / TEPBGA: M29)         | 011101 = GPIO29   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001110 = GPIO14 (EBGA: F1 / TEPBGA: D9)            | 011110 = GPIO30   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 001111 = GPIO15 (EBGA: G3 / TEPBGA: A8)            | 011111 = GPIO31   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100000 = GPIO32 (EBGA: AJ11 / TEPBGA: M28)         | 110000 = GPIO48   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100001 = GPIO33 (EBGA: AL10 / TEPBGA: L31)         | 110001 = GPIO49   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100010 = GPIO34 (EBGA: AK10 / TEPBGA: L30)         | 110010 = GPIO50   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100011 = GPIO35 (EBGA: AJ10 / TEPBGA: L29)         | 110011 = GPIO51   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100100 = GPIO36 (EBGA: AL9 / TEPBGA: L28)          | 110100 = GPIO52   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100101 = GPIO37 (EBGA: AK9 / TEPBGA: K31)          | 110101 = GPIO53   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100110 = GPIO38 (EBGA: AJ9 / TEPBGA: K28)          | 110110 = GPIO54   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 100111 = GPIO39 (EBGA: AL8 / TEPBGA: J31)          | 110111 = GPIO55   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101000 = GPIO40 (EBGA: A21 / TEPBGA: Y3)           | 111000 = GPIO56   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101001 = GPIO41 (EBGA: C19 / TEPBGA: W4)           | 111001 = GPIO57   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101010 = GPIO42                                    | 111010 = GPIO58   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101011 = GPIO43                                    | 111011 = GPIO59   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101100 = GPIO44                                    | 111100 = GPIO60   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101101 = GPIO45                                    | 111101 = GPIO61   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101110 = GPIO46                                    | 111110 = GPIO62   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 101111 = GPIO47                                    | 111111 = GPIO63 (Note)  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| <b>Offset 24h-27h</b>                              | <p align="center"><b>GPIO Signal Configuration Access Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000044h</b></span></p> <p>This register is used to indicate configuration for the GPIO signal that is selected in the GPIO Signal Configuration Select Register (above).</p> <p><b>Note:</b> PME debouncing, polarity, and edge/level configuration is only applicable on GPIO0-GPIO15 signals (Bank 0 = 00000 to 01111) and on GPIO32-GPIO47 signals (Bank 1 settings of 00000 to 01111). The remaining GPIOs (GPIO16-GPIO31 and GPIO48-GPIO63) can not generate PMEs, therefore these bits have no function and read 0.</p>   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 31:7   | <b>Reserved.</b> Must be set to 0.  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 6  | <p><b>PME Debounce Enable.</b> Enables/disables IRQ debounce (debounce period = 16 ms).</p> <p>0: Disable.</p> <p>1: Enable. (Default).</p> <p>See the note in the description of this register for more information about the default value of this bit.</p>   |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |
| 5  | <p><b>PME Polarity.</b> Selects the polarity of the signal that issues a PME from the selected GPIO signal (falling/low or rising/high).</p> <p>0: Falling edge or low level input. (Default)</p> <p>1: Rising edge or high level input.</p> <p>See the note in the description of this register for more information about the default value of this bit.</p>  |   |  |  |  |                |   |                |   |                |  |                |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |   |                 |   |                 |  |                 |  |                 |  |                 |  |                 |   |                 |   |                 |   |                 |   |                 |  |                 |  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                        |

Table 6-30. F0BAR0+I/O Offset: GPIO Configuration Registers (Continued)

| Bit                                      | Description  |
|--|--|
| 4  | <p><b>PME Edge/Level Select.</b> Selects the type (edge or level) of the signal that issues a PME from the selected GPIO signal.</p> <p>0: Edge input. (Default)</p> <p>1: Level input.</p> <p>For normal operation, always set this bit to 0 (edge input). Erratic system behavior results if this bit is set to 1.</p> <p>See the note in the description of this register for more information about the default value of this bit.</p> |
| 3  | <p><b>Lock.</b> This bit locks the selected GPIO signal. Once this bit is set to 1 by software, it can only be cleared to 0 by power on reset or by WATCHDOG reset.</p> <p>0: No effect. (Default)</p> <p>1: Direction, output type, pull-up and output value locked.</p>  |
| 2  | <p><b>Pull-Up Control.</b> Enables/disables the internal pull-up capability of the selected GPIO signal. It supports open-drain output signals with internal pull-ups and TTL input signals.</p> <p>0: Disable.</p> <p>1: Enable. (Default)</p> <p>Bits [1:0] of this register must = 01 for this bit to have effect.</p>  |
| 1  | <p><b>Output Type.</b> Controls the output buffer type (open-drain or push-pull) of the selected GPIO signal.</p> <p>0: Open-drain. (Default)</p> <p>1: Push-pull.</p> <p>Bit 0 of this register must be set to 1 for this bit to have effect.</p>   |
| 0  | <p><b>Output Enable.</b> Indicates the GPIO signal output state. It has no effect on input.</p> <p>0: TRI-STATE - Setting for GPIO to function as an input only. (Default)</p> <p>1: Output enabled.</p>   |
| <b>Offset 28h-2Bh</b>                    |  |
| <b>GPIO Reset Control Register (R/W)</b> |  |
| <b>Reset Value: 0000000h</b>             |  |
| 31:1                                     | <b>Reserved.</b> Must be set to 0.   |
| 0  | <p><b>GPIO Reset.</b> Reset the GPIO logic.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>Write 0 to clear.</p> <p>This bit is level-sensitive and must be cleared after the reset is enabled (normal operation requires this bit to be 0).</p>  |

### 6.4.1.2 LPC Support Registers

F0 Index 14h, Base Address Register 1 (F0BAR1) points to the base address of the register space that contains the configuration registers for LPC support. Table 6-31 gives the bit formats of the I/O mapped registers accessed through F0BAR1.

The LPC Interface supports all features described in the LPC bus specification 1.0, with the following exceptions:

- Only 8- or 16-bit DMA, depending on channel number. Does not support the optional larger transfer sizes.
- Only one external DRQ pin.

**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers**

| Bit   | Description   |
|---|---|
| <b>Offset 00h-03h</b> <b>SERIRQ_SRC — Serial IRQ Source Register (R/W)</b> <b>Reset Value: 0000000h</b><br><b>Note:</b> Some signals require additional programming to make them externally accessible. See Table 4-2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88 for pin multiplexing details and Table 3-6 "Strap Options" on page 58 for LPC_ROM strap information. |   |
| 31:21   | <b>Reserved.</b>  |
| 20  | <b>INTD Source.</b> Selects the interface source of the INTD# signal.<br>0: PCI - INTD# (EBGA ball B22; TEPBGA ball AA2).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).  |
| 19  | <b>INTC Source.</b> Selects the interface source of the INTC# signal.<br>0: PCI - INTC# (EBGA ball H4; TEPBGA ball C9).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).  |
| 18  | <b>INTB Source.</b> Selects the interface source of the INTB# signal.<br>0: PCI - INTB# (EBGA ball AF1; TEPBGA ball C26).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).  |
| 17  | <b>INTA Source.</b> Selects the interface source of the INTA# signal.<br>0: PCI - INTA# (EBGA ball AE3; TEPBGA ball D26).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).  |
| 16  | <b>Reserved.</b> Set to 0.  |
| 15  | <b>IRQ15 Source.</b> Selects the interface source of the IRQ15 signal.<br>0: ISA - IRQ15 (EBGA ball H30; TEPBGA ball AJ8).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 14  | <b>IRQ14 Source.</b> Selects the interface source of the IRQ14 signal.<br>0: ISA - IRQ14 (EBGA ball D25; TEPBGA ball AF1).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 13  | <b>IRQ13 Source.</b> Selects the interface source of the internal IRQ13 signal.<br>0: ISA - IRQ13 internal signal. (An input from the CPU indicating that a floating point error has been detected and that internal INTR should be asserted.)<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31). |
| 12  | <b>IRQ12 Source.</b> Selects the interface source of the IRQ12 signal.<br>0: ISA - IRQ12 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 11  | <b>IRQ11 Source.</b> Selects the interface source of the IRQ11 signal.<br>0: ISA - IRQ11 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 10  | <b>IRQ10 Source.</b> Selects the interface source of the IRQ10 signal.<br>0: ISA - IRQ10 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 9   | <b>IRQ9 Source.</b> Selects the interface source of the IRQ9 signal.<br>0: ISA - IRQ9 (EBGA ball C22; TEPBGA ball AA3).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).  |

**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)**

| Bit   | Description  |
|---|--|
| 8   | <b>IRQ8# Source.</b> Selects the interface source of the IRQ8# signal.<br>0: ISA - IRQ8# internal signal. (Connected to internal RTC.)<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).                              |
| 7   | <b>IRQ7 Source.</b> Selects the interface source of the IRQ7 signal.<br>0: ISA - IRQ7 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 6   | <b>IRQ6 Source.</b> Selects the interface source of the IRQ6 signal.<br>0: ISA - IRQ6 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 5   | <b>IRQ5 Source.</b> Selects the interface source of the IRQ5 signal.<br>0: ISA - IRQ5 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 4   | <b>IRQ4 Source.</b> Selects the interface source of the IRQ4 signal.<br>0: ISA - IRQ4 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 3   | <b>IRQ3 Source.</b> Selects the interface source of the IRQ3 signal.<br>0: ISA - IRQ3 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 2   | <b>Reserved.</b> Must be set to 0.   |
| 1   | <b>IRQ1 Source.</b> Selects the interface source of the IRQ1 signal.<br>0: ISA - IRQ1 (unavailable externally).<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31).   |
| 0   | <b>IRQ0 Source.</b> Selects the interface source of the IRQ0 signal.<br>0: ISA - IRQ0 Internal signal. (Connected to OUT0, System Timer, of the internal 8254 PIT.)<br>1: LPC - SERIRQ (EBGA ball AL8; TEPBGA ball J31). |
| <b>Offset 04h-07h SERIRQ_LVL — Serial IRQ Level Control Register (R/W) Reset Value: 00000000h</b> |  |
| 31:21   | <b>Reserved.</b>   |
| 20  | <b>INTD# Polarity.</b> If LPC is selected as the interface source for INTD# (F0BAR1+I/O Offset 00h[20] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.                             |
| 19  | <b>INTC# Polarity.</b> If LPC is selected as the interface source for INTC# (F0BAR1+I/O Offset 00h[19] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.                             |
| 18  | <b>INTB# Polarity.</b> If LPC is selected as the interface source for INTB# (F0BAR1+I/O Offset 00h[18] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.                             |
| 17  | <b>INTA# Polarity.</b> If LPC is selected as the interface source for INTA# (F0BAR1+I/O Offset 00h[17] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.                             |
| 16  | <b>Reserved.</b> Must be set to 0.   |
| 15  | <b>IRQ15 Polarity.</b> If LPC is selected as the interface source for IRQ15 (F0BAR1+I/O Offset 00h[15] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.                             |

**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)**

| Bit | Description  |
|-----|--|
| 14  | <b>IRQ14 Polarity.</b> If LPC is selected as the interface source for IRQ14 (F0BAR1+I/O Offset 00h[14] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low. |
| 13  | <b>IRQ13 Polarity.</b> If LPC is selected as the interface source for IRQ13 (F0BAR1+I/O Offset 00h[13] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low. |
| 12  | <b>IRQ12 Polarity.</b> If LPC is selected as the interface source for IRQ12 (F0BAR1+I/O Offset 00h[12] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low. |
| 11  | <b>IRQ11 Polarity.</b> If LPC is selected as the interface source for IRQ11 (F0BAR1+I/O Offset 00h[11] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low. |
| 10  | <b>IRQ10 Polarity.</b> If LPC is selected as the interface source for IRQ10 (F0BAR1+I/O Offset 00h[10] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low. |
| 9   | <b>IRQ9 Polarity.</b> If LPC is selected as the interface source for IRQ9 (F0BAR1+I/O Offset 00h[9] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |
| 8   | <b>IRQ8# Polarity.</b> If LPC is selected as the interface source for IRQ8# (F0BAR1+I/O Offset 00h[8] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.  |
| 7   | <b>IRQ7 Polarity.</b> If LPC is selected as the interface source for IRQ7 (F0BAR1+I/O Offset 00h[7] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |
| 6   | <b>IRQ6 Polarity.</b> If LPC is selected as the interface source for IRQ6 (F0BAR1+I/O Offset 00h[6] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |
| 5   | <b>IRQ5 Polarity.</b> If LPC is selected as the interface source for IRQ5 (F0BAR1+I/O Offset 00h[5] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |
| 4   | <b>IRQ4 Polarity.</b> If LPC is selected as the interface source for IRQ4 (F0BAR1+I/O Offset 00h[4] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |
| 3   | <b>IRQ3 Polarity.</b> If LPC is selected as the interface source for IRQ3 (F0BAR1+I/O Offset 00h[3] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.    |

**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)**

| Bit   | Description   |
|---|---|
| 2   | <b>SMI# Polarity.</b> This bit allows signal polarity selection of the SMI# generated from LPC.<br>0: Active high.<br>1: Active low.  |
| 1   | <b>IRQ1 Polarity.</b> If LPC is selected as the interface source for IRQ1 (F0BAR1+I/O Offset 00h[1] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.   |
| 0   | <b>IRQ0 Polarity.</b> If LPC is selected as the interface source for IRQ0 (F0BAR1+I/O Offset 00h[0] = 1), this bit allows signal polarity selection.<br>0: Active high.<br>1: Active low.   |
| <b>Offset 08h-0Bh SERIRQ_CNT — Serial IRQ Control Register (R/W) Reset Value: 00000000h</b>   |   |
| 31:8  | <b>Reserved.</b>  |
| 7   | <b>Serial IRQ Enable.</b><br>0: Disable.<br>1: Enable.  |
| 6   | <b>Serial IRQ Interface Mode.</b><br>0: Continuous.<br>1: Quiet.  |
| 5:2   | <b>Number of IRQ Data Frames.</b><br>0000: 17 frames      0100: 21 frames      1000: 25 frames      1100: 29 frames<br>0001: 18 frames      0101: 22 frames      1001: 26 frames      1101: 30 frames<br>0010: 19 frames      0110: 23 frames      1010: 27 frames      1110: 31 frames<br>0011: 20 frames      0111: 24 frames      1011: 28 frames      1111: 32 frames |
| 1:0   | <b>Start Frame Pulse Width.</b><br>00: 4 Clocks<br>01: 6 Clocks<br>10: 8 Clocks<br>11: Reserved   |
| <b>Offset 0Ch-0Fh DRQ_SRC — DRQ Source Register (R/W) Reset Value: 00000000h</b>  |   |
| <b>Note:</b> DRQx are internal signals between the Core Logic and SuperI/O modules. Some signals require additional programming to make them externally accessible. See Table 4-2 "Multiplexing, Interrupt Selection, and Base Address Registers" on page 88 for pin multiplexing details and Table 3-6 "Strap Options" on page 58 for LPC_ROM strap information. |   |
| 31:8  | <b>Reserved.</b>  |
| 7   | <b>DRQ7 Source.</b> Selects the interface source of the DRQ7 signal.<br>0: ISA - DRQ7 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| 6   | <b>DRQ6 Source.</b> Selects the interface source of the DRQ6 signal.<br>0: ISA - DRQ6 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| 5   | <b>DRQ5 Source.</b> Selects the interface source of the DRQ5 signal.<br>0: ISA - DRQ5 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| 4   | <b>LPC BM0 Cycles.</b> Allow LPC Bus Master 0 Cycles.<br>0: Enable.<br>1: Disable.  |
| 3   | <b>DRQ3 Source.</b> Selects the interface source of the DRQ3 signal.<br>0: ISA - DRQ3 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |

Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| 2  | <b>DRQ2 Source.</b> Selects the interface source of the DRQ2 signal.<br>0: ISA - DRQ2 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| 1  | <b>DRQ1 Source.</b> Selects the interface source of the DRQ1 signal.<br>0: ISA - DRQ1 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| 0  | <b>DRQ0 Source.</b> Selects the interface source of the DRQ0 signal.<br>0: ISA - DRQ0 (unavailable externally).<br>1: LPC - LDRQ# (EBGA ball AL9; TEPBGA ball L28).   |
| <b>Offset 10h-13h LAD_EN — LPC Address Enable Register (R/W) Reset Value: 0000000h</b> |   |
| 31:18  | <b>Reserved.</b>  |
| 17   | <b>LPC RTC.</b> RTC addresses I/O Ports 070h-073h. See bit 16 for decode.   |
| 16   | <b>LPC/ISA Default Mapping.</b> Works in conjunction with bits 17 and [14:0] of this register to enable mapping of specific peripherals to LPC or internal ISA interfaces.<br>If bit [x] = 0 and bit 16 = 0 then: Transaction routed to internal ISA bus.<br>If bit [x] = 0 and bit 16 = 1 then: Transaction routed to LPC interface.<br>If bit [x] = 1 and bit 16 = 0 then: Transaction routed to LPC interface.<br>If bit [x] = 1 and bit 16 = 1 then: Transaction routed to internal ISA bus.<br>Bit [x] is defined as bits 17 and [14:0]. |
| 15   | <b>LPC ROM Addressing.</b> Depends upon F0 Index 52h[2,0].<br>0: Disable.<br>1: Enable.   |
| 14   | <b>LPC Alternate SuperI/O Addressing.</b> Alternate SuperI/O control addresses 4Eh-4Fh. See bit 16 for decode.  |
| 13   | <b>LPC SuperI/O Addressing.</b> SuperI/O control addresses I/O Ports 2Eh-2Fh. See bit 16 for decode.<br><b>Note:</b> This bit should not be routed to LPC when using the internal SuperI/O module and if IO_SIOCFG_IN (F5BAR0+I/O Offset 00h[26:25]) = 10.  |
| 12   | <b>LPC Ad-Lib Addressing.</b> Ad-Lib addresses I/O Ports 388h-389h. See bit 16 for decode.  |
| 11   | <b>LPC ACPI Addressing.</b> ACPI microcontroller addresses I/O Ports 62h and 66h. See bit 16 for decode.  |
| 10   | <b>LPC Keyboard Controller Addressing.</b> KBC addresses I/O Ports 60h and 64h.<br><b>Note:</b> If this bit = 0 and bit 16 = 1, then F0 Index 5Ah[1] must be written 0.   |
| 9  | <b>LPC Wide Generic Addressing.</b> Wide generic addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 18h[15:9]<br><b>Note:</b> The selected range must not overlap any address range that is positively decoded by F0BAR1+I/O Offset 10h bits [17], [14:10], and [8:0].   |
| 8  | <b>LPC Game Port 1 Addressing.</b> Game Port 1 addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[22:19]   |
| 7  | <b>LPC Game Port 0 Addressing.</b> Game Port 0 addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[18:15].  |
| 6  | <b>LPC Floppy Disk Controller Addressing.</b> FDC addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[14]   |
| 5  | <b>LPC Microsoft Sound System (MSS) Addressing.</b> MSS addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[13:12].   |
| 4  | <b>LPC MIDI Addressing.</b> MIDI addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[11:10].  |
| 3  | <b>LPC Audio Addressing.</b> Audio addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[9:8].  |
| 2  | <b>LPC Serial Port 1 Addressing.</b> Serial Port 1 addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[7:5].  |



**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)**

| Bit   | Description   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
|---|---|------------------------------------|---|------------------------------------|----------------|----------------|----------------|----------------|----------------|------------|------------|------------|------------|------------|------------|------------|------------|
| 1   | <b>LPC Serial Port 0 Addressing.</b> Serial Port 0 addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[4:2].  |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0   | <b>LPC Parallel Port Addressing.</b> Parallel Port addresses. See bit 16 for decode.<br>Address selection made via F0BAR1+I/O Offset 14h[1:0].  |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| <b>Offset 14h-17h                                      LAD_D0 — LPC Address Decode 0 Register (R/W)                                      Reset Value: 00080020h</b> |   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 31:23   | <b>Reserved.</b>  |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 22:19   | <b>LPC Game Port 1 Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>0000: 200h</td> <td>0100: 204h</td> <td>1000: 208h</td> <td>1100: 20Ch</td> </tr> <tr> <td>0001: 201h</td> <td>0101: 205h</td> <td>1001: 209h</td> <td>1101: 20Dh</td> </tr> <tr> <td>0010: 202h</td> <td>0110: 206h</td> <td>1010: 20Ah</td> <td>1110: 20Eh</td> </tr> <tr> <td>0011: 203h</td> <td>0111: 207h</td> <td>1011: 20Bh</td> <td>1111: 20Fh</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[8]. | 0000: 200h                         | 0100: 204h                                | 1000: 208h                         | 1100: 20Ch     | 0001: 201h     | 0101: 205h     | 1001: 209h     | 1101: 20Dh     | 0010: 202h | 0110: 206h | 1010: 20Ah | 1110: 20Eh | 0011: 203h | 0111: 207h | 1011: 20Bh | 1111: 20Fh |
| 0000: 200h  | 0100: 204h  | 1000: 208h                         | 1100: 20Ch                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0001: 201h  | 0101: 205h  | 1001: 209h                         | 1101: 20Dh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0010: 202h  | 0110: 206h  | 1010: 20Ah                         | 1110: 20Eh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0011: 203h  | 0111: 207h  | 1011: 20Bh                         | 1111: 20Fh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 18:15   | <b>LPC Game Port 0 Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>0000: 200h</td> <td>0100: 204h</td> <td>1000: 208h</td> <td>1100: 20Ch</td> </tr> <tr> <td>0001: 201h</td> <td>0101: 205h</td> <td>1001: 209h</td> <td>1101: 20Dh</td> </tr> <tr> <td>0010: 202h</td> <td>0110: 206h</td> <td>1010: 20Ah</td> <td>1110: 20Eh</td> </tr> <tr> <td>0011: 203h</td> <td>0111: 207h</td> <td>1011: 20Bh</td> <td>1111: 20Fh</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[7]. | 0000: 200h                         | 0100: 204h                                | 1000: 208h                         | 1100: 20Ch     | 0001: 201h     | 0101: 205h     | 1001: 209h     | 1101: 20Dh     | 0010: 202h | 0110: 206h | 1010: 20Ah | 1110: 20Eh | 0011: 203h | 0111: 207h | 1011: 20Bh | 1111: 20Fh |
| 0000: 200h  | 0100: 204h  | 1000: 208h                         | 1100: 20Ch                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0001: 201h  | 0101: 205h  | 1001: 209h                         | 1101: 20Dh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0010: 202h  | 0110: 206h  | 1010: 20Ah                         | 1110: 20Eh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 0011: 203h  | 0111: 207h  | 1011: 20Bh                         | 1111: 20Fh                                |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 14  | <b>LPC Floppy Disk Controller Address Select.</b> Selects I/O Port:<br>0: 3F0h-3F7h.<br>1: 370h-377h.<br>Selected address range is enabled via F0BAR1+I/O Offset 10h[6].  |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 13:12   | <b>LPC Microsoft Sound System (MSS) Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>00: 530h-537h</td> <td>10: E80h-E87h</td> </tr> <tr> <td>01: 604h-60Bh</td> <td>11: F40h-F47h</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[5].  | 00: 530h-537h                      | 10: E80h-E87h                             | 01: 604h-60Bh                      | 11: F40h-F47h  |                |                |                |                |            |            |            |            |            |            |            |            |
| 00: 530h-537h   | 10: E80h-E87h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 01: 604h-60Bh   | 11: F40h-F47h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 11:10   | <b>LPC MIDI Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>00: 300h-301h</td> <td>10: 320h-321h</td> </tr> <tr> <td>01: 310h-311h</td> <td>11: 330h-331h</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[4].  | 00: 300h-301h                      | 10: 320h-321h                             | 01: 310h-311h                      | 11: 330h-331h  |                |                |                |                |            |            |            |            |            |            |            |            |
| 00: 300h-301h   | 10: 320h-321h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 01: 310h-311h   | 11: 330h-331h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 9:8   | <b>LPC Audio Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>00: 220h-233h</td> <td>10: 260h-273h</td> </tr> <tr> <td>01: 240h-253h</td> <td>11: 280h-293h</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[3].   | 00: 220h-233h                      | 10: 260h-273h                             | 01: 240h-253h                      | 11: 280h-293h  |                |                |                |                |            |            |            |            |            |            |            |            |
| 00: 220h-233h   | 10: 260h-273h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 01: 240h-253h   | 11: 280h-293h   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 7:5   | <b>LPC Serial Port 1 Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>000: 3F8h-3FFh</td> <td>010: 220h-227h</td> <td>100: 238h-23Fh</td> <td>110: 338h-33Fh</td> </tr> <tr> <td>001: 2F8h-2FFh</td> <td>011: 228h-22Fh</td> <td>101: 2E8h-2EFh</td> <td>111: 3E8h-3EFh</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[2].   | 000: 3F8h-3FFh                     | 010: 220h-227h                            | 100: 238h-23Fh                     | 110: 338h-33Fh | 001: 2F8h-2FFh | 011: 228h-22Fh | 101: 2E8h-2EFh | 111: 3E8h-3EFh |            |            |            |            |            |            |            |            |
| 000: 3F8h-3FFh  | 010: 220h-227h  | 100: 238h-23Fh                     | 110: 338h-33Fh                            |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 001: 2F8h-2FFh  | 011: 228h-22Fh  | 101: 2E8h-2EFh                     | 111: 3E8h-3EFh                            |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 4:2   | <b>LPC Serial Port 0 Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>000: 3F8h-3FFh</td> <td>010: 220h-227h</td> <td>100: 238h-23Fh</td> <td>110: 338h-33Fh</td> </tr> <tr> <td>001: 2F8h-2FFh</td> <td>011: 228h-22Fh</td> <td>101: 2E8h-2EFh</td> <td>111: 3E8h-3EFh</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[1].   | 000: 3F8h-3FFh                     | 010: 220h-227h                            | 100: 238h-23Fh                     | 110: 338h-33Fh | 001: 2F8h-2FFh | 011: 228h-22Fh | 101: 2E8h-2EFh | 111: 3E8h-3EFh |            |            |            |            |            |            |            |            |
| 000: 3F8h-3FFh  | 010: 220h-227h  | 100: 238h-23Fh                     | 110: 338h-33Fh                            |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 001: 2F8h-2FFh  | 011: 228h-22Fh  | 101: 2E8h-2EFh                     | 111: 3E8h-3EFh                            |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 1:0   | <b>LPC Parallel Port Address Select.</b> Selects I/O Port:<br><table border="0"> <tr> <td>00: 378h-37Fh (+778h-77Fh for ECP)</td> <td>01: 278h-27Fh (+678h-67Fh for ECP) (Note)</td> </tr> <tr> <td>10: 3BCh-3BFh (+7BCh-7BFh for ECP)</td> <td>11: Reserved</td> </tr> </table> Selected address range is enabled via F0BAR1+I/O Offset 10h[0].<br><b>Note:</b> 279h is read only, writes are forwarded to ISA for PnP.  | 00: 378h-37Fh (+778h-77Fh for ECP) | 01: 278h-27Fh (+678h-67Fh for ECP) (Note) | 10: 3BCh-3BFh (+7BCh-7BFh for ECP) | 11: Reserved   |                |                |                |                |            |            |            |            |            |            |            |            |
| 00: 378h-37Fh (+778h-77Fh for ECP)  | 01: 278h-27Fh (+678h-67Fh for ECP) (Note)   |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |
| 10: 3BCh-3BFh (+7BCh-7BFh for ECP)  | 11: Reserved  |                                    |   |                                    |                |                |                |                |                |            |            |            |            |            |            |            |            |

Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 18h-1Bh LAD_D1 — LPC Address Decode 1 Register (R/W) Reset Value: 00000000h</b> |   |
| 31:16   | <b>Reserved.</b> Must be set to 0.  |
| 15:9  | <b>Wide Generic Base Address Select.</b> Defines a 512 byte space. Can be mapped anywhere in the 64 KB I/O space. AC97 and other configuration registers are expected to be mapped to this range. It is wide enough to allow many unforeseen devices to be supported. Enabled at F0BAR1+I/O Offset 10h[9].<br><b>Note:</b> The selected range must not overlap any address range that is positively decoded by F0BAR1+I/O Offset 10h bits [17], [14:10], and [8:0]. |
| 8:0   | <b>Reserved.</b> Must be set to 0.  |
| <b>Offset 1Ch-1Fh LPC_ERR_SMI — LPC Error SMI Register (R/W) Reset Value: 00000080h</b>   |   |
| 31:12   | <b>Reserved.</b> Must be set to 0.  |
| 11  | <b>LPCPD# Override Enable.</b> Determines how LPCPD# output is controlled.<br>0: ACPI logic.<br>1: LPCPD# Override Value bit (bit 10 of this register).   |
| 10  | <b>LPCPD# Override Value.</b> Selects value of LPCPD# output if bit 11 of this register is set to 1.<br>0: Power down sequence.<br>1: Normal power.   |
| 9   | <b>SMI Serial IRQ Enable.</b> Allows serial IRQ to generate an SMI.<br>0: Disable.<br>1: Enable.<br>Top Level SMI status is reported at F1BAR0+I/O Offset 02h[3].<br>Second level status is reported at bit 6 of this register.   |
| 8   | <b>SMI Configuration for LPC Error Enable.</b> Allows LPC errors to generate an SMI.<br>0: Disable.<br>1: Enable.<br>Top Level SMI status is reported at F1BAR0+I/O Offset 02h[3].<br>Second level status is reported at bit 5 of this register.  |
| 7   | <b>LPCPD# Pin Status. (Read Only)</b> Reflects the current value of the LPCPD# output signal.   |
| 6   | <b>SMI Source is Serial IRQ.</b> Indicates whether or not an SMI was generated by an SERIRQ.<br>0: No.<br>1: Yes.<br>Write 1 to clear.<br>To enable SMI generation, set bit 9 of this register to 1.<br>This is the second level of status reporting. The top level status is reported in F1BAR0+I/O Offset 02h[3].<br>Writing a 1 to this bit also clears the top level status bit as long as bit 5 of this register is cleared.                                   |
| 5   | <b>LPC Error Status.</b> Indicates whether or not an SMI was generated by an error that occurred on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear.<br>To enable SMI generation, set bit 8 of this register to 1.<br>This is the second level of status reporting. The top level status is reported in F1BAR0+I/O Offset 02h[3].<br>Writing a 1 to this bit also clears the top level status bit as long as bit 6 of this register is cleared.                       |
| 4   | <b>LPC Multiple Errors Status.</b> Indicates whether or not multiple errors have occurred on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear.   |

**Table 6-31. F0BAR1+I/O Offset: LPC Interface Configuration Registers (Continued)**

| Bit  | Description   |
|--|---|
| 3  | <b>LPC Timeout Error Status.</b> Indicates whether or not an error was generated by a timeout on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear.             |
| 2  | <b>LPC Error Write Status.</b> Indicates whether or not an error was generated during a write operation on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear.   |
| 1  | <b>LPC Error DMA Status.</b> Indicates whether or not an error was generated during a DMA operation on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear.       |
| 0  | <b>LPC Error Memory Status.</b> Indicates whether or not an error was generated during a memory operation on LPC.<br>0: No.<br>1: Yes.<br>Write 1 to clear. |
| <b>Offset 20h-23h                          LPC_ERR_ADD — LPC Error Address Register (RO)                          Reset Value: 00000000h</b> |   |
| 31:0   | <b>LPC Error Address.</b>   |

### 6.4.2 SMI Status and ACPI Registers - Function 1

The register space designated as Function 1 (F1) is used to configure the PCI portion of support hardware for the SMI Status and ACPI Support registers. The bit formats for the PCI Header registers are given in Table 6-32.

Located in the PCI Header registers of F1 are two Base Address Registers (F1BARx) used for pointing to the register spaces designated for SMI status and ACPI support, described later in this section.

**Table 6-32. F1: PCI Header Registers for SMI Status and ACPI Support**

| Bit           | Description  |
|---------------|--|
| Index 00h-01h | Vendor Identification Register (RO) <span style="float:right">Reset Value: 100Bh</span>  |
| Index 02h-03h | Device Identification Register (RO) <span style="float:right">Reset Value: 0501h</span>  |
| Index 04h-05h | PCI Command Register (R/W) <span style="float:right">Reset Value: 0000h</span>   |
| 15:1          | <b>Reserved. (Read Only)</b>   |
| 0             | <b>I/O Space.</b> Allow the Core Logic module to respond to I/O cycles from the PCI bus.<br>0: Disable.<br>1: Enable.<br>This bit must be enabled to access I/O offsets through F1BAR0 and F1BAR1 (see F1 Index 10h and 40h).  |
| Index 06h-07h | PCI Status Register (RO) <span style="float:right">Reset Value: 0280h</span>   |
| Index 08h     | Device Revision ID Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 09h-0Bh | PCI Class Code Register (RO) <span style="float:right">Reset Value: 068000h</span>   |
| Index 0Ch     | PCI Cache Line Size Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 0Dh     | PCI Latency Timer Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 0Eh     | PCI Header Type (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Fh     | PCI BIST Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 10h-13h | Base Address Register 0 - F1BAR0 (R/W) <span style="float:right">Reset Value: 00000001h</span><br>This register allows access to I/O mapped SMI status related registers. Bits [7:0] are read only (0000 0001), indicating a 256-byte I/O address range. Refer to Table 6-33 on page 253 for bit formats and reset values of the SMI status registers.   |
| 31:8          | <b>SMI Status Base Address.</b>  |
| 7:0           | <b>Address Range. (Read Only)</b>  |
| Index 14h-2Bh | Reserved <span style="float:right">Reset Value: 00h</span>   |
| Index 2Ch-2Dh | Subsystem Vendor ID (RO) <span style="float:right">Reset Value: 100Bh</span>   |
| Index 2Eh-2Fh | Subsystem ID (RO) <span style="float:right">Reset Value: 0501h</span>  |
| Index 30h-3Fh | Reserved <span style="float:right">Reset Value: 00h</span>   |
| Index 40h-43h | Base Address Register 1 - F1BAR1 (R/W) <span style="float:right">Reset Value: 00000001h</span><br>This register allows access to I/O mapped ACPI related registers. Bits [7:0] are read only (0000 0001), indicating a 256 byte address range. Refer to Table 6-34 on page 263 for bit formats and reset values of the ACPI registers.<br><b>Note:</b> This Base Address register moved from its normal PCI Header Space (F1 Index 14h) to prevent plug and play software from relocating it after an FACP table is built. |
| 31:8          | <b>ACPI Base Address.</b>  |
| 7:1           | <b>Address Range. (Read Only)</b>  |
| 0             | <b>Enable. (Write Only)</b> This bit must be set to 1 to enable access to ACPI Support Registers.  |
| Index 44h-FFh | Reserved <span style="float:right">Reset Value: 00h</span>   |

### 6.4.2.1 SMI Status Support Registers

F1 Index 10h, Base Address Register 0 (F1BAR0), points to the base address for SMI Status register locations. Table 6-33 gives the bit formats of I/O mapped SMI Status registers accessed through F1BAR0.

The registers at F1BAR0+I/O Offset 50h-FFh can also be accessed F0 Index 50h-FFh. The preferred method is to program these registers through the F0 register space.

**Table 6-33. F1BAR0+I/O Offset: SMI Status Registers**

| Bit   | Description  |
|---|--|
| <b>Offset 00h-01h</b> <span style="float: right;"><b>Top Level PME/SMI Status Mirror Register (RO)</b></span> <span style="float: right;"><b>Reset Value: 0000h</b></span><br><b>Note:</b> Reading this register does not clear the status bits. For more information, see F1BAR0+I/O Offset 02h. |  |
| 15  | <b>Suspend Modulation Enable Mirror.</b> This bit mirrors the Suspend Mode Configuration bit (F0 Index 96h[0]). It is used by the SMI handler to determine if the SMI Speedup Disable Register (F1BAR0+I/O Offset 08h) must be cleared on exit.  |
| 14  | <b>SMI Source is USB.</b> Indicates whether or not an SMI was caused by USB activity<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F5BAR0+I/O Offset 00h[20:19] to 11.   |
| 13  | <b>SMI Source is Warm Reset Command.</b> Indicates whether or not an SMI was caused by a Warm Reset command.<br>0: No.<br>1: Yes.  |
| 12  | <b>SMI Source is NMI.</b> Indicates whether or not an SMI was caused by NMI activity.<br>0: No.<br>1: Yes.   |
| 11  | <b>SMI Source is IRQ2 of SIO Module.</b> Indicates whether or not an SMI was caused by IRQ2 of the SIO module.<br>0: No.<br>1: Yes.<br>The next level (second level) of SMI status is reported in the SuperI/O module. For more information, see Table 5-29 "Banks 0 and 1 - Common Control and Status Registers" on page 134, Offset 00h.   |
| 10  | <b>SMI Source is EXT_SMI[7:0].</b> Indicates whether or not an SMI was caused by a negative-edge event on EXT_SMI[7:0].<br>0: No.<br>1: Yes.<br>The next level (second level) of SMI status is at F1BAR0+I/O Offset 24h[23:8].   |
| 9   | <b>SMI Source is GP Timers/UDEF/PCI/ISA Function Trap.</b> Indicates if an SMI was caused by: <ul style="list-style-type: none"> <li>— Expiration of GP Timer 1 or 2.</li> <li>— Trapped access to UDEF1, 2, or 3.</li> <li>— Trapped access to F1-F5 or ISA Legacy register space.</li> </ul> 0: No.<br>1: Yes.<br>The next level (second level) of SMI status is at F1BAR0+I/O Offset 04h/06h. |
| 8   | <b>SMI Source is Software Generated.</b> Indicates whether or not an SMI was caused by software.<br>0: No.<br>1: Yes.  |
| 7   | <b>SMI on an A20M# Toggle.</b> Indicates whether or not an SMI was caused by a write access to either Port 92h or the keyboard command which initiates an A20M# SMI.<br>0: No.<br>1: Yes.<br>This method of controlling the internal A20M# in the GX1 module is used instead of a pin.<br>To enable SMI generation, set F0 Index 53h[0] to 1.  |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit  | Description   |
|--|---|
| 6  | <p><b>SMI Source is a VGA Timer Event.</b> Indicates whether or not an SMI was caused by the expiration of the VGA Timer (F0 Index 8Eh).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 83h[3] to 1.</p>   |
| 5  | <p><b>SMI Source is Video Retrace.</b> Indicates whether or not an SMI was caused by a video retrace event as decoded from the internal serial connection (P SERIAL register, bit 7) from the GX1 module.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 83h[2] to 1.</p>  |
| 4  | <b>Reserved.</b> Reads as 0.  |
| 3  | <p><b>SMI Source is LPC.</b> Indicates whether or not an SMI was caused by the LPC interface.</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (second level) of SMI status is at F0BAR1+I/O Offset 1Ch[6:5].</p>  |
| 2  | <p><b>SMI Source is ACPI.</b> Indicates whether or not an SMI was caused by an access (read or write) to one of the ACPI registers (F1BAR1).</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (second level) of SMI status is at F1BAR0+I/O Offset 20h.</p>  |
| 1  | <p><b>SMI Source is Audio Subsystem.</b> Indicates whether or not an SMI was caused by the audio subsystem.</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (second level) of SMI status is at F3BAR0+Memory Offset 10h/12h.</p>  |
| 0  | <p><b>SMI Source is Power Management Event.</b> Indicates whether or not an SMI was caused by one of the power management resources (except for GP timers, UDEFx and PCI/ISA function traps that are reported in bit 9).</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (second level) of SMI status is at F0 Index 84h-F4h/87h-F7h.</p> |
| <p><b>Offset 02h-03h</b> <b>Top Level PME/SMI Status Register (RO/RC)</b> <b>Reset Value: 0000h</b></p> <p><b>Note:</b> Reading this register clears all the SMI status bits except for the “read only” bits, because they have a second level of status reporting. Clearing the second level status bits also clears the top level (except for GPIOs).</p> <p>GPIO SMIs have third level of SMI status reporting at F0BAR0+I/O Offset 0Ch/1Ch. Clearing the third level GPIO status bits also clears the second and top levels.</p> <p>A read-only “Mirror” version of this register exists at F1BAR0+I/O Offset 00h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F1BAR0+I/O Offset 00h can be read instead.</p> |   |
| 15   | <p><b>Suspend Modulation Enable Mirror. (Read to Clear)</b></p> <p>This bit mirrors the Suspend Mode Configuration bit (F0 Index 96h[0]). It is used by the SMI handler to determine if the SMI Speedup Disable Register (F1BAR0+I/O Offset 08h) must be cleared on exit.</p>   |
| 14   | <p><b>SMI Source is USB. (Read to Clear)</b> Indicates whether or not an SMI was caused by USB activity.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F5BAR0+I/O Offset 00h[20:19] to 11.</p>   |
| 13   | <p><b>SMI Source is Warm Reset Command. (Read to Clear)</b> Indicates whether or not an SMI was caused by Warm Reset command</p> <p>0: No.<br/>1: Yes.</p>  |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit | Description   |
|-----|---|
| 12  | <b>SMI Source is NMI. (Read to Clear)</b> Indicates whether or not an SMI was caused by NMI activity.<br>0: No.<br>1: Yes.  |
| 11  | <b>SMI Source is IRQ2 of SIO Module. (Read to Clear)</b> Indicates whether or not an SMI was caused by IRQ2 of the SIO module.<br>0: No.<br>1: Yes.<br><br>The next level (second level) of SMI status is reported in the SuperI/O module. See Table 5-29 "Banks 0 and 1 - Common Control and Status Registers" on page 134 for details.                    |
| 10  | <b>SMI Source is EXT_SMI[7:0]. (Read Only. Read Does Not Clear)</b> Indicates whether or not an SMI was caused by a negative-edge event on EXT_SMI[7:0].<br>0: No.<br>1: Yes.<br><br>The next level (second level) of SMI status is at F1BAR0+I/O Offset 24h[23:8].   |
| 9   | <b>SMI Source is General Timers/Traps. (Read Only, Read Does Not Clear)</b> Indicates whether or not an SMI was caused by the expiration of one of the General Purpose Timers or one of the User Defined Traps.<br>0: No.<br>1: Yes.<br><br>The next level (second level) of SMI status is at F1BAR0+I/O Offset 04h/06h.                                    |
| 8   | <b>SMI Source is Software Generated. (Read to Clear)</b> Indicates whether or not an SMI was caused by software.<br>0: No.<br>1: Yes.   |
| 7   | <b>SMI on an A20M# Toggle. (Read to Clear)</b> Indicates whether or not an SMI was caused by an access to either Port 92h or the keyboard command which initiates an A20M# SMI<br>0: No.<br>1: Yes.<br><br>This method of controlling the internal A20M# in the GX1 module is used instead of a pin.<br>To enable SMI generation, set F0 Index 53h[0] to 1. |
| 6   | <b>SMI Source is a VGA Timer Event. (Read to Clear)</b> Indicates whether or not an SMI was caused by expiration of the VGA Timer (F0 Index 8Eh).<br>0: No.<br>1: Yes.<br><br>To enable SMI generation, set F0 Index 83h[3] to 1.   |
| 5   | <b>SMI Source is Video Retrace. (Read to Clear)</b> Indicates whether or not an SMI was caused by a video retrace event as decoded from the internal serial connection (PSERIAL register, bit 7) from the GX1 module.<br>0: No.<br>1: Yes.<br><br>To enable SMI generation, set F0 Index 83h[2] to 1.   |
| 4   | <b>Reserved.</b> Reads as 0.  |
| 3   | <b>SMI Source is LPC. (Read Only, Read Does Not Clear)</b> Indicates whether or not an SMI was caused by the LPC interface.<br>0: No.<br>1: Yes.<br><br>The next level (second level) of SMI status is at F0BAR1+I/O Offset 1Ch[6:5].   |
| 2   | <b>SMI Source is ACPI. (Read Only, Read Does Not Clear)</b> Indicates whether or not an SMI was caused by an access (read or write) to one of the ACPI registers (F1BAR1).<br>0: No.<br>1: Yes.<br><br>The next level (second level) of SMI status is at F1BAR0+I/O Offset 20h.   |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit  | Description   |
|--|---|
| 1  | <p><b>SMI Source is Audio Subsystem. (Read Only, Read Does Not Clear)</b> Indicates whether or not an SMI was caused by the audio subsystem.</p> <p>0: No.<br/>1: Yes.</p> <p>The second level of status is found in F3BAR0+Memory Offset 10h/12h.</p>  |
| 0  | <p><b>SMI Source is Power Management Event. (Read Only, Read Does Not Clear)</b> Indicates whether or not an SMI was caused by one of the power management resources (except for GP timers, UDEFx and PCI/ISA function traps which are reported in bit 9).</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (second level) of SMI status is at F0 Index 84h/F4h-87h/F7h.</p>   |
| <p><b>Offset 04h-05h</b> <span style="float: right;"><b>Reset Value: 0000h</b></span></p> <p style="text-align: center;"><b>Second Level General Traps &amp; Timers<br/>PME/SMI Status Mirror Register (RO)</b></p> <p>The bits in this register contain second level status reporting. Top level status is reported at F1BAR0+I/O Offset 00h/02h[9].<br/>Reading this register does not clear the SMI. For more information, see F1BAR0+I/O Offset 06h.</p> |   |
| 15:6   | <b>Reserved.</b>  |
| 5  | <p><b>PCI/ISA Function Trap.</b> Indicates whether or not an SMI was caused by a trapped PCI/ISA configuration cycle.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation for:</p> <ul style="list-style-type: none"> <li>— Trapped access to ISA Legacy I/O register space set F0 Index 41h[0] = 1.</li> <li>— Trapped access to F1 register space set F0 Index 41h[1] = 1.</li> <li>— Trapped access to F2 register space set F0 Index 41h[2] = 1.</li> <li>— Trapped access to F3 register space set F0 Index 41h[3] = 1.</li> <li>— Trapped access to F4 register space set F0 Index 41h[4] = 1.</li> <li>— Trapped access to F5 register space set F0 Index 41h[5] = 1.</li> </ul> |
| 4  | <p><b>SMI Source is Trapped Access to User Defined Device 3.</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to the User Defined Device 3 (F0 Index C8h).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[6] = 1.</p>  |
| 3  | <p><b>SMI Source is Trapped Access to User Defined Device 2.</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to the User Defined Device 2 (F0 Index C4h).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[5] = 1.</p>  |
| 2  | <p><b>SMI Source is Trapped Access to User Defined Device 1.</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to the User Defined Device 1 (F0 Index C0h).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 82h[4] = 1.</p>  |
| 1  | <p><b>SMI Source is Expired General Purpose Timer 2.</b> Indicates whether or not an SMI was caused by the expiration of General Purpose Timer 2 (F0 Index 8Ah).</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set F0 Index 83h[1] = 1.</p>  |



Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit   | Description   |
|---|---|
| 0   | <b>SMI Source is Expired General Purpose Timer 1.</b> Indicates whether or not an SMI was caused by the expiration of General Purpose Timer 1 (F0 Index 88h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[0] = 1.  |
| <b>Offset 06h-07h                                  Second Level General Traps &amp; Timers Status Register (RC)                                  Reset Value: 0000h</b>   |   |
| The bits in this register contain second level of status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[9]. Reading this register clears the status at both the second and top levels.<br>A read-only "Mirror" version of this register exists at F1BAR0+I/O Offset 04h. If the value of this register must be read without clearing the SMI source (and consequently de-asserting SMI), F1BAR0+I/O Offset 04h can be read instead. |   |
| 15:6  | <b>Reserved.</b>  |
| 5   | <b>PCI/ISA Function Trap.</b> Indicates whether or not an SMI was caused by a trapped PCI/ISA configuration cycle<br>0: No.<br>1: Yes.<br>To enable SMI generation for:<br>— Trapped access to ISA Legacy I/O register space set F0 Index 41h[0] = 1.<br>— Trapped access to F1 register space set F0 Index 41h[1] = 1.<br>— Trapped access to F2 register space set F0 Index 41h[2] = 1.<br>— Trapped access to F3 register space set F0 Index 41h[3] = 1.<br>— Trapped access to F4 register space set F0 Index 41h[4] = 1.<br>— Trapped access to F5 register space set F0 Index 41h[5] = 1. |
| 4   | <b>SMI Source is Trapped Access to User Defined Device 3 (UDEF3).</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to User Defined Device 3 (F0 Index C8h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[6] = 1.  |
| 3   | <b>SMI Source is Trapped Access to User Defined Device 2 (UDEF2).</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to User Defined Device 2 (F0 Index C4h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[5] = 1.  |
| 2   | <b>SMI Source is Trapped Access to User Defined Device 1 (UDEF1).</b> Indicates whether or not an SMI was caused by a trapped I/O or memory access to User Defined Device 1 (F0 Index C0h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 82h[4] = 1.  |
| 1   | <b>SMI Source is Expired General Purpose Timer 2.</b> Indicates whether or not an SMI was caused by the expiration of General Purpose Timer 2 (F0 Index 8Ah).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[1] = 1.  |
| 0   | <b>SMI Source is Expired General Purpose Timer 1.</b> Indicates whether or not an SMI was caused by the expiration of General Purpose Timer 1 (F0 Index 88h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F0 Index 83h[0] = 1.  |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 08h-09h</b> <b>SMI Speedup Disable Register (Read to Enable)</b> <b>Reset Value: 0000h</b>   |   |
| 15:0   | <b>SMI Speedup Disable.</b> If bit 1 in the Suspend Configuration Register is set (F0 Index 96h[1] = 1), a read of this register invokes the SMI handler to re-enable Suspend Modulation.<br><br>The data read from this register can be ignored. If the Suspend Modulation feature is disabled, reading this I/O location has no effect. |
| <b>Offset 0Ah-1Bh</b> <b>Reserved</b> <b>Reset Value: 00h</b><br>These addresses should not be written.  |   |
| <b>Offset 1Ch-1Fh</b> <b>ACPI Timer Register (RO)</b> <b>Reset Value: xxxxxxxh</b><br><b>Note:</b> This register can also be read at F1BAR1+I/O Offset 1Ch.  |   |
| 31:24  | <b>Reserved.</b>  |
| 23:0   | <b>TMR_VAL.</b> This field returns the running count of the power management timer.   |
| <b>Offset 20h-21h</b> <b>Second Level ACPI PME/SMI Status Mirror Register (RO)</b> <b>Reset Value: 0000h</b><br>The bits in this register contain second level SMI status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[2].<br>Reading this register does not clear the SMI. For more information, see F1BAR0+I/O Offset 22h. |   |
| 15:6   | <b>Reserved.</b> Always reads 0.  |
| 5  | <b>ACPI BIOS SMI Status.</b> Indicates whether or not an SMI was caused by ACPI software raising an event to BIOS software.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[2] to 1, and F1BAR1+I/O Offset 0Fh[0] to 1.   |
| 4  | <b>PLVL3 SMI Status.</b> Indicates whether or not an SMI was caused by a read of the ACPI PLVL3 register (F1BAR1+I/O Offset 05h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[11] to 1 (default).   |
| 3  | <b>Reserved.</b>  |
| 2  | <b>SLP_EN SMI Status.</b> Indicates whether or not an SMI was caused by a write of 1 to the ACPI SLP_EN bit (F1BAR1+I/O Offset 0Ch[13]).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[9] to 1 (default).   |
| 1  | <b>THT_EN SMI Status.</b> Indicates whether or not an SMI was caused by a write of 1 to the ACPI THT_EN bit (F1BAR1+I/O Offset 00h[4]).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[8] to 1 (default).  |
| 0  | <b>SMI_CMD SMI Status.</b> Indicates whether or not an SMI was caused by a write to the ACPI SMI_CMD register (F1BAR1+I/O Offset 06h).<br>0: No.<br>1: Yes.<br>A write to the ACPI SMI_CMD register always generates an SMI.  |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 22h-23h</b> <b>Second Level ACPI PME/SMI Status Register (RC)</b> <b>Reset Value: 0000h</b><br>The bits in this register contain second level of SMI status reporting. Top level is reported in F1BAR0+I/O Offset 00h/02h[2].<br>Reading this register clears the status at both the second and top levels.<br>A read-only "Mirror" version of this register exists at F1BAR0+I/O Offset 20h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F1BAR0+I/O Offset 20h can be read instead. |   |
| 15:6  | <b>Reserved.</b> Always reads 0.  |
| 5   | <b>ACPI BIOS SMI Status.</b> Indicates whether or not an SMI was caused by ACPI software raising an event to BIOS software.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 0Ch[2] to 1, and F1BAR1+I/O Offset 0Fh[0] to 1. |
| 4   | <b>PLVL3 SMI Status.</b> Indicates whether or not an SMI was caused by a read of the ACPI PLVL3 register (F1BAR1+I/O Offset 05h).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[11] to 1 (default).                   |
| 3   | <b>Reserved.</b>  |
| 2   | <b>SLP_EN SMI Status.</b> Indicates whether or not an SMI was caused by a write of 1 to the ACPI SLP_EN bit (F1BAR1+I/O Offset 0Ch[13]).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[9] to 1 (default).             |
| 1   | <b>THT_EN SMI Status.</b> Indicates whether or not an SMI was caused by a write of 1 to the ACPI THT_EN bit (F1BAR1+I/O Offset 00h[4]).<br>0: No.<br>1: Yes.<br>To enable SMI generation, set F1BAR1+I/O Offset 18h[8] to 1 (default).              |
| 0   | <b>SMI_CMD SMI Status.</b> Indicates whether or not an SMI was caused by a write to the ACPI SMI_CMD register (F1BAR1+I/O Offset 06h).<br>0: No.<br>1: Yes.<br>A write to the ACPI SMI_CMD register always generates an SMI.                        |
| <b>Offset 24h-27h</b> <b>External SMI Register (R/W)</b> <b>Reset Value: 00000000h</b><br><b>Note:</b> EXT_SMI[7:0] are external SMIs, meaning external to the Core Logic module.<br>Bits [23:8] of this register contain second level of SMI status reporting. Top level status is reported in F1BAR0+I/O Offset 00h/02h[10]. Reading bits [23:16] clears the second and top levels. If the value of the status bits must be read without clearing the SMI source (and consequently de-asserting SMI), bits [15:8] can be read instead.                          |   |
| 31:24   | <b>Reserved.</b> Must be set to 0.  |
| 23  | <b>EXT_SMI7 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by assertion of EXT_SMI7.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 7 to 1.  |
| 22  | <b>EXT_SMI6 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI6.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 6 to 1.   |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit | Description   |
|-----|---|
| 21  | <b>EXT_SMI5 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI5.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 5 to 1. |
| 20  | <b>EXT_SMI4 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI4.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 4 to 1. |
| 19  | <b>EXT_SMI3 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI3.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 3 to 1. |
| 18  | <b>EXT_SMI2 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI2.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 2 to 1. |
| 17  | <b>EXT_SMI1 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI1.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 1 to 1. |
| 16  | <b>EXT_SMI0 SMI Status. (Read to Clear)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI0.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 0 to 1. |
| 15  | <b>EXT_SMI7 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI7.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 7 to 1.     |
| 14  | <b>EXT_SMI6 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI6.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 6 to 1.     |
| 13  | <b>EXT_SMI5 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI5.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 5 to 1.     |
| 12  | <b>EXT_SMI4 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI4.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 4 to 1.     |
| 11  | <b>EXT_SMI3 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI3.<br>0: No.<br>1: Yes.<br>To enable SMI generation, set bit 3 to 1.     |

Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)

| Bit | Description   |
|-----|---|
| 10  | <p><b>EXT_SMI2 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI2.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set bit 2 to 1.</p>   |
| 9   | <p><b>EXT_SMI1 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI1.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set bit 1 to 1.</p>   |
| 8   | <p><b>EXT_SMI0 SMI Status. (Read Only)</b> Indicates whether or not an SMI was caused by an assertion of EXT_SMI0.</p> <p>0: No.<br/>1: Yes.</p> <p>To enable SMI generation, set bit 0 to 1.</p>   |
| 7   | <p><b>EXT_SMI7 SMI Enable.</b> When this bit is asserted, allow EXT_SMI7 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 23 (RC) and 15 (RO).</p>  |
| 6   | <p><b>EXT_SMI6 SMI Enable.</b> When this bit is asserted, allow EXT_SMI6 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 22 (RC) and 14 (RO).</p>  |
| 5   | <p><b>EXT_SMI5 SMI Enable.</b> When this bit is asserted, allow EXT_SMI5 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 21 (RC) and 13 (RO).</p>  |
| 4   | <p><b>EXT_SMI4 SMI Enable.</b> When this bit is asserted, allows EXT_SMI4 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 20 (RC) and 12 (RO).</p> |
| 3   | <p><b>EXT_SMI3 SMI Enable.</b> When this bit is asserted, allow EXT_SMI3 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 19 (RC) and 11 (RO).</p>  |
| 2   | <p><b>EXT_SMI2 SMI Enable.</b> When this bit is asserted, allow EXT_SMI2 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 18 (RC) and 10 (RO).</p>  |
| 1   | <p><b>EXT_SMI1 SMI Enable.</b> When this bit is asserted, allow EXT_SMI1 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 17 (RC) and 9 (RO).</p>   |

**Table 6-33. F1BAR0+I/O Offset: SMI Status Registers (Continued)**

| Bit                     | Description  |
|-------------------------|--|
| 0                       | <p><b>EXT_SMI0 SMI Enable.</b> When this bit is asserted, allow EXT_SMI0 to generate an SMI on negative-edge events.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+00h/02h[10].<br/>Second level SMI status is reported at bits 16 (RC) and 8 (RO).</p>  |
| <b>Offset 28h-4Fh</b>   |  |
| <b>Not Used</b>         |  |
| <b>Reset Value: 00h</b> |  |
| <b>Offset 50h-FFh</b>   | The I/O mapped registers located here (F1BAR0+I/O Offset 50h-FFh) can also be accessed at F0 Index 50h-FFh. The preferred method is to program these registers through the F0 register space. Refer to Table 6-29 "F0: PCI Header/Bridge Configuration Registers for GPIO and LPC Support" on page 206 for more information about these registers. |

### 6.4.2.2 ACPI Support Registers

F1 Index 40h, Base Address Register 1 (F1BAR1), points to the base address of where the ACPI Support registers are located. Table 6-34 shows the I/O mapped ACPI Support registers accessed through F1BAR1.

**Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers**

| Bit   | Description   |               |            |          |          |            |            |            |            |
|---|---|---------------|------------|----------|----------|------------|------------|------------|------------|
| <b>Offset 00h-03h</b> <b>P_CNT — Processor Control Register (R/W)</b> <b>Reset Value: 0000000h</b>        |   |               |            |          |          |            |            |            |            |
| 31:5  | <b>Reserved.</b> Always reads 0.  |               |            |          |          |            |            |            |            |
| 4   | <p><b>THT_EN (Throttle Enable).</b> When this bit is asserted, it enables throttling of the clock based on the CLK_VAL field (bits [2:0] of this register).</p> <p>0: Disable.<br/>1: Enable.</p> <p>If F1BAR1+I/O Offset 18h[8] =1, an SMI is generated when this bit is set.<br/>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[1].</p>   |               |            |          |          |            |            |            |            |
| 3   | <b>Reserved.</b> Always reads 0.  |               |            |          |          |            |            |            |            |
| 2:0   | <p><b>CLK_VAL (Clock Throttling Value).</b> CPU duty cycle:</p> <table border="0"> <tr> <td>000: Reserved</td> <td>010: 25%</td> <td>100: 50%</td> <td>110: 75%</td> </tr> <tr> <td>001: 12.5%</td> <td>011: 37.5%</td> <td>101: 62.5%</td> <td>111: 87.5%</td> </tr> </table>  | 000: Reserved | 010: 25%   | 100: 50% | 110: 75% | 001: 12.5% | 011: 37.5% | 101: 62.5% | 111: 87.5% |
| 000: Reserved   | 010: 25%  | 100: 50%      | 110: 75%   |          |          |            |            |            |            |
| 001: 12.5%  | 011: 37.5%  | 101: 62.5%    | 111: 87.5% |          |          |            |            |            |            |
| <b>Offset 04h</b> <b>Reserved</b> <b>Reset Value: 00h</b>   |   |               |            |          |          |            |            |            |            |
| <b>Note:</b> This register should not be read. It controls a reserved function of power management logic. |   |               |            |          |          |            |            |            |            |
| <b>Offset 05h</b> <b>P_LVL3 — Enter C3 Power State Register (RO)</b> <b>Reset Value: xxh</b>              |   |               |            |          |          |            |            |            |            |
| 7:0   | <p><b>P_LVL3 (Power Level 3).</b> Reading this 8-bit read only register causes the processor to enter the C3 power state. Reads of P_LVL3 return 0. Writes have no effect.</p> <p>The ACPI state machine always waits for an SMI (any SMI) to be generated and serviced before transfer into C3 power state.</p> <p>A read of this register causes an SMI if enabled: F1BAR1+I/O Offset 18h[11] = 1 (default).<br/>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[4].</p> |               |            |          |          |            |            |            |            |
| <b>Offset 06h</b> <b>SMI_CMD — OS/BIOS Requests Register (R/W)</b> <b>Reset Value: 00h</b>                |   |               |            |          |          |            |            |            |            |
| 7:0   | <p><b>SMI_CMD (SMI Command and OS / BIOS Requests).</b> A write to this register stores data and a read returns the last data written. In addition, a write to this register always generates an SMI. A read of this register does not generate an SMI.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[0].</p>   |               |            |          |          |            |            |            |            |
| <b>Offset 07h</b> <b>ACPI_FUN_CNT — ACPI Function Control Register (R/W)</b> <b>Reset Value: 00h</b>      |   |               |            |          |          |            |            |            |            |
| 7:6   | <p><b>LED_CNT (LED Output Control).</b> Controls the blinking of an LED when in the SL4 or SL5 sleep state</p> <p>00: Disable (LED# signal, is HiZ).<br/>01: Zero (LED# signal is HiZ).<br/>10: Blink @ 1 Hz rate, when in SL4 and SL5 sleep states. Duty cycle: LED# is 10% pulled low, 90% HiZ.<br/>11: One (LED# is pulled low, when in SL4 and SL5 sleep states)</p>  |               |            |          |          |            |            |            |            |
| 5   | <b>Reserved.</b> Must be set to 0.  |               |            |          |          |            |            |            |            |
| 4   | <p><b>INTR_WU_SL1.</b> Enables wakeup on enabled interrupts in sleep state SL1.</p> <p>0: Disable wakeup from SL1, when an enabled interrupt is active.<br/>1: Enable wakeup from SL1, when an enabled interrupt is active.</p>   |               |            |          |          |            |            |            |            |
| 3   | <p><b>GPWIO_DBNC_DIS (GPWIO0 and GPWIO1 Debounce).</b> When enabled, a high-to-low or low-to-high transition of greater than 15.8 ms is required for GPWIO0 and GPWIO1 to be recognized.</p> <p>0: Enable. (Default)<br/>1: Disable. (No debounce)</p> <p>GPWIO2 pin does not have debounce capability.</p>   |               |            |          |          |            |            |            |            |
| 2:1   | <b>Reserved.</b> Must be set to 0.  |               |            |          |          |            |            |            |            |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit   | Description   |
|---|---|
| 0   | <p><b>PWRBTN_DBNC_DIS (Power Button Debounce).</b> When enabled, a high-to-low or low-to-high transition of greater than 15.8 ms is required on PWRBTN# before it is recognized.</p> <p>0: Enable. (Default)<br/>1: Disable. (No debounce)</p>  |
| <p><b>Offset 08h-09h</b>                      <b>PM1A_STS — PM1A Top Level PME/SCI Status Register (R/W)</b>                      <b>Reset Value: 0000h</b></p> <p><b>Notes:</b> 1. This is the top level of PME/SCI status reporting for these events. There is no second level.<br/>2. If SCI generation is not desired, the status bits are still set by the described conditions and can be used for monitoring purposes.</p> |   |
| 15  | <p><b>WAK_STS (Wakeup Status).</b> Indicates whether or not an SCI was caused by the occurrence of an enabled wakeup event.</p> <p>0: No.<br/>1: Yes.</p> <p>This bit is set when the system is in any Sleep state and an enabled wakeup event occurs (wakeup events are configured at F1BAR1+I/O Offset 0Ah and 12h). After this bit is set, the system transitions to a Working state.<br/>SCI generation is always enabled.<br/>Write 1 to clear.</p>  |
| 14:12   | <b>Reserved.</b> Must be set to 0.  |
| 11  | <p><b>PWRBTNOR_STS (Power Button Override Status).</b> Indicates whether or not an SCI was caused by the power button being active for greater than 4 seconds.</p> <p>0: No.<br/>1: Yes.</p> <p>SCI generation is always enabled.<br/>Write 1 to clear.</p>   |
| 10  | <p><b>RTC_STS (Real-Time Clock Status).</b> Indicates if a Power Management Event (PME) was caused by the RTC generating an alarm (RTC IRQ signal is asserted).</p> <p>0: No.<br/>1: Yes.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 0Ah[10] to 1 and F1BAR1+I/O Offset 0Ch[0] to 1. (See Note 2 in the general description of this register.)<br/>Write 1 to clear.</p>  |
| 9   | <b>Reserved.</b> Must be set to 0.  |
| 8   | <p><b>PWRBTN_STS (Power Button Status).</b> Indicates if PME was caused by the PWRBTN# going low while the system is in a Working state.</p> <p>0: No.<br/>1: Yes.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 0Ah[8] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register.)<br/>In a Sleep state or the Soft-Off state, a wakeup event is generated when the power button is pressed (regardless of the PWRBTN_EN bit, F1BAR1+I/O Offset 0Ah[8], setting).<br/>Write 1 to clear.</p> |
| 7:6   | <b>Reserved.</b> Must be set to 0.  |
| 5   | <p><b>GBL_STS (Global Lock Status).</b> Indicates if PME was caused by the BIOS releasing control of the global lock.</p> <p>0: No.<br/>1: Yes.</p> <p>This bit is used by the BIOS to generate an SCI. BIOS writes the BIOS_RLS bit (F1BAR1+I/O Offset 0Fh[1]) which in turns sets the GBL_STS bit and raises a PME.<br/>For the PME to generate an SCI, set F1BAR1+I/O Offset 0Ah[5] to 1 and F1BAR1+I/O Offset 0Ch[0] to 1. (See Note 2 in the general description of this register.)<br/>Write 1 to clear.</p>                              |



Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit   | Description   |
|---|---|
| 4   | <p><b>BM_STS (Bus Master Status).</b> Indicates if PME was caused by a system bus master requesting the system bus.</p> <p>0: No.<br/>1: Yes.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 0Ch[1] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register.)</p> <p>Write 1 to clear.</p>  |
| 3:1   | <b>Reserved.</b> Must be set to 0.  |
| 0   | <p><b>TMR_STS (Timer Carry Status).</b> Indicates if SCI was caused by an MSB toggle (MSB changes from low-to-high or high-to-low) on the ACPI Timer (F1BAR0+I/O Offset 1Ch or F1BAR1+I/O Offset 1Ch).</p> <p>0: No.<br/>1: Yes.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 0Ah[0] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register.)</p> <p>Write 1 to clear.</p> |
| <p><b>Offset 0Ah-0Bh</b> <b>PM1A_EN — PM1A PME/SCI Enable Register (R/W)</b> <b>Reset Value: 0000h</b></p> <p>In order for the ACPI events described below to generate an SCI, the SCI_EN bit must also be set (F1BAR1+I/O Offset 0Ch[0] = 1). The SCIs enabled via this register are globally enabled by setting F1BAR1+I/O Offset 08h. There is no second level of SCI status reporting for these bits.</p> |   |
| 15:11   | <b>Reserved.</b> Must be set to 0.  |
| 10  | <p><b>RTC_EN (Real-Time Clock Enable).</b> Allow SCI generation when the RTC generates an alarm (RTC IRQ signal is asserted).</p> <p>0: Disable.<br/>1: Enable</p>  |
| 9   | <b>Reserved.</b> Must be set to 0.  |
| 8   | <p><b>PWRBTN_EN (Power Button Enable).</b> Allow SCI generation when PWRBTN# goes low while the system is in a Working state.</p> <p>0: Disable.<br/>1: Enable</p>  |
| 7:6   | <b>Reserved.</b> Must be set to 0.  |
| 5   | <p><b>GBL_EN (Global Lock Enable).</b> Allow SCI generation when the BIOS releases control of the global lock via the BIOS_RLS (F1BAR1+I/O Offset 0Fh[1] and GBL_STS (F1BAR1+I/O Offset 08h[5]) bits.</p> <p>0: Disable.<br/>1: Enable</p>  |
| 4:1   | <b>Reserved.</b> Must be set to 0.  |
| 0   | <p><b>TMR_EN (ACPI Timer Enable).</b> Allow SCI generation for MSB toggles (MSB changes from low-to-high or high-to-low) on the ACPI Timer (F1BAR0+I/O Offset 1Ch or F1BAR1+I/O Offset 1Ch).</p> <p>0: Disable.<br/>1: Enable</p>   |
| <p><b>Offset 0Ch-0Dh</b> <b>PM1A_CNT — PM1A Control Register (R/W)</b> <b>Reset Value: 0000h</b></p>  |   |
| 15:14   | <b>Reserved.</b> Must be set to 0.  |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit                                 | Description  |                               |                      |                      |                                 |                      |               |                      |               |
|-------------------------------------|--|-------------------------------|----------------------|----------------------|---------------------------------|----------------------|---------------|----------------------|---------------|
| 13                                  | <p><b>SLP_EN (Sleep Enable). (Write Only)</b> Allow the system to sequence into the sleeping state associated with the SLP_TYPx (bits [12:10]).</p> <p>0: Disable.<br/>1: Enable.</p> <p>This is a write only bit and reads of this bit always return a 0.</p> <p>The ACPI state machine always waits for an SMI (any SMI) to be generated and serviced before transitioning into a Sleep state.</p> <p>If F1BAR1+I/O Offset 18h[9] = 1, an SMI is generated when SLP_EN is set.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br/>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[2].</p>   |                               |                      |                      |                                 |                      |               |                      |               |
| 12:10                               | <p><b>SLP_TYPx (Sleep Type).</b> Defines the type of Sleep state the system enters when SLP_EN (bit 13) is set.</p> <table border="0"> <tr> <td>000: Sleep State S0 (Full on)</td> <td>100: Sleep State SL4</td> </tr> <tr> <td>001: Sleep State SL1</td> <td>101: Sleep State SL5 (Soft off)</td> </tr> <tr> <td>010: Sleep State SL2</td> <td>110: Reserved</td> </tr> <tr> <td>011: Sleep State SL3</td> <td>111: Reserved</td> </tr> </table>  | 000: Sleep State S0 (Full on) | 100: Sleep State SL4 | 001: Sleep State SL1 | 101: Sleep State SL5 (Soft off) | 010: Sleep State SL2 | 110: Reserved | 011: Sleep State SL3 | 111: Reserved |
| 000: Sleep State S0 (Full on)       | 100: Sleep State SL4   |                               |                      |                      |                                 |                      |               |                      |               |
| 001: Sleep State SL1                | 101: Sleep State SL5 (Soft off)  |                               |                      |                      |                                 |                      |               |                      |               |
| 010: Sleep State SL2                | 110: Reserved  |                               |                      |                      |                                 |                      |               |                      |               |
| 011: Sleep State SL3                | 111: Reserved  |                               |                      |                      |                                 |                      |               |                      |               |
| 9:3                                 | <b>Reserved.</b> Set to 0.   |                               |                      |                      |                                 |                      |               |                      |               |
| 2                                   | <p><b>GBL_RLS (Global Release). (Write Only)</b> This write only bit is used by ACPI software to raise an event to the BIOS software (i.e., it generates an SMI to pass execution control to the BIOS).</p> <p>0: Disable.<br/>1: Enable.</p> <p>This is a write only bit and reads of this bit always return a 0.</p> <p>To generate an SMI, ACPI software writes the GBL_RLS bit which in turn sets the BIOS_STS bit (F1BAR1+I/O Offset 0Eh[0]) and raises a PME. For the PME to generate an SMI, set BIOS_EN (F1BAR1+I/O Offset 0Fh[0] to 1).</p> <p>The top level SMI status is reported at F1BAR0+I/O offset 00h/02h.<br/>Second level status is at F1BAR0+I/O Offset 22h[5].</p> |                               |                      |                      |                                 |                      |               |                      |               |
| 1                                   | <p><b>BM_RLD (Bus Master RLD).</b> If the processor is in the C3 state and a bus master request is generated, force the processor to transition to the C0 state.</p> <p>0: Disable.<br/>1: Enable</p>  |                               |                      |                      |                                 |                      |               |                      |               |
| 0                                   | <p><b>SCI_EN (System Control Interrupt Enable).</b> Globally selects power management events (PMEs) reported in PM1A_STS and GPE0_STS (F1BAR1+I/O Offset 08h and 10h) to be either an SCI or SMI type of interrupt.</p> <p>0: APM Mode, generates an SMI and status is reported at F1BAR0+I/O Offset 00h/02h[0].<br/>1: ACPI Mode, generates an SCI if the corresponding PME enable bit is set and status is reported at F1BAR1+I/O Offset 08h and 10h.</p> <p><b>Note:</b> This bit enables the ACPI state machine.</p>   |                               |                      |                      |                                 |                      |               |                      |               |
| <b>Offset 0Eh</b>                   |  |                               |                      |                      |                                 |                      |               |                      |               |
| <b>ACPI_BIOS_STS Register (R/W)</b> |  |                               |                      |                      |                                 |                      |               |                      |               |
| <b>Reset Value: 00h</b>             |  |                               |                      |                      |                                 |                      |               |                      |               |
| 7:1                                 | <b>Reserved.</b> Must be set to 0.   |                               |                      |                      |                                 |                      |               |                      |               |
| 0                                   | <p><b>BIOS_STS (BIOS Status Release).</b> When 1 is written to the GBL_RLS bit (F1BAR1+I/O Offset 0Ch[2]), this bit is also set to 1.</p> <p>Write 1 to clear.</p>   |                               |                      |                      |                                 |                      |               |                      |               |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 0Fh</b> <b>ACPI_BIOS_EN Register (R/W)</b> <b>Reset Value: 00h</b>   |  |
| 7:2  | <b>Reserved.</b> Must be set to 0.   |
| 1  | <p><b>BIOS_RLS (BIOS Release). (Write Only)</b> When this bit is asserted, allow the BIOS to release control of the global lock.</p> <p>0: Disable.<br/>1: Enable.</p> <p>This is a write only bit and reads of this bit always return a 0.</p> <p>To generate an SCI, the BIOS writes the BIOS_RLS bit which in turn sets the GBL_STS bit (F1BAR1+I/O Offset 08h[5]) and raises a PME. For the PME to generate an SCI, set GBL_EN (F1BAR1+I/O Offset 0Ah[5] to 1).</p>  |
| 0  | <p><b>BIOS_EN (BIOS Enable).</b> When this bit is asserted, allow SMI generation by ACPI software via writes to GBL_RLS (F1BAR1+I/O Offset 0Ch[2]).</p> <p>0: Disable.<br/>1: Enable</p>   |
| <b>Offset 10h-11h</b> <b>GPE0_STS — General Purpose Event 0 PME/SCI Status Register (R/W)</b> <b>Reset Value: xxxh</b>   |  |
| <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1) This is the top level of PME/SCI status reporting. There is no second level except for bit 3 (GPIOs) where the next level of status is reported at F0BAR0+I/O Offset 0Ch/1Ch.</li> <li>2) If SCI generation is not desired, the status bits are still set by the described conditions and can be used for monitoring purposes.</li> </ol> |  |
| 15:12  | <b>Reserved.</b> Must be set to 0.   |
| 11   | <b>Reserved.</b>   |
| 10   | <p><b>GPWIO2_STS.</b> Indicates if PME was caused by activity on GPWIO2.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI:</p> <ol style="list-style-type: none"> <li>1) Ensure that GPWIO2 is enabled as an input (F1BAR1+I/O Offset 15h[2] = 0)</li> <li>2) Set F1BAR1+I/O Offset 12h[10] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</li> </ol> <p>If F1BAR1+I/O Offset 15h[6] = 1 it overrides these settings and GPWIO2 generates an SMI and the status is reported in F1BAR0+00h/02h[0].</p> |
| 9  | <p><b>GPWIO1_STS.</b> Indicates if PME was caused by activity on GPWIO1.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI:</p> <ol style="list-style-type: none"> <li>1) Ensure that GPWIO1 is enabled as an input (F1BAR1+I/O Offset 15h[1] = 0)</li> <li>2) Set F1BAR1+I/O Offset 12h[9] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</li> </ol> <p>If F1BAR1+I/O Offset 15h[5] = 1 it overrides these settings and GPWIO1 generates an SMI and the status is reported in F1BAR0+00h/02h[0].</p>  |
| 8  | <p><b>GPWIO0_STS.</b> Indicates if PME was caused by activity on GPWIO0.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI:</p> <ol style="list-style-type: none"> <li>1) Ensure that GPWIO0 is enabled as an input (F1BAR1+I/O Offset 15h[0] = 0)</li> <li>2) Set F1BAR1+I/O Offset 12h[8] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</li> </ol> <p>If F1BAR1+I/O Offset 15h[4] = 1 it overrides these settings and GPWIO0 generates an SMI and the status is reported in F1BAR0+00h/02h[0].</p>  |

**Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)**

| Bit | Description  |
|-----|--|
| 7   | <b>Reserved.</b> Must be set to 0.   |
| 6   | <p><b>USB_STS.</b> Indicates if PME was caused by a USB interrupt event.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 12h[6] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</p>  |
| 5   | <p><b>THRM_STS.</b> Indicates if PME was caused by activity on THRM#.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 12h[5] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</p>   |
| 4   | <p><b>SMI_STS.</b> Indicates if PME was caused by activity on the internal SMI# signal.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 12h[4] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</p>   |
| 3   | <p><b>GPIO_STS.</b> Indicates if PME was caused by activity on any of the GPIOs (GPIO47-GPIO32 and GPIO15-GPIO0).</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 12h[3] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above).</p> <p>F0BAR0+I/O Offset 08h/18h selects which GPIOs are enabled to generate a PME. In addition, the selected GPIO must be enabled as an input (F0BAR0+I/O Offset 20h and 24h).</p> |
| 2:1 | <b>Reserved.</b> Reads as 0.   |
| 0   | <p><b>PWR_U_REQ_STS.</b> Indicates if PME was caused by a power-up request event from the SuperI/O module.</p> <p>0: No.<br/>1: Yes.</p> <p>Write 1 to clear.</p> <p>For the PME to generate an SCI, set F1BAR1+I/O Offset 12h[0] = 1 and F1BAR1+I/O Offset 0Ch[0] = 1. (See Note 2 in the general description of this register above.)</p>  |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit                   | Description   |
|-----------------------|---|
| <b>Offset 12h-13h</b> | <b>GPE0_EN — General Purpose Event 0 Enable Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000h</b></span><br>In order for the ACPI events described below to generate an SCI, the SCI_EN bit must also be set (F1BAR1+I/O Offset 0Ch[0] = 1). The SCIs enabled in this register are globally enabled by setting F1BAR1+I/O Offset 0Ch[0] to 1. The status of the SCIs is reported in F1BAR1+I/O Offset 10h. |
| 15:12                 | <b>Reserved.</b>  |
| 11                    | <b>Reserved.</b>  |
| 10                    | <b>GPWIO2_EN.</b> Allow GPWIO2 to generate an SCI.<br>0: Disable.<br>1: Enable.<br>A fixed high-to-low or low-to-high transition (debounce period) of 31 $\mu$ s exists in order for GPWIO2 to be recognized. The setting of this bit can be overridden via F1BAR1+I/O Offset 15h[6] to force an SMI.   |
| 9                     | <b>GPWIO1_EN.</b> Allow GPWIO1 to generate an SCI.<br>0: Disable.<br>1: Enable.<br>See F1BAR1+I/O Offset 07h[3] for debounce information. The setting of this bit can be overridden via F1BAR1+I/O Offset 15h[5] to force an SMI.   |
| 8                     | <b>GPWIO0_EN.</b> Allow GPWIO0 to generate an SCI.<br>0: Disable.<br>1: Enable.<br>See F1BAR1+I/O Offset 07h[3] for debounce information. The setting of this bit can be overridden via F1BAR1+I/O Offset 15h[4] to force an SMI.   |
| 7                     | <b>Reserved.</b> Must be set to 0   |
| 6                     | <b>USB_EN.</b> Allow USB events to generate a SCI.<br>0: Disable.<br>1: Enable  |
| 5                     | <b>THRM_EN.</b> Allow THRM# to generate an SCI.<br>0: Disable.<br>1: Enable   |
| 4                     | <b>SMI_EN.</b> Allow SMI events to generate an SCI.<br>0: Disable.<br>1: Enable   |
| 3                     | <b>GPIO_EN.</b> Allow GPIOs (GPIO47-GPIO32 and GPIO15-GPIO0) to generate an SCI.<br>0: Disable.<br>1: Enable.<br>F0BAR0+I/O Offset 08h/18h selects which GPIOs are enabled for PME generation. This bit (GPIO_EN) globally enables those selected GPIOs for generation of an SCI.   |
| 2:1                   | <b>Reserved.</b> Must be set to 0.  |
| 0                     | <b>PWR_U_REQ_EN.</b> Allow power-up request events from the SuperI/O module to generate an SCI.<br>0: Disable.<br>1: Enable.<br>A power-up request event is defined as any of the following events/activities: Modem, Telephone, Keyboard, Mouse, CEIR (Consumer Electronic Infrared)   |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 14h</b> <b>GPWIO Control Register 1 (R/W)</b> <b>Reset Value: 00h</b> |   |
| 7:4   | <b>Reserved.</b> Must be set to 0.  |
| 3   | <b>Reserved.</b>  |
| 2   | <b>GPWIO2_POL.</b> Select GPWIO2 polarity.<br>0: Active high<br>1: Active low   |
| 1   | <b>GPWIO1_POL.</b> Select GPWIO1 polarity.<br>0: Active high<br>1: Active low   |
| 0   | <b>GPWIO0_POL.</b> Select GPWIO0 polarity.<br>0: Active high<br>1: Active low   |
| <b>Offset 15h</b> <b>GPWIO Control Register 2 (R/W)</b> <b>Reset Value: 00h</b> |   |
| 7   | <b>Reserved.</b>  |
| 6   | <b>GPWIO_SMIEN2.</b> Allow GPWIO2 to generate an SMI.<br>0: Disable. (Default)<br>1: Enable.<br><br>A fixed high-to-low or low-to-high transition (debounce period) of 31 $\mu$ s exists in order for GPWIO2 to be recognized.<br>Bit 2 of this register must be set to 0 (input) for GPWIO2 to be able to generate an SMI.<br>If asserted, this bit overrides the setting of F1BAR1+I/O Offset 12h[10] and its status is reported in F1BAR0+I/O Offset 00h/02h[0]. |
| 5   | <b>GPWIO_SMIEN1.</b> Allow GPWIO1 to generate an SMI.<br>0: Disable. (Default)<br>1: Enable.<br><br>See F1BAR1+I/O Offset 07h[3] for debounce information.<br>Bit 1 of this register must be set to 0 (input) for GPWIO1 to be able to generate an SMI.<br>If asserted, this bit overrides the setting of F1BAR1+I/O Offset 12h[9] and its status is reported in F1BAR0+I/O Offset 00h/02h[0].  |
| 4   | <b>GPWIO_SMIEN0.</b> Allow GPWIO0 to generate an SMI.<br>0: Disable. (Default)<br>1: Enable.<br><br>See F1BAR1+I/O Offset 07h[3] for debounce information.<br>Bit 0 of this register must be set to 0 (input) for GPWIO0 to be able to generate an SMI.<br>If enabled, this bit overrides the setting of F1BAR1+I/O Offset 12h[8] and its status is reported in F1BAR0+I/O Offset 00h/02h[0].   |
| 3   | <b>Reserved.</b>  |
| 2   | <b>GPWIO2_DIR.</b> Selects the direction of GPWIO2.<br>0: Input.<br>1: Output.  |
| 1   | <b>GPWIO1_DIR.</b> Selects the direction of GPWIO1.<br>0: Input.<br>1: Output.  |
| 0   | <b>GPWIO0_DIR.</b> Selects the direction of the GPWIO0.<br>0: Input.<br>1: Output.  |

Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 16h</b> <span style="float:right"><b>Reset Value: 00h</b></span>  |   |
| <b>GPWIO Data Register (R/W)</b>  |   |
| This register contains the direct values of the GPWIO2-GPWIO0 pins. Write operations are valid only for bits defined as outputs. Reads from this register read the last written value if the pin is an output. The pins are configured as inputs or outputs in F1BAR1+I/O Offset 15h. |   |
| 7:4   | <b>Reserved.</b> Must be set to 0.  |
| 3   | <b>Reserved.</b>  |
| 2   | <b>GPWIO2_DATA.</b> Reflects the level of GPWIO2.<br>0: Low.<br>1: High.<br>A fixed high-to-low or low-to-high transition (debounce period) of 31 $\mu$ s exists in order for GPWIO2 to be recognized.  |
| 1   | <b>GPWIO1_DATA.</b> Reflects the level of GPWIO1.<br>0: Low.<br>1: High.<br>See F1BAR1+I/O Offset 07h[3] for debounce information.  |
| 0   | <b>GPWIO0_DATA.</b> Reflects the level of GPWIO0.<br>0: Low.<br>1: High.<br>See F1BAR1+I/O Offset 07h[3] for debounce information.  |
| <b>Offset 17h</b> <span style="float:right"><b>Reset Value: 00h</b></span>  |   |
| <b>Reserved</b>   |   |
| <b>Offset 18h-1Bh</b> <span style="float:right"><b>Reset Value: 0000F00h</b></span>   |   |
| <b>ACPI SCI_ROUTING Register (R/W)</b>  |   |
| 31:17   | <b>Reserved.</b>  |
| 16  | <b>PCTL_DELAYEN.</b> Allow staggered delays on the activation and deactivation of the power control pins PWRCNT1, PWRCNT2, and ONCTL# by 2 ms each.<br>0: Disable. (Default)<br>1: Enable.  |
| 15:12   | <b>Reserved.</b> Must be set to 0.  |
| 11  | <b>PLVL3_SMIEN.</b> Allow SMI generation when the PLVL3 Register (F1BAR1+I/O Offset 05h) is read.<br>0: Disable.<br>1: Enable. (Default)<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[4]. |
| 10  | <b>Reserved.</b> Must be set to 0.  |
| 9   | <b>SLP_SMIEN.</b> Allow SMI generation when the SLP_EN bit (F1BAR1+I/O Offset 0Ch[13]) is set.<br>0: Disable.<br>1: Enable. (Default)<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[2].    |
| 8   | <b>THT_SMIEN.</b> Allow SMI generation when the THT_EN bit (F1BAR1+I/O Offset 00h[4]) is set.<br>0: Disable.<br>1: Enable. (Default)<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[2].<br>Second level SMI status is reported at F1BAR0+I/O Offset 20h/22h[1].     |
| 7:4   | <b>Reserved.</b> Must be set to 0.  |

**Table 6-34. F1BAR1+I/O Offset: ACPI Support Registers (Continued)**

| Bit  | Description  |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
|--|--|---------------|-------------|------------|-------------|------------|------------|------------|-------------|----------------|------------|-------------|-------------|------------|------------|-------------|-------------|
| 3:0  | <p><b>SCI_IRQ_ROUTE.</b> SCI is routed to:</p> <table border="0"> <tr> <td>0000: Disable</td> <td>0100: IRQ4</td> <td>1000: IRQ8</td> <td>1100: IRQ12</td> </tr> <tr> <td>0001: IRQ1</td> <td>0101: IRQ5</td> <td>1001: IRQ9</td> <td>1101: IRQ13</td> </tr> <tr> <td>0010: Reserved</td> <td>0010: IRQ6</td> <td>1010: IRQ10</td> <td>1110: IRQ14</td> </tr> <tr> <td>0011: IRQ3</td> <td>0011: IRQ7</td> <td>1011: IRQ11</td> <td>1111: IRQ15</td> </tr> </table> <p>For more details see Section 6.2.6.3 "Programmable Interrupt Controller" on page 171.</p> | 0000: Disable | 0100: IRQ4  | 1000: IRQ8 | 1100: IRQ12 | 0001: IRQ1 | 0101: IRQ5 | 1001: IRQ9 | 1101: IRQ13 | 0010: Reserved | 0010: IRQ6 | 1010: IRQ10 | 1110: IRQ14 | 0011: IRQ3 | 0011: IRQ7 | 1011: IRQ11 | 1111: IRQ15 |
| 0000: Disable  | 0100: IRQ4   | 1000: IRQ8    | 1100: IRQ12 |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 0001: IRQ1   | 0101: IRQ5   | 1001: IRQ9    | 1101: IRQ13 |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 0010: Reserved   | 0010: IRQ6   | 1010: IRQ10   | 1110: IRQ14 |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 0011: IRQ3   | 0011: IRQ7   | 1011: IRQ11   | 1111: IRQ15 |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| <p><b>Offset 1Ch-1Fh</b> <span style="float:right"><b>ACPI Timer Register (RO)</b></span> <span style="float:right"><b>Reset Value: xxxxxxxh</b></span></p> <p><b>Note:</b> This register can also be read at F1BAR0+I/O Offset 1Ch.</p> |  |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 31:24  | <b>Reserved.</b>   |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 23:0   | <b>TMR_VAL. (Read Only)</b> This bit field contains the running count of the power management timer.   |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| <p><b>Offset 20h</b> <span style="float:right"><b>PM2_CNT — PM2 Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00h</b></span></p>   |  |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 7:1  | <b>Reserved.</b>   |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| 0  | <p><b>Arbiter Disable.</b> Disables the PCI arbiter when set by the OS. Used during C3 transition.</p> <p>0: Arbiter not disabled. (Default)</p> <p>1: Disable arbiter.</p>  |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |
| <p><b>Offset 21h-FFh</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00h</b></span></p> <p>The read value for these registers is undefined.</p>   |  |               |             |            |             |            |            |            |             |                |            |             |             |            |            |             |             |



### 6.4.3 IDE Controller Registers - Function 2

The register space designated as Function 2 (F2) is used to configure Channels 0 and 1 and the PCI portion of support hardware for the IDE controllers. The bit formats for the PCI Header/Channels 0 and 1 Registers are given in Table 6-35.

Located in the PCI Header Registers of F2 is a Base Address Register (F2BAR4) used for pointing to the register space designated for support of the IDE controllers, described later in this section.

**Table 6-35. F2: PCI Header/Channels 0 and 1 Registers for IDE Controller Configuration**

| Bit           | Description   |
|---------------|---|
| Index 00h-01h | Vendor Identification Register (RO) <span style="float:right">Reset Value: 100Bh</span>   |
| Index 02h-03h | Device Identification Register (RO) <span style="float:right">Reset Value: 0502h</span>   |
| Index 04h-05h | PCI Command Register (R/W) <span style="float:right">Reset Value: 0000h</span>  |
| 15:3          | <b>Reserved. (Read Only)</b>  |
| 2             | <b>Bus Master.</b> Allow the Core Logic module bus mastering capabilities.<br>0: Disable.<br>1: Enable. (Default)<br>This bit must be set to 1.   |
| 1             | <b>Reserved. (Read Only)</b>  |
| 0             | <b>I/O Space.</b> Allow the Core Logic module to respond to I/O cycles from the PCI bus.<br>0: Disable.<br>1: Enable.<br>This bit must be enabled, in order to access I/O offsets through F2BAR4 (for more information see F2 Index 20h).   |
| Index 06h-07h | PCI Status Register (RO) <span style="float:right">Reset Value: 0280h</span>  |
| Index 08h     | Device Revision ID Register (RO) <span style="float:right">Reset Value: 01h</span>  |
| Index 09h-0Bh | PCI Class Code Register (RO) <span style="float:right">Reset Value: 010180h</span>  |
| Index 0Ch     | PCI Cache Line Size Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Dh     | PCI Latency Timer Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Eh     | PCI Header Type (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 0Fh     | PCI BIST Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 10h-13h | Base Address Register 0 - F2BAR0 (RO) <span style="float:right">Reset Value: 00000000h</span><br>Reserved. Reserved for possible future use by the Core Logic module.   |
| Index 14h-17h | Base Address Register 1 - F2BAR1 (RO) <span style="float:right">Reset Value: 00000000h</span><br>Reserved. Reserved for possible future use by the Core Logic module.   |
| Index 18h-1Bh | Base Address Register 2 - F2BAR2 (RO) <span style="float:right">Reset Value: 00000000h</span><br>Reserved. Reserved for possible future use by the Core Logic module.   |
| Index 1Ch-1Fh | Base Address Register 3 - F2BAR3 (RO) <span style="float:right">Reset Value: 00000000h</span><br>Reserved. Reserved for possible future use by the Core Logic module.   |
| Index 20h-23h | Base Address Register 4 - F2BAR4 (R/W) <span style="float:right">Reset Value: 00000001h</span><br><b>Base Address 0 Register.</b> This register allows access to I/O mapped Bus Mastering IDE registers. Bits [3:0] are read only (0001), indicating a 16-byte I/O address range. Refer to Table 6-36 on page 277 for the IDE controller register bit formats and reset values. |
| 31:4          | <b>Bus Mastering IDE Base Address.</b>  |
| 3:0           | <b>Address Range. (Read Only)</b>   |
| Index 24h-2Bh | Reserved <span style="float:right">Reset Value: 00h</span>  |
| Index 2Ch-2Dh | Subsystem Vendor ID (RO) <span style="float:right">Reset Value: 100Bh</span>  |
| Index 2Eh-2Fh | Subsystem ID (RO) <span style="float:right">Reset Value: 0502h</span>   |

Table 6-35. F2: PCI Header/Channels 0 and 1 Registers for IDE Controller Configuration (Continued)

| Bit  | Description   |
|--|---|
| Index 30h-3Fh  | Reserved<br>Reset Value: 00h  |
| Index 40h-43h  | Channel 0 Drive 0 PIO Register (R/W)<br>Reset Value: 00009172h              |
| <p>If Index 44h[31] = 0, Format 0. Bits [15:0] configure the same timing control for both command and data.</p> <p>Format 0 settings for a Fast-PCI clock frequency of 33.3 MHz:</p> <ul style="list-style-type: none"> <li>— PIO Mode 0 = 00009172h</li> <li>— PIO Mode 1 = 00012171h</li> <li>— PIO Mode 2 = 00020080h</li> <li>— PIO Mode 3 = 00032010h</li> <li>— PIO Mode 4 = 00040010h</li> </ul> <p>Format 0 settings for a Fast-PCI clock frequency of 66.7 MHz:</p> <ul style="list-style-type: none"> <li>— PIO Mode 0 = 0000FFF4h</li> <li>— PIO Mode 1 = 0001F353h</li> <li>— PIO Mode 2 = 00028141h</li> <li>— PIO Mode 3 = 00034231h</li> <li>— PIO Mode 4 = 00041131h</li> </ul> <p><b>Note:</b> All references to "cycle" in the following bit descriptions are to a Fast-PCI clock cycle.</p> |   |
| 31:20  | <b>Reserved.</b> Must be set to 0.  |
| 19:16  | <b>PIOMODE.</b> PIO mode.   |
| 15:12  | <b>t2I.</b> Recovery time (value + 1 cycle).                                |
| 11:8   | <b>t3.</b> IDE_IOW# data setup time (value + 1 cycle).                      |
| 7:4  | <b>t2W.</b> IDE_IOW# width minus t3 (value + 1 cycle).                      |
| 3:0  | <b>t1.</b> Address Setup Time (value + 1 cycle).                            |
| <p>If Index 44h[31] = 1, Format 1. Bits [31:0] allow independent timing control for both command and data.</p> <p>Format 1 settings for a Fast-PCI clock frequency of 33.3 MHz:</p> <ul style="list-style-type: none"> <li>— PIO Mode 0 = 9172D132h</li> <li>— PIO Mode 1 = 21717121h</li> <li>— PIO Mode 2 = 00803020h</li> <li>— PIO Mode 3 = 20102010h</li> <li>— PIO Mode 4 = 00100010h</li> </ul> <p>Format 1 settings for a Fast-PCI clock frequency of 66.7 MHz:</p> <ul style="list-style-type: none"> <li>— PIO Mode 0 = F8E4F8E4h</li> <li>— PIO Mode 1 = 53F3F353h</li> <li>— PIO Mode 2 = 13F18141h</li> <li>— PIO Mode 3 = 42314231h</li> <li>— PIO Mode 4 = 11311131h</li> </ul> <p><b>Note:</b> All references to "cycle" in the following bit descriptions are to a Fast-PCI clock cycle.</p>  |   |
| 31:28  | <b>t2IC.</b> Command cycle recovery time (value + 1 cycle).                 |
| 27:24  | <b>t3C.</b> Command cycle IDE_IOW# data setup (value + 1 cycle).            |
| 23:20  | <b>t2WC.</b> Command cycle IDE_IOW# pulse width minus t3 (value + 1 cycle). |
| 19:16  | <b>t1C.</b> Command cycle address setup time (value + 1 cycle).             |
| 15:12  | <b>t2ID.</b> Data cycle recovery time (value + 1 cycle).                    |
| 11:8   | <b>t3D.</b> Data cycle IDE_IOW# data setup (value + 1 cycle).               |
| 7:4  | <b>t2WD.</b> Data cycle IDE_IOW# pulse width minus t3 (value + 1 cycle).    |
| 3:0  | <b>t1D.</b> Data cycle address Setup Time (value + 1 cycle).                |

**Table 6-35. F2: PCI Header/Channels 0 and 1 Registers for IDE Controller Configuration (Continued)**

| Bit  | Description  |
|--|--|
| <b>Index 44h-47h</b>   | <b>Channel 0 Drive 0 DMA Control Register (R/W)</b> <span style="float: right;"><b>Reset Value: 00077771h</b></span>   |
| The structure of this register depends on the value of bit 20.   |  |
| If bit 20 = 0, Multiword DMA   |  |
| Settings for a Fast-PCI clock frequency of 33.3 MHz:<br>— Multiword DMA Mode 0 = 00077771h<br>— Multiword DMA Mode 1 = 00012121h<br>— Multiword DMA Mode 2 = 00002020h |  |
| Settings for a Fast-PCI clock frequency of 66.7 MHz:<br>— Multiword DMA Mode 0 = 000FFF3h<br>— Multiword DMA Mode 1 = 00035352h<br>— Multiword DMA Mode 2 = 00015151h  |  |
| <b>Note:</b> All references to "cycle" in the following bit descriptions are to a Fast-PCI clock cycle.  |  |
| 31   | <b>PIO Mode Format.</b> This bit sets the PIO mode format for all channels and drives. Bit 31 of Offsets 2Ch, 34h, and 3Ch are R/W, but have no function so are defined as reserved.<br>0: Format 0.<br>1: Format 1. |
| 30:21  | <b>Reserved.</b> Must be set to 0.   |
| 20   | <b>DMA Select.</b> Selects type of DMA operation. 0: Multiword DMA   |
| 19:16  | <b>tKR.</b> IDE_IOR# recovery time (4-bit) (value + 1 cycle).  |
| 15:12  | <b>tDR.</b> IDE_IOR# pulse width (value + 1 cycle).  |
| 11:8   | <b>tKW.</b> IDE_IOW# recovery time (4-bit) (value + 1 cycle).  |
| 7:4  | <b>tDW.</b> IDE_IOW# pulse width (value + 1 cycle).  |
| 3:0  | <b>tM.</b> IDE_CS[1:0]# to IDE_IOR#/IOW# setup; IDE_CS[1:0]# setup to IDE_DACK0#/DACK1#.   |
| If bit 20 = 1, UltraDMA  |  |
| Settings for a Fast-PCI clock frequency of 33.3 MHz:<br>— UltraDMA Mode 0 = 00921250h<br>— UltraDMA Mode 1 = 00911140h<br>— UltraDMA Mode 2 = 00911030h                |  |
| Settings for a Fast-PCI clock frequency of 66.7 MHz:<br>— UltraDMA Mode 0 = 009436A1h<br>— UltraDMA Mode 1 = 00933481h<br>— UltraDMA Mode 2 = 00923261h                |  |
| <b>Note:</b> All references to "cycle" in the following bit descriptions are to a Fast-PCI clock cycle.  |  |
| 31   | <b>PIO Mode Format.</b> This bit sets the PIO mode format for all channels and drives. Bit 31 of Offsets 2Ch, 34h, and 3Ch are R/W, but have no function so are defined as reserved.<br>0: Format 0<br>1: Format 1   |
| 30:24  | <b>Reserved.</b> Must be set to 0.   |
| 23:21  | <b>BSIZE.</b> Input buffer threshold.  |
| 20   | <b>DMA Select.</b> Selects type of DMA operation. 1: UltraDMA.   |
| 19:16  | <b>tCRC.</b> CRC setup UDMA in IDE_DACK# (value + 1 cycle) (for host terminate CRC setup = tMLI + tSS).  |
| 15:12  | <b>tSS.</b> UDMA out (value + 1 cycle).  |
| 11:8   | <b>tCYC.</b> Data setup and cycle time UDMA out (value + 2 cycles).  |
| 7:4  | <b>tRP.</b> Ready to pause time (value + 1 cycle). Note: tRFS + 1 tRP on next clock.   |
| 3:0  | <b>tACK.</b> IDE_CS[1:0]# setup to IDE_DACK0#/DACK1# (value + 1 cycle).  |

Table 6-35. F2: PCI Header/Channels 0 and 1 Registers for IDE Controller Configuration (Continued)

| Bit           | Description   | Reset Value |
|---------------|---|-------------|
| Index 48h-4Bh | Channel 0 Drive 1 PIO Register (R/W)<br>Channel 0 Drive 1 Programmed I/O Control Register. See F2 Index 40h for bit descriptions.   | 00009172h   |
| Index 4Ch-4Fh | Channel 0 Drive 1 DMA Control Register (R/W)<br>Channel 0 Drive 1 MDMA/UDMA Control Register. See F2 Index 44h for bit descriptions.<br><b>Note:</b> The PIO Mode format is selected in F2 Index 44h[31], bit 31 of this register is defined as reserved. | 00077771h   |
| Index 50h-53h | Channel 1 Drive 0 PIO Register (R/W)<br>Channel 1 Drive 0 Programmed I/O Control Register. See F2 Index 40h for bit descriptions.   | 00009172h   |
| Index 54h-57h | Channel 1 Drive 0 DMA Control Register (R/W)<br>Channel 1 Drive 0 MDMA/UDMA Control Register. See F2 Index 44h for bit descriptions.<br><b>Note:</b> The PIO Mode format is selected in F2 Index 44h[31], bit 31 of this register is defined as reserved. | 00077771h   |
| Index 58h-5Bh | Channel 1 Drive 1 PIO Register (R/W)<br>Channel 1 Drive 1 Programmed I/O Control Register. See F2 Index 40h for bit descriptions.   | 00009172h   |
| Index 5Ch-5Fh | Channel 1 Drive 1 DMA Control Register (R/W)<br>Channel 1 Drive 1 MDMA/UDMA Control Register. See F2 Index 44h for bit descriptions.<br><b>Note:</b> The PIO Mode format is selected in F2 Index 44h[31], bit 31 of this register is defined as reserved. | 00077771h   |
| Index 60h-FFh | Reserved  | 00h         |

### 6.4.3.1 IDE Controller Support Registers

F2 Index 20h, Base Address Register 4 (F2BAR4), points to the base address of where the registers for IDE controller configuration are located. Table 6-36 gives the bit for-

mat of the I/O mapped IDE Controller Configuration registers that are accessed through F2BAR4.

**Table 6-36. F2BAR4+I/O Offset: IDE Controller Configuration Registers**

| Bit  | Description  |
|--|--|
| <b>Offset 00h IDE Bus Master 0 Command Register — Primary (R/W) Reset Value: 00h</b>           |  |
| 7:4  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 3  | <b>Read or Write Control.</b> Sets the direction of bus master transfers.<br>0: PCI reads performed.<br>1: PCI writes performed.<br>This bit should not be changed when the bus master is active.  |
| 2:1  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 0  | <b>Bus Master Control.</b> Controls the state of the bus master.<br>0: Disable master.<br>1: Enable master.<br>Bus master operations can be halted by setting this bit to 0. Once an operation has been halted, it cannot be resumed. If this bit is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer. |
| <b>Offset 01h Not Used</b>   |  |
| <b>Offset 02h IDE Bus Master 0 Status Register — Primary (R/W) Reset Value: 00h</b>            |  |
| 7  | <b>Simplex Mode. (Read Only)</b> Indicates if both the primary and secondary channel operate independently.<br>0: Yes.<br>1: No (simplex mode).  |
| 6  | <b>Drive 1 DMA Enable.</b> When asserted, allows Drive 1 to perform DMA transfers.<br>0: Disable.<br>1: Enable.  |
| 5  | <b>Drive 0 DMA Enable.</b> When asserted, allows Drive 0 to perform DMA transfers.<br>0: Disable.<br>1: Enable.  |
| 4:3  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 2  | <b>Bus Master Interrupt.</b> Indicates if the bus master detected an interrupt.<br>0: No.<br>1: Yes. Write 1 to clear.   |
| 1  | <b>Bus Master Error.</b> Indicates if the bus master detected an error during data transfer.<br>0: No.<br>1: Yes. Write 1 to clear.  |
| 0  | <b>Bus Master Active.</b> Indicates if the bus master is active.<br>0: No.<br>1: Yes.  |
| <b>Offset 03h Not Used</b>   |  |
| <b>Offset 04h-07h IDE Bus Master 0 PRD Table Address — Primary (R/W) Reset Value: 0000000h</b> |  |
| 31:2   | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains a PRD table pointer for IDE Bus Master 0.<br>When written, this field points to the first entry in a PRD table. Once IDE Bus Master 0 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this field (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.                              |
| 1:0  | <b>Reserved.</b> Must be set to 0.   |

Table 6-36. F2BAR4+I/O Offset: IDE Controller Configuration Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 08h IDE Bus Master 1 Command Register — Secondary (R/W) Reset Value: 00h</b>           |  |
| 7:4  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 3  | <b>Read or Write Control.</b> Sets the direction of bus master transfers.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit should not be changed when the bus master is active.  |
| 2:1  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 0  | <b>Bus Master Control.</b> Controls the state of the bus master.<br>0: Disable master.<br>1: Enable master.<br>Bus master operations can be halted by setting this bit to 0. Once an operation has been halted, it cannot be resumed. If this bit is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer. |
| <b>Offset 09h Not Used</b>   |  |
| <b>Offset 0Ah IDE Bus Master 1 Status Register — Secondary (R/W) Reset Value: 00h</b>            |  |
| 7  | <b>Reserved. (Read Only)</b>   |
| 6  | <b>Drive 1 DMA Capable.</b> Allow Drive 1 to perform DMA transfers.<br>0: Disable.<br>1: Enable.   |
| 5  | <b>Drive 0 DMA Capable.</b> Allow Drive 0 to perform DMA transfers.<br>0: Disable.<br>1: Enable.   |
| 4:3  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 2  | <b>Bus Master Interrupt.</b> Indicates if the bus master detected an interrupt.<br>0: No.<br>1: Yes. Write 1 to clear.   |
| 1  | <b>Bus Master Error.</b> Indicates if the bus master detected an error during data transfer.<br>0: No.<br>1: Yes. Write 1 to clear.  |
| 0  | <b>Bus Master Active.</b> Indicates if the bus master is active.<br>0: No.<br>1: Yes.  |
| <b>Offset 0Bh Not Used</b>   |  |
| <b>Offset 0Ch-0Fh IDE Bus Master 1 PRD Table Address — Secondary (R/W) Reset Value: 0000000h</b> |  |
| 31:2   | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains a PRD table pointer for IDE Bus Master 1.<br>When written, this field points to the first entry in a PRD table. Once IDE Bus Master 1 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this field (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.                              |
| 1:0  | <b>Reserved.</b> Must be set to 0.   |

### 6.4.4 Audio Registers - Function 3

The register designated as Function 3 (F3) is used to configure the PCI portion of support hardware for the audio registers. The bit formats for the PCI Header registers are given in Table 6-37.

A Base Address register (F3BAR0), located in the PCI Header registers of F3, is used for pointing to the register space designated for support of audio, described later in this section.

**Table 6-37. F3: PCI Header Registers for Audio Configuration**

| Bit           | Description   |
|---------------|---|
| Index 00h-01h | Vendor Identification Register (RO) <span style="float: right;">Reset Value: 100Bh</span>   |
| Index 02h-03h | Device Identification Register (RO) <span style="float: right;">Reset Value: 0503h</span>   |
| Index 04h-05h | PCI Command Register (R/W) <span style="float: right;">Reset Value: 0000h</span>  |
| 15:3          | Reserved. (Read Only)   |
| 2             | <b>Bus Master.</b> Allow the Core Logic module bus mastering capabilities.<br>0: Disable.<br>1: Enable. (Default)<br>This bit must be set to 1.   |
| 1             | <b>Memory Space.</b> Allow the Core Logic module to respond to memory cycles from the PCI bus.<br>0: Disable.<br>1: Enable.<br>This bit must be enabled to access memory offsets through F3BAR0 (See F3 Index 10h).   |
| 0             | Reserved. (Read Only)   |
| Index 06h-07h | PCI Status Register (RO) <span style="float: right;">Reset Value: 0280h</span>  |
| Index 08h     | Device Revision ID Register (RO) <span style="float: right;">Reset Value: 00h</span>  |
| Index 09h-0Bh | PCI Class Code Register (RO) <span style="float: right;">Reset Value: 040100h</span>  |
| Index 0Ch     | PCI Cache Line Size Register (RO) <span style="float: right;">Reset Value: 00h</span>   |
| Index 0Dh     | PCI Latency Timer Register (RO) <span style="float: right;">Reset Value: 00h</span>   |
| Index 0Eh     | PCI Header Type (RO) <span style="float: right;">Reset Value: 00h</span>  |
| Index 0Fh     | PCI BIST Register (RO) <span style="float: right;">Reset Value: 00h</span>  |
| Index 10h-13h | Base Address Register - F3BAR0 (R/W) <span style="float: right;">Reset Value: 00000000h</span><br>This register sets the base address of the memory mapped audio interface control register block. This is a 128-byte block of registers used to control the audio FIFO and codec interface, as well as to support VSA SMIs. Bits [11:0] are read only (0000 0000 0000), indicating a 4 KB memory address range. Refer to Table 6-38 on page 280 for the audio configuration register bit formats and reset values. |
| 31:12         | Audio Interface Base Address  |
| 11:0          | Address Range. (Read Only)  |
| Index 14h-2Bh | Reserved <span style="float: right;">Reset Value: 00h</span>  |
| Index 2Ch-2Dh | Subsystem Vendor ID (RO) <span style="float: right;">Reset Value: 100Bh</span>  |
| Index 2Eh-2Fh | Subsystem ID (RO) <span style="float: right;">Reset Value: 0503h</span>   |
| Index 30h-FFh | Reserved <span style="float: right;">Reset Value: 00h</span>  |

#### 6.4.4.1 Audio Support Registers

F3 Index 10h, Base Address Register 0 (F3BAR0), points to the base address of where the registers for audio support are located. Table 6-38 gives the bit formats of the

memory mapped audio configuration registers that are accessed through F3BAR0.

**Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers**

| Bit   | Description  |
|---|--|
| <b>Offset 00h-03h</b> <span style="float:right"><b>Codec GPIO Status Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span>  |  |
| 31  | <b>Codec GPIO Interface.</b><br>0: Disable.<br>1: Enable.  |
| 30  | <b>Codec GPIO SMI.</b> When asserted, allows codec GPIO interrupt to generate an SMI.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].<br>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[1].         |
| 29:21   | <b>Reserved.</b> Must be set to 0.   |
| 20  | <b>Codec GPIO Status Valid. (Read Only)</b> Indicates if the status read is valid.<br>0: Yes.<br>1: No.  |
| 19:0  | <b>Codec GPIO Pin Status. (Read Only)</b> This field indicates the GPIO pin status that is received from the codec in slot 12 on the SDATA_IN signal.  |
| <b>Offset 04h-07h</b> <span style="float:right"><b>Codec GPIO Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span> |  |
| 31:20   | <b>Reserved.</b> Must be set to 0.   |
| 19:0  | <b>Codec GPIO Pin Data.</b> This field indicates the GPIO pin data that is sent to the codec in slot 12 on the SDATA_OUT signal.   |
| <b>Offset 08h-0Bh</b> <span style="float:right"><b>Codec Status Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span>       |  |
| 31:24   | <b>Codec Status Address. (Read Only)</b> Address of the register for which status is being returned. This address comes from slot 1 bits [19:12].  |
| 23  | <b>Codec Serial INT Enable.</b> When asserted, allows codec serial interrupt to cause an SMI.<br>0: Disable.<br>1: Enable.<br>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].<br>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[1]. |
| 22  | <b>SYNC Pin.</b> Sets SYNC high or low.<br>0: Low.<br>1: High.   |
| 21  | <b>SDATA_IN2_EN.</b> When enabled, allows use of SDATA_IN2 input.<br>0: Disable.<br>1: Enable.   |
| 20  | <b>Audio Bus Master 5 AC97 Slot Select.</b> Selects slot for Audio Bus Master 5 to receive data.<br>0: Slot 6.<br>1: Slot 11.  |
| 19  | <b>Audio Bus Master 4 AC97 Slot Select.</b> Selects slot for Audio Bus Master 4 to transmit data.<br>0: Slot 6.<br>1: Slot 11.   |
| 18  | <b>Reserved.</b> Must be set to 0.   |
| 17  | <b>Status Tag. (Read Only)</b> The codec status data in bits [15:0] of this register is updated in the current AC97 frame. (codec ready, slot1 and slot2 bits in tag slot are all set in current AC97 frame).<br>0: Not new.<br>1: New, updated in current frame.          |



Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| 16  | <b>Codec Status Valid. (Read Only)</b> Indicates if the status in bits [15:0] of this register is valid. This bit is high during slots 3 to 11 of the AC97 frame (i.e., for approximately 14.5 $\mu$ s), for every frame.<br>0: No.<br>1: Yes.   |
| 15:0  | <b>Codec Status. (Read Only)</b> This is the codec status data that is received from the codec in slot 2 on SDATA_IN. Only bits [19:4] are used from slot 2. If this register is read with both bits 16 and 17 of this register set to 1, this field is updated in the current AC97 frame, and codec status data is valid. This bit field is updated only if the codec sent status data. |
| <b>Offset 0Ch-0Fh</b> <b>Codec Command Register (R/W)</b> <b>Reset Value: 0000000h</b>  |  |
| 31:24   | <b>Codec Command Address.</b> Address of the codec control register for which the command is being sent. This address goes in slot 1 bits [19:12] on SDATA_OUT.  |
| 23:22   | <b>Codec Communication.</b> Indicates the codec that the Core Logic module is communicating with.<br>00: Primary codec<br>01: Secondary codec<br>10: Third codec<br>11: Fourth codec<br>Only 00 and 01 are valid settings for this bit field.  |
| 21:17   | <b>Reserved.</b> Must be set to 0.   |
| 16  | <b>Codec Command Valid. (Read Only)</b> Indicates if the command in bits [15:0] of this register is valid.<br>0: No.<br>1: Yes.<br>This bit is set by hardware when a codec command is written to the Codec Command register. It remains set until the command has been sent to the codec.   |
| 15:0  | <b>Codec Command.</b> This is the command being sent to the codec in bits [19:4] of slot 2 on SDATA_OUT.   |
| <b>Offset 10h-11h</b> <b>Second Level Audio SMI Status Register (RC)</b> <b>Reset Value: 0000h</b><br>The bits in this register contain second level SMI status reporting. Top level is reported at F1BAR0+I/O Offset 00h/02h[1]. Reading this register clears the status bits at both the second and top levels. Note that bit 0 has a third level of status reporting which also must be "read to clear".<br>A read-only "Mirror" version of this register exists at F3BAR0+I/O Memory Offset 12h. If the value of the register must be read without clearing the SMI source (and consequently de-asserting SMI), F3BAR0+Memory Offset 12h can be read instead. |  |
| 15:8  | <b>Reserved.</b> Must be set to 0.   |
| 7   | <b>Audio Bus Master 5 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 5.<br>0: No.<br>1: Yes.<br>SMI generation is enabled when Audio Bus Master 5 is enabled (F3BAR0+Memory Offset 48h[0] = 1).<br>An SMI is then generated when the End of Page bit is set in the Audio Bus Master 5 SMI Status Register (F3BAR0+Memory Offset 49h[0] = 1).   |
| 6   | <b>Audio Bus Master 4 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 4.<br>0: No.<br>1: Yes.<br>SMI generation is enabled when Audio Bus Master 4 is enabled (F3BAR0+Memory Offset 40h[0] = 1).<br>An SMI is then generated when the End of Page bit is set in the Audio Bus Master 4 SMI Status Register (F3BAR0+Memory Offset 41h[0] = 1).   |
| 5   | <b>Audio Bus Master 3 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 3.<br>0: No.<br>1: Yes.<br>SMI generation is enabled when Audio Bus Master 3 is enabled (F3BAR0+Memory Offset 38h[0] = 1).<br>An SMI is then generated when the End of Page bit is set in the Audio Bus Master 3 SMI Status Register (F3BAR0+Memory Offset 39h[0] = 1).   |



**Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)**

| Bit  | Description  |
|--|--|
| 4  | <p><b>Audio Bus Master 2 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 2.</p> <p>0: No.<br/>1: Yes.</p> <p>SMI generation is enabled when Audio Bus Master 2 is enabled (F3BAR0+Memory Offset 30h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR0+Memory Offset 31h[0] = 1). The End of Page bit must be cleared before this bit can be cleared.</p>   |
| 3  | <p><b>Audio Bus Master 1 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 1.</p> <p>0: No.<br/>1: Yes.</p> <p>SMI generation is enabled when Audio Bus Master 1 is enabled (F3BAR0+Memory Offset 28h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR0+Memory Offset 29h[0] = 1). The End of Page bit must be cleared before this bit can be cleared.</p>   |
| 2  | <p><b>Audio Bus Master 0 SMI Status.</b> Indicates if an SMI was caused by an event occurring on Audio Bus Master 0.</p> <p>0: No.<br/>1: Yes.</p> <p>SMI generation is enabled when Audio Bus Master 0 is enabled (F3BAR0+Memory Offset 20h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR0+Memory Offset 21h[0] = 1). The End of Page bit must be cleared before this bit can be cleared.</p>   |
| 1  | <p><b>Codec Serial or GPIO Interrupt SMI Status.</b> Indicates if an SMI was caused by a serial or GPIO interrupt from codec.</p> <p>0: No.<br/>1: Yes.</p> <p>SMI generation enabling for codec serial interrupt: F3BAR0+Memory Offset 08h[23] = 1.<br/>SMI generation enabling for codec GPIO interrupt: F3BAR0+Memory Offset 00h[30] = 1.</p>   |
| 0  | <p><b>I/O Trap SMI Status.</b> Indicates if an SMI was caused by an I/O trap.</p> <p>0: No.<br/>1: Yes.</p> <p>The next level (third level) of SMI status reporting is at F3BAR0+Memory Offset 14h.</p>  |
| <p><b>Offset 14h-17h I/O Trap SMI and Fast Write Status Register (RO/RC) Reset Value: 0000000h</b></p> <p><b>Note:</b> For the four SMI status bits (bits [13:10]), if the activity was a fast write to an even address, no SMI is generated regardless of the DMA, MPU, or Sound Card status. If the activity was a fast write to an odd address, an SMI is generated but bit 13 is set to a 1.</p> |  |
| 31:24  | <p><b>Fast Path Write Even Access Data. (Read Only)</b> This bit field contains the data from the last Fast Path Write Even access. These bits change only on a fast write to an even address.</p>   |
| 23:16  | <p><b>Fast Path Write Odd Access Data. (Read Only)</b> This bit field contains the data from the last Fast Path Write Odd access. These bits change on a fast write to an odd address, and also on any non-fast write.</p>   |
| 15   | <p><b>Fast Write A1. (Read Only)</b> This bit contains the A1 value for the last Fast Write access.</p>  |
| 14   | <p><b>Read or Write I/O Access. (Read Only)</b> Indicates if the last trapped I/O access was a read or a write.</p> <p>0: Read.<br/>1: Write.</p>  |
| 13   | <p><b>Sound Card or FM Trap SMI Status. (Read to Clear)</b> Indicates if an SMI was caused by a trapped I/O access to the Sound Card or FM I/O Trap.</p> <p>0: No.<br/>1: Yes. (See the note included in the general description of this register above.)</p> <p>Fast Path Write must be enabled, F3BAR0+Memory Offset 18h[11] = 1, for the SMI to be reported here. If Fast Path Write is disabled, the SMI is reported in bit 10 of this register.</p> <p>This is the third level of SMI status reporting.<br/>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].<br/>Top level is reported at F1BAR0+I/O Offset 00h/02h[1].<br/>SMI generation enabling is at F3BAR0+Memory Offset 18h[2].</p> |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| 12   | <p><b>DMA Trap SMI Status. (Read to Clear)</b> Indicates if an SMI was caused by a trapped I/O access to the DMA I/O Trap.</p> <p>0: No.</p> <p>1: Yes. (See the note included in the general description of this register above.)</p> <p>This is the third level of SMI status reporting.</p> <p>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Top level is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>SMI generation enabling is at F3BAR0+Memory Offset 18h[8:7].</p>   |
| 11   | <p><b>MPU Trap SMI Status. (Read to Clear)</b> Indicates if an SMI was caused by a trapped I/O access to the MPU I/O Trap.</p> <p>0: No.</p> <p>1: Yes. (See the note included in the general description of this register above.)</p> <p>This is the third level of SMI status reporting.</p> <p>Second level of SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Top level is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>SMI generation enabling is at F3BAR0+Memory Offset 18h[6:5].</p>  |
| 10   | <p><b>Sound Card or FM Trap SMI Status. (Read to Clear)</b> Indicates if an SMI was caused by a trapped I/O access to the Sound Card or FM I/O Trap.</p> <p>0: No.</p> <p>1: Yes. (See the note included in the general description of this register above.)</p> <p>Fast Path Write must be disabled, F3BAR0+Memory Offset 18h[11] = 0, for the SMI to be reported here. If Fast Path Write is enabled, the SMI is reported in bit 13 of this register.</p> <p>This is the third level of SMI status reporting.</p> <p>Second level of SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Top level is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>SMI generation enabling is at F3BAR0+Memory Offset 18h[2].</p> |
| 9:0  | <b>X-Bus Address (Read Only).</b> This bit field] contains the captured ten bits of X-Bus address.  |
| <b>Offset 18h-19h I/O Trap SMI Enable Register (R/W) )Reset Value: 0000h</b> |   |
| 15:12  | <b>Reserved.</b> Must be set to 0.  |
| 11   | <p><b>Fast Path Write Enable.</b> Fast Path Write (an SMI is not generated on certain writes to specified addresses).</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>In Fast Path Write, the Core Logic module responds to writes to addresses: 388h, 38Ah, 38B, 2x0h, 2x2h, and 2x8h.</p>   |
| 10:9   | <b>Fast Read.</b> These two bits hold part of the response that the Core Logic module returns for reads to several I/O locations.   |
| 8  | <p><b>High DMA I/O Trap.</b> If this bit is enabled and an access occurs at I/O Port C0h-DFh, an SMI is generated.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Third level SMI status is reported at F3BAR0+Memory Offset 14h[12].</p>  |
| 7  | <p><b>Low DMA I/O Trap.</b> If this bit is enabled and an access occurs at I/O Port 00h-0Fh, an SMI is generated.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Third level SMI status is reported at F3BAR0+Memory Offset 14h[12].</p>   |
| 6  | <p><b>High MPU I/O Trap.</b> If this bit is enabled and an access occurs at I/O Port 330h-331h, an SMI is generated.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].</p> <p>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p> <p>Third level SMI status is reported at F3BAR0+Memory Offset 14h[11].</p>  |

**Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)**

| Bit                                       | Description  |
|---|--|
| 5   | <p><b>Low MPU I/O Trap.</b> If this bit is enabled and an access occurs at I/O Port 300h-301h, an SMI is generated.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].<br/>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].<br/>Third level SMI status is reported at F3BAR0+Memory Offset 14h[11].</p>                           |
| 4   | <p><b>Fast Path Read Enable/SMI Disable.</b> When asserted, read Fast Path (an SMI is not generated on reads from specified addresses).</p> <p>0: Disable.<br/>1: Enable.</p> <p>In Fast Path Read the Core Logic module responds to reads of addresses: 388h-38Bh; 2x0h, 2x1, 2x2h, 2x3, 2x8 and 2x9h.<br/>If neither sound card nor FM I/O mapping is enabled, then status read trapping is not possible.</p>  |
| 3   | <p><b>FM I/O Trap.</b> If this bit is enabled and an access occurs at I/O Port 388h-38Bh, an SMI is generated.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].<br/>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].</p>  |
| 2   | <p><b>Sound Card I/O Trap.</b> If this bit is enabled and an access occurs in the address ranges selected by bits [1:0], an SMI is generated.</p> <p>0: Disable.<br/>1: Enable.</p> <p>Top level SMI status is reported at F1BAR0+I/O Offset 00h/02h[1].<br/>Second level SMI status is reported at F3BAR0+Memory Offset 10h/12h[0].<br/>Third level SMI status is reported at F3BAR0+Memory Offset 14h[10].</p> |
| 1:0                                       | <p><b>Sound Card Address Range Select.</b> These bits select the address range for the sound card I/O trap.</p> <p>00: I/O Port 220h-22Fh                      10: I/O Port 260h-26Fh<br/>01: I/O Port 240h-24Fh                      11: I/O Port 280h-28Fh</p>   |
| <b>Offset 1Ah-1Bh</b>                     |  |
| <b>Internal IRQ Enable Register (R/W)</b> |  |
| <b>Reset Value: 0000h</b>                 |  |
| 15  | <p><b>IRQ15 Internal.</b> Configures IRQ15 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 14  | <p><b>IRQ14 Internal.</b> Configures IRQ14 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 13  | <b>Reserved.</b> Must be set to 0.   |
| 12  | <p><b>IRQ12 Internal.</b> Configures IRQ12 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 11  | <p><b>IRQ11 Internal.</b> Configures IRQ11 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 10  | <p><b>IRQ10 Internal.</b> Configures IRQ10 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 9   | <p><b>IRQ9 Internal.</b> Configures IRQ9 for internal (software) or external (hardware) use.</p> <p>0: External.<br/>1: Internal.</p>  |
| 8   | <b>Reserved.</b> Must be set to 0.   |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| 7  | <b>IRQ7 Internal.</b> Configures IRQ7 for internal (software) or external (hardware) use.<br>0: External.<br>1: Internal. |
| 6  | <b>Reserved.</b> Must be set to 0.  |
| 5  | <b>IRQ5 Internal.</b> Configures IRQ5 for internal (software) or external (hardware) use.<br>0: External.<br>1: Internal. |
| 4  | <b>IRQ4 Internal.</b> Configures IRQ4 for internal (software) or external (hardware) use.<br>0: External.<br>1: Internal. |
| 3  | <b>IRQ3 Internal.</b> Configures IRQ3 for internal (software) or external (hardware) use.<br>0: External.<br>1: Internal. |
| 2  | <b>Reserved.</b> Must be set to 0.  |
| 1  | <b>IRQ1 Internal.</b> Configures IRQ1 for internal (software) or external (hardware) use.<br>0: External.<br>1: Internal. |
| 0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Offset 1Ch-1Fh</b>  |   |
| <b>Internal IRQ Control Register (R/W)</b>   |   |
| <b>Reset Value: 0000000h</b>   |   |
| <b>Note:</b> Bits 31:16 of this register are Write Only. Reads to these bits always return a value of 0. |   |
| 31   | <b>Mask Internal IRQ15. (Write Only)</b><br>0: Disable.<br>1: Enable.   |
| 30   | <b>Mask Internal IRQ14. (Write Only)</b><br>0: Disable.<br>1: Enable.   |
| 29   | <b>Reserved. (Write Only)</b> Must be set to 0.   |
| 28   | <b>Mask Internal IRQ12. (Write Only)</b><br>0: Disable.<br>1: Enable.   |
| 27   | <b>Mask Internal IRQ11. (Write Only)</b><br>0: Disable.<br>1: Enable.   |
| 26   | <b>Mask Internal IRQ10. (Write Only)</b><br>0: Disable.<br>1: Enable.   |
| 25   | <b>Mask Internal IRQ9. (Write Only)</b><br>0: Disable.<br>1: Enable.  |
| 24   | <b>Reserved. (Write Only)</b> Must be set to 0.   |
| 23   | <b>Mask Internal IRQ7. (Write Only)</b><br>0: Disable.<br>1: Enable.  |
| 22   | <b>Reserved. (Write Only)</b> Must be set to 0.   |
| 21   | <b>Mask Internal IRQ5. (Write Only)</b><br>0: Disable.<br>1: Enable.  |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit | Description  |
|-----|--|
| 20  | <b>Mask Internal IRQ4. (Write Only)</b><br>0: Disable.<br>1: Enable. |
| 19  | <b>Mask Internal IRQ3. (Write Only)</b><br>0: Disable.<br>1: Enable. |
| 18  | <b>Reserved. (Write Only)</b> Must be set to 0.                      |
| 17  | <b>Mask Internal IRQ1. (Write Only)</b><br>0: Disable.<br>1: Enable. |
| 16  | <b>Reserved. (Write Only)</b> Must be set to 0.                      |
| 15  | <b>Assert Masked Internal IRQ15.</b><br>0: Disable.<br>1: Enable.    |
| 14  | <b>Assert Masked Internal IRQ14.</b><br>0: Disable.<br>1: Enable.    |
| 13  | <b>Reserved.</b> Set to 0.   |
| 12  | <b>Assert Masked Internal IRQ12.</b><br>0: Disable.<br>1: Enable.    |
| 11  | <b>Assert masked internal IRQ11.</b><br>0: Disable.<br>1: Enable.    |
| 10  | <b>Assert Masked Internal IRQ10.</b><br>0: Disable.<br>1: Enable.    |
| 9   | <b>Assert Masked Internal IRQ9.</b><br>0: Disable.<br>1: Enable.     |
| 8   | <b>Reserved.</b> Set to 0.   |
| 7   | <b>Assert Masked Internal IRQ7.</b><br>0: Disable.<br>1: Enable.     |
| 6   | <b>Reserved.</b> Set to 0.   |
| 5   | <b>Assert Masked Internal IRQ5.</b><br>0: Disable.<br>1: Enable.     |
| 4   | <b>Assert Masked Internal IRQ4.</b><br>0: Disable.<br>1: Enable.     |
| 3   | <b>Assert Masked Internal IRQ3.</b><br>0: Disable.<br>1: Enable.     |
| 2   | <b>Reserved.</b> Must be set to 0.                                   |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| 1  | <b>Assert Masked Internal IRQ1.</b><br>0: Disable.<br>1: Enable.  |
| 0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Offset 20h Audio Bus Master 0 Command Register (R/W) Reset Value: 00h</b>           |   |
| Audio Bus Master 0: Output to codec; 32-bit; Left and Right Channels; Slots 3 and 4.   |   |
| 7:4  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 3  | <b>Read or Write Control.</b> Sets the transfer direction of the Audio Bus Master.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 0 (read), and should not be changed when the bus master is active.   |
| 2:1  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 0  | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers.<br>When writing 0 to this bit, the bus master must either be paused, or reach EOT. Writing 0 to this bit while the bus master is operating may result in unpredictable behavior (and may crash the bus master state machine). The only recovery from such unpredictable behavior is a PCI reset. |
| <b>Offset 21h Audio Bus Master 0 SMI Status Register (RC) Reset Value: 00h</b>         |   |
| Audio Bus Master 0: Output to codec; 32-bit; Left and Right Channels; Slots 3 and 4.   |   |
| 7:2  | <b>Reserved.</b>  |
| 1  | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software has cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.   |
| 0  | <b>End of Page.</b> Indicates if the bus master transferred data which is marked by EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.   |
| <b>Offset 22h-23h Not Used</b>   |   |
| <b>Offset 24h-27h Audio Bus Master 0 PRD Table Address (R/W) Reset Value: 0000000h</b> |   |
| Audio Bus Master 0: Output to codec; 32-bit; Left and Right Channels; Slots 3 and 4.   |   |
| 31:2   | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains a PRD table pointer for Audio Bus Master 0.<br>When written, this register points to the first entry in a PRD table. Once Audio Bus Master 0 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.   |
| 1:0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Note:</b>   | The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs.<br><br>DWORD 0:        [31:0] = Memory Region Physical Base Address<br>DWORD 1:        31    = End of Table Flag<br>30    = End of Page Flag<br>29    = Loop Flag (JMP)<br>[28:16] = Reserved (0)<br>[15:0] = Byte Count of the Region (Size)                                     |



Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 28h</b> <b>Audio Bus Master 1 Command Register (R/W)</b> <b>Reset Value: 00h</b>  |  |
| Audio Bus Master 1: Input from codec; 32-Bit; Left and Right Channels; Slots 3 and 4.   |  |
| 7:4   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 3   | <b>Read or Write Control.</b> Set the transfer direction of Audio Bus Master 1.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 1 (write) and should not be changed when the bus master is active.   |
| 2:1   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 0   | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master 1.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior (and may cause a crash of the bus master state machine). The only recovery from this condition is a PCI reset. |
| <b>Offset 29h</b> <b>Audio Bus Master 1 SMI Status Register (RC)</b> <b>Reset Value: 00h</b>  |  |
| Audio Bus Master 1: Input from codec; 32-Bit; Left and Right Channels; Slots 3 and 4.   |  |
| 7:2   | <b>Reserved.</b>   |
| 1   | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software has cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.  |
| 0   | <b>End of Page.</b> Indicates if the bus master transferred data which is marked by EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.  |
| <b>Offset 2Ah-2Bh</b> <b>Not Used</b>   |  |
| <b>Offset 2Ch-2Fh</b> <b>Audio Bus Master 1 PRD Table Address (R/W)</b> <b>Reset Value: 0000000h</b>  |  |
| Audio Bus Master 1: Input from codec; 32-Bit; Left and Right Channels; Slots 3 and 4.   |  |
| 31:2  | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field is a PRD table pointer for Audio Bus Master 1.<br>When written, this register points to the first entry in a PRD table. Once Audio Bus Master 1 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.  |
| 1:0   | <b>Reserved.</b> Must be set to 0.   |
| <b>Note:</b> The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs.<br><div style="margin-left: 40px;">           DWORD 0:        [31:0] = Memory Region Physical Base Address<br/>           DWORD 1:        31     = End of Table Flag<br/>                            30     = End of Page Flag<br/>                            29     = Loop Flag (JMP)<br/>                            [28:16] = Reserved (0)<br/>                            [15:0] = Byte Count of the Region (Size)         </div> |  |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 30h</b> <b>Audio Bus Master 2 Command Register (R/W)</b> <b>Reset Value: 00h</b>   |   |
| Audio Bus Master 2: Output to codec; 16-Bit; Slot 5.   |   |
| 7:4  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 3  | <b>Read or Write Control.</b> Sets the transfer direction of Audio Bus Master 2.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 0 (read) and should not be changed when the bus master is active.  |
| 2:1  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 0  | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master 2.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers. When writing 0 to this bit, the bus master must be either paused or reached EOT. Writing 0 to this bit while the bus master is operating results in unpredictable behavior (and may crash the bus master state machine). The only recovery from this condition is a PCI reset. |
| <b>Offset 31h</b> <b>Audio Bus Master 2 SMI Status Register (RC)</b> <b>Reset Value: 00h</b>   |   |
| Audio Bus Master 2: Output to codec; 16-Bit; Slot 5.   |   |
| 7:2  | <b>Reserved.</b>  |
| 1  | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software has cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.   |
| 0  | <b>End of Page.</b> Indicates if the Bus master transferred data which is marked by the EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.   |
| <b>Offset 32h-33h</b> <b>Not Used</b> <b>Reset Value: 00h</b>  |   |
| <b>Offset 34h-37h</b> <b>Audio Bus Master 2 PRD Table Address (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| Audio Bus Master 2: Output to codec; 16-Bit; Slot 5.   |   |
| 31:2   | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains a PRD table pointer for Audio Bus Master 2.<br>When written, this field points to the first entry in a PRD table. Once Audio Bus Master 2 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.                                      |
| 1:0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Note:</b> The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs. |   |
|  | DWORD 0: [31:0] = Memory Region Physical Base Address   |
|  | DWORD 1: 31 = End of Table Flag   |
|  | 30 = End of Page Flag   |
|  | 29 = Loop Flag (JMP)  |
|  | [28:16] = Reserved (0)  |
|  | [15:0] = Byte Count of the Region (Size)  |

**Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)**

| Bit   | Description  |
|---|--|
| <b>Offset 38h</b> <b>Audio Bus Master 3 Command Register (R/W)</b> <b>Reset Value: 00h</b><br>Audio Bus Master 3: Input from codec; 16-Bit; Slot 5.   |  |
| 7:4   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 3   | <b>Read or Write Control.</b> Sets the transfer direction of Audio Bus Master 3.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 1 (write) and should not be changed when the bus master is active.  |
| 2:1   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.   |
| 0   | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master 3.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers. When writing 0 to this bit, the bus master must be either paused or have reached EOT. Writing 0 to this bit while the bus master is operating results in unpredictable behavior (and may crash the bus master state machine). The only recovery from this condition is a PCI reset. |
| <b>Offset 39h</b> <b>Audio Bus Master 3 SMI Status Register (RC)</b> <b>Reset Value: 00h</b><br>Audio Bus Master 3: Input from codec; 16-Bit; Slot 5.   |  |
| 7:2   | <b>Reserved.</b>   |
| 1   | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software cleared the first, it causes the bus master to pause until this register is read to clear the error.  |
| 0   | <b>End of Page.</b> Indicates if the bus master transferred data which is marked by the EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.  |
| <b>Offset 3Ah-3Bh</b> <b>Not Used</b>   |  |
| <b>Offset 3Ch-3Fh</b> <b>Audio Bus Master 3 PRD Table Address (R/W)</b> <b>Reset Value: 0000000h</b><br>Audio Bus Master 3: Input from codec; 16-Bit; Slot 5.   |  |
| 31:2  | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains is a PRD table pointer for Audio Bus Master 3.<br>When written, this field points to the first entry in a PRD table. Once Audio Bus Master 3 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.  |
| 1:0   | <b>Reserved.</b> Must be set to 0.   |
| <b>Note:</b> The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs.<br><p style="margin-left: 40px;">           DWORD 0:        [31:0] = Memory Region Physical Base Address<br/>           DWORD 1:        31     = End of Table Flag<br/>                            30     = End of Page Flag<br/>                            29     = Loop Flag (JMP)<br/>                            [28:16] = Reserved (0)<br/>                            [15:0] = Byte Count of the Region (Size)         </p> |  |

Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 40h</b> <b>Audio Bus Master 4 Command Register (R/W)</b> <b>Reset Value: 00h</b>   |   |
| Audio Bus Master 4: Output to codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[19] selects slot).   |   |
| 7:4  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 3  | <b>Read or Write Control.</b> Set the transfer direction of Audio Bus Master 4.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 0 (read) and should not be changed when the bus master is active.   |
| 2:1  | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 0  | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master 4.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers. When writing 0 to this bit, the bus master must be either paused or have reached EOT. Writing 0 to this bit while the bus master is operating, results in unpredictable behavior (and may crash the bus master state machine). The only recovery from this condition is a PCI reset. |
| <b>Offset 41h</b> <b>Audio Bus Master 4 SMI Status Register (RC)</b> <b>Reset Value: 00h</b>   |   |
| Audio Bus Master 4: Output to codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[19] selects slot).   |   |
| 7:2  | <b>Reserved.</b>  |
| 1  | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software cleared the first, it causes the bus master to pause until this register is read to clear the error.   |
| 0  | <b>End of Page.</b> Bus master transferred data which is marked by the EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.  |
| <b>Offset 42h-43h</b> <b>Not Used</b>  |   |
| <b>Offset 44h-47h</b> <b>Audio Bus Master 4 PRD Table Address (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| Audio Bus Master 4: Output to codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[19] selects slot).   |   |
| 31:2   | <b>Pointer to the Physical Region Descriptor Table.</b> This register is a PRD table pointer for Audio Bus Master 4.<br>When written, this register points to the first entry in a PRD table. Once Audio Bus Master 4 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.  |
| 1:0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Note:</b> The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs. |   |
|  | DWORD 0: [31:0] = Memory Region Physical Base Address   |
|  | DWORD 1: 31 = End of Table Flag   |
|  | 30 = End of Page Flag   |
|  | 29 = Loop Flag (JMP)  |
|  | [28:16] = Reserved (0)  |
|  | [15:0] = Byte Count of the Region (Size)  |

**Table 6-38. F3BAR0+Memory Offset: Audio Configuration Registers (Continued)**

| Bit   | Description   |
|---|---|
| <b>Offset 48h</b> <b>Audio Bus Master 5 Command Register (R/W)</b> <b>Reset Value: 00h</b>  |   |
| Audio Bus Master 5: Input from codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[20] selects slot).   |   |
| 7:4   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 3   | <b>Read or Write Control.</b> Set the transfer direction of Audio Bus Master 5.<br>0: PCI reads are performed.<br>1: PCI writes are performed.<br>This bit must be set to 1 (write) and should not be changed when the bus master is active.  |
| 2:1   | <b>Reserved.</b> Must be set to 0. Must return 0 on reads.  |
| 0   | <b>Bus Master Control.</b> Controls the state of the Audio Bus Master 5.<br>0: Disable.<br>1: Enable.<br>Setting this bit to 1 enables the bus master to begin data transfers. When writing 0 to this bit, the bus master must be either paused or have reached EOT. Writing 0 to this bit while the bus master is operating, results in unpredictable behavior (and may crash the bus master state machine). The only recovery from this condition is a PCI reset. |
| <b>Offset 49h</b> <b>Audio Bus Master 5 SMI Status Register (RC)</b> <b>Reset Value: 00h</b>  |   |
| Audio Bus Master 5: Input from codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[20] selects slot).   |   |
| 7:2   | <b>Reserved.</b>  |
| 1   | <b>Bus Master Error.</b> Indicates if hardware encountered a second EOP before software cleared the first.<br>0: No.<br>1: Yes.<br>If hardware encounters a second EOP (end of page) before software cleared the first, it causes the bus master to pause until this register is read to clear the error.   |
| 0   | <b>End of Page.</b> Indicates if the Bus master transferred data which is marked by the EOP bit in the PRD table (bit 30).<br>0: No.<br>1: Yes.   |
| <b>Offset 4Ah-4Bh</b> <b>Not Used</b>   |   |
| <b>Offset 4Ch-4Fh</b> <b>Audio Bus Master 5 PRD Table Address (R/W)</b> <b>Reset Value: 0000000h</b>  |   |
| Audio Bus Master 5: Input from codec; 16-Bit; Slot 6 or 11 (F3BAR0+Memory Offset 08h[20] selects slot).   |   |
| 31:2  | <b>Pointer to the Physical Region Descriptor Table.</b> This bit field contains a PRD table pointer for Audio Bus Master 5.<br>When written, this register points to the first entry in a PRD table. Once Audio Bus Master 5 is enabled (Command Register bit 0 = 1), it loads the pointer and updates this register (by adding 08h) so that it points to the next PRD.<br>When read, this register points to the next PRD.   |
| 1:0   | <b>Reserved.</b> Must be set to 0.  |
| <b>Note:</b> The Physical Region Descriptor (PRD) table consists of one or more entries - each describing a memory region to or from which data is to be transferred. Each entry consists of two DWORDs.<br><div style="margin-left: 40px;">           DWORD 0:        [31:0] = Memory Region Physical Base Address<br/>           DWORD 1:        31     = End of Table Flag<br/>                            30     = End of Page Flag<br/>                            29     = Loop Flag (JMP)<br/>                            [28:16] = Reserved (0)<br/>                            [15:0] = Byte Count of the Region (Size)         </div> |   |

### 6.4.5 X-Bus Expansion Interface - Function 5

The register space designated as Function 5 (F5) is used to configure the PCI portion of support hardware for accessing the X-Bus Expansion support registers. The bit formats for the PCI Header Registers are given in Table 6-39.

Located in the PCI Header Registers of F5 are six Base Address Registers (F5BARx) used for pointing to the register spaces designated for X-Bus Expansion support, described later in this section.

**Table 6-39. F5: PCI Header Registers for X-Bus Expansion**

| Bit           | Description   |
|---------------|---|
| Index 00h-01h | Vendor Identification Register (RO) <span style="float:right">Reset Value: 100Bh</span>   |
| Index 02h-03h | Device Identification Register (RO) <span style="float:right">Reset Value: 0505h</span>   |
| Index 04h-05h | PCI Command Register (R/W) <span style="float:right">Reset Value: 0000h</span>  |
| 15:2          | <b>Reserved. (Read Only)</b>  |
| 1             | <p><b>Memory Space.</b> Allow the Core Logic module to respond to memory cycles from the PCI bus.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If F5BAR0, F5BAR1, F5BAR2, F5BAR3, F5BAR4, and F5BAR5 (F5 Index 10h, 14h, 18h, 1Ch, 20h, and 24h) are defined as allowing access to memory mapped registers, this bit must be set to 1. BAR configuration is programmed through the corresponding mask register (see F5 Index 40h, 44h, 48h, 4Ch, 50h, and 54h)</p>  |
| 0             | <p><b>I/O Space.</b> Allow the Core Logic module to respond to I/O cycle from the PCI bus.</p> <p>0: Disable.<br/>1: Enable.</p> <p>If F5BAR0, F5BAR1, F5BAR2, F5BAR3, F5BAR4, and F5BAR5 (F5 Index 10h, 14h, 18h, 1Ch, 20h, and 24h) are defined as allowing access to I/O mapped registers, this bit must be set to 1. BAR configuration is programmed through the corresponding mask register (see F5 Index 40h, 44h, 48h, 4Ch, 50h, and 54h)</p>  |
| Index 06h-07h | PCI Status Register (RO) <span style="float:right">Reset Value: 0280h</span>  |
| Index 08h     | Device Revision ID Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 09h-0Bh | PCI Class Code Register (RO) <span style="float:right">Reset Value: 068000h</span>  |
| Index 0Ch     | PCI Cache Line Size Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Dh     | PCI Latency Timer Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Eh     | PCI Header Type (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 0Fh     | PCI BIST Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 10h-13h | <p>Base Address Register 0 - F5BAR0 (R/W) <span style="float:right">Reset Value: 00000000h</span></p> <p><b>X-Bus Expansion Address Space.</b> This register allows PCI access to I/O mapped X-Bus Expansion support registers. Bits [5:0] must be set to 000001, indicating a 64-byte aligned I/O address space. Refer to Table 6-40 on page 298 for the X-Bus Expansion configuration register bit formats and reset values.</p> <p><b>Note:</b> The size and type of accessed offsets can be reprogrammed through F5BAR0 Mask Register (F5 Index 40h).</p> |
| 31:6          | <b>X-Bus Expansion Base Address.</b>  |
| 5:0           | <b>Address Range.</b> This bit field must be set to 000001 for this register to operate correctly.  |
| Index 14h-17h | <p>Base Address Register 1 - F5BAR1 (R/W) <span style="float:right">Reset Value: 00000000h</span></p> <p><b>Reserved.</b> Reserved for possible future use by the Core Logic module.</p> <p>Configuration of this register is programmed through the F5BAR1 Mask Register (F5 Index 44h)</p>  |
| Index 18h-1Bh | <p>Base Address Register 2 - F5BAR2 (R/W) <span style="float:right">Reset Value: 00000000h</span></p> <p><b>Reserved.</b> Reserved for possible future use by the Core Logic module.</p> <p>Configuration of this register is programmed through the F5BAR1 Mask Register (F5 Index 48h)</p>  |

Table 6-39. F5: PCI Header Registers for X-Bus Expansion (Continued)

| Bit   | Description   |
|---|---|
| <b>Index 1Ch-1Fh</b>                            | <b>Base Address Register 3 - F5BAR3 (R/W)</b> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br><b>Reserved.</b> Reserved for possible future use by the Core Logic module.<br>Configuration of this register is programmed through the F5BAR3 Mask Register (F5 Index 4Ch).  |
| <b>Index 20h-23h</b>                            | <b>Base Address Register 4 - F5BAR4 (R/W)</b> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br><b>Reserved.</b> Reserved for possible future use by the Core Logic module.<br>Configuration of this register is programmed through the F5BAR4 Mask Register (F5 Index 50h).  |
| <b>Index 24h-27h</b>                            | <b>Base Address Register 5 - F5BAR5 (R/W)</b> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br><b>Reserved.</b> Reserved for possible future use by the Core Logic module.<br>Configuration of this register is programmed through the F5BAR5 Mask Register (F5 Index 54h).  |
| <b>Index 28h-2Bh</b>                            | <b>Reserved</b> <span style="float: right;"><b>Reset Value: 00h</b></span>  |
| <b>Index 2Ch-2Dh</b>                            | <b>Subsystem Vendor ID (RO)</b> <span style="float: right;"><b>Reset Value: 100Bh</b></span>  |
| <b>Index 2Eh-2Fh</b>                            | <b>Subsystem ID (RO)</b> <span style="float: right;"><b>Reset Value: 0505h</b></span>   |
| <b>Index 30h-3Fh</b>                            | <b>Reserved</b> <span style="float: right;"><b>Reset Value: 00h</b></span>  |
| <b>Index 40h-43h</b>                            | <b>F5BAR0 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: FFFFFFFC1h</b></span><br>To use F5BAR0, the mask register should be programmed first. The mask register defines the size of F5BAR0 and whether the accessed offset registers are memory or I/O mapped.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR0 must also be written (even if the value for F5BAR0 has not changed).   |
| <b>Memory Base Address Register (Bit 0 = 0)</b> |   |
| 31:4  | <b>Address Mask.</b> Determines the size of the BAR.<br>— Every bit that is a 1 is programmable in the BAR.<br>— Every bit that is a 0 is fixed 0 in the BAR.<br><br>Since the address mask goes down to bit 4, the smallest memory region is 16 bytes, however, the PCI specification suggests not using less than a 4 KB address range.   |
| 3   | <b>Prefetchable.</b> Indicates whether or not the data in memory is prefetchable. This bit should be set to 1 only if all the following are true:<br>— There are no side-effects from reads (i.e., the data at the location is not changed as a result of the read).<br>— The device returns all bytes regardless of the byte enables.<br>— Host bridges can merge processor writes into this range without causing errors.<br>— The memory is not cached from the host processor.<br><br>0: Data is not prefetchable. This value is recommended if one or more of the above listed conditions is not true.<br>1: Data is prefetchable. |
| 2:1   | <b>Type.</b><br>00: Located anywhere in the 32-bit address space<br>01: Located below 1 MB<br>10: Located anywhere in the 64-bit address space<br>11: Reserved  |
| 0   | This bit must be set to 0, to indicate memory base address register.  |
| <b>I/O Base Address Register (Bit 0 = 1)</b>    |   |
| 31:2  | <b>Address Mask.</b> Determines the size of the BAR.<br>— Every bit that is a 1 is programmable in the BAR.<br>— Every bit that is a 0 is fixed 0 in the BAR.<br><br>Since the address mask goes down to bit 2, the smallest I/O region is 4 bytes, however, the PCI Specification suggests not using less than a 4 KB address range.   |
| 1   | <b>Reserved.</b> Must be set to 0.  |
| 0   | This bit must be set to 1, to indicate an I/O base address register.  |

Table 6-39. F5: PCI Header Registers for X-Bus Expansion (Continued)

| Bit                  | Description   |
|----------------------|---|
| <b>Index 44h-47h</b> | <b>F5BAR1 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>To use F5BAR1, the mask register should be programmed first. The mask register defines the size of F5BAR1 and whether the accessed offset registers are memory or I/O mapped. See F5 Index 40h (F5BAR0 Mask Address Register) above for bit descriptions.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR1 must also be written (even if the value for F5BAR1 has not changed). |
| <b>Index 48h-4Bh</b> | <b>F5BAR2 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>To use F5BAR2, the mask register should be programmed first. The mask register defines the size of F5BAR2 and whether the accessed offset registers are memory or I/O mapped. See F5 Index 40h (F5BAR0 Mask Address Register) above for bit descriptions.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR2 must also be written (even if the value for F5BAR2 has not changed). |
| <b>Index 4Ch-4Fh</b> | <b>F5BAR3 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>To use F5BAR3, the mask register should be programmed first. The mask register defines the size of F5BAR3 and whether the accessed offset registers are memory or I/O mapped. See F5 Index 40h (F5BAR0 Mask Address Register) above for bit descriptions.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR3 must also be written (even if the value for F5BAR3 has not changed). |
| <b>Index 50h-53h</b> | <b>F5BAR4 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>To use F5BAR4, the mask register should be programmed first. The mask register defines the size of F5BAR4 and whether the accessed offset registers are memory or I/O mapped. See F5 Index 40h (F5BAR0 Mask Address Register) above for bit descriptions.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR4 must also be written (even if the value for F5BAR4 has not changed). |
| <b>Index 54h-57h</b> | <b>F5BAR5 Mask Address Register (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>To use F5BAR5, the mask register should be programmed first. The mask register defines the size of F5BAR5 and whether the accessed offset registers are memory or I/O mapped. See F5 Index 40h (F5BAR0 Mask Address Register) above for bit descriptions.<br><b>Note:</b> Whenever a value is written to this mask register, F5BAR5 must also be written (even if the value for F5BAR5 has not changed). |
| <b>Index 58h</b>     | <b>F5BARx Initialized Register (R/W)</b> <span style="float: right;"><b>Reset Value: 00h</b></span>   |
| 7:6                  | <b>Reserved.</b> Must be set to 0.  |
| 5                    | <b>F5BAR5 Initialized.</b> This bit indicates if F5BAR5 (F5 Index 24h) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR5 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR5 is disabled until either this bit is set to 1 or F5BAR5 is written (which causes this bit to be set to 1).   |
| 4                    | <b>F5BAR4 Initialized.</b> This bit indicates if F5BAR4 (F5 Index 28h) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR4 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR4 is disabled until either this bit is set to 1 or F5BAR4 is written (which causes this bit to be set to 1).   |
| 3                    | <b>F5BAR3 Initialized.</b> This bit indicates if F5BAR3 (F5 Index 1Ch) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR3 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR3 is disabled until either this bit is set to 1 or F5BAR3 is written (which causes this bit to be set to 1).   |
| 2                    | <b>F5BAR2 Initialized.</b> This bit indicates if F5BAR2 (F5 Index 18h) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR2 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR2 is disabled until either this bit is set to 1 or F5BAR2 is written (which causes this bit to be set to 1).   |
| 1                    | <b>F5BAR1 Initialized.</b> This bit indicates if F5BAR1 (F5 Index 14h) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR1 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR1 is disabled until either this bit is set to 1 or F5BAR1 is written (which causes this bit to be set to 1).   |
| 0                    | <b>F5BAR0 Initialized.</b> This bit indicates if F5BAR0 (F5 Index 10h) has been initialized.<br>At reset this bit is cleared (0). Writing F5BAR0 sets this bit to 1. If this bit programmed to 0, the decoding of F5BAR0 is disabled until either this bit is set to 1 or F5BAR0 is written (which causes this bit to be set to 1).   |
| <b>Index 59h-5Fh</b> | <b>Reserved</b> <span style="float: right;"><b>Reset Value: xxh</b></span>  |
| <b>Index 60h-63h</b> | <b>Scratchpad: Usually used for Device Number (R/W)</b> <span style="float: right;"><b>Reset Value: 0000000h</b></span><br>BIOS writes a value, of the Device number. Expected value: 00003200h.  |



**Table 6-39. F5: PCI Header Registers for X-Bus Expansion (Continued)**

| Bit           | Description  |
|---------------|--|
| Index 64h-67h | Scratchpad: Usually used for Configuration Block Address (R/W)      Reset Value: 00000000h<br>BIOS writes a value, of the Configuration Block Address. |
| Index 68h-FFh | Reserved   |

### 6.4.5.1 X-Bus Expansion Support Registers

F5 Index 10h, Base Address Register 0 (F5BAR0) set the base address that allows PCI access to additional I/O Con-

trol support registers. Table 6-40 shows the support registers accessed through F5BAR0.

**Table 6-40. F5BAR0+I/O Offset: X-Bus Expansion Registers**

| Bit                                 | Description  |
|-------------------------------------|--|
| <b>Offset 00h-03h</b>               |  |
| <b>I/O Control Register 1 (R/W)</b> |  |
| <b>Reset Value: 010C0007h</b>       |  |
| 31:28                               | <b>Reserved.</b>   |
| 27                                  | <b>IO_ENABLE_SIO_IR (Enable Integrated SIO Infrared).</b><br>0: Disable.<br>1: Enable.   |
| 26:25                               | <b>IO_SIOCFG_IN (Integrated SIO Input Configuration).</b> These two bits can be used to disable the integrated SIO totally or limit/control the base address.<br>00: Integrated SIO disable.<br>01: Integrated SIO configuration access disable.<br>10: Integrated SIO base address 02Eh/02Fh enable.<br>11: Integrated SIO base address 015Ch/015Dh enable. |
| 24                                  | <b>IO_ENABLE_SIO_DRIVING_ISA_BUS (Enable Integrated SIO ISA Bus Control).</b> Allow the integrated SIO to drive the internal ISA bus.<br>0: Disable.<br>1: Enable. (Default)   |
| 23:21                               | <b>Reserved.</b> Set to 0.   |
| 20                                  | <b>IO_USB_SMI_PWM_EN (USB Internal SMI).</b> Route USB-generated SMI to SMI Status Register in F1BAR0+I/O Offset 00h/02h[14].<br>0: Disable.<br>1: Enable.   |
| 19                                  | <b>IO_USB_SMI_EN (USB SMI Configuration).</b> Allow USB-generated SMIs.<br>0: Disable<br>1: Enable.<br>If bits 19 and 20 are enabled, the SMI generated by the USB is reported via the Top Level SMI status register at F1BAR0+I/O Offset 00h/02h[14].<br>If only bit 19 is enabled, the USB can generate an SMI but there is no status reporting.           |
| 18                                  | <b>IO_USB_PCI_EN (USB).</b> Enables USB ports.<br>0: Disable.<br>1: Enable.  |
| 17:0                                | <b>Reserved.</b>   |

Table 6-40. F5BAR0+I/O Offset: X-Bus Expansion Registers (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 04h-07h</b> <span style="float:right"><b>I/O Control Register 2 (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000002h</b></span>  |  |
| 31:2  | <b>Reserved.</b> Write as read.  |
| 1   | <b>Video Processor Access Enable.</b> Allows access to video processor using F4BAR0.<br>0: Disable.<br>1: Enable. (Default)<br><b>Note:</b> This bit is readable after the register (F5BAR0+Offset 04h) has been written once.               |
| 0   | <b>IO_STRAP_IDSEL_SELECT (IDSEL Strap Override).</b><br>0: IDSEL: AD28 for Chipset Register Space (F0-F5), AD29 for USB Register Space (PCIUSB).<br>1: IDSEL: AD26 for Chipset Register Space (F0-F5), AD27 for USB Register Space (PCIUSB). |
| <b>Offset 08h-0Bh</b> <span style="float:right"><b>I/O Control Register 3 (R/W)</b></span> <span style="float:right"><b>Reset Value: 00009000h</b></span> |  |
| 31:16   | <b>Reserved.</b> Write as read.  |
| 15:13   | <b>IO_USB_XCVR_VADJ (USB Voltage Adjustment Connection).</b> These bits connect to the voltage adjustment interface on the three USB transceivers. Default = 100.  |
| 12:8  | <b>IO_USB_XCVT_CADJ (USB Current Adjustment).</b> These bits connect to the current adjustment interface on the three USB transceivers. Default = 10000.   |
| 7   | <b>IO_TEST_PORT_EN (Debug Test Port Enable).</b><br>0: Disable<br>1: Enable  |
| 6:0   | <b>IO_TEST_PORT_REG (Debug Port Pointer).</b> These bits are used to point to the 16-bit slice of the test port bus.   |

### 6.4.6 USB Controller Registers - PCIUSB

The registers designated as PCIUSB are 32-bit registers decoded from the PCI address bits [7:2] and C/BE[3:0]#, when IDSEL is high, AD[10:8] select the appropriate function, and AD[1:0] are 00.

The PCI Configuration registers are listed in Table 6-41. They can be accessed as any number of bytes within a single 32-bit aligned unit. They are selected by the PCI-standard Index and Byte-Enable method.

In the PCI Configuration space, there is one Base Address Register (BAR), at Index 10h, which is used to map the

USB Host Controller's operational register set into a 4K memory space. Once the BAR register has been initialized, and the PCI Command register at Index 04h has been set to enable the Memory space decoder, these "USB Controller" registers are accessible.

The memory-mapped USB Controller registers are listed in Table 6-42. They follow the Open Host Controller Interface (OHCI) specification. Registers marked as "Reserved", and reserved bits within a register, should not be changed by software.

**Table 6-41. PCIUSB: USB PCI Configuration Registers**

| Bit  | Description  |
|--|--|
| <b>Index 00h-01h</b> Vendor Identification Register (RO) <b>Reset Value: 0E11h</b> |  |
| <b>Index 02h-03h</b> Device Identification Register (RO) <b>Reset Value: A0F8h</b> |  |
| <b>Index 04h-05h</b> Command Register (R/W) <b>Reset Value: 00h</b>                |  |
| 15:10  | <b>Reserved.</b> Must be set to 0.   |
| 9  | <b>Fast Back-to-Back Enable. (Read Only)</b> USB only acts as a master to a single device, so this functionality is not needed. It is always disabled (i.e., this bit must always be set to 0).  |
| 8  | <b>SERR#.</b> When this bit is enabled, USB asserts SERR# when it detects an address parity error.<br>0: Disable.<br>1: Enable.  |
| 7  | <b>Wait Cycle Control.</b> USB does not need to insert a wait state between the address and data on the AD lines. It is always disabled (i.e., this bit is set to 0).  |
| 6  | <b>Parity Error.</b> USB asserts PERR# when it is the agent receiving data and it detects a data parity error.<br>0: Disable.<br>1: Enable.  |
| 5  | <b>VGA Palette Snoop Enable. (Read Only)</b> USB does not support this function. It is always disabled (i.e., this bit is set to 0).   |
| 4  | <b>Memory Write and Invalidate.</b> Allow USB to run Memory Write and Invalidate commands.<br>0: Disable.<br>1: Enable.<br><br>The Memory Write and Invalidate Command only occurs if the cache-line size is set to 32 bytes and the memory write is exactly one cache line.<br>This bit must be set to 0. |
| 3  | <b>Special Cycles.</b> USB does not run special cycles on PCI. It is always disabled (i.e., this bit is set to 0).   |
| 2  | <b>PCI Master Enable.</b> Allow the USB to run PCI master cycles.<br>0: Disable.<br>1: Enable.   |
| 1  | <b>Memory Space.</b> Allow the USB to respond as a target to memory cycles from the PCI bus.<br>0: Disable.<br>1: Enable.  |
| 0  | <b>I/O Space.</b> Allow the USB to respond as a target to I/O cycles from the PCI bus.<br>0: Disable.<br>1: Enable.  |

Table 6-41. PCIUSB: USB PCI Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Index 06h-07h</b> <b>Status Register (R/W)</b> <b>Reset Value: 0280h</b>  |   |
| The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.                    |   |
| 15   | <b>Detected Parity Error.</b> This bit is set to 1 whenever the USB detects a parity error, even if the Parity Error (Response) Detection Enable Bit (Command Register, bit 6) is disabled.<br>Write 1 to clear.                        |
| 14   | <b>SERR# Status.</b> This bit is set whenever the USB detects a PCI address error.<br>Write 1 to clear.   |
| 13   | <b>Received Master Abort Status.</b> This bit is set when the USB, acting as a PCI master, aborts a PCI bus memory cycle.<br>Write 1 to clear.  |
| 12   | <b>Received Target Abort Status.</b> This bit is set when a USB generated PCI cycle (USB is the PCI master) is aborted by a PCI target.<br>Write 1 to clear.  |
| 11   | <b>Signaled Target Abort Status.</b> This bit is set whenever the USB signals a target abort.<br>Write 1 to clear.  |
| 10:9   | <b>DEVSEL# Timing. (Read Only)</b> These bits indicate the DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.  |
| 8  | <b>Data Parity Reported. (Read Only)</b> This bit is set to 1 if the Parity Error Response bit (Command Register bit 6) is set, and the USB detects PERR# asserted while acting as PCI master (whether or not PERR# was driven by USB). |
| 7  | <b>Fast Back-to-Back Capable.</b> The USB supports fast back-to-back transactions when the transactions are not to the same agent.<br>This bit is always 1.   |
| 6:0  | <b>Reserved.</b> Must be set to 0.  |
| <b>Index 08h</b> <b>Device Revision ID Register (RO)</b> <b>Reset Value: 08h</b>   |   |
| <b>Index 09h-0Bh</b> <b>PCI Class Code Register (RO)</b> <b>Reset Value: 0C0310h</b>   |   |
| This register identifies the generic function of the USB the specific register level programming interface. The Base Class is 0Ch (Serial Bus Controller). The Sub Class is 03h (Universal Serial Bus). The Programming Interface is 10h (OpenHCI).  |   |
| <b>Index 0Ch</b> <b>Cache Line Size Register (R/W)</b> <b>Reset Value: 00h</b>   |   |
| This register identifies the system cache-line size in units of 32-bit WORDs. The USB only stores the value of bit 3 in this register since the cache-line size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register is read back as 00h. |   |
| <b>Index 0Dh</b> <b>Latency Timer Register (R/W)</b> <b>Reset Value: 00h</b>   |   |
| This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles. Bits [2:0] of this register are always set to 0.  |   |
| <b>Index 0Eh</b> <b>Header Type Register (RO)</b> <b>Reset Value: 00h</b>  |   |
| This register identifies the type of the predefined header in the configuration space. Since the USB is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.   |   |
| <b>Index 0Fh</b> <b>BIST Register (RO)</b> <b>Reset Value: 00h</b>   |   |
| This register identifies the control and status of Built-In Self-Test (BIST). The USB does not implement BIST, so this register is read only.  |   |
| <b>Index 10h-13h</b> <b>Base Address Register - USB_BAR0 (R/W)</b> <b>Reset Value: 00000000h</b>   |   |
| 31:12  | <b>Base Address.</b> POST writes the value of the memory base address to this register.   |
| 11:4   | <b>Always 0.</b> Indicates that a 4 KB address range is requested.  |
| 3  | <b>Always 0.</b> Indicates that there is no support for prefetchable memory.  |
| 2:1  | <b>Always 0.</b> Indicates that the base register is 32-bits wide and can be placed anywhere in 32-bit memory space.  |
| 0  | <b>Always 0.</b> Indicates that the operational registers are mapped into memory space.   |

Table 6-41. PCIUSB: USB PCI Configuration Registers (Continued)

| Bit           | Description   | Reset Value |
|---------------|---|-------------|
| Index 14h-2Bh | Reserved  | 00h         |
| Index 2Ch-2Dh | Subsystem Vendor ID (RO)  | 0E11h       |
| Index 2Eh-2Fh | Subsystem ID (RO)   | A0F8h       |
| Index 30h-3Bh | Reserved  | 00h         |
| Index 3Ch     | Interrupt Line Register (R/W)<br>This register identifies the system interrupt controllers to which the device's interrupt pin is connected. The value of this register is used by device drivers and has no direct meaning to USB. | 00h         |
| Index 3Dh     | Interrupt Pin Register (R/W)<br>This register selects which interrupt pin the device uses. USB uses INTA# after reset. INTB#, INTC# or INTD# can be selected by writing 2, 3 or 4, respectively.                                    | 01h         |
| Index 3Eh     | Min. Grant Register (RO)<br>This register specifies how long a burst is needed by the USB, assuming a clock rate of 33 MHz. The value in this register specifies a period of time in units of 1/4 microsecond.                      | 00h         |
| Index 3Fh     | Max. Latency Register (RO)<br>This register specifies how often (in units of 1/4 microsecond) the USB needs access to the PCI bus assuming a clock rate of 33 MHz.  | 50h         |
| Index 40h-43h | ASIC Test Mode Enable Register (R/W)<br>Used for internal debug and test purposes only.   | 000F0000h   |
| Index 44h     | ASIC Operational Mode Enable Register (R/W)   | 00h         |
| 7:1           | <b>Write Only.</b> Read as 0s.  |             |
| 0             | <b>Data Buffer Region 16</b><br>0: The size of the region for the data buffer is 32 bytes.<br>1: The size of the region for the data buffer is 16 bytes.  |             |
| Index 45h-FFh | Reserved  | 00h         |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers

| Bit  | Description  |
|--|--|
| <b>Offset 00h-03h</b> <span style="float:right"><b>HcRevision Register (RO)</b></span> <span style="float:right"><b>Reset Value = 00000110h</b></span>         |  |
| 31:8   | <b>Reserved.</b> Read/Write 0s.  |
| 7:0  | <b>Revision (Read Only).</b> Indicates the Open HCI Specification revision number implemented by the Hardware. USB supports 1.0 specification. (X.Y = XYh).  |
| <b>Offset 04h-07h</b> <span style="float:right"><b>HcControl Register (R/W)</b></span> <span style="float:right"><b>Reset Value = 00000000h</b></span>         |  |
| 31:11  | <b>Reserved.</b> Read/Write 0s.  |
| 10   | <b>RemoteWakeupConnectedEnable.</b> If a remote wakeup signal is supported, this bit enables that operation. Since there is no remote wakeup signal supported, this bit is ignored.  |
| 9  | <b>RemoteWakeupConnected (Read Only).</b> This bit indicated whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hard-coded to 0.   |
| 8  | <b>InterruptRouting.</b> This bit is used for interrupt routing:<br>0: Interrupts routed to normal interrupt mechanism (INT).<br>1: Interrupts routed to SMI.  |
| 7:6  | <b>HostControllerFunctionalState.</b> This field sets the HC state. The HC may force a state change from UsbSuspend to UsbResume after detecting resume signaling from a downstream port. States are:<br>00: UsbReset<br>01: UsbResume<br>10: UsbOperational<br>11: UsbSuspend |
| 5  | <b>BulkListEnable.</b> When set, this bit enables processing of the Bulk list.   |
| 4  | <b>ControlListEnable.</b> When set, this bit enables processing of the Control list.   |
| 3  | <b>IsochronousEnable.</b> When clear, this bit disables the Isochronous List when the Periodic List is enabled (so Interrupt EDs may be serviced). While processing the Periodic List, the HC will check this bit when it finds an isochronous ED.                             |
| 2  | <b>PeriodicListEnable.</b> When set, this bit enables processing of the Periodic (interrupt and isochronous) list. The HC checks this bit prior to attempting any periodic transfers in a frame.   |
| 1:0  | <b>ControlBulkServiceRatio.</b> Specifies the number of Control Endpoints serviced for every Bulk Endpoint. Encoding is N-1 where N is the number of Control Endpoints (i.e., 00: 1 Control Endpoint; 11: 3 Control Endpoints).  |
| <b>Offset 08h-0Bh</b> <span style="float:right"><b>HcCommandStatus Register (R/W)</b></span> <span style="float:right"><b>Reset Value = 00000000h</b></span>   |  |
| 31:18  | <b>Reserved.</b> Read/Write 0s.  |
| 17:16  | <b>ScheduleOverrunCount.</b> This field increments every time the SchedulingOverrun bit in HcInterruptStatus is set. The count wraps from 11 to 00.  |
| 15:4   | <b>Reserved.</b> Read/Write 0s.  |
| 3  | <b>OwnershipChangeRequest.</b> When set by software, this bit sets the OwnershipChange field in HcInterruptStatus. The bit is cleared by software.   |
| 2  | <b>BulkListFilled.</b> Set to indicate there is an active ED on the Bulk List. The bit may be set by either software or the HC and cleared by the HC each time it begins processing the head of the Bulk List.   |
| 1  | <b>ControlListFilled.</b> Set to indicate there is an active ED on the Control List. It may be set by either software or the HC and cleared by the HC each time it begins processing the head of the Control List.   |
| 0  | <b>HostControllerReset.</b> This bit is set to initiate a software reset. This bit is cleared by the HC upon completion of the reset operation.  |
| <b>Offset 0Ch-0Fh</b> <span style="float:right"><b>HcInterruptStatus Register (R/W)</b></span> <span style="float:right"><b>Reset Value = 00000000h</b></span> |  |
| 31   | <b>Reserved.</b> Read/Write 0s.  |
| 30   | <b>OwnershipChange.</b> This bit is set when the OwnershipChangeRequest bit of HcCommandStatus is set.   |
| 29:7   | <b>Reserved.</b> Read/Write 0s.  |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit  | Description  |
|--|--|
| 6  | <b>RootHubStatusChange.</b> This bit is set when the content of HcRhStatus or the content of any HcRhPortStatus register has changed.                        |
| 5  | <b>FrameNumberOverflow.</b> Set when bit 15 of FrameNumber changes value.  |
| 4  | <b>UnrecoverableError (Read Only).</b> This event is not implemented and is hard-coded to 0. Writes are ignored.   |
| 3  | <b>ResumeDetected.</b> Set when HC detects resume signaling on a downstream port.  |
| 2  | <b>StartOfFrame.</b> Set when the Frame Management block signals a Start of Frame event.   |
| 1  | <b>WritebackDoneHead.</b> Set after the HC has written HcDoneHead to HccaDoneHead.   |
| 0  | <b>SchedulingOverrun.</b> Set when the List Processor determines a Schedule Overrun has occurred.  |
| <b>Note:</b> All bits are set by hardware and cleared by software.   |  |
| <b>Offset 10h-13h HcInterruptEnable Register (R/W) Reset Value = 0000000h</b>  |  |
| 31   | <b>MasterInterruptEnable.</b> This bit is a global interrupt enable. A write of 1 allows interrupts to be enabled via the specific enable bits listed above. |
| 30   | <b>OwnershipChangeEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Ownership Change.   |
| 29:7   | <b>Reserved.</b> Read/Write 0s.  |
| 6  | <b>RootHubStatusChangeEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Root Hub Status Change.   |
| 5  | <b>FrameNumberOverflowEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Frame Number Overflow.  |
| 4  | <b>UnrecoverableErrorEnable.</b> This event is not implemented. All writes to this bit are ignored.  |
| 3  | <b>ResumeDetectedEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Resume Detected.   |
| 2  | <b>StartOfFrameEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Start of Frame.  |
| 1  | <b>WritebackDoneHeadEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Writeback Done Head.  |
| 0  | <b>SchedulingOverrunEnable.</b><br>0: Ignore.<br>1: Enable interrupt generation due to Scheduling Overrun.   |
| <b>Note:</b> Writing a 1 to a bit in this register sets the corresponding bit, while writing a 0 leaves the bit unchanged. |  |
| <b>Offset 14h-17h HcInterruptDisable Register (R/W) Reset Value = 0000000h</b>   |  |
| 31   | <b>MasterInterruptEnable.</b> Global interrupt disable. A write of 1 disables all interrupts.  |
| 30   | <b>OwnershipChangeEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Ownership Change.  |
| 29:7   | <b>Reserved.</b> Read/Write 0s.  |



Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit   | Description   |
|---|---|
| 6   | <b>RootHubStatusChangeEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Root Hub Status Change. |
| 5   | <b>FrameNumberOverflowEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Frame Number Overflow.  |
| 4   | <b>UnrecoverableErrorEnable.</b> This event is not implemented. All writes to this bit will be ignored.           |
| 3   | <b>ResumeDetectedEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Resume Detected.             |
| 2   | <b>StartOfFrameEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Start of Frame.                |
| 1   | <b>WritebackDoneHeadEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Writeback Done Head.      |
| 0   | <b>SchedulingOverrunEnable.</b><br>0: Ignore.<br>1: Disable interrupt generation due to Scheduling Overrun.       |
| <b>Note:</b> Writing a 1 to a bit in this register clears the corresponding bit, while writing a 0 to a bit leaves the bit unchanged. |   |
| <b>Offset 18h-1Bh</b> <b>HcHCCA Register (R/W)</b> <b>Reset Value = 00000000h</b>   |   |
| 31:8  | <b>HCCA.</b> Pointer to HCCA base address.  |
| 7:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 1Ch-1Fh</b> <b>HcPeriodCurrentED Register (R/W)</b> <b>Reset Value = 00000000h</b>  |   |
| 31:4  | <b>PeriodCurrentED.</b> Pointer to the current Periodic List ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 20h-23h</b> <b>HcControlHeadED Register (R/W)</b> <b>Reset Value = 00000000h</b>  |   |
| 31:4  | <b>ControlHeadED.</b> Pointer to the Control List Head ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 24h-27h</b> <b>HcControlCurrentED Register (R/W)</b> <b>Reset Value = 00000000h</b>   |   |
| 31:4  | <b>ControlCurrentED.</b> Pointer to the current Control List ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 28h-2Bh</b> <b>HcBulkHeadED Register (R/W)</b> <b>Reset Value = 00000000h</b>   |   |
| 31:4  | <b>BulkHeadED.</b> Pointer to the Bulk List Head ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 2Ch-2Fh</b> <b>HcBulkCurrentED Register (R/W)</b> <b>Reset Value = 00000000h</b>  |   |
| 31:4  | <b>BulkCurrentED.</b> Pointer to the current Bulk List ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |
| <b>Offset 30h-33h</b> <b>HcDoneHead Register (R/W)</b> <b>Reset Value = 00000000h</b>   |   |
| 31:4  | <b>DoneHead.</b> Pointer to the current Done List Head ED.  |
| 3:0   | <b>Reserved.</b> Read/Write 0s.   |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 34h-37h</b> <b>HcFmInterval Register (R/W)</b> <b>Reset Value = 00002EDFh</b>    |   |
| 31   | <b>FrameIntervalToggle (Read Only).</b> This bit is toggled by HCD when it loads a new value into FrameInterval.  |
| 30:16  | <b>FSLargestDataPacket (Read Only).</b> This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame.   |
| 15:14  | <b>Reserved.</b> Read/Write 0s.   |
| 13:0   | <b>FrameInterval.</b> This field specifies the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.   |
| <b>Offset 38h-3Bh</b> <b>HcFrameRemaining Register (RO)</b> <b>Reset Value = 00000000h</b> |   |
| 31   | <b>FrameRemainingToggle (Read Only).</b> Loaded with FrameIntervalToggle when FrameRemaining is loaded.   |
| 30:14  | <b>Reserved.</b> Read 0s.   |
| 13:0   | <b>FrameRemaining (Read Only).</b> When the HC is in the UsbOperational state, this 14-bit field decrements each 12 MHz clock period. When the count reaches 0, (end of frame) the counter reloads with FrameInterval. In addition, the counter loads when the HC transitions into UsbOperational.  |
| <b>Offset 3Ch-3Fh</b> <b>HcFmNumber Register (RO)</b> <b>Reset Value = 00000000h</b>       |   |
| 31:16  | <b>Reserved.</b> Read 0s.   |
| 15:0   | <b>FrameNumber (Read Only).</b> This 16-bit incrementing counter field is incremented coincident with the loading of FrameRemaining. The count rolls over from FFFFh to 0h.   |
| <b>Offset 40h-43h</b> <b>HcPeriodicStart Register (R/W)</b> <b>Reset Value = 00000000h</b> |   |
| 31:14  | <b>Reserved.</b> Read/Write 0s.   |
| 13:0   | <b>PeriodicStart.</b> This field contains a value used by the List Processor to determine where in a frame the Periodic List processing must begin.   |
| <b>Offset 44h-47h</b> <b>HcLSThreshold Register (R/W)</b> <b>Reset Value = 00000628h</b>   |   |
| 31:12  | <b>Reserved.</b> Read/Write 0s.   |
| 11:0   | <b>LSThreshold.</b> This field contains a value used by the Frame Management block to determine whether or not a low speed transaction can be started in the current frame.   |
| <b>Offset 48h-4Bh</b> <b>HcRhDescriptorA Register (R/W)</b> <b>Reset Value = 01000003h</b> |   |
| 31:24  | <b>PowerOnToPowerGoodTime.</b> This field value is represented as the number of 2 ms intervals, ensuring that the power switching is effective within 2 ms. Only bits [25:24] are implemented as R/W. The remaining bits are read only as 0. It is not expected that these bits be written to anything other than 1h, but limited adjustment is provided. This field should be written to support system implementation. This field should always be written to a non-zero value. |
| 23:13  | <b>Reserved.</b> Read/Write 0s.   |
| 12   | <b>NoOverCurrentProtection.</b> This bit should be written to support the external system port over-current implementation.<br>0: Over-current status is reported.<br>1: Over-current status is not reported.   |
| 11   | <b>OverCurrentProtectionMode.</b> This bit should be written 0 and is only valid when NoOverCurrentProtection is cleared.<br>0: Global Over-Current.<br>1: Individual Over-Current  |
| 10   | <b>DeviceType (Read Only).</b> USB is not a compound device.  |
| 9  | <b>NoPowerSwitching.</b> This bit should be written to support the external system port power switching implementation.<br>0: Ports are power switched.<br>1: Ports are always powered on.  |
| 8  | <b>PowerSwitchingMode.</b> This bit is only valid when NoPowerSwitching is cleared. This bit should be written 0.<br>0: Global Switching.<br>1: Individual Switching  |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit  | Description   |
|--|---|
| 7:0  | <b>NumberDownstreamPorts (Read Only).</b> USB supports three downstream ports.  |
| <b>Note:</b> This register is only reset by a power-on reset (PCIRST#). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation. |   |
| <b>Offset 4Ch-4Fh HcRhDescriptorB Register (R/W) Reset Value = 00000000h</b>   |   |
| 31:16  | <b>PortPowerControlMask.</b> Global-power switching. This field is only valid if NoPowerSwitching is cleared and PowerSwitchingMode is set (individual port switching). When set, the port only responds to individual port power switching commands (Set/ClearPortPower). When cleared, the port only responds to global power switching commands (Set/ClearGlobalPower).<br>0: Device not removable.<br>1: Global-power mask.<br>Port Bit relationship - Unimplemented ports are reserved, read/write 0.<br>0 = Reserved<br>1 = Port 1<br>2 = Port 2<br>...<br>15 = Port 15 |
| 15:0   | <b>DeviceRemoveable.</b> USB ports default to removable devices.<br>0: Device not removable.<br>1: Device removable.<br>Port Bit relationship<br>0 = Reserved<br>1 = Port 1<br>2 = Port 2<br>...<br>15 = Port 15<br>Unimplemented ports are reserved, read/write 0.   |
| <b>Note:</b> This register is only reset by a power-on reset (PCIRST#). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation. |   |
| <b>Offset 50h-53h HcRhStatus Register (R/W) Reset Value = 00000000h</b>  |   |
| 31   | <b>ClearRemoteWakeupEnable (Write Only).</b> Writing a 1 to this bit clears DeviceRemoteWakeupEnable. Writing a 0 has no effect.  |
| 30:18  | <b>Reserved.</b> Read/Write 0s.   |
| 17   | <b>OverCurrentIndicatorChange.</b> This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.   |
| 16   | <b>Read: LocalPowerStatusChange.</b> Not supported. Always read 0.<br><b>Write: SetGlobalPower.</b> Write a 1 issues a SetGlobalPower command to the ports. Writing a 0 has no effect.  |
| 15   | <b>Read: DeviceRemoteWakeupEnable.</b> This bit enables ports' ConnectStatusChange as a remote wakeup event.<br>0: Disabled.<br>1: Enabled.<br><b>Write: SetRemoteWakeupEnable.</b> Writing a 1 sets DeviceRemoteWakeupEnable. Writing a 0 has no effect.   |
| 14:2   | <b>Reserved.</b> Read/Write 0s.   |
| 1  | <b>OverCurrentIndicator.</b> This bit reflects the state of the OVRCUR pin. This field is only valid if NoOverCurrentProtection and OverCurrentProtectionMode are cleared.<br>0: No over-current condition.<br>1:Over-current condition.  |
| 0  | <b>Read: LocalPowerStatus.</b> Not Supported. Always read 0.<br><b>Write: ClearGlobalPower.</b> Writing a 1 issues a ClearGlobalPower command to the ports. Writing a 0 has no effect.  |
| <b>Note:</b> This register is reset by the UsbReset state.   |   |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit                                     | Description  |
|---|--|
| <b>Offset 54h-57h</b>                   |  |
| <b>HcRhPortStatus[1] Register (R/W)</b> |  |
| <b>Reset Value = 0000000h</b>           |  |
| 31:21                                   | <b>Reserved.</b> Read/Write 0s.  |
| 20                                      | <b>PortResetStatusChange.</b> This bit indicates that the port reset signal has completed.<br>0: Port reset is not complete.<br>1: Port reset is complete.   |
| 19                                      | <b>PortOverCurrentIndicatorChange.</b> This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.  |
| 18                                      | <b>PortSuspendStatusChange.</b> This bit indicates the completion of the selective resume sequence for the port.<br>0: Port is not resumed.<br>1: Port resume is complete.   |
| 17                                      | <b>PortEnableStatusChange.</b> This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus).<br>0: Port has not been disabled.<br>1: PortEnableStatus has been cleared.   |
| 16                                      | <b>ConnectStatusChange.</b> This bit indicates a connect or disconnect event has been detected. Writing a 1 clears this bit. Writing a 0 has no effect.<br>0: No connect/disconnect event.<br>1: Hardware detection of connect/disconnect event.<br>If DeviceRemoveable is set, this bit resets to 1.  |
| 15:10                                   | <b>Reserved.</b> Read/Write 0s.  |
| 9                                       | <b>Read: LowSpeedDeviceAttached.</b> This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set.<br>0: Full Speed device.<br>1: Low Speed device.<br><b>Write: ClearPortPower.</b> Writing a 1 clears PortPowerStatus. Writing a 0 has no effect.   |
| 8                                       | <b>Read: PortPowerStatus.</b> This bit reflects the power state of the port regardless of the power switching mode.<br>0: Port power is off.<br>1: Port power is on.<br>If NoPowerSwitching is set, this bit is always read as 1.<br><b>Write: SetPortPower.</b> Writing a 1 sets PortPowerStatus. Writing a 0 has no effect.  |
| 7:5                                     | <b>Reserved.</b> Read/Write 0s.  |
| 4                                       | <b>Read: PortResetStatus.</b><br>0: Port reset signal is not active.<br>1: Port reset signal is active.<br><b>Write: SetPortReset.</b> Writing a 1 sets PortResetStatus. Writing a 0 has no effect.  |
| 3                                       | <b>Read: PortOverCurrentIndicator.</b> This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set.<br>0: No over-current condition.<br>1: Over-current condition.<br><b>Write: ClearPortSuspend.</b> Writing a 1 initiates the selective resume sequence for the port. Writing a 0 has no effect. |
| 2                                       | <b>Read: PortSuspendStatus.</b><br>0: Port is not suspended.<br>1: Port is selectively suspended.<br><b>Write: SetPortSuspend.</b> Writing a 1 sets PortSuspendStatus. Writing a 0 has no effect.  |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit   | Description   |
|---|---|
| 1   | <p><b>Read: PortEnableStatus.</b></p> <p>0: Port disabled.<br/>1: Port enabled.</p> <p><b>Write: SetPortEnable.</b> Writing a 1 sets PortEnableStatus. Writing a 0 has no effect.</p>   |
| 0   | <p><b>Read: CurrentConnectStatus.</b></p> <p>0: No device connected.<br/>1: Device connected.</p> <p>If DeviceRemoveable is set (not removable) this bit is always 1.</p> <p><b>Write: ClearPortEnable.</b> Writing 1 a clears PortEnableStatus. Writing a 0 has no effect.</p>   |
| <b>Note:</b> This register is reset by the UsbReset state.                    |   |
| <b>Offset 58h-5Bh HcRhPortStatus[2] Register (R/W) Reset Value = 0000000h</b> |   |
| 31:21   | <b>Reserved.</b> Read/Write 0s.   |
| 20  | <p><b>PortResetStatusChange.</b> This bit indicates that the port reset signal has completed.</p> <p>0: Port reset is not complete.<br/>1: Port reset is complete.</p>  |
| 19  | <p><b>PortOverCurrentIndicatorChange.</b> This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.</p>  |
| 18  | <p><b>PortSuspendStatusChange.</b> This bit indicates the completion of the selective resume sequence for the port.</p> <p>0: Port is not resumed.<br/>1: Port resume is complete.</p>  |
| 17  | <p><b>PortEnableStatusChange.</b> This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus).</p> <p>0: Port has not been disabled.<br/>1: PortEnableStatus has been cleared.</p>  |
| 16  | <p><b>ConnectStatusChange.</b> This bit indicates a connect or disconnect event has been detected. Writing a 1 clears this bit. Writing a 0 has no effect.</p> <p>0: No connect/disconnect event.<br/>1: Hardware detection of connect/disconnect event.</p> <p>If DeviceRemoveable is set, this bit resets to 1.</p>                             |
| 15:10   | <b>Reserved.</b> Read/Write 0s.   |
| 9   | <p><b>Read: LowSpeedDeviceAttached.</b> This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set.</p> <p>0: Full speed device.<br/>1: Low speed device.</p> <p><b>Write: ClearPortPower.</b> Writing a 1 clears PortPowerStatus. Writing a 0 has no effect.</p>                        |
| 8   | <p><b>Read: PortPowerStatus.</b> This bit reflects the power state of the port regardless of the power switching mode.</p> <p>0: Port power is off.<br/>1: Port power is on.</p> <p>If NoPowerSwitching is set, this bit is always read as 1.</p> <p><b>Write: SetPortPower.</b> Writing a 1 sets PortPowerStatus. Writing a 0 has no effect.</p> |
| 7:5   | <b>Reserved.</b> Read/Write 0s.   |
| 4   | <p><b>Read: PortResetStatus.</b></p> <p>0: Port reset signal is not active.<br/>1: Port reset signal is active.</p> <p><b>Write: SetPortReset.</b> Writing a 1 sets PortResetStatus. Writing a 0 has no effect.</p>   |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit   | Description  |
|---|--|
| 3   | <p><b>Read: PortOverCurrentIndicator.</b> This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set.</p> <p>0: No over-current condition.<br/>1: Over-current condition.</p> <p><b>Write: ClearPortSuspend.</b> Writing a 1 initiates the selective resume sequence for the port. Writing a 0 has no effect.</p> |
| 2   | <p><b>Read: PortSuspendStatus.</b></p> <p>0: Port is not suspended.<br/>1: Port is selectively suspended.</p> <p><b>Write: SetPortSuspend.</b> Writing a 1 sets PortSuspendStatus. Writing a 0 has no effect.</p>  |
| 1   | <p><b>Read: PortEnableStatus.</b></p> <p>0: Port disabled.<br/>1: Port enabled.</p> <p><b>Write: SetPortEnable.</b> Writing a 1 sets PortEnableStatus. Writing a 0 has no effect.</p>  |
| 0   | <p><b>Read: CurrentConnectStatus.</b></p> <p>0: No device connected.<br/>1: Device connected.</p> <p>If DeviceRemoveable is set (not removable) this bit is always 1.</p> <p><b>Write: ClearPortEnable.</b> Writing 1 a clears PortEnableStatus. Writing a 0 has no effect.</p>  |
| <b>Note:</b> This register is reset by the UsbReset state.                                  |  |
| <b>Offset 5Ch-5Fh</b> <b>HcRhPortStatus[3] Register (R/W)</b> <b>Reset Value = 0000000h</b> |  |
| 31:21   | <b>Reserved.</b> Read/Write 0s.  |
| 20  | <p><b>PortResetStatusChange.</b> This bit indicates that the port reset signal has completed.</p> <p>0: Port reset is not complete.<br/>1: Port reset is complete.</p>   |
| 19  | <p><b>PortOverCurrentIndicatorChange.</b> This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.</p>   |
| 18  | <p><b>PortSuspendStatusChange.</b> This bit indicates the completion of the selective resume sequence for the port.</p> <p>0: Port is not resumed.<br/>1: Port resume is complete.</p>   |
| 17  | <p><b>PortEnableStatusChange.</b> This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus).</p> <p>0: Port has not been disabled.<br/>1: PortEnableStatus has been cleared.</p>   |
| 16  | <p><b>ConnectStatusChange.</b> This bit indicates a connect or disconnect event has been detected. Writing a 1 clears this bit. Writing a 0 has no effect.</p> <p>0: No connect/disconnect event.<br/>1: Hardware detection of connect/disconnect event.</p> <p>If DeviceRemoveable is set, this bit resets to 1.</p>  |
| 15:10   | <b>Reserved.</b> Read/Write 0s.  |
| 9   | <p><b>Read: LowSpeedDeviceAttached.</b> This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set.</p> <p>0: Full speed device.<br/>1: Low speed device.</p> <p><b>Write: ClearPortPower.</b> Writing a 1 clears PortPowerStatus. Writing a 0 has no effect.</p>   |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit  | Description  |
|--|--|
| 8  | <p><b>Read: PortPowerStatus.</b> This bit reflects the power state of the port regardless of the power switching mode.</p> <p>0: Port power is off.<br/>1: Port power is on.</p> <p>If NoPowerSwitching is set, this bit is always read as 1.</p> <p><b>Write: SetPortPower.</b> Writing a 1 sets PortPowerStatus. Writing a 0 has no effect.</p>  |
| 7:5  | <b>Reserved.</b> Read/Write 0s.  |
| 4  | <p><b>Read: PortResetStatus.</b></p> <p>0: Port reset signal is not active.<br/>1: Port reset signal is active.</p> <p><b>Write: SetPortReset.</b> Writing a 1 sets PortResetStatus. Writing a 0 has no effect.</p>  |
| 3  | <p><b>Read: PortOverCurrentIndicator.</b> This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set.</p> <p>0: No over-current condition.<br/>1: Over-current condition.</p> <p><b>Write: ClearPortSuspend.</b> Writing a 1 initiates the selective resume sequence for the port. Writing a 0 has no effect.</p> |
| 2  | <p><b>Read: PortSuspendStatus.</b></p> <p>0: Port is not suspended.<br/>1: Port is selectively suspended.</p> <p><b>Write: SetPortSuspend.</b> Writing a 1 sets PortSuspendStatus. Writing a 0 has no effect.</p>  |
| 1  | <p><b>Read: PortEnableStatus.</b></p> <p>0: Port disabled.<br/>1: Port enabled.</p> <p><b>Write: SetPortEnable.</b> Writing a 1 sets PortEnableStatus. Writing a 0 has no effect.</p>  |
| 0  | <p><b>Read: CurrentConnectStatus.</b></p> <p>0: No device connected.<br/>1: Device connected.</p> <p>If DeviceRemoveable is set (not removable) this bit is always 1.</p> <p><b>Write: ClearPortEnable.</b> Writing 1 a clears PortEnableStatus. Writing a 0 has no effect.</p>  |
| <b>Note:</b> This register is reset by the UsbReset state.   |  |
| <b>Offset 60h-9Fh</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value = xxh</b></span>                         |  |
| <b>Offset 100h-103h</b> <span style="float:right"><b>HceControl Register (R/W)</b></span> <span style="float:right"><b>Reset Value = 0000000h</b></span> |  |
| 31:9   | <b>Reserved.</b> Read/Write 0s.  |
| 8  | <b>A20State.</b> Indicates current state of Gate A20 on keyboard controller. Compared against value written to 60h when GateA20Sequence is active.   |
| 7  | <b>IRQ12Active.</b> Indicates a positive transition on IRQ12 from keyboard controller occurred. Software writes this bit to 1 to clear it (set it to 0); a 0 write has no effect.  |
| 6  | <b>IRQ1Active.</b> Indicates a positive transition on IRQ1 from keyboard controller occurred. Software writes this bit to 1 to clear it (set it to 0); a 0 write has no effect.  |
| 5  | <b>GateA20Sequence.</b> Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.   |
| 4  | <b>ExternalIRQEn.</b> When set to 1, IRQ1 and IRQ12 from the keyboard controller cause an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.  |
| 3  | <b>IRQEn.</b> When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, IRQ1 is generated; if 1, then an IRQ12 is generated.  |
| 2  | <b>CharacterPending.</b> When set, an emulation interrupt will be generated when the OutputFull bit of the HceStatus register is set to 0.   |

Table 6-42. USB\_BAR+Memory Offset: USB Controller Registers (Continued)

| Bit   | Description  |
|---|--|
| 1   | <b>EmulationInterrupt (Read Only).</b> This bit is a static decode of the emulation interrupt condition.   |
| 0   | <b>EmulationEnable.</b> When set to 1 the HC is enabled for legacy emulation and will decode accesses to I/O registers 60h and 64h and generate IRQ1 and/or IRQ12 when appropriate. The HC also generates an emulation interrupt at appropriate times to invoke the emulation software.  |
| <b>Note:</b> This register is used to enable and control the emulation hardware and report various status information.                            |  |
| <b>Offset 104h-107h HceInput Register (R/W) Reset Value = 000000xxh</b>   |  |
| 31:8  | <b>Reserved.</b> Read/Write 0s.  |
| 7:0   | <b>InputData.</b> This register holds data written to I/O ports 60h and 64h.   |
| <b>Note:</b> This register is the emulation side of the legacy Input Buffer register.   |  |
| <b>Offset 108h-10Bh HceOutput Register (R/W) Reset Value = 000000xxh</b>  |  |
| 31:8  | <b>Reserved.</b> Read/Write 0s.  |
| 7:0   | <b>OutputData.</b> This register hosts data that is returned when an I/O read of port 60h is performed by application software.  |
| <b>Note:</b> This register is the emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software. |  |
| <b>Offset 10Ch-10Fh HceStatus Register (R/W) Reset Value = 00000000h</b>  |  |
| 31:8  | <b>Reserved.</b> Read/Write 0s.  |
| 7   | <b>Parity.</b> Indicates parity error on keyboard/mouse data.  |
| 6   | <b>Timeout.</b> Used to indicate a time-out  |
| 5   | <b>AuxOutputFull.</b> IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.   |
| 4   | <b>Inhibit Switch.</b> This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.   |
| 3   | <b>CmdData.</b> The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h the HC will set this bit to 1.   |
| 2   | <b>Flag.</b> Nominally used as a system flag by software to indicate a warm or cold boot.  |
| 1   | <b>InputFull.</b> Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.  |
| 0   | <b>OutputFull.</b> The HC will set this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0 then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1 then and IRQ12 will be generated a long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists. |
| <b>Note:</b> This register is the emulation side of the legacy Status register.   |  |



### 6.4.7 ISA Legacy Register Space

The ISA Legacy registers reside in the ISA I/O address space in the address range from 000h to FFFh and are accessed through typical input/output instructions (i.e., CPU direct R/W) with the designated I/O port address and 8-bit data.

The bit formats for the ISA Legacy I/O Registers plus two chipset-specific configuration registers used for interrupt mapping in the Core Logic module are given in this section. The ISA Legacy registers are separated into the following DMA Channel Control Registers, see Table 6-43

- DMA Page Registers, see Table 6-44
- Programmable Interval Timer Registers, see Table 6-45
- Programmable Interrupt Controller Registers, see Table 6-46
- Keyboard Controller Registers, see Table 6-47
- Real-Time Clock Registers, see Table 6-48
- Miscellaneous Registers, see Table 6-49 (includes 4D0h and 4D1h Interrupt Edge/Level Select Registers)

**Table 6-43. DMA Channel Control Registers**

| Bit   | Description  |
|---|--|
| <b>I/O Port 000h DMA Channel 0 Address Register (R/W)</b><br>Written as two successive bytes, byte 0, 1.        |  |
| <b>I/O Port 001h DMA Channel 0 Transfer Count Register (R/W)</b><br>Written as two successive bytes, byte 0, 1. |  |
| <b>I/O Port 002h DMA Channel 1 Address Register (R/W)</b><br>Written as two successive bytes, byte 0, 1.        |  |
| <b>I/O Port 003h DMA Channel 1 Transfer Count Register (R/W)</b><br>Written as two successive bytes, byte 0, 1. |  |
| <b>I/O Port 004h DMA Channel 2 Address Register (R/W)</b><br>Written as two successive bytes, byte 0, 1.        |  |
| <b>I/O Port 005h DMA Channel 2 Transfer Count Register (R/W)</b><br>Written as two successive bytes, byte 0, 1. |  |
| <b>I/O Port 006h DMA Channel 3 Address Register (R/W)</b><br>Written as two successive bytes, byte 0, 1.        |  |
| <b>I/O Port 007h DMA Channel 3 Transfer Count Register (R/W)</b><br>Written as two successive bytes, byte 0, 1. |  |
| <b>I/O Port 008h (R/W)</b>  |  |
| <b>Read DMA Status Register, Channels 3:0</b>   |  |
| 7   | <b>Channel 3 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 6   | <b>Channel 2 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 5   | <b>Channel 1 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 4   | <b>Channel 0 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 3   | <b>Channel 3 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes. |

Table 6-43. DMA Channel Control Registers (Continued)

| Bit  | Description  |
|--|--|
| 2  | <b>Channel 2 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes.                           |
| 1  | <b>Channel 1 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes.                           |
| 0  | <b>Channel 0 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes.                           |
| <b>Write DMA Command Register, Channels 3:0</b>                      |  |
| 7  | <b>DACK Sense.</b><br>0: Active low.<br>1: Active high.  |
| 6  | <b>DREQ Sense.</b><br>0: Active high.<br>1: Active low.  |
| 5  | <b>Write Selection.</b><br>0: Late write.<br>1: Extended write.  |
| 4  | <b>Priority Mode.</b><br>0: Fixed.<br>1: Rotating.   |
| 3  | <b>Timing Mode.</b><br>0: Normal.<br>1: Compressed.  |
| 2  | <b>Channels 3:0.</b><br>0: Disable.<br>1: Enable.  |
| 1:0  | <b>Reserved.</b> Must be set to 0.   |
| <b>I/O Port 009h Software DMA Request Register, Channels 3:0 (W)</b> |  |
| 7:3  | <b>Reserved.</b> Must be set to 0.   |
| 2  | <b>Request Type.</b><br>0: Reset.<br>1: Set.   |
| 1:0  | <b>Channel Number Request Select</b><br>00: Channel 0.<br>01: Channel 1.<br>10: Channel 2.<br>11: Channel 3. |
| <b>I/O Port 00Ah DMA Channel Mask Register, Channels 3:0 (WO)</b>    |  |
| 7:3  | <b>Reserved.</b> Must be set to 0.   |
| 2  | <b>Channel Mask.</b><br>0: Not masked.<br>1: Masked.   |
| 1:0  | <b>Channel Number Mask Select.</b><br>00: Channel 0.<br>01: Channel 1.<br>10: Channel 2.<br>11: Channel 3.   |

Table 6-43. DMA Channel Control Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>I/O Port 00Bh DMA Channel Mode Register, Channels 3:0 (WO)</b>                  |  |
| 7:6  | <b>Transfer Mode.</b><br>00: Demand.<br>01: Single.<br>10: Block.<br>11: Cascade.  |
| 5  | <b>Address Direction.</b><br>0: Increment.<br>1: Decrement.  |
| 4  | <b>Auto-initialize.</b><br>0: Disable.<br>1: Enable.   |
| 3:2  | <b>Transfer Type.</b><br>00: Verify.<br>01: Write transfer (I/O to memory).<br>10: Read transfer (memory to I/O).<br>11: Reserved. |
| 1:0  | <b>Channel Number Mode Select.</b><br>00: Channel 0.<br>01: Channel 1.<br>10: Channel 2.<br>11: Channel 3.                         |
| <b>I/O Port 00Ch DMA Clear Byte Pointer Command, Channels 3:0 (W)</b>              |  |
| <b>I/O Port 00Dh DMA Master Clear Command, Channels 3:0 (W)</b>                    |  |
| <b>I/O Port 00Eh DMA Clear Mask Register Command, Channels 3:0 (W)</b>             |  |
| <b>I/O Port 00Fh DMA Write Mask Register Command, Channels 3:0 (W)</b>             |  |
| <b>I/O Port 0C0h DMA Channel 4 Address Register (R/W)</b><br>Not used.             |  |
| <b>I/O Port 0C2h DMA Channel 4 Transfer Count Register (R/W)</b><br>Not used.      |  |
| <b>I/O Port 0C4h DMA Channel 5 Address Register (R/W)</b><br>Not supported.        |  |
| <b>I/O Port 0C6h DMA Channel 5 Transfer Count Register (R/W)</b><br>Not supported. |  |
| <b>I/O Port 0C8h DMA Channel 6 Address Register (R/W)</b><br>Not supported.        |  |
| <b>I/O Port 0CAh DMA Channel 6 Transfer Count Register (R/W)</b><br>Not supported. |  |
| <b>I/O Port 0CCh DMA Channel 7 Address Register (R/W)</b><br>Not supported.        |  |
| <b>I/O Port 0CEh DMA Channel 7 Transfer Count Register (R/W)</b><br>Not supported. |  |

Table 6-43. DMA Channel Control Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>I/O Port 0D0h (R/W)</b>                           |  |
| <b>Read DMA Status Register, Channels 7:4</b>        |  |
| <b>Note:</b> Channels 5, 6, and 7 are not supported. |  |
| 7  | <b>Channel 7 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 6  | <b>Channel 6 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 5  | <b>Channel 5 Request.</b> Indicates if a request is pending.<br>0: No.<br>1: Yes.  |
| 4  | <b>Undefined.</b>  |
| 3  | <b>Channel 7 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes. |
| 2  | <b>Channel 6 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes. |
| 1  | <b>Channel 5 Terminal Count.</b> Indicates if TC was reached.<br>0: No.<br>1: Yes. |
| 0  | <b>Undefined.</b>  |
| <b>Write DMA Command Register, Channels 7:4</b>      |  |
| <b>Note:</b> Channels 5, 6, and 7 are not supported. |  |
| 7  | <b>DACK Sense.</b><br>0: Active low.<br>1: Active high.                            |
| 6  | <b>DREQ Sense.</b><br>0: Active high.<br>1: Active low.                            |
| 5  | <b>Write Selection.</b><br>0: Late write.<br>1: Extended write.                    |
| 4  | <b>Priority Mode.</b><br>0: Fixed.<br>1: Rotating.                                 |
| 3  | <b>Timing Mode.</b><br>0: Normal.<br>1: Compressed.                                |
| 2  | <b>Channels 7:4.</b><br>0: Disable.<br>1: Enable.                                  |
| 1:0  | <b>Reserved.</b> Must be set to 0.   |

Table 6-43. DMA Channel Control Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>I/O Port 0D2h Software DMA Request Register, Channels 7:4 (W)</b>   |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |
| 7:3  | <b>Reserved.</b> Must be set to 0.  |
| 2  | <b>Request Type.</b><br>0: Reset.<br>1: Set.  |
| 1:0  | <b>Channel Number Request Select.</b><br>00: Illegal.<br>01: Channel 5.<br>10: Channel 6.<br>11: Channel 7.   |
| <b>I/O Port 0D4h DMA Channel Mask Register, Channels 7:4 (WO)</b>      |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |
| 7:3  | <b>Reserved.</b> Must be set to 0.  |
| 2  | <b>Channel Mask.</b><br>0: Not masked.<br>1: Masked.  |
| 1:0  | <b>Channel Number Mask Select.</b><br>00: Channel 4.<br>01: Channel 5.<br>10: Channel 6.<br>11: Channel 7.  |
| <b>I/O Port 0D6h DMA Channel Mode Register, Channels 7:4 (WO)</b>      |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |
| 7:6  | <b>Transfer Mode.</b><br>00: Demand.<br>01: Single.<br>10: Block.<br>11: Cascade.   |
| 5  | <b>Address Direction.</b><br>0: Increment.<br>1: Decrement.   |
| 4  | <b>Auto-initialize.</b><br>0: Disabled<br>1: Enable   |
| 3:2  | <b>Transfer Type.</b><br>00: Verify.<br>01: Write transfer (I/O to memory).<br>10: Read transfer (memory to I/O).<br>11: Reserved.  |
| 1:0  | <b>Channel Number Mode Select.</b><br>00: Channel 4.<br>01: Channel 5.<br>10: Channel 6.<br>11: Channel 7.<br>Channel 4 must be programmed in cascade mode. This mode is not the default. |
| <b>I/O Port 0D8h DMA Clear Byte Pointer Command, Channels 7:4 (W)</b>  |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |
| <b>I/O Port 0DAh DMA Master Clear Command, Channels 7:4 (W)</b>        |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |
| <b>I/O Port 0DCh DMA Clear Mask Register Command, Channels 7:4 (W)</b> |   |
| <b>Note:</b> Channels 5, 6, and 7 are not supported.                   |   |

Table 6-43. DMA Channel Control Registers (Continued)

| Bit  | Description                                       |
|--|---|
| I/O Port 0DEh  | DMA Write Mask Register Command, Channels 7:4 (W) |
| <b>Note:</b> Channels 5, 6, and 7 are not supported. |   |

Table 6-44. DMA Page Registers

| Bit   | Description                            |
|---|--|
| I/O Port 081h<br>Address bits [23:16] (byte 2).   | DMA Channel 2 Low Page Register (R/W)  |
| I/O Port 082h<br>Address bits [23:16] (byte 2).   | DMA Channel 3 Low Page Register (R/W)  |
| I/O Port 083h<br>Address bits [23:16] (byte 2).   | DMA Channel 1 Low Page Register (R/W)  |
| I/O Port 087h<br>Address bits [23:16] (byte 2).   | DMA Channel 0 Low Page Register (R/W)  |
| I/O Port 089h<br>Not supported.   | DMA Channel 6 Low Page Register (R/W)  |
| I/O Port 08Ah<br>Not supported.   | DMA Channel 7 Low Page Register (R/W)  |
| I/O Port 08Bh<br>Not supported.   | DMA Channel 5 Low Page Register (R/W)  |
| I/O Port 08Fh<br>Refresh address.   | ISA Refresh Low Page Register (R/W)    |
| I/O Port 481h<br>Address bits [31:24] (byte 3).<br><b>Note:</b> This register is reset to 00h on any access to Port 081h. | DMA Channel 2 High Page Register (R/W) |
| I/O Port 482h<br>Address bits [31:24] (byte 3).<br><b>Note:</b> This register is reset to 00h on any access to Port 082h. | DMA Channel 3 High Page Register (R/W) |
| I/O Port 483h<br>Address bits [31:24] (byte 3).<br><b>Note:</b> This register is reset to 00h on any access to Port 083h. | DMA Channel 1 High Page Register (R/W) |
| I/O Port 487h<br>Address bits [31:24] (byte 3).<br><b>Note:</b> This register is reset to 00h on any access to Port 087h. | DMA Channel 0 High Page Register (R/W) |
| I/O Port 489h<br>Not supported  | DMA Channel 6 High Page Register (R/W) |
| I/O Port 48Ah<br>Not supported  | DMA Channel 7 High Page Register (R/W) |
| I/O Port 48Bh<br>Not supported  | DMA Channel 5 High Page Register (R/W) |

Table 6-45. Programmable Interval Timer Registers

| Bit  | Description  |
|--|--|
| <b>I/O Port 040h</b>   |  |
| <b>Write</b> <span style="float: right;"><b>PIT Timer 0 Counter</b></span>           |  |
| 7:0  | <b>Counter Value.</b>  |
| <b>Read</b> <span style="float: right;"><b>PIT Timer 0 Status</b></span>             |  |
| 7  | <b>Counter Output.</b> State of counter output signal.   |
| 6  | <b>Counter Loaded.</b> Indicates if the last count written is loaded.<br>0: Yes.<br>1: No.   |
| 5:4  | <b>Current Read/Write Mode.</b><br>00: Counter latch command.<br>01: R/W LSB only.<br>10: R/W MSB only.<br>11: R/W LSB, followed by MSB. |
| 3:1  | <b>Current Counter Mode.</b> 0-5.  |
| 0  | <b>BCD Mode.</b><br>0: Binary.<br>1: BCD (Binary Coded Decimal).   |
| <b>I/O Port 041h</b>   |  |
| <b>Write</b> <span style="float: right;"><b>PIT Timer 1 Counter (Refresh)</b></span> |  |
| 7:0  | <b>Counter Value.</b>  |
| <b>Read</b> <span style="float: right;"><b>PIT Timer 1 Status (Refresh)</b></span>   |  |
| 7  | <b>Counter Output.</b> State of counter output signal.   |
| 6  | <b>Counter Loaded.</b> Indicates if the last count written is loaded.<br>0: Yes.<br>1: No.   |
| 5:4  | <b>Current Read/Write Mode.</b><br>00: Counter latch command.<br>01: R/W LSB only.<br>10: R/W MSB only.<br>11: R/W LSB, followed by MSB. |
| 3:1  | <b>Current Counter Mode.</b> 0-5.  |
| 0  | <b>BCD Mode.</b><br>0: Binary.<br>1: BCD (Binary Coded Decimal).   |

Table 6-45. Programmable Interval Timer Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>I/O Port 042h</b>   |  |
| <b>Write</b> <span style="float: right;"><b>PIT Timer 2 Counter (Speaker)</b></span>   |  |
| 7:0  | <b>Counter Value.</b>  |
| <b>Read</b> <span style="float: right;"><b>PIT Timer 2 Status (Speaker)</b></span>   |  |
| 7  | <b>Counter Output.</b> State of counter output signal.   |
| 6  | <b>Counter Loaded.</b> Indicates if the last count written is loaded.<br>0: Yes.<br>1: No.   |
| 5:4  | <b>Current Read/Write Mode.</b><br>00: Counter latch command.<br>01: R/W LSB only.<br>10: R/W MSB only.<br>11: R/W LSB, followed by MSB. |
| 3:1  | <b>Current Counter Mode.</b> 0-5.  |
| 0  | <b>BCD Mode.</b><br>0: Binary.<br>1: BCD (Binary Coded Decimal).   |
| <b>I/O Port 043h (R/W) <span style="float: right;">PIT Mode Control Word Register</span></b>   |  |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>If bits [7:6] = 11: Register functions as Read Status Command and: <ul style="list-style-type: none"> <li>Bit 5 = Latch Count</li> <li>Bit 4 = Latch Status</li> <li>Bit 3 = Select Counter 2</li> <li>Bit 2 = Select Counter 1</li> <li>Bit 1 = Select Counter 0</li> <li>Bit 0 = Reserved</li> </ul> </li> <li>If bits [5:4] = 00: Register functions as Counter Latch Command and: <ul style="list-style-type: none"> <li>Bits [7:6] = Selects Counter</li> <li>Bits [3:0] = Don't care</li> </ul> </li> </ol> |  |
| 7:6  | <b>Counter Select.</b><br>00: Counter 0.<br>01: Counter 1.<br>10: Counter 2.<br>11: Read-back command (Note 1).                          |
| 5:4  | <b>Current Read/Write Mode.</b><br>00: Counter latch command.<br>01: R/W LSB only.<br>10: R/W MSB only.<br>11: R/W LSB, followed by MSB. |
| 3:1  | <b>Current Counter Mode.</b> 0-5.  |
| 0  | <b>BCD Mode.</b><br>0: Binary.<br>1: BCD (Binary Coded Decimal).   |



Table 6-46. Programmable Interrupt Controller Registers

| Bit   | Description  |
|---|--|
| <b>I/O Port 020h / 0A0h</b> <span style="float:right"><b>Master / Slave PIC ICW1 (WO)</b></span>  |  |
| 7:5   | <b>Reserved.</b> Must be set to 0.   |
| 4   | <b>Reserved.</b> Must be set to 1.   |
| 3   | <b>Trigger Mode.</b><br>0: Edge.<br>1: Level.                                  |
| 2   | <b>Vector Address Interval</b><br>0: 8 byte intervals.<br>1: 4 byte intervals. |
| 1   | <b>Reserved.</b> Must be set to 0 (cascade mode).                              |
| 0   | <b>Reserved.</b> Must be set to 1 (ICW4 must be programmed).                   |
| <b>I/O Port 021h / 0A1h</b> <span style="float:right"><b>Master / Slave PIC ICW2 (after ICW1 is written) (WO)</b></span>                                |  |
| 7:3   | <b>A[7:3].</b> Address lines [7:3] for base vector for interrupt controller.   |
| 2:0   | <b>Reserved.</b> Must be set to 0.   |
| <b>I/O Port 021h / 0A1h</b> <span style="float:right"><b>Master / Slave PIC ICW3 (after ICW2 is written) (WO)</b></span>                                |  |
| <b>Master PIC ICW3</b>  |  |
| 7:0   | <b>Cascade IRQ.</b> Must be 04h.   |
| <b>Slave PIC ICW3</b>   |  |
| 7:0   | <b>Slave ID.</b> Must be 02h.  |
| <b>I/O Port 021h / 0A1h</b> <span style="float:right"><b>Master / Slave PIC ICW4 (after ICW3 is written) (WO)</b></span>                                |  |
| 7:5   | <b>Reserved.</b> Must be set to 0.   |
| 4   | <b>Special Fully Nested Mode.</b><br>0: Disable.<br>1: Enable.                 |
| 3:2   | <b>Reserved.</b> Must be set to 0.   |
| 1   | <b>Auto EOI.</b><br>0: Normal EOI.<br>1: Auto EOI.                             |
| 0   | <b>Reserved.</b> Must be set to 1 (8086/8088 mode).                            |
| <b>I/O Port 021h / 0A1h (R/W)</b> <span style="float:right"><b>Master / Slave PIC OCW1</b><br/><b>(except immediately after ICW1 is written)</b></span> |  |
| 7   | <b>IRQ7 / IRQ15 Mask.</b><br>0: Not Masked.<br>1: Mask.                        |
| 6   | <b>IRQ6 / IRQ14 Mask.</b><br>0: Not Masked.<br>1: Mask.                        |
| 5   | <b>IRQ5 / IRQ13 Mask.</b><br>0: Not Masked.<br>1: Mask.                        |
| 4   | <b>IRQ4 / IRQ12 Mask.</b><br>0: Not Masked.<br>1: Mask.                        |
| 3   | <b>IRQ3 / IRQ11 Mask.</b><br>0: Not Masked.<br>1: Mask.                        |

Table 6-46. Programmable Interrupt Controller Registers (Continued)

| Bit   | Description  |
|---|--|
| 2   | <b>IRQ2 / IRQ10 Mask.</b><br>0: Not Masked.<br>1: Mask.  |
| 1   | <b>IRQ1 / IRQ9 Mask.</b><br>0: Not Masked.<br>1: Mask.   |
| 0   | <b>IRQ0 / IRQ8 Mask.</b><br>0: Not Masked.<br>1: Mask.   |
| <b>I/O Port 020h / 0A0h Master / Slave PIC OCW2 (WO)</b>  |  |
| 7:5   | <b>Rotate/EOI Codes.</b><br>000: Clear rotate in Auto EOI mode<br>001: Non-specific EOI<br>010: No operation<br>011: Specific EOI (bits [2:0] must be valid)<br>100: Set rotate in Auto EOI mode<br>101: Rotate on non-specific EOI command<br>110: Set priority command (bits [2:0] must be valid)<br>111: Rotate on specific EOI command |
| 4:3   | <b>Reserved.</b> Must be set to 0.   |
| 2:0   | <b>IRQ Number (000-111).</b>   |
| <b>I/O Port 020h / 0A0h Master / Slave PIC OCW3 (WO)</b>  |  |
| 7   | <b>Reserved.</b> Must be set to 0.   |
| 6:5   | <b>Special Mask Mode.</b><br>00: No operation.<br>01: No operation.<br>10: Reset Special Mask Mode.<br>11: Set Special Mask Mode.  |
| 4   | <b>Reserved.</b> Must be set to 0.   |
| 3   | <b>Reserved.</b> Must be set to 1.   |
| 2   | <b>Poll Command.</b><br>0: Disable.<br>1: Enable.  |
| 1:0   | <b>Register Read Mode.</b><br>00: No operation.<br>01: No operation.<br>10: Read interrupt request register on next read of Port 20h.<br>11: Read interrupt service register on next read of Port 20h.   |
| <b>I/O Port 020h / 0A0h Master / Slave PIC Interrupt Request and Service Registers for OCW3 Commands (RO)</b> |  |
| The function of this register is set with bits [1:0] in a write to 020h.                                      |  |
| <b>Interrupt Request Register</b>   |  |
| 7   | <b>IRQ7 / IRQ15 Pending.</b><br>0: Yes.<br>1: No.  |
| 6   | <b>IRQ6 / IRQ14 Pending.</b><br>0: Yes.<br>1: No.  |
| 5   | <b>IRQ5 / IRQ13 Pending.</b><br>0: Yes.<br>1: No.  |
| 4   | <b>IRQ4 / IRQ12 Pending.</b><br>0: Yes.<br>1: No.  |

Table 6-46. Programmable Interrupt Controller Registers (Continued)

| Bit                               | Description  |
|-----------------------------------|--|
| 3                                 | <b>IRQ3 / IRQ11 Pending.</b><br>0: Yes.<br>1: No.    |
| 2                                 | <b>IRQ2 / IRQ10 Pending.</b><br>0: Yes.<br>1: No.    |
| 1                                 | <b>IRQ1 / IRQ9 Pending.</b><br>0: Yes.<br>1: No.     |
| 0                                 | <b>IRQ0 / IRQ8 Pending.</b><br>0: Yes.<br>1: No.     |
| <b>Interrupt Service Register</b> |  |
| 7                                 | <b>IRQ7 / IRQ15 In-Service.</b><br>0: No.<br>1: Yes. |
| 6                                 | <b>IRQ6 / IRQ14 In-Service.</b><br>0: No.<br>1: Yes. |
| 5                                 | <b>IRQ5 / IRQ13 In-Service.</b><br>0: No.<br>1: Yes. |
| 4                                 | <b>IRQ4 / IRQ12 In-Service.</b><br>0: No.<br>1: Yes. |
| 3                                 | <b>IRQ3 / IRQ11 In-Service.</b><br>0: No.<br>1: Yes. |
| 2                                 | <b>IRQ2 / IRQ10 In-Service.</b><br>0: No.<br>1: Yes. |
| 1                                 | <b>IRQ1 / IRQ9 In-Service.</b><br>0: No.<br>1: Yes.  |
| 0                                 | <b>IRQ0 / IRQ8 In-Service.</b><br>0: No.<br>1: Yes.  |

Table 6-47. Keyboard Controller Registers

| Bit   | Description  |
|---|--|
| <b>I/O Port 060h External Keyboard Controller Data Register (R/W)</b>   |  |
| <b>Keyboard Controller Data Register.</b> All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# signal or cause a warm CPU reset.    |  |
| <b>I/O Port 061h Port B Control Register (R/W) Reset Value: 00x01100b</b>   |  |
| 7   | <b>PERR#/SERR# Status. (Read Only)</b> Indicates if a PCI bus error (PERR#/SERR#) was asserted by a PCI device or by the SC3200.<br>0: No.<br>1: Yes.<br>This bit can only be set if ERR_EN (bit 2) is set 0. This bit is set 0 after a write to ERR_EN with a 1 or after reset.                                     |
| 6   | <b>IOCHK# Status. (Read Only)</b> Indicates if an I/O device is reporting an error to the SC3200.<br>0: No.<br>1: Yes.<br>This bit can only be set if IOCHK_EN (bit 3) is set 0. This bit is set 0 after a write to IOCHK_EN with a 1 or after reset.  |
| 5   | <b>PIT OUT2 State. (Read Only)</b> This bit reflects the current status of the of the PIT Counter 2 (OUT2).  |
| 4   | <b>Toggle. (Read Only)</b> This bit toggles on every falling edge of Counter 1 (OUT1).   |
| 3   | <b>IOCHK# Enable.</b><br>0: Generates an NMI if IOCHK# is driven low by an I/O device to report an error. Note that NMI is under SMI control.<br>1: Ignores the IOCHK# input signal and does not generate NMI.   |
| 2   | <b>PERR/ SERR Enable.</b> Generate an NMI if PERR#/SERR# is driven active to report an error.<br>0: Enable.<br>1: Disable.   |
| 1   | <b>PIT Counter2 (SPKR).</b><br>0: Forces Counter 2 output (OUT2) to zero.<br>1: Allows Counter 2 output (OUT2) to pass to the speaker.   |
| 0   | <b>PIT Counter2 Enable.</b><br>0: Sets GATE2 input low.<br>1: Sets GATE2 input high.   |
| <b>I/O Port 062h External Keyboard Controller Mailbox Register (R/W)</b>  |  |
| <b>Keyboard Controller Mailbox Register.</b>  |  |
| <b>I/O Port 064h External Keyboard Controller Command Register (R/W)</b>  |  |
| <b>Keyboard Controller Command Register.</b> All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# signal or cause a warm CPU reset. |  |
| <b>I/O Port 066h External Keyboard Controller Mailbox Register (R/W)</b>  |  |
| <b>Keyboard Controller Mailbox Register.</b>  |  |
| <b>I/O Port 092h Port A Control Register (R/W) Reset Value: 02h</b>   |  |
| 7:2   | <b>Reserved.</b> Must be set to 0.   |
| 1   | <b>A20M# Assertion.</b> Assert A20# (internally).<br>0: Enable.<br>1: Disable.<br>This bit reflects A20# status and can be changed by keyboard command monitoring.<br>An SMI event is generated when this bit is changed, if enabled by F0 index 53h[0]. The SMI status is reported in F1BAR0+I/O Offset 00h/02h[7]. |
| 0   | <b>Fast CPU Reset.</b> WM_RST SMI is asserted to the BIOS.<br>0: Disable.<br>1: Enable.<br>This bit must be cleared before the generation of another reset.  |

Table 6-48. Real-Time Clock Registers

| Bit  | Description   |
|--|---|
| <b>I/O Port 070h</b> <span style="float: right;"><b>RTC Address Register (WO)</b></span>   |   |
| This register is shadowed within the Core Logic module and is read through the RTC Shadow Register (F0 Index BBh).   |   |
| 7  | <b>NMI Mask.</b><br>0: Enable.<br>1: Mask.  |
| 6:0  | <b>RTC Register Index.</b> A write of this register sends the data out on the ISA bus and also causes RTCALE to be triggered. (RTCALE is an internal signal between the Core Logic module and the internal RTC controller.) |
| <b>I/O Port 071h</b> <span style="float: right;"><b>RTC Data Register (R/W)</b></span>   |   |
| A read of this register returns the value of the register indexed by the RTC Address Register.<br>A write of this register sets the value into the register indexed by the RTC Address Register                    |   |
| <b>I/O Port 072h</b> <span style="float: right;"><b>RTC Extended Address Register (WO)</b></span>  |   |
| 7  | <b>Reserved.</b>  |
| 6:0  | <b>RTC Register Index.</b> A write of this register sends the data out on the ISA bus and also causes RTCALE to be triggered. (RTCALE is an internal signal between the Core Logic module and the internal RTC controller.) |
| <b>I/O Port 073h</b> <span style="float: right;"><b>RTC Data Register (R/W)</b></span>   |   |
| AA read of this register returns the value of the register indexed by the RTC Extended Address Register.<br>A write of this register sets the value into the register indexed by the RTC Extended Address Register |   |

Table 6-49. Miscellaneous Registers

| Bit   | Description  |
|---|--|
| <b>I/O Port 0F0h, 0F1h</b> <span style="float: right;"><b>Coprocessor Error Register (W)</b></span> <span style="float: right;"><b>Reset Value: F0h</b></span>  |  |
| A write to either port when the internal FERR# signal is asserted causes the Core Logic Module to assert internal IGNNE#. IGNNE# remains asserted until the FERR# de-asserts.   |  |
| <b>I/O Ports 170h-177h/376h-377h</b> <span style="float: right;"><b>Secondary IDE Registers (R/W)</b></span>  |  |
| When the local IDE functions are enabled, reads or writes to these registers cause the local IDE interface signals to operate according to their configuration rather than generating standard ISA bus cycles.  |  |
| <b>I/O Ports 1F0h-1F7h/3F6h-3F7h</b> <span style="float: right;"><b>Primary IDE Registers (R/W)</b></span>  |  |
| When the local IDE functions are enabled, reads or writes to these registers cause the local IDE interface signals to operate according to their configuration rather than generating standard ISA bus cycles.  |  |
| <b>I/O Port 4D0h</b> <span style="float: right;"><b>Interrupt Edge/Level Select Register 1 (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00h</b></span>  |  |
| <b>Notes:</b> 1. If ICW1 - bit 3 in the PIC is set as level, it overrides the setting for bits [7:3] in this register.<br>2. Bits [7:3] in this register are used to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared). |  |
| 7   | <b>IRQ7 Edge or Level Sensitive Select.</b> Selects PIC IRQ7 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 6   | <b>IRQ6 Edge or Level Sensitive Select.</b> Selects PIC IRQ6 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 5   | <b>IRQ5 Edge or Level Sensitive Select.</b> Selects PIC IRQ5 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 4   | <b>IRQ4 Edge or Level Sensitive Select.</b> Selects PIC IRQ4 sensitivity configuration.<br>0: Edge.<br>1: Level. |

Table 6-49. Miscellaneous Registers (Continued)

| Bit   | Description  |
|---|--|
| 3   | <b>IRQ3 Edge or Level Sensitive Select.</b> Selects PIC IRQ3 sensitivity configuration.<br>0: Edge.<br>1: Level.   |
| 2:0   | <b>Reserved.</b> Must be set to 0.   |
| <b>I/O Port 4D1h</b> <span style="float: right;"><b>Interrupt Edge/Level Select Register 2 (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00h</b></span>  |  |
| <b>Notes:</b> 1. If ICW1 - bit 3 in the PIC is set as level, it overrides the setting for bits 7:6 and 4:1 in this register.<br>2. Bits [7:6] and [4:1] in this register are used to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared). |  |
| 7   | <b>IRQ15 Edge or Level Sensitive Select.</b> Selects PIC IRQ15 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 6   | <b>IRQ14 Edge or Level Sensitive Select.</b> Selects PIC IRQ14 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 5   | <b>Reserved.</b> Must be set to 0.   |
| 4   | <b>IRQ12 Edge or Level Sensitive Select.</b> Selects PIC IRQ12 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 3   | <b>IRQ11 Edge or Level Sensitive Select.</b> Selects PIC IRQ11 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 2   | <b>IRQ10 Edge or Level Sensitive Select.</b> Selects PIC IRQ10 sensitivity configuration.<br>0: Edge.<br>1: Level. |
| 1   | <b>IRQ9 Edge or Level Sensitive Select.</b> Selects PIC IRQ9 sensitivity configuration.<br>0: Edge.<br>1: Level.   |
| 0   | <b>Reserved.</b> Must be set to 0.   |

# Video Processor Module

# 7

The Video Processor module contains a high performance video back-end accelerator, a video/graphics Mixer/Blender, a Video Input Port (VIP), supporting a TFT interface. The back-end accelerator functions include horizontal and vertical scaling and filtering of the video stream. The Mixer/Blender function includes color space conversion, gamma correction, and mixing or alpha blending the video and graphics streams.

## General Features

- Hardware video acceleration
- Graphics/video overlay and blending
- Integrated PLL - programmable up to 135 MHz
- Selection of interlaced and progressive video from the GX1 module and the Direct Video Port

## Video Input Port (VIP)

- CCIR-656 compatible
- Capture Video/VBI modes
- Direct Video/VBI modes

## Hardware Video Acceleration

- Arbitrary X and Y interpolation using three line-buffers
- YUV-to-RGB color space conversion
- Horizontal filtering and downscaling
- Supports 4:2:2, 4:2:0 YUV formats and RGB 5:6:5 format

## Graphics-Video Overlay and Blending

- Overlay of video up to 16 bpp
- Supports chroma key and color key for both graphics and video streams
- Supports alpha-blending with up to three alpha windows that can overlap one another
- 8-Bit alpha values with automatic increment or decrement on each frame
- Optional Gamma Correction for video or graphics

## Compatibility

- Supports Microsoft's DirectDraw®/Direct Video and Display Control Interface (DCI) Version 2.0 for full motion playback acceleration
- Compliant with PC98 and PC99 V0.7
- Compatible with VESA, VGA, DPMS, and DDC2 standards for enhanced display control and power management

## TFT Interface

- TFT modes:
  - TFT on IDE: FPCLK max is 40 MHz
  - TFT on Parallel Port: FPCLK max is 80 MHz
  - 640x480x16 bpp at 60-85 Hz vertical refresh rates
  - 800x600x16 bpp at 60-85 Hz vertical refresh rates
  - 1024x768x16 bpp at 60-75 Hz vertical refresh rates
  - 1280x1024x8 bpp at 60 Hz vertical refresh rate

## 7.1 Module Architecture

Figure 7-1 shows a top-level block diagram of the Video Processor. For information about the relationship between the Video Processor and the other modules of the SC3200, see Section 2.2 on page 22. The Video Processor module includes the following functions:

- Video Input Port
  - CCIR-656 decoder
  - Capture Video/VBI modes
  - Direct Video mode
- Video Formatter
  - Asynchronous video interface
  - Horizontal/vertical scalers
  - Filters

- Mixer/Blender
  - Overlay with color/chroma key
  - Gamma correction
  - Color space converters
  - Alpha blender

- TFT interface
- Dot Clock PLL

The following subsections describe each block in detail.

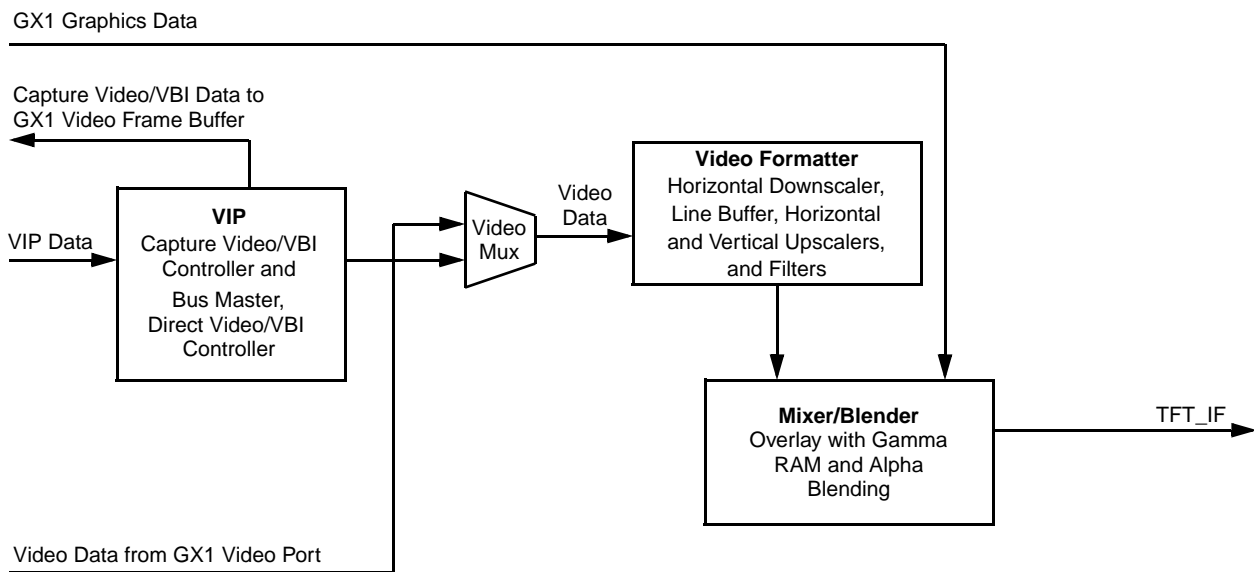


Figure 7-1. Video Processor Block Diagram



## 7.2 Functional Description

To understand why the Video Processor functions as it does, it is first important to understand the difference between video and graphics. Video is pictures in motion, which usually starts out in an encoded format (i.e., MPEG2, AVI, MPEG4) or is a TV broadcast. These pictures or frames are generally dynamic and are drawn 24 to 30 frames per second. Conversely, graphic data is relatively static and is drawn - usually using hardware accelerators. Most IA devices need to support both video and graphics displayed at the same time. For some IA devices, such as set-top boxes, video is dominant. While for other devices, such as consumer access devices and thin clients, graphics is dominant. What this means for the Video Processor is that for video centric devices, graphics overlays the video; and for graphics centric devices, video overlays the graphics.

### Video Support

The SC3200 gets video from two sources, either the VIP block or the GX1 module's video frame buffer. The VIP block supports the CCIR-656 data protocol. The CCIR-656 protocol supports TV data (NTSC or PAL) and defines the format for active video data and vertical blanking interval (VBI) data. Conforming CCIR-656 data matches exactly what is needed for a TV: full frame, interlaced, 27 MHz pixel clock, and 50 or 60 Hz refresh rate. Full frame pixel resolution and the refresh rate depends on the TV standard: NTSC, PAL, or SECAM.

If the VIP input data is full frame (conforming data), the data can go directly from the VIP block to the Video Formatter. This is known as Direct Video mode. In this mode, the data never leaves the Video Processor module. Direct Video mode can only be used under very specific conditions which will be explained later. If the VIP data is less than full frame (non conforming data), the VIP block will bus master the video data to the GX1 module's video frame buffer. The GX1 module's display controller then moves the video data out of the video frame buffer and sends it to the Video Formatter. Using this method the temporal (refresh rate) and/or spatial (image less than full screen) differences between the VIP data and the output device are reconciled. This method is known as Capture Video mode. How each mode is setup and operates is explained further in Section 7.2.1 on page 331.

### VBI Support

VBI (vertical blanking interval) data is placed in the video data stream during a portion of the vertical retrace period. The vertical retrace period physically consists of several horizontal lines (24 for NTSC and 25 for PAL systems) of non-active video. Data can be placed on some of these lines for other uses.

The active video and vertical retrace period horizontal lines are logically defined into 23 types: logical line 2 through logical line 24 (no logical line 1). Logical lines 2 through 23 occur during the vertical retrace period and logical line 24 represents all the active video lines. Logical lines 10 through 21 for NTSC and 6 through 23 for PAL are the nominal VBI lines. The rest of the logical lines, 2 through 9, 22, and 23 for NTSC and 2 through 6 for PAL occur during the vertical retrace period but do not normally carry user data. An example of VBI usage is Closed Captioning, which occupies VBI logical line 21 for NTSC. Figure 7-2 and Figure 7-3 on page 330 show the (relationship between the) physical scan lines and logical scan lines for the odd and even fields in the NTSC format.

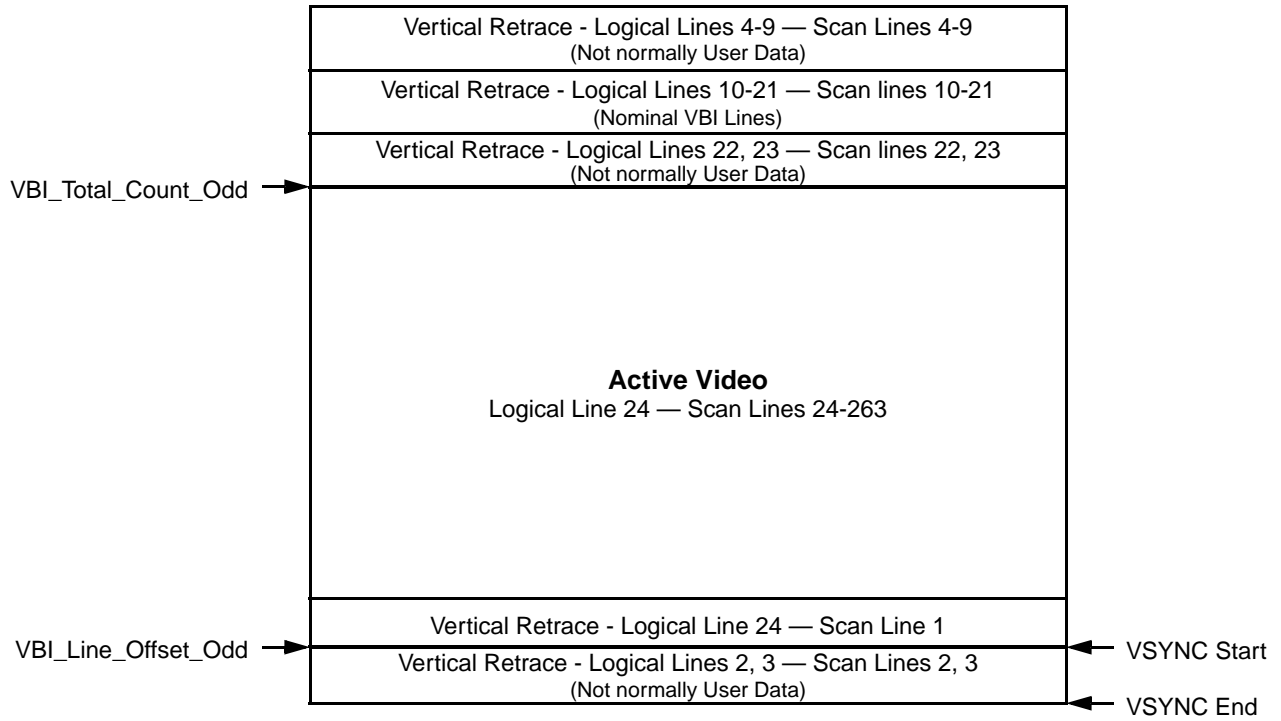


Figure 7-2. NTSC 525 Lines, 60 Hz, Odd Field

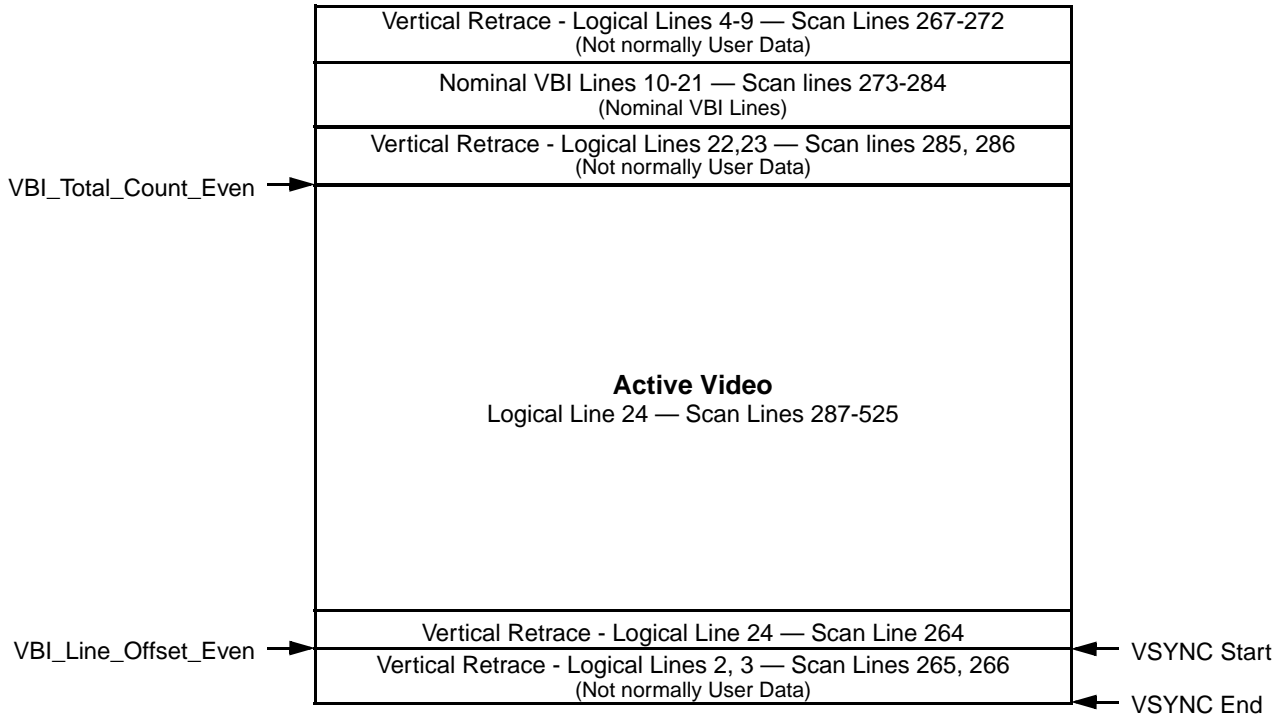


Figure 7-3. NTSC 525 Lines, 60 Hz, Even Field

### 7.2.1 Video Input Port (VIP)

The VIP block is designed to interface the SC3200 with external video processors (e.g., Philips PNX1300 or Sigma Designs EM8400) or external TV decoders (e.g., Philips SAA7114). It inputs CCIR-656 Video and raw VBI data sourced by those devices, decodes the data, and delivers the data directly to the Video Formatter (Direct Video mode) or to the GX1 module's video frame buffer (Capture Video/VBI modes). Figure 7-4 shows a diagram of the VIP block.

From the VIP block's perspective, Direct Video mode is always on. There are no registers that enable/disable Direct Video mode. The data source selected at the video mux (F4BAR0+Memory Offset 400h[1:0]) determines if the data from the VIP interface is moved directly or must be captured.

Two FIFOs in the VIP block support the efficient movement of Video and VBI data. For Capture Video/VBI modes, a 128-byte FIFO buffers both Video and raw VBI data processed by the CCIR-656 decoder. For Direct Video mode, there is a 2048-byte FIFO that buffer the CCIR-656 decoder's video data. The FIFOs are also used to provide clock domain changes. The VIP interface clock (nominally 27 MHz) is the input clock domain for both FIFOs. For the Capture Video/VBI FIFO, the data is clocked out using the FPCI clock (33 or 66 MHz). For the Direct Video FIFO, the

Video data is clocked out using the GX1's Video port clock (75, 116, or 133 MHz GX1 core clock divided by 2 or 4).

#### 7.2.1.1 Direct Video Mode

As stated previously, Direct Video mode is on by default so no registers need to be programmed to support this mode other than to select the direct video data at the video mux. The video mux control register is located at F4BAR0+Memory Offset 400h[1:0].

Direct Video mode while supported is not an optimal mode of operation. This mode supports only one vertical resolution and refresh rate, which is that of the incoming data. Horizontal resolution can be scaled if desired. Since the incoming data has odd and even fields, incoming line must be doubled for it to display properly. This is equivalent to the Bob technique which is explained later in this section.

#### GenLock

Because video input data from the VIP is sent directly, without significant buffering frame-to-field synchronization is required with the GX1 module's graphics data. This synchronization is known as GenLock. The GenLock registers are located at F4BAR0+Memory Offset 420h and 424h.

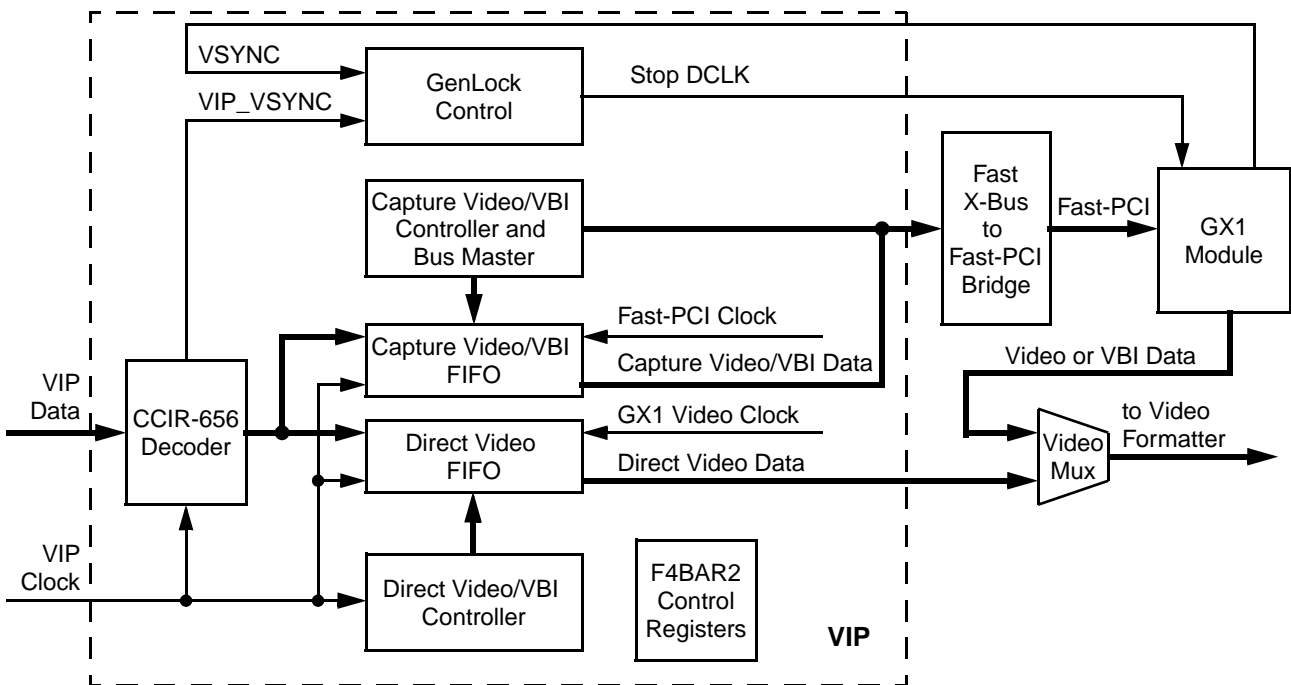


Figure 7-4. VIP Block Diagram

The GenLock control hardware is used to synchronize the video input's field with the GX1 module's graphics frame. The graphics data is always sent full frame. For the GenLock function to perform correctly, the GX1 module's Display Controller must be programmed to have a slightly faster frame time than the video input's field time. This is best accomplished by programming the GX1 module's Display Controller with a few less (three to five) horizontal lines than the VIP interface. GenLock is accomplished by stopping the clock driving the GX1 module's graphics frame until the VIP vertical sync occurs (plus some additional delay, via F4BAR0+Memory Offset 424h).

The GenLock function provides a timeout feature (GENLOCK\_TOUT\_EN, F4BAR0+Memory Offset 420h[4]) in case the video port input clock stops due to a problem with incoming video.

### 7.2.1.2 Capture Video Mode

Capture Video mode is a process for bus mastering Video data received from the VIP block to the GX1 module's Video Frame Buffer. The GX1 module's Display Controller then moves the data from the Video Frame Buffer to the Video Formatter. Usually Capture Video mode is used because the data coming in from the VIP block is interlaced and has a 30 Hz refresh rate (NTSC format) and the TFT panel, is progressive and has a 60 to 85 Hz refresh rate. The Capture Video mode process must convert the interlaced data to progressive data and change the frames per second. There are two methods to perform the interlaced to progressive conversion; Bob and Weave. Each method uses a different mechanism to up the refresh rate

#### Bob

The Bob method displays the odd frame followed by the even frame. If a full-scale image is displayed, each line in the odd and even field must be vertically doubled (see Section 7.2.2.5 "2-Tap Vertical and Horizontal Upscalers" on page 337) because each odd and each even field only contain one-half a frames worth of data. This means that the Bob method reduces the video image resolution, but has a higher effective refresh rate. If there is a change of refresh rate from the VIP block to the display device, then a field will sometimes be displayed twice. The advantage of this method is that the process is simple as only half the data is transmitted from the GX1 module's Video Frame Buffer to the Video Processor per a given amount of time, therefore reducing the memory bandwidth requirement. The disadvantage is that there are some observable visual effects due to the reduction in resolution.

Figure 7-5 on page 333 is an example of how the Bob method is performed. The example assumes that the display device is a TFT at 85 Hz refresh and single buffering is used for the data. The example does not assume anything regarding scaling that may be performed in the Video Processor. The example is only presented to allow for a general understanding of how the SC3200's video support hardware works and not as an all-inclusive statement of operation.

The following procedure is an example of how to create a Bob method. This example assumes single buffering in the GX1 module's video frame buffer. The Video Processor registers that control the VIP bus master only need to be initialized.

#### 1) Program the VIP bus master address registers.

Three registers control where the VIP video data is stored in the GX1 module's frame buffer:

- F4BAR2+Memory Offset 20h – Video Data Odd Base Address
- F4BAR2+Memory Offset 24h – Video Data Even Base Address
- F4BAR2+Memory Offset 28h – Video Data Pitch

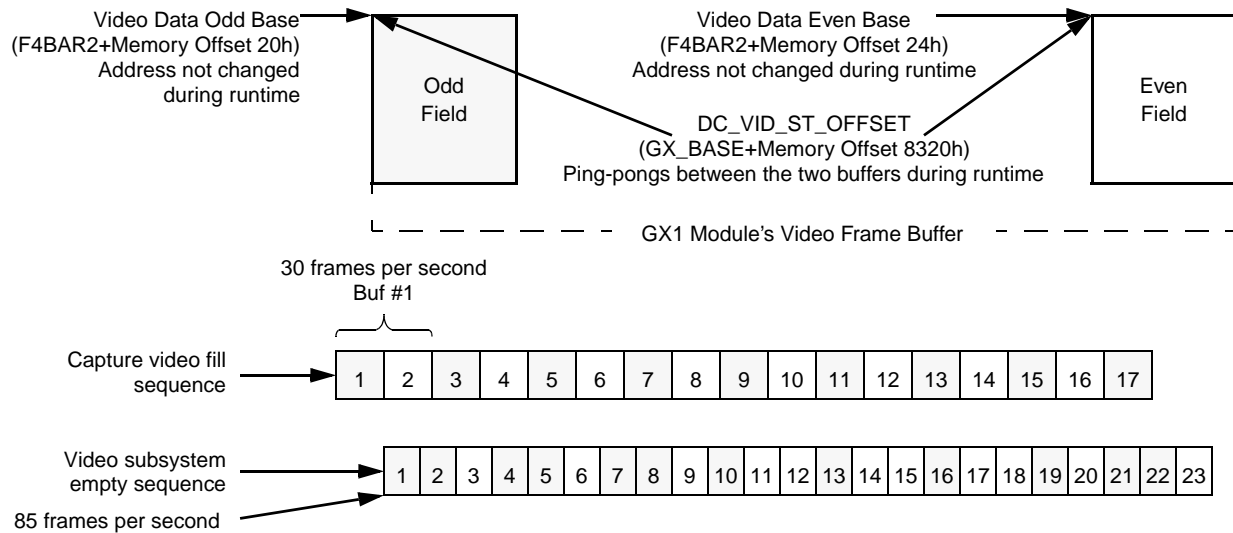
The Video Data Even Base Address must be separated from the Video Data Odd Base Address by at least the field data size. The Video Data Pitch register must be programmed to 00000000h.

#### 2) Program other VIP bus master support registers.

In F4BAR2+Memory Offset 00h, make sure that the VIP FIFO bus request threshold is set to 32 bytes (bit 22 = 1) and that the Video Input Port mode is set to CCIR-656. An interrupt needs to be generated so that the GX1 module's video frame buffer pointer can flip to the field that has completed transfer to the video frame buffer. So in F4BAR2+Memory Offset 04h, enable the Field Interrupt bit. Auto-Flip is normally set to allow the CCIR-656 Decoder to identify which field is being processed. Capture video data needs to be enabled and Run Mode Capture is set to Start Capture at beginning of next field. Data is now being captured to the frame buffer.

#### 3) Field Interrupt.

When the field interrupt occurs, the interrupt handler must program the GX1 module's video buffer start offset value (GX\_BASE+Memory Offset 8320h) with the address of the field that was just received from the VIP interface. This action will cause the display controller to ping-pong between the two fields. The new address will not take affect until the start of a new display controller frame. The field that was just received can be known by reading the Current Field bit at F4BAR2+Memory Offset 08h[24].



**Figure 7-5. Capture Video Mode Bob Example Using One Video Frame Buffer**

### Weave

The Weave method assembles the odd field and even field together to form the complete frame, and then renders the “weaved” frames to the display device. The Video data is converted from interlaced to progressive. Since both fields are rendered simultaneously, the GX1 module’s video frame buffer must be at least double buffered. The Weave method has the advantage of not creating the temporal effects that Bob does. The disadvantage of Weave is twice as much data is transferred from the video frame buffer to the Video Processor; meaning that Weave uses more memory bandwidth.

Figure 7-6 on page 334 is an example of the Weave method in action. As in the Bob example (Figure 7-5), a TPT panel at 85 Hz refresh is assumed. Double buffering of the incoming data is also assumed. The example does not assume anything about any scaling that may be done in the Video Processor. No attempt has been made to assure that this example is absolutely workable. The example is only presented to allow for a general understanding of how the SC3200’s video support hardware works.

The following procedure is an example of how to create the Weave method. Since at least double buffering is required, more of the VIP’s control registers are used for Weave than required for Bob during video runtime.

### 1) Program the VIP bus master address registers.

Three registers control where the VIP video data is stored in the GX1 module’s frame buffer:

- F4BAR2+Memory Offset 20h – Video Data Odd Base Address
- F4BAR2+Memory Offset 24h – Video Data Even Base Address
- F4BAR2+Memory Offset 28h – Video Data Pitch

The Video Data Even Base Address must be separated from the Video Data Odd Base Address by one horizontal line. The Video Data Pitch register must be programmed to one horizontal line.

### 2) Program other VIP bus master support registers.

Ensure the VIP FIFO Bus Request Threshold is set to 32 bytes (F4BAR2+Memory Offset 00h[22] = 1) and the Video Input Port mode is set to CCIR-656 (F4BAR2+Memory Offset 00h[1:0] = 10). An interrupt needs to be generated so that the GX1 module’s video frame buffer pointer can flip to the field that has completed transfer to the video frame buffer. So the Field Interrupt bit (F4BAR2+Memory Offset 04h[16] = 1), must be enabled. Auto-Flip is normally set (F4BAR2+Memory Offset 04h[10] = 0) to allow the CCIR-656 decoder to identify which field is being processed. Capture video data needs to be enabled (F4BAR2+Memory Offset 04h[10] = 1) and Run Mode Capture is set to Start Capture (F4BAR2+Memory Offset 04h[1:0] = 11) at beginning of next field. Data is now being captured to the frame buffer.

3) **Field Interrupt.**

When the field interrupt occurs on the completion of an odd field, the interrupt must program the Video Data Odd Base Address with the other buffer's address. The odd field will ping-pong between the two buffers. When the interrupt is due to the completion of an even field, the interrupt handler must program the GX1 module's video buffer start offset value (GX\_BASE+Memory Offset 8320h) with the address of the frame (both odd and even fields) that was just received from the VIP block. This new address will not take affect until the start of a new frame. It must also program the Video Data Even Base Address with the other buffer so that the even field will ping-pong just like the odd field. The field just received can be known by reading the Current Field bit (F4BAR2+Memory Offset 08h[24]).

7.2.1.3 **Capture VBI Mode**

There are three types of VBI data defined by the CCIR-656 protocol: Task A data, Task B data, and Ancillary data. The VIP block supports the capture for each data type. Generally Task A data is the data type captured. Just as in Capture Video mode, there are three registers that tell the bus master where to put the raw VBI data in the GX1 module's frame buffer. Once the raw VBI data has been captured, the data can be manipulated or decoded. The data can also be used by an application. An example of this would be an Internet address that is encoded on one or more of the VBI lines, or have an application decode the Closed Captioning information put in the graphics frame buffer.

The registers, F4BAR2+Memory Offset 40h, 44h, and 48h, tell the bus master the destination addresses for the VBI data in the GX1 module's frame buffer. Five bits (F4BAR2+Memory Offset 00h[21:17]) are used to tell the bus master the data types to store. Capture VBI mode needs to be enabled at F4BAR2+Memory Offset 04h[9,1:0]. The Field Interrupt bit (F4BAR2+Memory Offset 04h[16]) should be used by the software driver to know when the captured VBI data has been completed for a field.

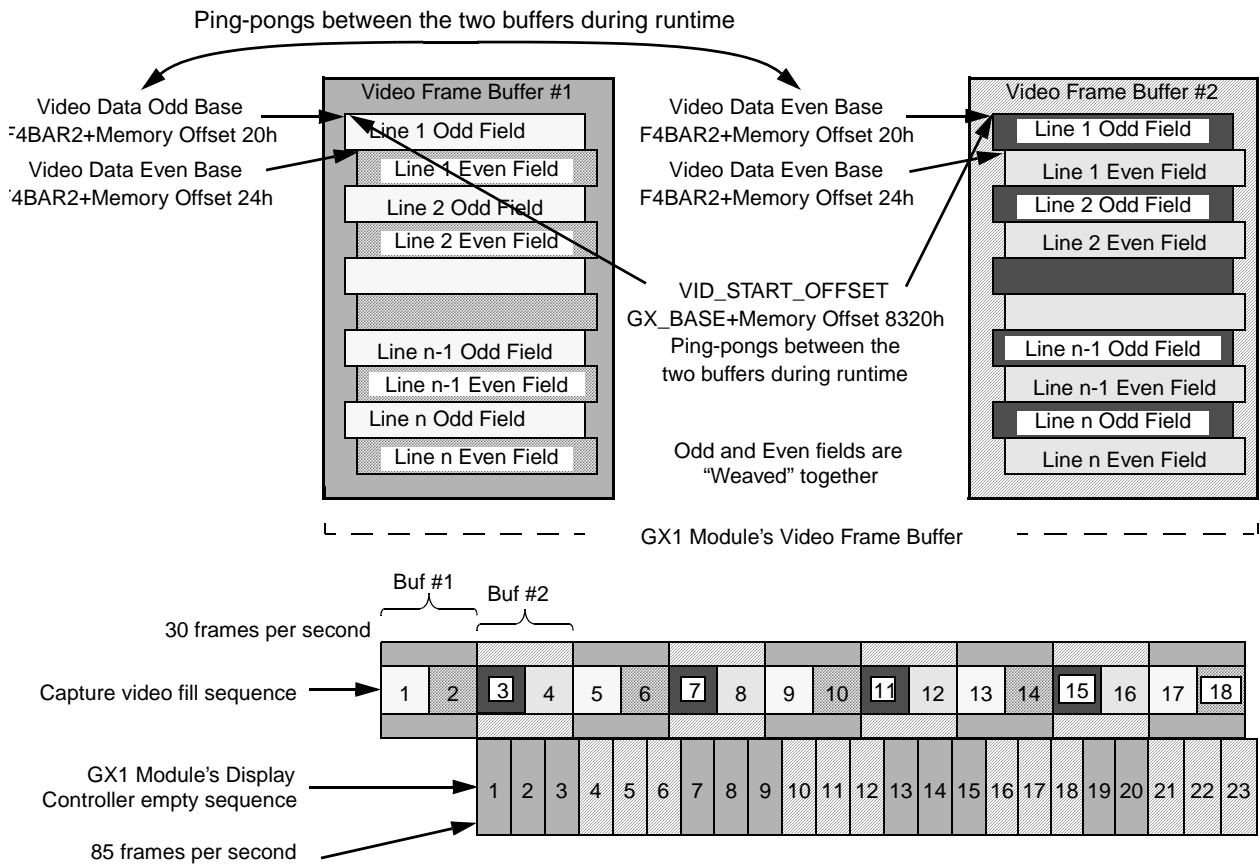


Figure 7-6. Capture Video Mode Weave Example Using Two Video Frame Buffers

## 7.2.2 Video Block

The Video block receives video data from the VIP block or the GX1 module's video frame buffer. The video data is formatted and scaled and then sent to the Mixer/Blender. The video data also changes clock domains while in the Video block. It is clocked in with the GX1 module's video clock and it is clocked out with the GX1 module's graphics clock. A diagram of the Video block is shown in Figure 7-7.

### 7.2.2.1 Video Input Formatter

The Video Input Formatter accepts video data 8 bits at a time in YUV 4:2:2, YUV 4:2:0, or RGB 6:5:6 format. The GX1 module's video clock is the source clock. The data can be interlaced or progressive. When the data comes directly from the VIP block it is usually interlaced. The video format is configured via the EN\_42X bit (F4BAR0+Memory Offset 00h[28]) and the GV\_SEL bit (F4BAR0+Memory Offset 4Ch[13]). The byte order for each format is configured in the VID\_FMT bits (F4BAR0+Offset 00h[3:2]).

**RGB 5:6:5** – For this format each pixel is described as a 16-bit value:

Bits [15:11] = Red  
 Bits [10:5] = Green  
 Bits [4:0] = Blue

**YUV 4:2:0** – This format is not supported by the GX1 module. The Horizontal Downscaler in the Video block cannot be used if the video data is in this format. In this format, 4 bytes of data are used to describe two pixels. The 4 bytes contain two Y values one for each pixel; one U and one V for both pixels. For each horizontal line, all the Y values are received first. The U values are received next and the V values are received last. For example for a horizontal line that has 720 pixels, there are 720 bytes of Y, followed by 360 bytes of U, followed by 360 bytes of V.

**YUV 4:2:2** – In this format each DWORD in the horizontal line represent two pixels. There are two Y values and one each U and V in a DWORD. Just as in the YUV 4:2:0 format, each U and V value describes the two pixels.

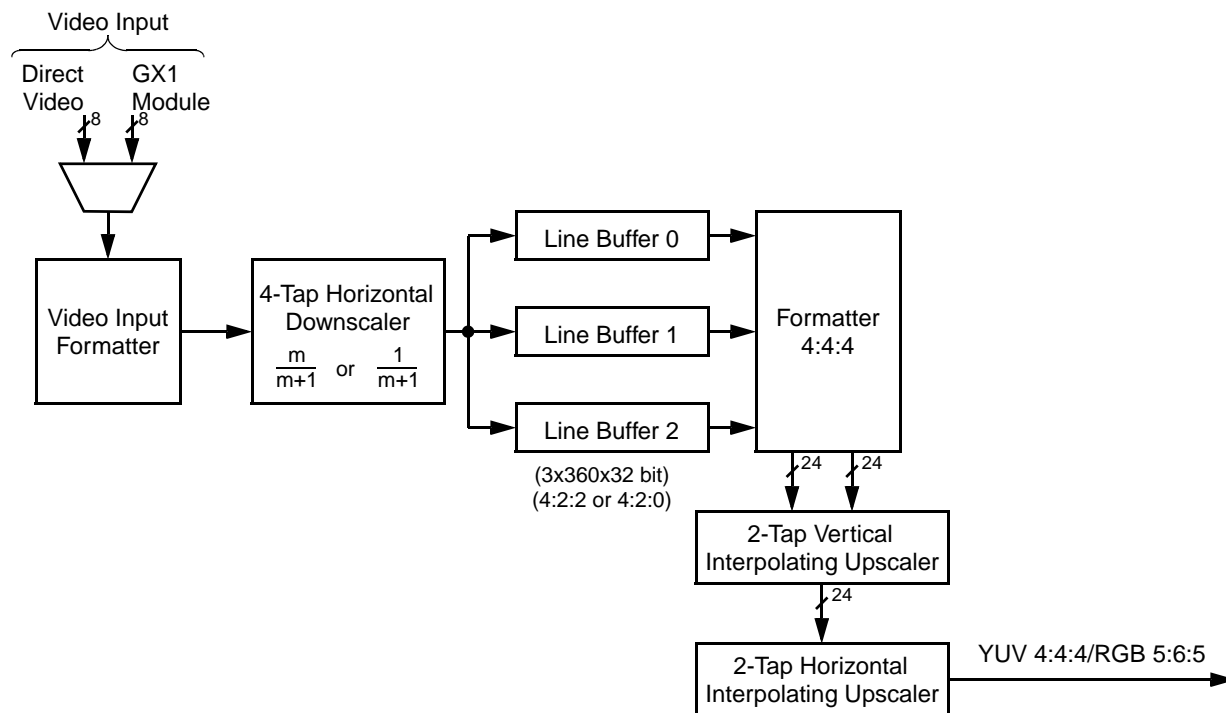


Figure 7-7. Video Block Diagram

### 7.2.2.2 Horizontal Downscaler with 4-Tap Filtering

The Video Processor implements up to 8:1 horizontal downscaling with 4-tap filtering for horizontal interpolation. Filtering is performed on video data input to the Video Processor. This data is fed to the filter and then to the downscaler. There is a bypass path for both filtering and downscaling logic. If this bypass is enabled, video data is written directly into the line buffers. (See Figure 7-8.)

#### Filtering

There are four 4-bit coefficients which can have programmed values of 0 to 15. The filter coefficients can be programmed via the Video Downscaler Coefficient register (F4BAR0+Memory Offset 40h) to increase picture quality.

#### Horizontal Downscaler

The Video Processor supports horizontal downscaling. The downscaler can be implemented in the Video Processor to shrink the video window by a factor of up to 8:1, in 1-pixel increments. The downscaler factor ( $m$ ) is programmed in the Video Downscaler Control register (F4BAR0+Memory Offset 3Ch[4:1]). If bit 0 of this register is set to 0, the downscaler logic is bypassed.

The horizontal downscaler supports downscaling of video data input format YUV 4:2:2 only.

The downscaler supports up to 29 downscaler factors. There are two types of factors:

- Type A is  $(1/m+1)$ . One pixel is retained, and  $m$  pixels are dropped. This enables downscaling factors of 1/16, 1/15, 1/14, 1/13, 1/12, 1/11, 1/10, 1/9, 1/8, 1/7, 1/6, 1/5, 1/4, 1/3, and 1/2.
- Type B is  $(m/m+1)$ .  $m$  pixels are retained, and one pixel is dropped. This enables downscaling factors of 2/3, 3/4, 4/5, 5/6, 6/7, 7/8, 8/9, 9/10, 10/11, 11/12, 12/13, 13/14, 14/15, and 15/16.

Bit 6 of the Video Downscaler Control register (F4BAR0+Memory Offset 3Ch) selects the type of downscaling factor to be used.

**Note:** There is no vertical downscaling in the Video Processor.

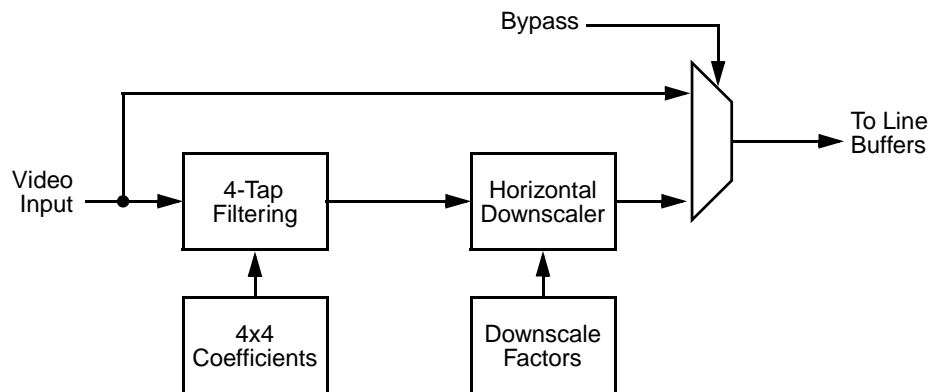


Figure 7-8. Horizontal Downscaler Block Diagram



### 7.2.2.3 Line Buffers

After the data has been optionally horizontally downscaled the video data is stored in a 3-line buffer. Each line is 360 DWORDs, which means a line width of up to 720 pixels can be stored. This buffer supports two functions. First, the clock domain of the video data changes from the GX1 module's video clock to the GX1 module's graphics clock. This clock domain change is required because the video data and graphics data can only be mixed/blended in the same clock domain. The second function the line buffer performs is to provide the necessary look ahead and look behind data in the vertical direction for the vertical upscaler. There is no direct program control of the line buffer.

### 7.2.2.4 Formatter

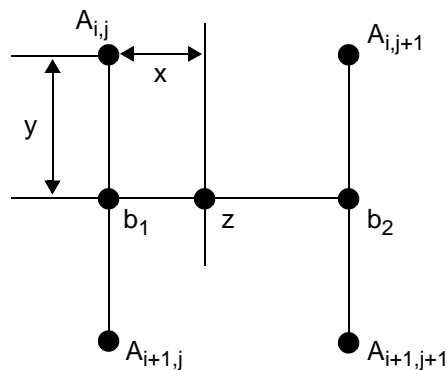
Video data in YUV 4:2:2 or YUV 4:2:0 format is converted to YUV 4:4:4 format. RGB data is not translated. There is no direct program control of the Formatter.

### 7.2.2.5 2-Tap Vertical and Horizontal Upscalers

After the video data has been buffered, the upscaling algorithm can be applied. The Video Processor employs a Digital Differential Analyzer-style (DDA) algorithm for both horizontal and vertical upscaling. The scaling parameters are programmed via the Video Upscale register (F4BAR0+Memory Offset 10h). The scalers support up to 8x factors for both horizontal and vertical scaling. The scaled video pixel stream is then passed through bi-linear interpolating filters (2-tap, 8-phase) to smooth the output video, significantly enhancing the quality of the displayed image.

The X and Y Upscaler uses the DDA and linear interpolating filter to calculate (via interpolation) the values of the pixels to be generated. The interpolation formula uses  $A_{i,j}$ ,  $A_{i,j+1}$ ,  $A_{i+1,j}$ , and  $A_{i+1,j+1}$  values to calculate the value of intermediate points. The actual location of calculated points is determined by the DDA algorithm.

The location of each intermediate point is one of eight phases between the original pixels (see Figure 7-9).



Notes:

$x$  and  $y$  are 0 - 7

$$b_1 = (A_{i,j}) \frac{8-y}{8} + (A_{i+1,j}) \frac{y}{8}$$

$$b_2 = (A_{i,j+1}) \frac{8-y}{8} + (A_{i+1,j+1}) \frac{y}{8}$$

$$z = (b_1) \frac{8-x}{8} + (b_2) \frac{x}{8}$$

Figure 7-9. Linear Interpolation Calculation

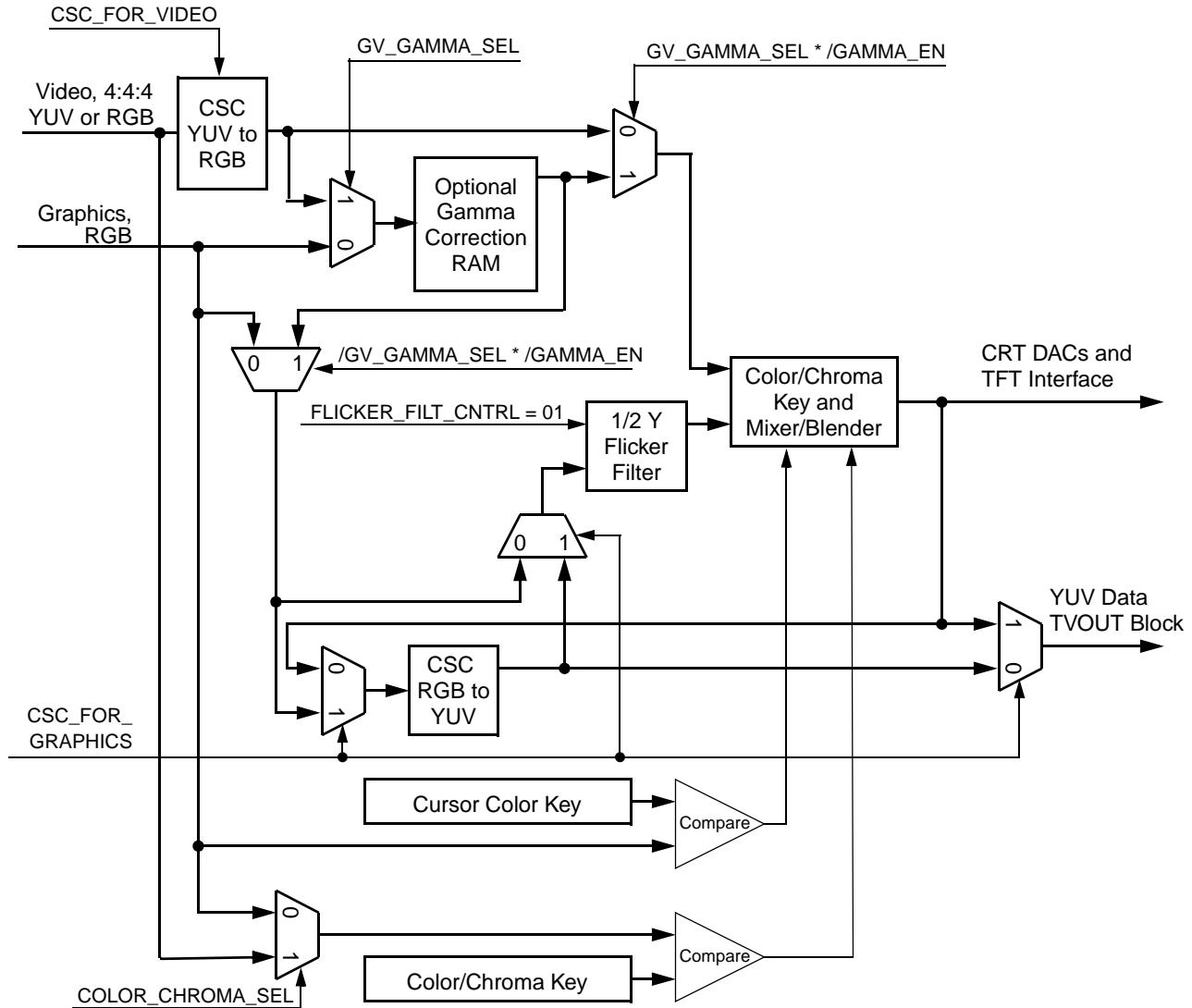
**7.2.3 Mixer/Blender Block**

The Mixer/Blender block of the Video Processor module performs all the necessary functions to properly mix/blend the video data and the graphics data. These functions include Color Space Conversion (CSC), optional Gamma correction, color/chroma key, and the mixing/blending logic. See Figure 7-10 for block diagram of the Mixer/Blender Block.

Video/Graphics mixing/blending must be performed in the RGB format. The YUV to RGB CSC (Section 7.2.3.1 on page 339) must be used on the video data if it is in YUV format. There is not a post mix/blend YUV to RGB CSC to support the TFT output. If Gamma Correction (see Section 7.2.3.2) on the video data is desired, it must be done in the color space of the input video data, which can be either YUV or RGB. If Gamma Correction on the graphics data is

desired, it must be done in the color space of the input graphics data, which is RGB.

The video data can be in progressive or interlaced format, while the graphics data is always in the progressive format. The Mixer/Blender can mix/blend either format of video data with graphics data. F4BAR0+Memory Offset 4Ch[9] programs the mix/blend format. Considering the color space and the data format, the Mixer/Blender supports five types of mixing/blending. Some of the mixing/blending types have additional programming considerations to enable them to work optimally. The valid mixing/blending configurations are listed in see Table 7-1 on page 339 along with any additional programming requirements.



**Figure 7-10. Mixer/Blender Block Diagram**

Table 7-1. Valid Mixing/Blending Configurations

| Mixing/Blending <sup>1</sup><br>(Bit) |    |    |   | Flicker<br>Filter <sup>2</sup> (Bit) |    | Mode  | Comment   |
|---------------------------------------|----|----|---|--------------------------------------|----|---|---|
| 13                                    | 11 | 10 | 9 | 30                                   | 29 |   |   |
| 0                                     | 0  | 1  | 0 | 0                                    | 0  | Input: YUV Progressive Video<br>Mixing: RGB                 | <ul style="list-style-type: none"> <li>Produces highest quality RGB output (see Section 7.2.1.2 "Capture Video Mode", Weave subsection on page 333).</li> </ul>   |
| 1                                     | 0  | 0  | 0 | 0                                    | 0  | Input: RGB Progressive Video<br>Mixing: RGB                 | <ul style="list-style-type: none"> <li>Produces highest quality RGB output (see Section 7.2.1.2 "Capture Video Mode", Weave subsection on page 333).</li> </ul>   |
| 0                                     | 1  | 0  | 1 | 0                                    | 1  | Input: YUV Interlaced Video<br>Mixing: YUV                  | <ul style="list-style-type: none"> <li>Not supported.</li> </ul>  |
| 0                                     | 1  | 0  | 0 | 0                                    | 0  | Input: YUV Progressive Video<br>Mixing: YUV                 | <ul style="list-style-type: none"> <li>Not supported.</li> </ul>  |
| 0                                     | 0  | 1  | 0 | 0                                    | 0  | Input: YUV Interlaced Video<br>upscaled by 2<br>Mixing: RGB | <ul style="list-style-type: none"> <li>Typically Direct Video mode.</li> <li>Must be vertically upscaled by a factor of 2 (see Section 7.2.2.5 "2-Tap Vertical and Horizontal Upscalers" on page 337).</li> </ul> |

1. F4BAR0+Memory Offset 4Ch[13, 11:9].

2. F4BAR0+Memory Offset 814h[30:29].

### 7.2.3.1 YUV to RGB CSC in Video Data Path

This CSC must be enabled if the video data is in the YUV color space. The CSC\_FOR\_VIDEO bit, F4BAR0+Memory Offset 4Ch[10], controls this CSC.

YUV video data is passed through this CSC to obtain 24-bit RGB data using the following CCIR-601-1 recommended formula:

- $R = 1.1640625(Y - 16) + 1.59375(V - 128)$
- $G = 1.1640625(Y - 16) - 0.8125(V - 128) - 0.390625(U - 128)$
- $B = 1.1640625(Y - 16) + 2.015625(U - 128)$

The CSC clamps inputs to prevent them from exceeding acceptable limits.

### 7.2.3.2 Gamma Correction

Either the video or graphics data can be routed through an integrated palette RAM for Gamma correction. There are three 256-byte RAMs, one for each color component value. Gamma correction supported in the YUV or RGB color space for the video data and RGB color space for the graphics data. Gamma correction is accomplished by treating each color component as an address into each RAM. The output of the RAM is the new color. A simple RGB Gamma correction example is to increase each color component by one. The address 00h in the RAMs would contain the data 01h. The address 01h would contain the data 02h and so on. This would have the effect of increasing each original Red, Green, and Blue value by one.

- G\_V\_GAMMA, F4BAR0+Memory Offset 04h[21] selects which data path (video or graphics) to send to the Gamma correction block. GAMMA\_EN, F4BAR0+Memory Offset 28h[0] enables the Gamma correction function. To load the Gamma correction palette RAM, use F4BAR0+Memory Offset 1Ch and 20h.

### 7.2.3.3 Color/Chroma Key

A color/chroma key mechanism is used to support the Mixer/Blender logic. There are two keys: key1 is for the cursor and key2 is for graphics or video data. Key1, the cursor key, is always a color key. The cursor color key registers are located at, F4BAR0+Memory Offset 50h-5CF. How the cursor key mechanism works with the Mixer/Blender is explained in Section 7.2.3.4. COLOR\_CHROMA\_KEY (F4BAR0+Memory Offset 04h[20]) determines whether key2 is a color key or a chroma key. The Video Color Key Register (F4BAR0+Memory Offset 14h) stores the key. Color keying is used when video is overlaid on the graphics (GFX\_INS\_VIDEO, F4BAR0+Memory Offset 4Ch[8] = 0). Chroma keying is used when graphics is overlaid on the video (GFX\_INS\_VIDEO = 1). How the color/chroma key mechanism works with the Mixer/Blender is explained in Section 7.2.3.4.

**7.2.3.4 Color/Chroma Key and Mixer/Blender**

The Mixer/Blender takes each pixel of the graphics and video data streams and mixes or blends them together. Mixing is simply choosing the graphics pixel or the video pixel. Blending takes a percentage of a graphics pixel (Alpha\_value \* Graphics\_pixel\_value) and percentage of the video pixel (1 - Alpha\_Value \* Video\_pixel\_value) and adds them together. The percentages of each add up to 100%. The actual formula is:

- Blended Pixel = (Alpha\_value \* Graphics\_pixel\_value) / 256 + ((256 – Alpha\_value) \* Video\_pixel\_value) / 256

Where: Alpha\_value = 0 to 255

Mixing and blending are supported simultaneously for every rendered frame, however, each pixel can only be mixed or blended. The mix or blend question is decided by the pixel position, whether video is overlaid on the graphics or visa versa (GFX\_INS\_VIDEO, F4BAR0+Memory Offset 4Ch[8]), and several programmed “windows”. Figure 7-11 illustrates and example frame.

**Graphics Window**

The graphics window is defined in the GX1 module’s display controller and is always the full screen resolution.

**Video Window**

The video window tells the Mixer/Blender where the video window is and its size. If Direct Video mode is enabled (see Section 7.2.1.1 "Direct Video Mode" on page 331), the video window must be defined as the resolution of the video port data resolution (720x480 for NTSC, 720x576 for

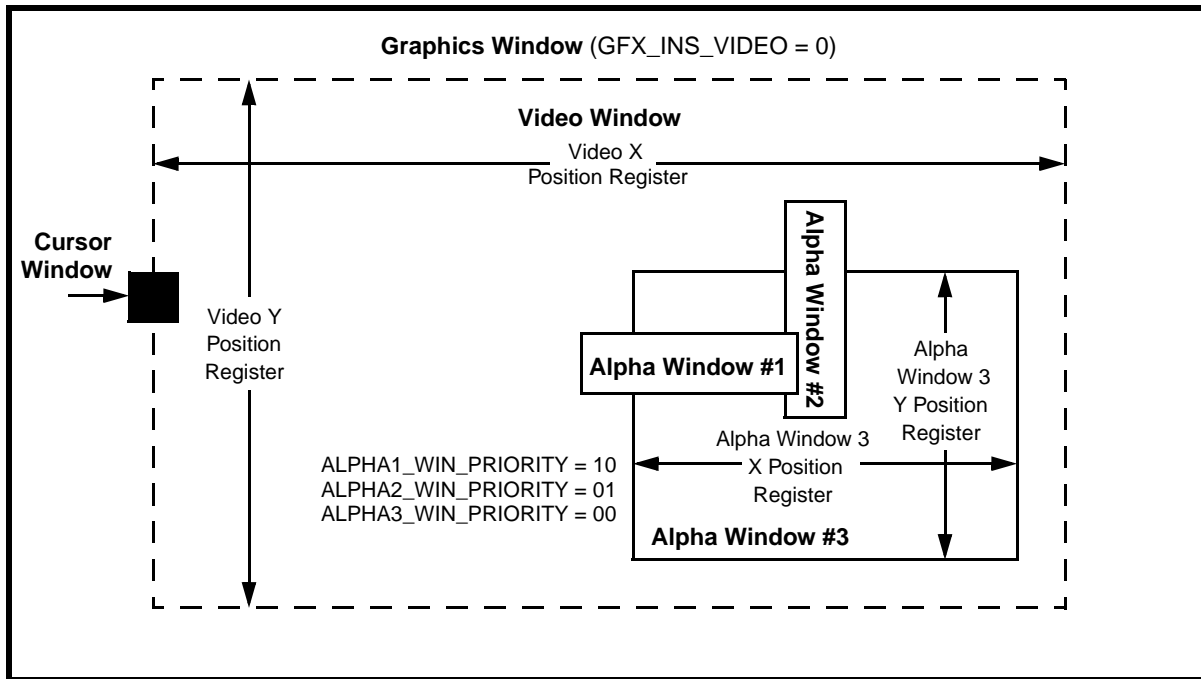
PAL). Vertical scaling is not allowed. Horizontal scaling is allowed. If the video source is from the GX1 module’s video frame buffer (which includes Capture Video mode, see Section 7.2.1.2 "Capture Video Mode" on page 332) then the video data can be scaled both horizontally and vertically. The video data size, scaled or unscaled, must equal the video window size. The Video X Position (horizontal) and Video Y Position (vertical) registers (F4BAR0+Memory Offset 08h and 0Ch) define the video window.

**Cursor Window**

The cursor window can be managed two ways: with the GX1 module’s hardware cursor or a software cursor. When using the hardware cursor, the displayed colors of the hardware cursor must be the cursor color keys (see Section 5.5.3 “Hardware Cursor” in the AMD Geode™ GX1 Processor Data Book). When the software cursor is used, the cursor size and position are not defined using registers. The cursor size, position, and image are determined through the use of the cursor color key colors in the graphics frame buffer. When the cursor is described in this manner, the cursor can be of any size and shape.

**Alpha Windows**

Up to three alpha windows can be defined. They are used only for blending. They can be of any size up to the graphics window size and they may overlap. To support overlapping of the alpha windows they can be prioritized as to which one is on top (F4BAR0+Memory Offset 4Ch[20:16]). The alpha windows are programmed at F4BAR0+Memory Offset 60h-88h.



**Figure 7-11. Graphics/Video Frame with Alpha Windows**

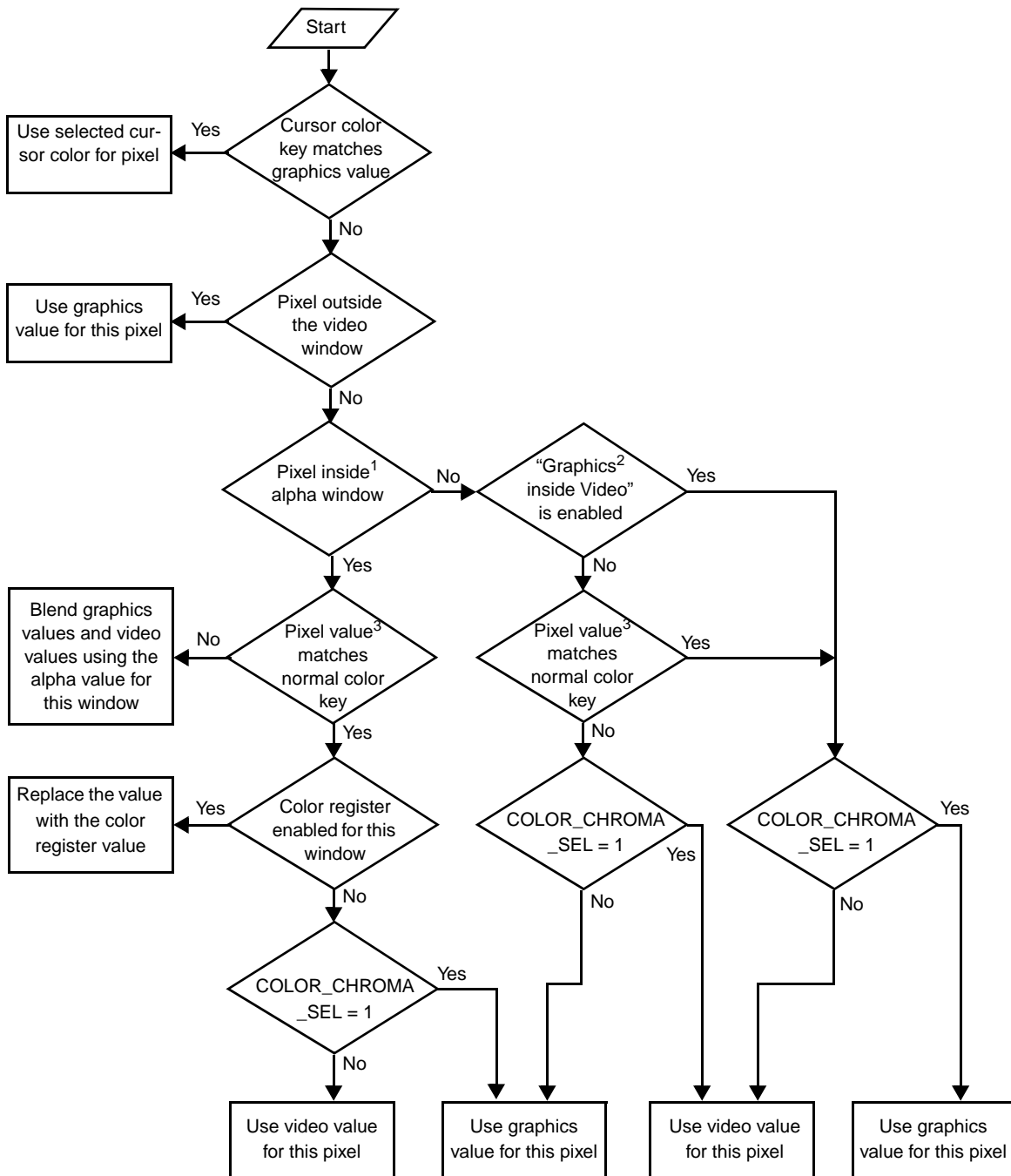
### Mixing/Blending Operation

Table 7-2 on page 341 shows the truth table used to create the flow diagram, Figure 7-12 on page 342, that the Mixer/Blender logic uses to determine each pixels disposition.

**Table 7-2. Truth Table for Alpha Blending**

| COLOR_<br>CHROMA_SEL <sup>1</sup>                      | Windows                   | Configuration <sup>2</sup> | Graphics<br>Data Match<br>Cursor<br>Color Key | Graphics<br>Data Match<br>Normal<br>Color Key | Video Data<br>Match<br>Normal<br>Color Key | Mixer Output                 |
|--|---------------------------|----------------------------|---|---|--|------------------------------|
| x  | x                         | x                          | Yes   | x   | x  | Cursor Color                 |
| x  | Not in Video<br>Window    | x                          | No  | x   | x  | Graphics Data                |
| Graphics Color<br>Key<br>(COLOR_<br>CHROMA_SEL<br>= 0) | Not in an Alpha<br>Window | GFX_INS_VIDEO = 0          | No  | Yes   | x  | Video Data                   |
|  |                           |                            | No  | No  | x  | Graphics Data                |
|  | GFX_INS_VIDEO = 1         | No                         | x   | x   | Video Data                                 |                              |
|  | Inside Alpha<br>Window x  | ALPHAx_COLOR_REG_EN = 1    | No  | Yes   | x  | Color from<br>Color Register |
|  |                           | ALPHAx_COLOR_REG_EN = 0    | No  | Yes   | x  | Video Data                   |
| x  | No                        | No                         | x   | Alpha-blended<br>Data                         |  |                              |
| Video Chroma<br>Key<br>(COLOR_<br>CHROMA_SEL<br>= 1)   | Not in an Alpha<br>Window | GFX_INS_VIDEO = 0          | No  | x   | Yes  | Graphics Data                |
|  |                           |                            | No  | x   | No   | Video Data                   |
|  |                           | GFX_INS_VIDEO = 1          | No  | x   | x  | Graphics Data                |
|  | Inside Alpha<br>Window x  | ALPHAx_COLOR_REG_EN = 1    | No  | x   | Yes  | Color from<br>Color Register |
|  |                           | ALPHAx_COLOR_REG_EN = 0    | No  | x   | Yes  | Graphics Data                |
| x  | No                        | x                          | No  | Alpha-blended<br>Data                         |  |                              |

1. COLOR\_CHROMA\_SEL: F4BAR0+Memory Offset 04h[20].
2. GFX\_INS\_VIDEO: F4BAR0+Memory Offset 4Ch[8].  
ALPHAx\_COLOR\_REG\_EN: F4BAR0+Memory Offsets 68h[24], 78h[24], and 88h[24].



**Notes:**

- 1) Alpha window should not be placed outside of the video window.
- 2) "Graphics inside Video" is enabled via bit GFX\_INS\_VIDEO in the Video De-interlacing and Alpha Control register (F4BAR0+Memory Offset 4Ch[8]).
- 3) The "Pixel Value" refers to either the Video value or the Graphics value, depending on the setting of bit COLOR\_CHROMA\_SEL in the Display Configuration register (F4BAR0+Memory Offset 04h[20]).

**Figure 7-12. Color Key and Alpha Blending Logic**

### 7.2.4 TFT Interface

The TFT interface can be programmed to one of two sets of balls: IDE balls or Parallel Port balls. PMR[23] of the General Configuration registers program where the TFT interface exists (see Table 4-2 on page 88).

**Note:** If the TFT interface is on the IDE balls, the maximum FPCLK supported is 40 MHz. If the TFT interface is on the Parallel Port balls the maximum FPCLK supported is 80 MHz.

Support for a TFT panel requires power sequencing and an 18-bit (6-bit RGB), digital output. The relevant digital output signals are available from the SC3200.

TFT output signals are:

- TFTD[5:0] for blue signals
- TFTD[11:6] for green signals
- TFTD[17:12] for red signals
- HSYNC and VSYNC - sync signals

- TFTDCK - data clock signal.
- TFTDE - data enable signal.
- FP\_VDD\_ON - power control signal

#### Power Sequence

Power sequence is used to control assertion of FP\_VDD\_ON and TFTD signals.

All bits related to power sequence configuration are located in the Display Configuration register (F4BAR0+Memory Offset 04h).

After enabling TFT\_EN (bit 0), and FP\_PWR\_EN (bit 6), the state machine waits until the next VSYNC to switch on the FP\_VDD\_ON signal. The state machine then asserts the TFTD[17:0] signals after the delay programmed via PWR\_SEQ\_DLY (bits [19:17]) When FP\_PWR\_EN (bit 6) is set to 0, the reverse sequence happens for powering down the TFT.

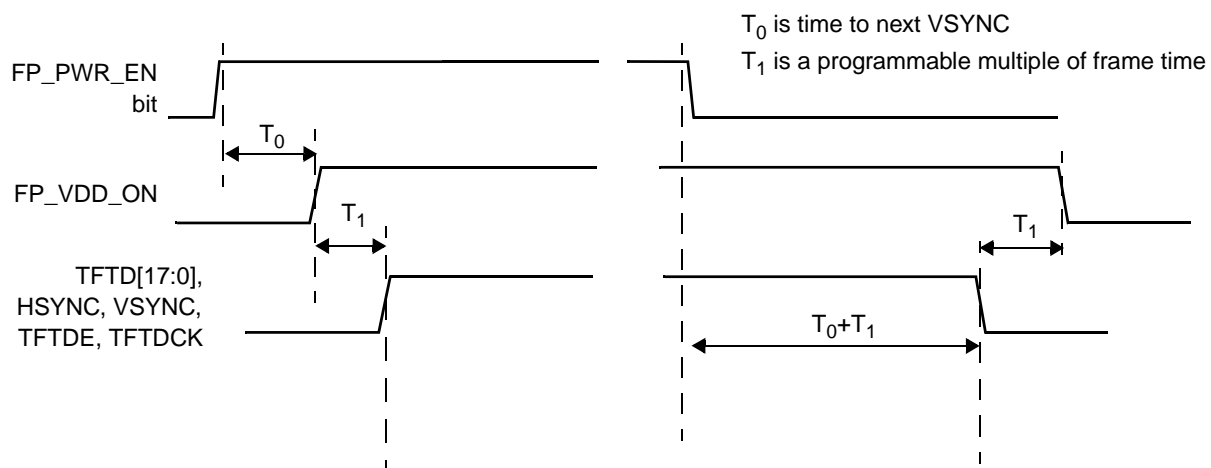


Figure 7-13. TFT Power Sequence

### 7.2.5 Integrated PLL

The integrated PLL can generate frequencies up to 135 MHz from a single 27 MHz source. The clock frequency is programmable using two registers. Figure 7-14 shows the block diagram of the Video Processor integrated PLL.

$F_{REF}$  is 27 MHz, generated by an external crystal and an integrated oscillator.  $F_{OUT}$  is calculated from:

$$F_{OUT} = (m + 1) / (n + 1) \times F_{REF}$$

The integrated PLL can generate any frequency by writing into the “m” and “n” bit fields (F4BAR0+Memory Offset 2Ch, m = bits [14:8] and n = bits [3:0]). Additionally, 16 preprogrammed VGA frequencies can be selected via the PLL Clock Select register (F4BAR0+Memory Offset 2Ch[19:16]), if the crystal oscillator has a frequency of 27 MHz. This PLL can be powered down via the Miscellaneous register (F4BAR0+Memory Offset 28h[12]).

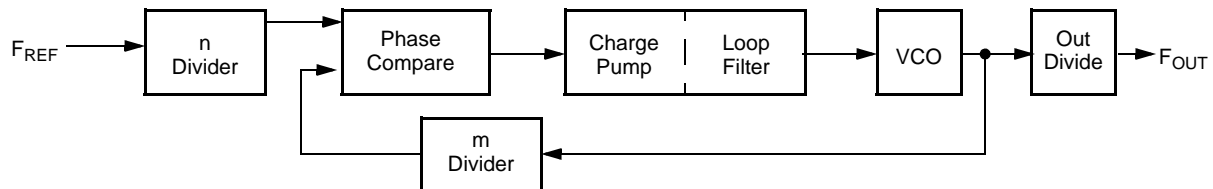


Figure 7-14. PLL Block Diagram



## 7.3 Register Descriptions

The register space for accessing and configuring the Video Processor is located in the Core Logic Chipset Register Space (F0-F5). The Chipset Register Space is accessed via the PCI interface using the PCI Type One Configuration Mechanism (see Section 6.3.1 "PCI Configuration Space and Access Methods" on page 191).

### 7.3.1 Register Summary

The tables in this subsection summarize the registers of the Video Processor. Included in the tables are the register's reset values and page references where the bit formats are found.

**Table 7-3. F4: PCI Header Registers for Video Processor Support Summary**

| F4 Index | Width (Bits) | Type | Name  | Reset Value | Reference (Table 7-6) |
|----------|--------------|------|---|-------------|-----------------------|
| 00h-01h  | 16           | RO   | Vendor Identification Register  | 100Bh       | Page 348              |
| 02h-03h  | 16           | RO   | Device Identification Register  | 0504h       | Page 348              |
| 04h-05h  | 16           | R/W  | PCI Command Register  | 0000h       | Page 348              |
| 06h-07h  | 16           | RO   | PCI Status Register   | 0280h       | Page 348              |
| 08h      | 8            | RO   | Device Revision ID Register   | 01h         | Page 348              |
| 09h-0Bh  | 24           | RO   | PCI Class Code Register   | 030000h     | Page 348              |
| 0Ch      | 8            | RO   | PCI Cache Line Size Register  | 00h         | Page 348              |
| 0Dh      | 8            | RO   | PCI Latency Timer Register  | 00h         | Page 348              |
| 0Eh      | 8            | RO   | PCI Header Type Register  | 00h         | Page 348              |
| 0Fh      | 8            | RO   | PCI BIST Register   | 00h         | Page 348              |
| 10h-13h  | 32           | R/W  | Base Address Register 0 (F4BAR0). Sets the base address for the memory-mapped Video Configuration Registers within the Video Processor. Refer to Table 7-7 on page 350 for programming information regarding the register offsets accessed through this register. | 00000000h   | Page 348              |
| 14h-17h  | 32           | R/W  | Base Address Register 1 (F4BAR1). Reserved.   | 00000000h   | Page 348              |
| 18h-1Bh  | 32           | R/W  | Base Address Register 2 (F4BAR2). Sets the base address for the memory-mapped VIP (Video Interface Port) Registers (summarized in Table 7-8 on page 363).   | 00000000h   | Page 348              |
| 1Ch-2Bh  | --           | --   | Reserved  | 00h         | Page 348              |
| 2Ch-2Dh  | 16           | RO   | Subsystem Vendor ID   | 100Bh       | Page 348              |
| 2Eh-2Fh  | 16           | RO   | Subsystem ID  | 0504h       | Page 348              |
| 30h-3Bh  | --           | --   | Reserved  | 00h         | Page 348              |
| 3Ch      | 8            | R/W  | Interrupt Line Register   | 00h         | Page 348              |
| 3Dh      | 8            | R/W  | Interrupt Pin Register  | 03h         | Page 349              |
| 3Eh-FFh  | ---          | ---  | Reserved  | 00h         | Page 349              |

**Table 7-4. F4BAR0: Video Processor Configuration Registers Summary**

| F4BAR0+ Memory Offset | Width (Bits) | Type | Name                           | Reset Value | Reference (Table 7-7) |
|-----------------------|--------------|------|--------------------------------|-------------|-----------------------|
| 00h-03h               | 32           | R/W  | Video Configuration Register   | 00000000h   | Page 350              |
| 04h-07h               | 32           | R/W  | Display Configuration Register | x0000000h   | Page 351              |
| 08h-0Bh               | 32           | R/W  | Video X Position Register      | 00000000h   | Page 352              |
| 0Ch-0Fh               | 32           | R/W  | Video Y Position Register      | 00000000h   | Page 352              |
| 10h-13h               | 32           | R/W  | Video Upscaler Register        | 00000000h   | Page 352              |
| 14h-17h               | 32           | R/W  | Video Color Key Register       | 00000000h   | Page 353              |
| 18h-1Bh               | 32           | R/W  | Video Color Mask Register      | 00000000h   | Page 353              |
| 1Ch-1Fh               | 32           | R/W  | Palette Address Register       | xxxxxxxxh   | Page 353              |
| 20h-23h               | 32           | R/W  | Palette Data Register          | xxxxxxxxh   | Page 353              |
| 24h-27h               | 32           | RO   | Reserved                       | ---         | Page 353              |

Table 7-4. F4BAR0: Video Processor Configuration Registers Summary (Continued)

| F4BAR0+<br>Memory<br>Offset | Width<br>(Bits) | Type | Name  | Reset<br>Value | Reference<br>(Table 7-7) |
|-----------------------------|-----------------|------|---|----------------|--------------------------|
| 28h-2Bh                     | 32              | R/W  | Miscellaneous Register                          | 00001400h      | Page 354                 |
| 2Ch-2Fh                     | 32              | R/W  | PLL2 Clock Select Register                      | 00000000h      | Page 354                 |
| 30h-33h                     | 32              | ---  | Reserved  | 00000000h      | Page 354                 |
| 34h-37h                     | 32              | RO   | Reserved  | 00000000h      | Page 354                 |
| 38h-3Bh                     | 32              | RO   | Reserved  | 00000000h      | Page 354                 |
| 3Ch-3Fh                     | 32              | R/W  | Video Downscaler Control Register               | 00000000h      | Page 355                 |
| 40h-43h                     | 32              | R/W  | Video Downscaler Coefficient Register           | 00000000h      | Page 355                 |
| 44h-47h                     | 32              | R/W  | CRC Signature Register                          | xxxxx100h      | Page 355                 |
| 48h-4Bh                     | 32              | RO   | Device and Revision Identification              | 0000015xh      | Page 355                 |
| 4Ch-4Fh                     | 32              | R/W  | Video De-Interlacing and Alpha Control Register | 00060000h      | Page 356                 |
| 50h-53h                     | 32              | R/W  | Cursor Color Key Register                       | 00000000h      | Page 357                 |
| 54h-57h                     | 32              | R/W  | Cursor Color Mask Register                      | 00000000h      | Page 357                 |
| 58h-5Bh                     | 32              | R/W  | Cursor Color Register 1                         | 00000000h      | Page 357                 |
| 5Ch-5Fh                     | 32              | R/W  | Cursor Color Register 2                         | 00000000h      | Page 357                 |
| 60h-63h                     | 32              | R/W  | Alpha Window 1 X Position Register              | 00000000h      | Page 358                 |
| 64h-67h                     | 32              | R/W  | Alpha Window 1 Y Position Register              | 00000000h      | Page 358                 |
| 68h-6Bh                     | 32              | R/W  | Alpha Window 1 Color Register                   | 00000000h      | Page 358                 |
| 6Ch-6Fh                     | 32              | R/W  | Alpha Window 1 Control Register                 | 00000000h      | Page 358                 |
| 70h-73h                     | 32              | R/W  | Alpha Window 2 X Position Register              | 00000000h      | Page 359                 |
| 74h-77h                     | 32              | R/W  | Alpha Window 2 Y Position Register              | 00000000h      | Page 359                 |
| 78h-7Bh                     | 32              | R/W  | Alpha Window 2 Color Register                   | 00000000h      | Page 359                 |
| 7Ch-7Fh                     | 32              | R/W  | Alpha Window 2 Control Register                 | 00000000h      | Page 359                 |
| 80h-83h                     | 32              | R/W  | Alpha Window 3 X Position Register              | 00000000h      | Page 360                 |
| 84h-87h                     | 32              | R/W  | Alpha Window 3 Y Position Register              | 00000000h      | Page 360                 |
| 88h-8Bh                     | 32              | R/W  | Alpha Window 3 Color Register                   | 00000000h      | Page 360                 |
| 8Ch-8Fh                     | 32              | R/W  | Alpha Window 3 Control Register                 | 00000000h      | Page 360                 |
| 90h-93h                     | 32              | R/W  | Video Request Register                          | 001B0017h      | Page 361                 |
| 94h-97h                     | 32              | RO   | Alpha Watch Register                            | 00000000h      | Page 361                 |
| 98h-3FFh                    |                 | ---  | Reserved  | ---            | Page 361                 |
| 400h-403h                   | 32              | R/W  | Video Processor Display Mode Register           | 00000000h      | Page 361                 |
| 404h-407h                   | 32              | ---  | Reserved  | 00000000h      | Page 361                 |
| 408h-40Bh                   | 32              | R/W  | Video Processor Test Mode Register              | 00000000h      | Page 361                 |
| 40Ch-41Fh                   | ---             | ---  | Reserved  | 00000000h      | Page 361                 |
| 420h-423h                   | 32              | R/W  | GenLock Register                                | 00000000h      | Page 362                 |
| 424h-427h                   | 32              | R/W  | GenLock Delay Register                          | 00000000h      | Page 362                 |
| 428h-43Bh                   | ---             | ---  | Reserved  | ---            | Page 362                 |
| 43Ch-43Fh                   | 32              | R/W  | Continuous GenLock Time-out Register            | 1FFF1FFFh      | Page 362                 |

Table 7-5. F4BAR2: VIP Support Registers Summary

| F4BAR2+<br>Memory<br>Offset | Width<br>(Bits) | Type | Name  | Reset<br>Value | Reference<br>(Table 7-8) |
|-----------------------------|-----------------|------|---|----------------|--------------------------|
| 00h-03h                     | 32              | R/W  | Video Interface Port Configuration Register | 00000000h      | Page 363                 |
| 04h-07h                     | 32              | R/W  | Video Interface Control Register            | 00000000h      | Page 363                 |
| 08h-0Bh                     | 32              | R/W  | Video Interface Status Register             | xxxxxxxh       | Page 364                 |
| 0Ch-0Fh                     | --              | --   | Reserved                                    | 00000000h      | Page 365                 |
| 10h-13h                     | 32              | RO   | Video Current Line Register                 | xxxxxxxh       | Page 365                 |
| 14h-17h                     | 32              | R/W  | Video Line Target Register                  | 00000000h      | Page 365                 |
| 18h-1Fh                     | ---             | ---  | Reserved                                    | 00000000h      | Page 365                 |
| 20h-23h                     | 32              | R/W  | Video Data Odd Base Register                | 00000000h      | Page 365                 |
| 24h-27h                     | 32              | R/W  | Video Data Even Base Register               | 00000000h      | Page 365                 |
| 28h-2Bh                     | 32              | R/W  | Video Data Pitch Register                   | 00000000h      | Page 365                 |
| 2Ch-3Fh                     | --              | --   | Reserved                                    | 00000000h      | Page 365                 |
| 40h-43h                     | 32              | R/W  | VBI Data Odd Base Register                  | 00000000h      | Page 366                 |
| 44h-47h                     | 32              | R/W  | VBI Data Even Base Register                 | 00000000h      | Page 366                 |
| 48h-4Bh                     | 32              | R/W  | VBI Data Pitch Register                     | 00000000h      | Page 366                 |
| 4Ch-1FFh                    | --              | --   | Reserved                                    | 00000000h      | Page 366                 |

### 7.3.2 Video Processor Registers - Function 4

The register space designated as Function 4 (F4) is used to configure the PCI portion of support hardware for accessing the Video Processor support registers, including VIP (separate BAR). The bit formats for the PCI Header registers are given in Table 7-6.

Located in the PCI Header Registers of F4 are three Base Address Registers (F4BARx) used for pointing to the register spaces designated for Video Processor support. F4BAR0 is for Video Processor Configuration, F4BAR1 is reserved, and F4BAR2 is for VIP configuration.

**Table 7-6. F4: PCI Header Registers for Video Processor Support Registers**

| Bit  | Description   |
|--|---|
| Index 00h-01h  | Vendor Identification Register (RO) <span style="float:right">Reset Value: 100Bh</span>   |
| Index 02h-03h  | Device Identification Register (RO) <span style="float:right">Reset Value: 0504h</span>   |
| Index 04h-05h  | PCI Command Register (R/W) <span style="float:right">Reset Value: 0000h</span>  |
| 15:2   | Reserved. (Read Only)   |
| 1  | <b>Memory Space.</b> Allow the Core Logic module to respond to memory cycles from the PCI bus.<br>0: Disable.<br>1: Enable.<br>This bit must be enabled to access memory offsets through F4BAR0, F4BAR1, and F4BAR2 (see F4 Index 10h, 14h, and 18h). |
| 0  | Reserved. (Read Only)   |
| Index 06h-07h  | PCI Status Register (RO) <span style="float:right">Reset Value: 0280h</span>  |
| Index 08h  | Device Revision ID Register (RO) <span style="float:right">Reset Value: 01h</span>  |
| Index 09h-0Bh  | PCI Class Code Register (RO) <span style="float:right">Reset Value: 030000h</span>  |
| Index 0Ch  | PCI Cache Line Size Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Dh  | PCI Latency Timer Register (RO) <span style="float:right">Reset Value: 00h</span>   |
| Index 0Eh  | PCI Header Type (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 0Fh  | PCI BIST Register (RO) <span style="float:right">Reset Value: 00h</span>  |
| Index 10h-13h  | Base Address Register 0 - F4BAR0 (R/W) <span style="float:right">Reset Value: 00000000h</span>  |
| <b>Video Processor Video Memory Address Space.</b> This register allows PCI access to the memory mapped Video Processor configuration registers. Bits [11:0] are read only (0000 0000 0000) indicating a 4 KB memory address range. See Table 7-7 on page 350 for bit formats and reset values of the registers accessed through this base address register. |   |
| 31:12  | Video Processor Video Memory Base Address.  |
| 11:0   | Address Range. (Read Only)  |
| Index 14h-17h  | Base Address Register 1 - F4BAR1 (R/W) <span style="float:right">Reset Value: 00000000h</span>  |
| Reserved   |   |
| Index 18h-1Bh  | Base Address Register 2 - F4BAR2 (R/W) <span style="float:right">Reset Value: 00000000h</span>  |
| <b>VIP Address Space.</b> This register allows access to memory mapped VIP (Video Interface Port) related registers. Bits [11:0] are read only (0000 0000 0000), indicating a 4 KB I/O address range. Refer to Table 7-8 for the VIP register bit formats and reset values.  |   |
| 31:12  | VIP Base Address.   |
| 11:0   | Address Range. (Read Only)  |
| Index 1Ch-2Bh  | Reserved <span style="float:right">Reset Value: 00h</span>  |
| Index 2Ch-2Dh  | Subsystem Vendor ID (RO) <span style="float:right">Reset Value: 100Bh</span>  |
| Index 2Eh-2Fh  | Subsystem ID (RO) <span style="float:right">Reset Value: 0504h</span>   |
| Index 30h-3Bh  | Reserved <span style="float:right">Reset Value: 00h</span>  |
| Index 3Ch  | Interrupt Line Register (R/W) <span style="float:right">Reset Value: 00h</span>   |
| This register identifies the system interrupt controllers to which the device's interrupt pin is connected. The value of this register is used by device drivers and has no direct meaning to this function.   |   |

**Table 7-6. F4: PCI Header Registers for Video Processor Support Registers (Continued)**

| Bit                  | Description  |
|----------------------|--|
| <b>Index 3Dh</b>     | <b>Interrupt Pin Register (R/W)</b> <span style="float: right;"><b>Reset Value: 03h</b></span><br>This register selects which interrupt pin the device uses. VIP uses INTC# after reset. INTA#, INTB# or INTD# can be selected by writing 1, 2 or 4, respectively. |
| <b>Index 3Eh-FFh</b> | <b>Reserved</b> <span style="float: right;"><b>Reset Value: 00h</b></span>   |

### 7.3.2.1 Video Processor Support Registers - F4BAR0

F4 Index 10h, Base Address Register 0 (F4BAR0) sets the base address that allows PCI access to the Video Processor support registers, not including VIP. A separate base address register (F4BAR2) is used to access VIP support registers (see Section 7.3.2.2 on page 363).

**Note:** Reserved bits that are not defined as “must be set to 0 or 1” should be written with a value that is read from them.

**Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers**

| Bit   | Description  |
|---|--|
| <b>Offset 00h-03h</b>   |  |
| <b>Video Configuration Register (R/W)</b>                                     |  |
| <b>Reset Value: 0000000h</b>  |  |
| Configuration register for options of the motion video acceleration hardware. |  |
| 31:29   | <b>Reserved.</b> Must be set to 0.   |
| 28  | <b>EN_42X (Enable 4:2:x Format).</b> Allows format selection.<br>0: 4:2:2 format.<br>1: 4:2:0 format.<br><b>Note:</b> When input video stream is RGB (i.e., F4BAR0+Memory Offset 4Ch[13] = 1), this bit must be set to 0.  |
| 27  | <b>BIT_8_LINE_SIZE.</b> When enabled, this bit increases line size from VID_LIN_SIZ (bits [15:8]) DWORDs by adding 256 DWORDs.<br>0: Disable.<br>1: Enable.  |
| 26:25   | <b>Reserved.</b> Must be set to 0.   |
| 24:16   | <b>INIT_RD_ADDR (Initial Buffer Read Address).</b> This field preloads the starting read address for the line buffers at the beginning of each display line. It is used for hardware clipping of the video window at the left edge of the active display. It represents the DWORD address of the source pixel which is to be displayed first.<br>For an unclipped window, this value should be 0. For 4:2:0 format, set bits [17:16] to 00.  |
| 15:8  | <b>VID_LIN_SIZ (Video Line Size).</b> Represents the number of DWORDs that make up the horizontal size of the source video data.   |
| 7   | <b>YFILT_EN (Y Filter Enable).</b> Enables/disables the vertical filter.<br>0: Disable. Upscaling done by repeating pixels.<br>1: Enable. Upscaling done by interpolating pixels.<br><b>Note:</b> This bit is used with Y upscaling logic. Reset to 0 when not required.   |
| 6   | <b>XFILT_EN (X Filter Enable).</b> Enables/disables the horizontal filter.<br>0: Disable. Upscaling done by repeating pixels.<br>1: Enable. Upscaling done by interpolating pixels.<br><b>Note:</b> This bit is used with X upscaling logic. Reset to 0 when not required.   |
| 5:4   | <b>Reserved.</b>   |
| 3:2   | <b>VID_FMT (Video Format).</b> Byte ordering of video data on the Video Input bus (VPD[7:0]). The interpretation of these bits depends on the settings of bit 13 (GV_SEL) in the Video De-Interlacing and Alpha Control register (F4BAR0+Memory Offset 4Ch) and bit 28 (EN_42X) of this register.<br>If GV_SEL = 0 and EN_42X = 0:<br>00: Cb Y0 Cr Y1                                      10: Y0 Cb Y1 Cr<br>01: Y1 Cr Y0 Cb                                      11: Y0 Cr Y1 Cb<br>If GV_SEL = 0 and EN_42X = 1:<br>00: Y0 Y1 Y2 Y3                                      10: Y1 Y0 Y3 Y2<br>01: Y3 Y2 Y1 Y0                                      11: Y1 Y2 Y3 Y0<br>If GV_SEL = 1 and EN_42X = 0:<br>00: P1L P1M P2L P2M                                      10: P1M P1L P2M P2L<br>01: P2M P2L P1M P1L                                      11: P1M P2L P2M P1L<br>If GV_SEL = 1 and EN_42X = 1: Reserved<br><b>Note:</b> Both RGB 5:6:5 and YUV 4:2:2 contain two pixels in each 32-bit DWORD. YUV 4:2:0 contains a stream of Y data for each line, followed by U and V data for that same line. |
| 1   | <b>Reserved.</b>   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| 0   | <b>VID_EN (Video Enable).</b> Enables video acceleration hardware.<br>0: Disable (reset) video module.<br>1: Enable.   |
| <b>Offset 04h-07h</b> <b>Display Configuration Register (R/W)</b> <b>Reset Value: x0000000h</b>   |  |
| General configuration register for display control. This register is also used to determine how graphics and video data are to be combined in the display on the output device. |  |
| 31  | <b>Reserved.</b> Write as read.  |
| 30:28   | <b>Reserved.</b>   |
| 27  | <b>FP_ON_STATUS (Flat Panel On Status). (Read Only)</b> Shows whether power to the attached flat panel is on or off. This bit transitions at the end of the power-up or power-down sequence.<br>0: Power to the flat panel is off.<br>1: Power to the flat panel is on.  |
| 26  | <b>Reserved.</b> Set to 0.   |
| 25  | <b>Reserved.</b> Must be set to 0.   |
| 24:22   | <b>Reserved.</b> Set to 0.   |
| 21  | <b>GV_GAMMA_SEL (Graphics or Video Gamma Source Data).</b> Selects whether the graphics or video data goes to the Gamma Correction RAM. GAMMA_EN (F4BAR0+Memory Offset 28h[0]) must be enabled for the selected data source to pass through the Gamma Correction RAM.<br>0: Graphics data to Gamma Correction RAM.<br>1: Video data to Gamma Correction RAM.<br><b>Note:</b> Gamma Correction is always in the RGB domain for graphics data.<br>Gamma Correction can be in the YUV or RGB domain for video data. |
| 20  | <b>COLOR_CHROMA_SEL (Color or Chroma Key Select).</b> Selects whether the graphics is used for color keying or the video data stream is used for chroma keying.<br>0: Graphics data is compared to the color key.<br>1: Video data is compared to the chroma key.  |
| 19:17   | <b>PWR_SEQ_DLY (Power Sequence Delay).</b> Selects the number of frame periods that transpire between successive transitions of the power sequence control lines.  |
| 16:14   | <b>Reserved.</b> Write as read.  |
| 13:8  | <b>Reserved.</b> Write as read.  |
| 7   | <b>FP_DATA_EN (Flat Panel Output Enable).</b> Controls the data, data-enable, clock and sync output signals.<br>0: Flat panel data outputs are forced to zero depending on the value of bit 3 (BL_EN). Bit 6 (FP_PWR_EN) is ignored.<br>1: Flat panel outputs are forced to zero until power-up, and later, data outputs are subject to the value of bit 3 (BL_EN).  |
| 6   | <b>FP_PWR_EN (Flat Panel Power Enable).</b> Changing this bit initiates a flat panel power-up or power-down.<br>0-to-1: Power-up flat panel.<br>1-to-0: Power-down flat panel.   |
| 5:4   | <b>Reserved.</b>   |
| 3   | <b>BL_EN (Blank Enable).</b> Controls blanking of TFT data.<br>0: TFT data is constantly blanked.<br>1: TFT data is blanked normally (i.e., during horizontal and vertical blank).   |
| 2   | <b>VSYNC_EN (Vertical Sync Enable).</b> Enables/disables display vertical sync (used for VESA DPMS support).<br>0: Disable.<br>1: Enable.  |
| 1   | <b>HSYNC_EN (Horizontal Sync Enable).</b> Enables/disables display horizontal sync (used for VESA DPMS support).<br>0: Disable.<br>1: Enable.  |
| 0   | <b>TFT_EN (TFT Enable).</b> Enables the TFT control logic and is also used to reset the TFT control logic.<br>0: Reset TFT control logic.<br>1: Enable TFT control logic.  |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 08h-0Bh</b> <span style="float:right"><b>Video X Position Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span><br>Provides the window X position. This register is programmed relative to CRT horizontal sync input (not physical screen position).<br><b>Note:</b> H_TOTAL and H_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8330h[26:19] and 8338h[10:3], respectively). The value of (H_TOTAL – H_SYNC_END) is sometimes referred to as "horizontal back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> . |  |
| 31:28  | <b>Reserved.</b>   |
| 27:16  | <b>VID_X_END (Video X End Position).</b> Represents the horizontal end position of the video window (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 13.  |
| 15:12  | <b>Reserved.</b>   |
| 11:0   | <b>VID_X_START (Video X Start Position).</b> Represents the horizontal start position of the video window. This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 14.  |
| <b>Offset 0Ch-0Fh</b> <span style="float:right"><b>Video Y Position Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span><br>Provides the window Y position. This register is programmed relative to CRT vertical sync input (not physical screen position).<br><b>Note:</b> V_TOTAL and V_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8340h[26:16] and 8348h[26:16], respectively). The value of (V_TOTAL – V_SYNC_END) is sometimes referred to as "vertical back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .    |  |
| 31:27  | <b>Reserved.</b>   |
| 26:16  | <b>VID_Y_END (Video Y End Position).</b> Represents the vertical end position of the video window (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 2.   |
| 15:11  | <b>Reserved.</b>   |
| 10:0   | <b>VID_Y_START (Video Y Start Position).</b> Represents the vertical start position of the video window. This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 1.   |
| <b>Offset 10h-13h</b> <span style="float:right"><b>Video Upscale Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 0000000h</b></span><br>Provides horizontal and vertical upscale factors of the window.  |  |
| 31:30  | <b>Reserved.</b>   |
| 29:16  | <b>VID_Y_SCL (Video Y Scale Factor).</b> Represents the vertical upscale factor of the video window according to the following formula:<br>$\text{VID\_Y\_SCL} = 8192 * (\text{Ys} - 1) / (\text{Yd} - 1)$ where:<br>Ys = Video source vertical size in pixels<br>Yd = Video destination vertical size in pixels<br><b>Note:</b> Upscale factor must be used. Yd is equal or bigger than Ys. If no scaling is intended, set to 2000h. The actual scale factor used is VID_Y_SCL/8192, but the formula above fits a given source number of lines into a destination window size.<br><b>Note:</b> When progressive mixing/blending is programmed (F4BAR0+Memory Offset 4Ch[9] = 0) and the video data is interlaced, this register should be programmed to 1000h to double the vertical lines, |
| 15:14  | <b>Reserved.</b>   |
| 13:0   | <b>VID_X_SCL (Video X Scale Factor).</b> Represents horizontal upscale factor of the video window according to the following formula:<br>$\text{VID\_X\_SCL} = 8192 * (\text{Xs} - 1) / (\text{Xd} - 1)$ where:<br>Xs = Video source horizontal size in pixels<br>Xd = Video destination vertical size in pixels<br><b>Note:</b> Upscale factor must be used. Xd is equal or bigger than Xs. If no scaling is intended, set to 2000h. The actual scale factor used is VID_X_SCL/8192, but the formula above fits a given source number of pixels into a destination window size.   |



Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 14h-17h</b> <span style="float: right;"><b>Video Color Key Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br>Provides the video color key. The color key can be used to allow irregular shaped overlays of graphics onto video, or video onto graphics, within a scaled video window.  |  |
| 31:24  | <b>Reserved.</b>   |
| 23:0   | <b>VID_CLR_KEY (Video Color Key).</b> The video color key is a 24-bit RGB or YUV value. <ul style="list-style-type: none"> <li>If the COLOR_CHROMA_SEL bit (F4BAR0+Memory Offset 04h[20]) = 0:               <ul style="list-style-type: none"> <li>The video pixel is selected within the target window if the corresponding graphics pixel matches the color key. The color key in an RGB value.</li> </ul> </li> <li>If the COLOR_CHROMA_SEL bit (F4BAR0+Memory Offset 04h[20]) = 1:               <ul style="list-style-type: none"> <li>The video pixel is selected within the target window only if it (the video pixel) does not match the color key. The color key is usually an RGB value. However, if both the CSC_for VIDEO and GV_SEL bits (F4BAR0+Memory Offset 4Ch bits 10 and 13, respectively) are programmed to 0, the color key is a YUV value (i.e., video is not converted to RGB).</li> </ul> </li> </ul> The graphics or video data being compared can be masked prior to the compare via the Video Color Mask register (described in F4BAR0+Memory Offset 18h). |
| <b>Offset 18h-1Bh</b> <span style="float: right;"><b>Video Color Mask Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br>Provides the video color mask. This value is used to mask bits of the graphics or video stream being compared to the video color key (described in F4BAR0+Memory Offset 14h). It can be used to allow a range of values to serve as the color key.   |  |
| 31:24  | <b>Reserved.</b>   |
| 23:0   | <b>VID_CLR_MASK (Video Color Mask).</b> This mask is a 24-bit value. Zeros in the mask cause the corresponding bits in the graphics or video stream to be ignored.   |
| <b>Offset 1Ch-1Fh</b> <span style="float: right;"><b>Palette (Gamma Correction RAM) Address Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: xxxxxxxh</b></span>  |  |
| 31:8   | <b>Reserved.</b>   |
| 7:0  | <b>PAL_ADDR (Palette Address).</b> Specifies the address to be used for the next access to the Palette Data register (F4BAR0+Memory Offset 20h[31:8]). Each access to the data register automatically increments the Palette Address register. If non-sequential access is made to the palette, the address register must be loaded between each non-sequential data block.  |
| <b>Offset 20h-23h</b> <span style="float: right;"><b>Palette (Gamma Correction RAM) Data Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: xxxxxxxh</b></span><br>Provides the video palette data. The data can be read or written to the Gamma Correction RAM (palette) via this register. Prior to accessing this register, an appropriate address should be loaded to the Palette Address register (F4BAR0+Memory Offset 1Ch[7:0]). Subsequent accesses to the Palette Data register cause the internal address counter to be incremented for the next cycle. |  |
| 31:8   | <b>PAL_DATA (Palette Data).</b> Contains the read or write data for a Gamma Correction RAM (palette).<br>Blue[7:0] = Bits [31:24]<br>Green[7:0] = Bits [23:16]<br>Red[7:0] = Bits [15:8]<br><b>Note:</b> When a read or write to the Gamma Correction RAM occurs, the previous output value is held for one additional DOTCLK period. This effect should go unnoticed during normal operation.   |
| 7:0  | <b>Reserved.</b>   |
| <b>Offset 24h-27h</b> <span style="float: right;"><b>Reserved</b></span>   |  |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit   | Description   |
|---|---|
| <b>Offset 28h-2Bh</b> <span style="float:right"><b>Miscellaneous Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00001400h</b></span>     |   |
| Configuration and control register for miscellaneous characteristics of the Video Processor.  |   |
| 31:13   | <b>Reserved.</b>  |
| 12  | <b>PLL2_PWR_EN (PLL2 Power-Down Enable).</b><br>0: Power-down.<br>1: Normal.  |
| 11:10   | <b>Reserved.</b> Set to 1.  |
| 9:1   | <b>Reserved.</b>  |
| 0   | <b>GAMMA_EN (Gamma Correction RAM Enable).</b> Allows video or graphics (selected by F4BAR0+Memory Offset 04h[21]) to go to the Gamma Correction RAM.<br>0: Enable.<br>1: Disable.  |
| <b>Offset 2Ch-2Fh</b> <span style="float:right"><b>PLL2 Clock Select Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span> |   |
| Determines the characteristics of the integrated PLL2.  |   |
| 31:23   | <b>Reserved.</b> Must be set to 0.  |
| 22:21   | <b>CLK_DIV_SEL (Clock Divider Select).</b><br>00: No division<br>01: Divide by 2<br>10: Divide by 4<br>11: Divide by 8<br>Divides the clock generated by the PLL2, using the programmed m (bits [14:8]) and n (bits [3:0]) values.  |
| 20  | <b>SEL_REG_CAL.</b> Selects specific or previously-calculated values.<br>0: Values previously calculated from the CLK_SEL bits (bits [19:16]).<br>1: Values according to the m (bits [14:8]), n (bits [3:0]), and CLK_DIV_SEL (bits [22:21]) fields.  |
| 19:16   | <b>CLK_SEL (Clock Select).</b> Selects frequency (in MHz) of the display clock.<br>0000: 25.175      0100: 50      1000: 65      1100: 108<br>0001: 31.5      0101: 49.5      1001: 75      1101: 135<br>0010: 36      0110: 56.25      1010: 78.5      1110: 27<br>0011: 40      0111: 44.9      1011: 94.5      1111: 24.923052 |
| 15  | <b>LFTC (Loop Filter Time Constant).</b> This bit should be set when m (bits [14:8]) value is higher than 30.   |
| 14:8  | <b>m (Defines m PLL2 Value).</b> Relevant when SEL_REG_CAL (bit 20) = 1. The following formula is used for calculating the frequency using m and n values:<br>$F_{vco} = OSCCLK * K_m / K_n$<br>$K_m = m + 1$<br>$K_n = n + 1$<br>OSCCLK = 27 MHz   |
| 7:4   | <b>Reserved</b>   |
| 3:0   | <b>n (Defines n PLL2 Value).</b> Relevant when SEL_REG_CAL (bit 20) = 1. The following formula is used for calculating the frequency using m and n values:<br>$F_{vco} = OSCCLK * K_m / K_n$<br>$K_m = m + 1$<br>$K_n = n + 1$<br>OSCCLK = 27 MHz   |
| <b>Offset 30h-33h</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>                         |   |
| <b>Offset 34h-37h</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>                         |   |
| <b>Offset 38h-3Bh</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>                         |   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 3Ch-3Fh</b> <b>Video Downscaler Control Register (R/W)</b> <b>Reset Value: 0000000h</b>   |  |
| Controls the characteristics of the integrated video downscaler.  |  |
| 31:7  | <b>Reserved</b>  |
| 6   | <b>DTS (Downscale Type Select).</b><br>0: Type A (Downscale formula is $1/m+1$ , m pixels are dropped, 1 pixel is kept).<br>1: Type B (Downscale formula is $m/m+1$ , m pixels are kept, 1 pixel is dropped).  |
| 5   | <b>Reserved.</b>   |
| 4:1   | <b>DFS (Downscale Factor Select).</b> Determines the downscale factor to be programmed into these bits, where m is used to derive the desired downscale factor depending on bit 6 (DTS).   |
| 0   | <b>DCF (Downscaler and Filtering).</b> Enables/disables downscaler and filtering logic.<br>0: Disable.<br>1: Enable.<br><b>Note:</b> No downscaling support for RGB 5:6:5 and YUV 4:2:0 video formats.   |
| <b>Offset 40h-43h</b> <b>Video Downscaler Coefficient Register (R/W)</b> <b>Reset Value: 0000000h</b>   |  |
| Indicates filter coefficients. The filters can be programmed independently to increase video quality when the downscaler is implemented. Valid values for each filter coefficient are 0-15. The sum of coefficients must be 16. FLT_CO_4 is used with the earliest pixels and FLT_CO_1 is used with the latest. Only luminance values of pixels are filtered. |  |
| 31:28   | <b>Reserved</b>  |
| 27:24   | <b>FLT_CO_4 (Filter Coefficient 4).</b> For the tap-4 filter.  |
| 23:20   | <b>Reserved</b>  |
| 19:16   | <b>FLT_CO_3 (Filter Coefficient 3).</b> For the tap-3 filter.  |
| 15:12   | <b>Reserved</b>  |
| 11:8  | <b>FLT_CO_2 (Filter Coefficient 2).</b> For the tap-2 filter.  |
| 7:4   | <b>Reserved</b>  |
| 3:0   | <b>FLT_CO_1 (Filter Coefficient 1).</b> For the tap-1 filter.  |
| <b>Offset 44h-47h</b> <b>CRC Signature Register (R/W)</b> <b>Reset Value: xxxxx100h</b>   |  |
| Signature values stored in this register can be read by the host. This register is used for test purposes.  |  |
| 31:8  | <b>SIG_VALUE (Signature Value). (Read Only)</b> A 24-bit signature value is stored in this bit field and can be read at any time. The signature is produced from the RGB data output of the mixer. This bit field is used for test purpose only. See SIGN_EN (bit 0) description for more information.   |
| 7:3   | <b>Reserved</b>  |
| 2   | <b>SIGN_FREE (Signature Free Run).</b><br>0: Disable. (Default) If this bit was previously set to 1, the signature process stops at the end of the current frame (i.e., at the next falling edge of VSYNC).<br>1: Enable. If SIGN_EN (bit 0) = 1, the signature register captures data continuously across multiple frames.  |
| 1   | <b>Reserved.</b>   |
| 0   | <b>SIGN_EN (Signature Enable).</b><br>0: Disable. (Default) The SIG_VALUE (bits [31:8]) is reset to 000001h and held (no capture).<br>1: Enable. The next falling edge of VSYNC is counted as the start of the frame to be used for CRC checking with each pixel clock beginning with the next VSYNC.<br>If SIGN_FREE (bit 2) = 1, the signature register captures the pixel data signature continuously across multiple frames.<br>If SIGN_FREE (bit 2) = 0, a signature is captured for one frame at a time, starting from the next falling VSYNC.<br>After a signature capture, the SIG_VALUE can be read to determine the CRC check status. SIGN_EN can then be reset to initialize the SIG_VALUE as an essential preparation for the next round of CRC check. |
| <b>Offset 48h-4Bh</b> <b>Device and Revision Identification (RO)</b> <b>Reset Value: 0000xxxxh</b>  |  |
| 31:16   | <b>Reserved.</b>   |
| 15:8  | <b>REV_ID (Revision ID).</b> See the <i>AMD Geode™ SC3200 Specification Update</i> document for value.   |
| 7:0   | <b>DEV_ID (Device ID).</b> See the <i>AMD Geode™ SC3200 Specification Update</i> document for value.   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 4Ch-4Fh</b>  |  |
| <b>Video De-Interlacing and Alpha Control Register (R/W)</b> |  |
| <b>Reset Value: 00060000h</b>                                |  |
| 31:22  | <b>Reserved.</b>   |
| 21:20  | <p><b>ALPHA3_WIN_PRIORITY (Alpha Window 3 Priority).</b> Determines the priority of Alpha Window 3. A higher number indicates a higher priority. Priority is used to determine display order for overlapping alpha windows.</p> <p>00: Lowest priority (default).<br/> 01: Medium priority.<br/> 10: Highest priority.<br/> 11: Illegal.</p> <p><b>Note:</b> Priority of enabled alpha windows must be different.</p>  |
| 19:18  | <p><b>ALPHA2_WIN_PRIORITY (Alpha Window 2 Priority).</b> Determines the priority of Alpha Window 2. A higher number indicates a higher priority. Priority is used to determine display order for overlapping alpha windows.</p> <p>00: Lowest priority (default).<br/> 01: Medium priority.<br/> 10: Highest priority.<br/> 11: Illegal.</p> <p><b>Note:</b> Priority of enabled alpha windows must be different.</p>  |
| 17:16  | <p><b>ALPHA1_WIN_PRIORITY (Alpha Window 1 Priority).</b> Determines the priority of Alpha Window 1. A higher number indicates a higher priority. Priority is used to determine display order for overlapping alpha windows.</p> <p>00: Lowest priority (default).<br/> 01: Medium priority.<br/> 10: Highest priority.<br/> 11: Illegal.</p> <p><b>Note:</b> Priority of enabled alpha windows must be different.</p>  |
| 15:14  | <b>Reserved</b>  |
| 13   | <p><b>GV_SEL (GV Select).</b> Selects input video format.</p> <p>0: YUV format.<br/> 1: RGB format.</p> <p><b>Note:</b> Mixing and blending configurations are created using bits [13, 11:9] of this register. See Table 7-1 "Valid Mixing/Blending Configurations" on page 339.</p> <p>If this bit is set to 1, EN_42X (F4BAR0+Memory Offset 00h[28]) must be programmed to 0.</p>  |
| 12   | <p><b>VID_LIN_INV (Video Line Invert).</b> When this bit is set, it allows the video window to be positioned at odd offsets with respect to the first line. The values below are recommended if VID_Y_START (F4BAR0+Memory Offset 0Ch[10:0]) is an odd (set to 1) or even (set to 0) number of lines from the start of the active display.</p> <p>0: Even.<br/> 1: Odd.</p>  |
| 11   | <b>Reserved: Set to 0.</b>   |
| 10   | <p><b>CSC_FOR_VIDEO (Color Space Converter for Video).</b> Determines whether or not the video stream from the video module is passed through the CSC.</p> <p>0: Disable. The video stream is sent "as is" to the video Mixer/Blender.<br/> 1: Enable. The video stream is passed through the CSC (for YUV to RGB conversion).</p> <p><b>Note:</b> Mixing and blending configurations are created using bits [13,11:9] of this register. See Table 7-1 "Valid Mixing/Blending Configurations" on page 339.</p> |
| 9  | <p><b>VIDEO_BLEND_MODE (Video Blending Mode).</b> Allows selection of the type of video (i.e., interlaced or progressive) used for blending.</p> <p>0: Progressive video used for blending.<br/> 1: Interlaced video used for blending.</p> <p><b>Note:</b> Mixing and blending configurations are created using bits [13,11:9] of this register. See Table 7-1 "Valid Mixing/Blending Configurations" on page 339.</p>  |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit   | Description   |
|---|---|
| 8   | <b>GFX_INS_VIDEO (Graphics Inside Video).</b> This bit works in conjunction with bit COLOR_CHROMA_SEL (F4BAR0+Memory Offset 4Ch[20]). COLOR_CHROMA_SEL selects whether the graphics is used for color keying or the video data stream is used for chroma keying. If COLOR_CHROMA_SEL = 0, graphics data is compared to the color key. If COLOR_CHROMA_SEL = 1, video data is compared to the chroma key.<br>0: Outside the alpha windows, graphics or video is displayed depending on the result of the color key comparison.<br>1: Outside the alpha windows, only video is displayed (if COLOR_CHROMA_SEL = 0) or only graphics is displayed (if COLOR_CHROMA_SEL = 1) color key comparison is not performed outside the alpha windows. |
| 7   | <b>VID_WIN_PUSH_EN (Video Window Push Enable).</b> Video window repositioning at an offset of 1 line below the programmed value. Facilitates line rate matching in both fields.<br>0: Disable. (Default)<br>1: Enable.  |
| 6   | <b>TOP_LINE_IN_ODD (Top Line in Odd Field).</b> Allows selection of what field the top line is in.<br>0: Top line is in even field. (Default)<br>1: Top line is in odd field.   |
| 5   | <b>Reserved.</b>  |
| 4   | <b>INSERT_EN (Insert Enable).</b> When this bit is set, the odd frame is shifted with respect to the even frame.<br>0: No shifting occurs.<br>1: The odd frame is shifted according to the offset specified in bits [2:0].  |
| 3   | <b>Reserved.</b>  |
| 2:0   | <b>OFFSET (Vertical Scaler Offset).</b> For a non-interlaced video stream and when bob de-interlacing is used, program a value of 100 (i.e., shift one line); otherwise, leave at 000.  |
| <b>Offset 50h-53h</b> <b>Cursor Color Key Register (R/W)</b> <b>Reset Value: 00000000h</b>  |   |
| 31:29   | <b>Reserved.</b>  |
| 28:24   | <b>COLOR_REG_OFFSET (Cursor Color Register Offset).</b> This field indicates a bit in the incoming graphics stream. It is used to indicate which of the two possible cursor color registers should be used for color key matches for the bits in the graphics stream.   |
| 23:0  | <b>CUR_COLOR_KEY (Cursor Color Key).</b> Specifies the 24-bit RGB value of the cursor color key. The incoming graphics stream is compared with this value. If a match is detected, the pixel is replaced by a 24-bit value from one of the Cursor Color registers.  |
| <b>Offset 54h-57h</b> <b>Cursor Color Mask Register (R/W)</b> <b>Reset Value: 00000000h</b> |   |
| 31:24   | <b>Reserved</b>   |
| 23:0  | <b>CUR_COLOR_MASK (Cursor Color Mask).</b> This mask is a 24-bit value. Zeroes in the mask cause the corresponding bits in the incoming graphics stream to be ignored.  |
| <b>Offset 58h-5Bh</b> <b>Cursor Color Register 1 (R/W)</b> <b>Reset Value: 00000000h</b>    |   |
| 31:24   | <b>Reserved</b>   |
| 23:0  | <b>CUR_COLOR_REG1 (Cursor Color Register 1).</b> Specifies a 24-bit cursor color value. This is an RGB value (for RGB blending) or a YUV value (for YUV blending). In interlaced YUV blending mode, Y/2 value should be used.<br>This is one of two possible cursor color values. The COLOR_REG_OFFSET bits (F4BAR0+Memory Offset 50h[28:24]) determine a bit of the graphics data that if even, selects this color to be used.   |
| <b>Offset 5Ch-5Fh</b> <b>Cursor Color Register 2 (R/W)</b> <b>Reset Value: 00000000h</b>    |   |
| 31:24   | <b>Reserved</b>   |
| 23:0  | <b>CUR_COLOR_REG2 (Cursor Color Register 2).</b> Specifies a 24-bit cursor color value. This is an RGB value (for RGB blending) or a YUV value (for YUV blending). In interlaced YUV blending mode, Y/2 value should be used.<br>This is one of two possible cursor color values. The COLOR_REG_OFFSET bits (F4BAR0+Memory Offset 50h[28:24]) determine a bit of the graphics data that if even, selects this color to be used.   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 60h-63h</b> <b>Alpha Window 1 X Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| <b>Note:</b> H_TOTAL and H_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8330h[26:19] and 8338h[10:3], respectively). The value of (H_TOTAL – H_SYNC_END) is sometimes referred to as "horizontal back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .<br>Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch). |   |
| 31:27  | <b>Reserved.</b>  |
| 26:16  | <b>ALPHA1_X_END (Alpha Window 1 Horizontal End).</b> Determines the horizontal end position of Alpha Window 1 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 1.  |
| 15:11  | <b>Reserved.</b>  |
| 10:0   | <b>ALPHA1_X_START (Alpha Window 1 Horizontal Start).</b> Determines the horizontal start position of Alpha Window 1. This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 2.  |
| <b>Offset 64h-67h</b> <b>Alpha Window 1 Y Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| <b>Note:</b> V_TOTAL and V_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8340h[26:16] and 8348h[26:16], respectively). The value of (V_TOTAL – V_SYNC_END) is sometimes referred to as "vertical back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .<br>Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch).  |   |
| 31:27  | <b>Reserved.</b>  |
| 26:16  | <b>ALPHA1_Y_END (Alpha Window 1 Vertical End).</b> Determines the vertical end position of Alpha Window 1 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 2.  |
| 15:11  | <b>Reserved.</b>  |
| 10:0   | <b>ALPHA1_Y_START (Alpha Window 1 Vertical Start).</b> Determines the vertical start position of Alpha Window 1. This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 1.  |
| <b>Offset 68h-6Bh</b> <b>Alpha Window 1 Color Register (R/W)</b> <b>Reset Value: 0000000h</b>  |   |
| 31:25  | <b>Reserved.</b>  |
| 24   | <b>ALPHA1_COLOR_REG_EN (Alpha Window 1 Color Register Enable).</b> Enable bit for the color key matching in Alpha Window 1.<br>1: Enable. If this bit is enabled and the alpha window is enabled, then where there is a color key match. The color value (in bits [23:0], ALPHA1_COLOR_REG) is displayed.<br>0: Disable. Where there is a color key match, no blending is performed.  |
| 23:0   | <b>ALPHA1_COLOR_REG (Alpha Window 1 Color Register).</b> Specifies the color to be displayed inside Alpha Window 1 when there is a color key match in the alpha window. This is an RGB value (for RGB blending) or a YUV value (for YUV blending). In interlaced YUV blending mode, Y/2 value should be used.<br>This color is only displayed if the alpha window is enabled and bit 24 (ALPHA1_COLOR_REG_EN) is enabled.                   |
| <b>Offset 6Ch-6Fh</b> <b>Alpha Window 1 Control Register (R/W)</b> <b>Reset Value: 0000000h</b>  |   |
| 31:18  | <b>Reserved.</b>  |
| 17   | <b>LOAD_ALPHA (Load Alpha Value). (Write Only)</b> When set to 1, this bit causes the Video Processor to load the alpha value (in bits [7:0], ALPHA_VAL) at the start of the next frame.  |
| 16   | <b>ALPHA1_WIN_EN (Alpha Window 1 Enable).</b> Enable bit for Alpha Window 1.<br>1: Enable Alpha Window 1.<br>0: Disable Alpha Window 1.<br><b>Note:</b> Valid only if video window is enabled (F4BAR0+Memory Offset 00h[0] = 1).  |
| 15:8   | <b>ALPHA1_INC (Alpha Window 1 Increment).</b> Specifies the alpha value increment/decrement. This is a signed 8-bit value that is added to the alpha value for each frame. The MSB (bit 15) indicates the sign (i.e., increment or decrement). When this value reaches either the maximum or the minimum alpha value (255 or 0) it keeps that value (i.e., it is not incremented/decremented) until it is reloaded via bit 17 (LOAD_ALPHA). |
| 7:0  | <b>ALPHA1_VAL (Alpha Window 1 Value).</b> Specifies the alpha value to be used for this window.   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 70h-73h</b> <b>Alpha Window 2 X Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| <b>Note:</b> H_TOTAL and H_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8330h[26:19] and 8338h[10:3], respectively). The value of (H_TOTAL – H_SYNC_END) is sometimes referred to as "horizontal back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .<br>Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch). |   |
| 31:27  | <b>Reserved.</b>  |
| 26:16  | <b>ALPHA2_X_END (Alpha Window 2 Horizontal End).</b> Determines the horizontal end position of Alpha Window 2 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 1.  |
| 15:11  | <b>Reserved.</b>  |
| 10:0   | <b>ALPHA2_X_START (Alpha Window 2 Horizontal Start).</b> Determines the horizontal start position of Alpha Window 2. This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 2.  |
| <b>Offset 74h-77h</b> <b>Alpha Window 2 Y Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |   |
| <b>Note:</b> V_TOTAL and V_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8340h[26:16] and 8348h[26:16], respectively). The value of (V_TOTAL – V_SYNC_END) is sometimes referred to as "vertical back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .<br>Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch).  |   |
| 31:27  | <b>Reserved.</b>  |
| 26:16  | <b>ALPHA2_Y_END (Alpha Window 2 Vertical End).</b> Determines the vertical end position of Alpha Window 2 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 2.  |
| 15:11  | <b>Reserved.</b>  |
| 10:0   | <b>ALPHA2_Y_START (Alpha Window 2 Vertical Start).</b> Determines the vertical start position of Alpha Window 2. This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 1.  |
| <b>Offset 78h-7Bh</b> <b>Alpha Window 2 Color Register (R/W)</b> <b>Reset Value: 0000000h</b>  |   |
| 31:25  | <b>Reserved.</b>  |
| 24   | <b>ALPHA2_COLOR_REG_EN (Alpha Window 2 Color Register Enable).</b> Enable bit for the color key matching in Alpha Window 2.<br>0: Disable. Where there is a color key match, graphics and video are alpha-blended.<br>1: Enable. If this bit is enabled and the alpha window is enabled, then where there is a color key match, the color value (in bits [23:0], ALPHA2_COLOR_REG) is displayed.  |
| 23:0   | <b>ALPHA2_COLOR_REG (Alpha Window 1 Color Register).</b> Specifies the color to be displayed inside Alpha Window 2 when there is a color key match in the alpha window. This is an RGB value (for RGB blending) or a YUV value (for YUV blending). In Interlaced YUV blending mode, Y/2 value should be used.<br>This color is only displayed if the alpha window is enabled and bit 24 (ALPHA2_COLOR_REG_EN) is enabled.                       |
| <b>Offset 7Ch-7Fh</b> <b>Alpha Window 2 Control Register (R/W)</b> <b>Reset Value: 0000000h</b>  |   |
| 31:18  | <b>Reserved.</b>  |
| 17   | <b>LOAD_ALPHA (Load Alpha Value). (Write Only)</b> When set to 1, this bit causes the Video Processor to load the alpha value (in bits [7:0], ALPHA2_VAL) at the start of the next frame.   |
| 16   | <b>ALPHA2_WIN_EN (Alpha Window 2 Enable).</b> Enable bit for Alpha Window 2.<br>0: Disable Alpha Window 2.<br>1: Enable Alpha Window 2.<br><b>Note:</b> Valid only if video window is enabled (F4BAR0+Memory Offset 00h[0] = 1).  |
| 15:8   | <b>ALPHA2_INCR (Alpha Window 2 Increment).</b> Specifies the alpha value increment/decrement.<br>This is a signed 8-bit value that is added to the alpha value for each frame. The MSB (bit 15) indicates the sign (i.e., increment or decrement). When this value reaches either the maximum or the minimum alpha value (255 or 0) it keeps that value (i.e., it is not incremented/decremented) until it is reloaded via bit 17 (LOAD_ALPHA). |
| 7:0  | <b>ALPHA2_VAL (Alpha Window 1 Value).</b> Specifies the alpha value to be used for this window.   |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description  |
|--|--|
| <b>Offset 80h-83h</b> <b>Alpha Window 3 X Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |  |
| <b>Note:</b> H_TOTAL and H_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8330h[26:19] and 8338h[10:3], respectively). The value of (H_TOTAL – H_SYNC_END) is sometimes referred to as "horizontal back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> . |  |
| <b>Note:</b> Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch).  |  |
| 31:27  | <b>Reserved.</b>   |
| 26:16  | <b>ALPHA3_X_END (Alpha Window 3 Horizontal End).</b> Determines the horizontal end position of Alpha Window 3 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 1.   |
| 15:11  | <b>Reserved.</b>   |
| 10:0   | <b>ALPHA3_X_START (Alpha Window 3 Horizontal Start).</b> Determines the horizontal start position of Alpha Window 3. This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 2.   |
| <b>Offset 84h-87h</b> <b>Alpha Window 3 Y Position Register (R/W)</b> <b>Reset Value: 0000000h</b>   |  |
| <b>Note:</b> V_TOTAL and V_SYNC_END are values programmed in the GX1 module's Display Controller Timing registers (GX_BASE+Memory Offset 8340h[26:16] and 8348h[26:16], respectively). The value of (V_TOTAL – V_SYNC_END) is sometimes referred to as "vertical back porch". For more information, see the <i>AMD Geode™ GX1 Processor Data Book</i> .  |  |
| <b>Note:</b> Desired screen position should not be outside a video window (F4BAR0+Memory Offset 08h and 0Ch).  |  |
| 31:27  | <b>Reserved</b>  |
| 26:16  | <b>ALPHA3_Y_END (Alpha Window 3 Vertical End).</b> Determines the vertical end position of Alpha Window 3 (not inclusive). This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 2.   |
| 15:11  | <b>Reserved</b>  |
| 10:0   | <b>ALPHA3_Y_START (Alpha Window 3 Vertical End).</b> Determines the vertical start position of Alpha Window 3. This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 1.   |
| <b>Offset 88h-8Bh</b> <b>Alpha Window 3 Color Register (R/W)</b> <b>Reset Value: 0000000h</b>  |  |
| 31:25  | <b>Reserved.</b>   |
| 24   | <b>ALPHA3_COLOR_REG_EN (Alpha Window 3 Color Register Enable).</b> Enable bit for the color key matching in Alpha Window 3.<br><br>0: Disable. Where there is a color key match, graphics and video are alpha-blended.<br>1: Enable. If this bit is enabled and the alpha window is enabled, then where there is a color key match, the color value (in bits [23:0], ALPHA3_COLOR_REG) is displayed.   |
| 23:0   | <b>ALPHA3_COLOR_REG (Alpha Window 3 Color Register).</b> Specifies the color to be displayed inside Alpha Window 3 when there is a color key match in the alpha window. This is an RGB value (for RGB blending) or a YUV value (for YUV blending). In Interlaced YUV blending mode, Y/2 value should be used.<br><br>This color is only displayed if the alpha window is enabled and the bit 24 (ALPHA3_COLOR_REG_EN) is enabled.            |
| <b>Offset 8Ch-8Fh</b> <b>Alpha Window 3 Control Register (R/W)</b> <b>Reset Value: 0000000h</b>  |  |
| 31:18  | <b>Reserved</b>  |
| 17   | <b>LOAD_ALPHA (Load Alpha Value). (Write Only)</b> When set to 1, this bit causes the Video Processor to load the alpha value (in bits [7:0], ALPHA3_VAL) at the start of the next frame.  |
| 16   | <b>ALPHA3_WIN_EN (Alpha Window 3 Enable).</b> Enable bit for Alpha Window 3.<br><br>0: Disable Alpha Window 3.<br>1: Enable Alpha Window 3.<br><br>Valid only if video window is enabled (F4BAR0+Memory Offset 00h[0] = 1)   |
| 15:8   | <b>ALPHA3_INCR (Alpha Window 3 Increment).</b> Specifies the alpha value increment/decrement. This is a signed 8-bit value that is added to the alpha value for each frame. The MSB (bit 15) indicates the sign (i.e., increment or decrement). When this value reaches either the maximum or the minimum alpha value (255 or 0) it keeps that value (i.e., it is not incremented/decremented) until it is reloaded via bit 17 (LOAD_ALPHA). |
| 7:0  | <b>ALPHA3_VAL (Alpha Window 3 Value).</b> Specifies the alpha value to be used for this window.  |



Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 90h-93h</b> <span style="float:right"><b>Video Request Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 001B0017h</b></span>                     |  |
| 31:28   | <b>Reserved.</b> Set to 0.   |
| 27:16   | <b>VIDEO_X_REQ (Video Horizontal Request).</b> Determines the horizontal (pixel) location at which to start requesting video data out of the video FIFO. This value is calculated according to the following formula:<br>Value = Desired screen position + (H_TOTAL – H_SYNC_END) – 2. |
| 15:11   | <b>Reserved</b>  |
| 10:0  | <b>VIDEO_Y_REQ (Video Vertical Request).</b> Determines the line number at which to start requesting video data out of the video FIFO. This value is calculated according to the following formula:<br>Value = Desired screen position + (V_TOTAL – V_SYNC_END) + 1.                   |
| <b>Offset 94h-97h</b> <span style="float:right"><b>Alpha Watch Register (RO)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>                        |  |
| Alpha values may be automatically incremented/decremented for successive frames. This register can be used to read the alpha values that are being used in the current frame. |  |
| 31:24   | <b>Reserved.</b>   |
| 23:16   | <b>ALPHA3_VAL (Value for Alpha Window 3).</b>  |
| 15:8  | <b>ALPHA2_VAL (Value for Alpha Window 2).</b>  |
| 7:0   | <b>ALPHA1_VAL (Value for Alpha Window 1).</b>  |
| <b>Offset 98h-3FFh</b> <span style="float:right"><b>Reserved</b></span>   |  |
| <b>Offset 400h-403h</b> <span style="float:right"><b>Video Processor Display Mode Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>    |  |
| Selects various Video Processor modes.  |  |
| 31  | <b>Video FIFO Underflow (Empty).</b><br>0: No underflow has occurred.<br>1: Underflow has occurred.<br>Write 1 to reset this bit.  |
| 30  | <b>Video FIFO Overflow (Full).</b><br>0: No overflow has occurred.<br>1: Overflow has occurred.<br>Write 1 to reset this bit.  |
| 29  | <b>Reserved.</b> Write as read.  |
| 28  | <b>Reserved.</b> Write as read.  |
| 27:4  | <b>Reserved.</b> Set to 0.   |
| 3   | <b>Reserved.</b> Write as read.  |
| 2   | <b>Note: Reserved.</b> Write as read.  |
| 1:0   | <b>VID_SEL (Video Select).</b> Selects the source of the video data.<br>00: GX1 module.<br>10: VIP block.<br>01: Reserved.<br>11: Reserved.<br>The GX1 module's video clock must be active at all times, regardless of the source of video input.                                      |
| <b>Offset 404h-407h</b> <span style="float:right"><b>Reserved</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>                                       |  |
| <b>Offset 408h-40Bh</b> <span style="float:right"><b>Video Processor Test Mode Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>       |  |
| 31:0  | <b>Reserved.</b>   |
| <b>Offset 40Ch-41Fh</b> <span style="float:right"><b>Reserved</b></span>  |  |

Table 7-7. F4BAR0+Memory Offset: Video Processor Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| <b>Offset 420h-423h</b>                          |   |
| <b>GenLock Register (R/W)</b>                    |   |
| <b>Reset Value: 00000000h</b>                    |   |
| 31:24  | <b>Reserved.</b> Must be set to 0.  |
| 23   | <b>ODD_TO (Odd Field Time Out).</b> Indicates CGENTO0 (F4BAR0+Memory Offset 43Ch[15:0]) has expired. This bit can be reset by writing 1 to it.  |
| 22   | <b>EVEN_TO (Even Field Time Out).</b> Indicates CGENTO1 (F4BAR0+Memory Offset 43Ch[31:16]) has expired. This bit can be reset by writing 1 to it.   |
| 21:9   | <b>Reserved.</b>  |
| 8  | <b>Reserved.</b> Set to 0.  |
| 7  | <b>Reserved.</b> Set to 0.  |
| 6  | <b>Reserved.</b> Set to 0.  |
| 5  | <b>Reserved.</b> Set to 0.  |
| 4  | <b>GENLOCK_TOUT_EN (GenLock Timeout Enable).</b><br>0: Disable.<br>1: Enable timeout.   |
| 3  | <b>VIP_VSYNC_EDGE_SEL (VIP VSYNC Edge Select).</b> Selects which edge of the VSYNC signal should be synchronized with VIP.<br>0: Rising edge.<br>1: Falling edge.   |
| 2  | <b>GX1_VSYNC_EDGE_SEL (GX1 VSYNC Edge Select).</b> Selects which edge of the VSYNC signal should be synchronized with the GX1 module.<br>0: Rising edge.<br>1: Falling edge.  |
| 1  | <b>CT_GENLOCK_EN (Enable Continuous GenLock Function).</b><br>0: The continuous GenLock function is disabled.<br>1: Enable locking (i.e., synchronization) of the GX1 VSYNC with the VIP VSYNC on every VSYNC (i.e., continuous locking).<br><b>Note:</b> If bit 0 (SG_GENLOCK_EN) = 1, it overrides the value of this bit. |
| 0  | <b>Reserved.</b> Set to 0.  |
| <b>Offset 424h-427h</b>                          |   |
| <b>GenLock Delay Register (R/W)</b>              |   |
| <b>Reset Value: 00000000h</b>                    |   |
| 31:21  | <b>Reserved.</b>  |
| 20:0   | <b>GENLOCK_DEL (GenLock Delay).</b> Indicates the delay (in 27 MHz clocks) between the VIP VSYNC and the GX1 module's Display Controller VSYNC.   |
| <b>Offset 428h-43Bh</b>                          |   |
| <b>Reserved</b>                                  |   |
| <b>Offset 43Ch-43Fh</b>                          |   |
| <b>Continuous GenLock Timeout Register (R/W)</b> |   |
| <b>Reset Value: 1FFF1FFFh</b>                    |   |
| 31:16  | <b>CGENTO1 (Even Field Continuous GenLock Timeout).</b>   |
| 15:0   | <b>CGENTO0 (Odd Field Continuous GenLock Timeout).</b>  |

### 7.3.2.2 VIP Support Registers - F4BAR2

F4 Index 18h, Base Address Register 2 (F4BAR2) points to the base address of where the VIP Configuration registers are located. Table 7-8 shows the memory mapped VIP support registers accessed through F4BAR2.

**Table 7-8. F4BAR2+Memory Offset: VIP Configuration Registers**

| Bit  | Description  |
|--|--|
| <b>Offset 00h-03h</b> <span style="float:right"><b>Video Interface Port Configuration Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span> |  |
| 31:23  | <b>Reserved.</b> Must be set to 0.   |
| 22   | <b>VIP FIFO Bus Request Threshold.</b> VIP FIFO issues a bus request when it is filled with 32 or 64 bytes.<br>0: 64 bytes.<br>1: 32 bytes   |
| 21   | <b>VBI Task B Store to Memory.</b> When this bit is enabled, raw VBI task B data is stored to memory.<br>0: Disable.<br>1: Enable.<br>This bit is relevant only if bit 18 (VBI Configuration Override) = 1 (enabled).  |
| 20   | <b>VBI Task A Store to Memory.</b> When this bit is enabled, raw VBI task A data is stored to memory.<br>0: Disable.<br>1: Enable.<br>This bit is relevant only if bit 18 (VBI Configuration Override) = 1 (enabled).  |
| 19   | <b>VBI Ancillary Store to Memory.</b> When this bit is enabled, raw VBI Ancillary data is stored to memory.<br>0: Disable.<br>1: Enable.<br>This bit is relevant only if bit 18 (VBI Configuration Override) = 1 (enabled).  |
| 18   | <b>VBI Configuration Override.</b> When this bit is enabled, bits [21:19] override the setup specified in bits 17 and 16.<br>0: Disable.<br>1: Enable.   |
| 17   | <b>VBI Data Task.</b> Specifies the CCIR656 video stream task used to store raw VBI data to memory.<br>0: Task B.<br>1: Task A.<br>This bit is relevant only if bit 16 (VBI Mode for CCIR656) = 1 and bit 18 (VBI Configuration Override) = 0 (disabled).  |
| 16   | <b>VBI Mode for CCIR656.</b> Specifies the mode in which to store VBI data to memory.<br>0: Use CCIR656 ancillary data to store VBI data to memory.<br>1: Use CCIR656 video task A or B to store VBI data to memory, depending on the value of bit 17 (VBI Data Task).<br>This bit is only used if bit 18 (VBI Configuration Override) = 0 (disabled). |
| 15:2   | <b>Reserved.</b> Set to 0.   |
| 1:0  | <b>Video Input Port Mode.</b> Selects VIP operating mode.<br>10: CCIR656 mode.<br>All other decodes: Reserved.   |
| <b>Offset 04h-07h</b> <span style="float:right"><b>Video Interface Control Register (R/W)</b></span> <span style="float:right"><b>Reset Value: 00000000h</b></span>            |  |
| 31:18  | <b>Reserved.</b> Must be set to 0.   |
| 17   | <b>Line Interrupt.</b> When asserted, allows interrupt (INTC#) generation when the Video Current Line register (F4BAR2+ Memory Offset 10h) contents equal the Video Line Target Register (F4BAR2+ Memory Offset 14h) contents.<br>0: Disable.<br>1: Enable.  |
| 16   | <b>Field Interrupt.</b> When asserted, allows interrupt (INTC#) generation at the end of a field (i.e., the end of active video for the current field). Interrupt generation can be enabled regardless of whether or not video capture (store to memory) is enabled.<br>0: Disable.<br>1: Enable.  |
| 15:11  | <b>Reserved.</b> Must be set to 0.   |

**Table 7-8. F4BAR2+Memory Offset: VIP Configuration Registers (Continued)**

| Bit  | Description   |
|--|---|
| 10   | <p><b>Auto-Flip.</b> Video port operation mode.</p> <p>0: The video port automatically detects the even and odd fields based on the VP_HREF and VP_VSYNC_IN signals or the CCIR656 control codes.</p> <p>1: The even/odd field detect logic is disabled and the video port automatically toggles between the even and odd buffers during capture. The odd buffer is the first to be filled in this mode.</p> <p>This bit must be programmed to 0 when Direct Video mode is used. Direct Video mode is used when VID_SEL = 10 (F4BAR0+Memory Offset 400h[1:0]). Otherwise the video select from the GX1 module. VID_SEL indicates the source of the video data.)</p> |
| 9  | <p><b>Capture (Store to Memory) VBI Data.</b></p> <p>0: Disable.</p> <p>1: Enable.</p>  |
| 8  | <p><b>Capture (Store to Memory) Video Data.</b></p> <p>0: Disable.</p> <p>1: Enable.</p>  |
| 7:2  | <b>Reserved.</b> Must be set to 0.  |
| 1:0  | <p><b>Run Mode Capture.</b> Selects capture run mode.</p> <p>00: Stop capture at end of current line.</p> <p>01: Stop capture at end of current field.</p> <p>10 Reserved.</p> <p>11: Start capture at beginning of next field.</p>   |
| <b>Offset 08h-0Bh</b>                        |   |
| <b>Video Interface Status Register (R/W)</b> |   |
| <b>Reset Value: xxxxxxxh</b>                 |   |
| 31:25  | <b>Reserved. (Read Only)</b>  |
| 24   | <p><b>Current Field. (Read Only)</b></p> <p>0: Even field is being processed.</p> <p>1: Odd field is being processed.</p>   |
| 23:22  | <b>Reserved. (Read Only)</b>  |
| 21   | <p><b>Base Register Not Updated. (Read Only)</b> When set to 1, this bit indicates that one of the base registers (at F4BAR2+Memory Offset 20h, 24h, 40h, and 44h) has been written but has not yet been updated.</p> <p>0: All base registers are updated.</p> <p>1: One or more of the base registers has not been updated.</p>   |
| 20   | <p><b>FIFO Overflow Status Indication.</b></p> <p>0: No overflow occurred.</p> <p>1: An overflow occurred for the FIFO between the VIP and the Fast X-Bus.</p> <p>Writing a 1 to this bit clears the status.</p>  |
| 19:18  | <b>Reserved. (Read Only)</b>  |
| 17   | <p><b>Line Interrupt (INTC#) Pending Status.</b></p> <p>0: Interrupt not pending.</p> <p>1: Interrupt pending.</p> <p>Writing a 1 to this bit clears the status.</p>  |
| 16   | <p><b>Field Interrupt (INTC) Pending Status.</b></p> <p>0: Interrupt not pending.</p> <p>1: Interrupt pending.</p> <p>Writing a 1 to this bit clears the status.</p>  |
| 15:10  | <b>Reserved. (Read Only)</b>  |
| 9  | <p><b>VBI Data Capture Active. (Read Only)</b></p> <p>0: VBI data is not being stored to memory.</p> <p>1: VBI data is now being stored to memory.</p>  |

Table 7-8. F4BAR2+Memory Offset: VIP Configuration Registers (Continued)

| Bit  | Description   |
|--|---|
| 8  | <b>Video Data Capture Active. (Read Only)</b><br>0: Video data is not being stored to memory.<br>1: Video data is now being stored to memory.                     |
| 7:1  | <b>Reserved. (Read Only)</b>  |
| 0  | <b>Run Status. (Read Only)</b><br>0: Video port capture is not active.<br>1: Video port capture is in progress.   |
| <b>Offset 0Ch-0Fh</b> <span style="float:right">Reset Value: 00h</span>  |   |
| <b>Offset 10h-13h</b> <span style="float:right">Reset Value: xxxxxxxh</span>   |   |
| 31:10  | <b>Reserved.</b>  |
| 9:0  | <b>Current Line.</b> Indicates the video line currently being stored to memory. The count indicated in this field is reset to 0 at the start of each field.       |
| <b>Offset 14h-17h</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| 31:10  | <b>Reserved.</b> Must be set to 0.  |
| 9:0  | <b>Line Target.</b> Indicates the video line to generate an interrupt on.   |
| <b>Offset 18h-1Bh</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| <b>Offset 1Ch-1Fh</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| <b>Offset 20h-23h</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| This register specifies the base address in graphics memory where odd video field data are stored. Changes to this register take effect at the beginning of the next field. The value in this register is 16-byte aligned.   |   |
| <b>Note:</b> This register is double-buffered. When a new value is written to this register, the new value is placed in a special "pending" register, and the "Base Register Not Updated" bit (F4BAR2+MemoryOffset 08h[21]) is set to 1. The Video Data Odd Base register (this register) is not updated at this point. When the first data of the next field is stored to memory, the pending values of all base registers (including this one) are written to the appropriate base registers, and the "Base Register Not Updated" bit is cleared.  |   |
| 31:0   | <b>Video Odd Base Address.</b> Base address where odd video data are stored in graphics memory. Bits [3:0] are always 0, and define the required address space.   |
| <b>Offset 24h-27h</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| This register specifies the base address in graphics memory where even video field data are stored. Changes to this register take effect at the beginning of the next field. The value in this register is 16-byte aligned.  |   |
| <b>Note:</b> This register is double-buffered. When a new value is written to this register, the new value is placed in a special "pending" register, and the "Base Register Not Updated" bit (F4BAR2+MemoryOffset 08h[21]) is set to 1. The Video Data Even Base register (this register) is not updated at this point. When the first data of the next field is stored to memory, the pending values of all base registers (including this one) are written to the appropriate base registers, and the "Base Register Not Updated" bit is cleared. |   |
| 31:0   | <b>Video Even Base Address.</b> Base address where even video data are stored in graphics memory. Bits [3:0] are always 0, and define the required address space. |
| <b>Offset 28h-2Bh</b> <span style="float:right">Reset Value: 0000000h</span>   |   |
| This register specifies the logical width of the video data buffer. This value is added to the start of the line address to get the address of the next line where video data are stored to memory. This value must be an integral number of DWORDs.   |   |
| 31:16  | <b>Reserved.</b>  |
| 15:0   | <b>Video Data Pitch.</b> Specifies the logical width of the video data buffer. Bits [1:0] are always 0.   |
| <b>Offset 2Ch-3Fh</b> <span style="float:right">Reset Value: 0000000h</span>   |   |

Table 7-8. F4BAR2+Memory Offset: VIP Configuration Registers (Continued)

| Bit   | Description  |
|---|--|
| <b>Offset 40h-43h</b> <span style="float: right;"><b>VBI Data Odd Base Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br>This register specifies the base address in graphics memory where VBI data for odd fields are stored. Changes to this register take effect at the beginning of the next field. The value in this register is 16-byte aligned.<br><b>Note:</b> This register is double-buffered. When a new value is written this register, the new value is placed in a special "pending" register, and the "Base Register Not Updated" bit (F4BAR2+MemoryOffset 08h[21]) is set to 1. The VBI Data Odd Base Register (this register) is not updated at this point. When the first data of the next field is stored to memory, the pending values of all base registers (including this one) are written to the appropriate base registers, and the "Base Register Not Updated" bit is cleared.      |  |
| 31:0  | <b>VBI Odd Base Address.</b> Base address where VBI data for odd fields is stored in graphics memory. Bits [3:0] are always 0 and define the required address space.   |
| <b>Offset 44h-47h</b> <span style="float: right;"><b>VBI Data Even Base Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br>This register specifies the base address in graphics memory where VBI data for even fields is stored. Changes to this register take effect at the beginning of the next field. The value in this register is 16-byte aligned.<br><b>Note:</b> This register is double-buffered. When a new value is written to this register, the new value is placed in a special "pending" register, and the "Base Register Not Updated" bit (F4BAR2+MemoryOffset 08h[21]) is set to 1. The VBI Data Even Base Register (this register) is not updated at this point. When the first data of the next field is stored to memory, the pending values of all base registers (including this one) are written to the appropriate base registers, and the "Base Register Not Updated" bit is cleared. |  |
| 31:0  | <b>VBI Even Base Address.</b> Base address where VBI data for even fields is stored in graphics memory. Bits [3:0] are always 0 and define the required address space. |
| <b>Offset 48h-4Bh</b> <span style="float: right;"><b>VBI Data Pitch Register (R/W)</b></span> <span style="float: right;"><b>Reset Value: 00000000h</b></span><br>This register specifies the logical width of the VBI data buffer. This value is added to the start of the line address to get the address of the next line where VBI data are stored to memory. This value must be an integral number of DWORDs.  |  |
| 31:16   | <b>Reserved.</b>   |
| 15:0  | <b>VBI Data Pitch.</b> Specifies the logical width of the video data buffer. Bits [1:0] are always 0.  |
| <b>Offset 4Ch-1FFh</b> <span style="float: right;"><b>Reserved</b></span> <span style="float: right;"><b>Reset Value: 00h</b></span>  |  |

# Debugging and Monitoring

# 8

## 8.1 Testability (JTAG)

The Test Access Port (TAP) allows board level interconnection verification and chip production tests. An IEEE-1149.1a compliant test interface, TAP supports all IEEE mandatory instructions as well as several optional instructions for added functionality. See Table 8-1 for a summary of all instructions support. For further information on JTAG, refer to IEEE Standard 1149.1a-1993 Test Access Port and Boundary-Scan Architecture.

### 8.1.1 Mandatory Instruction Support

The TAP supports all IEEE mandatory instructions, including:

- **BYPASS.**  
Presents the shortest path through a given chip (a 1-bit shift register).
- **EXTEST**  
Drives data loaded into the JTAG path (possibly with a SAMPLE/PRELOAD instruction) to output pins.
- **SAMPLE/PRELOAD**  
Captures chip inputs and outputs.

### 8.1.2 Optional Instruction Support

The TAP supports the following IEEE optional instructions:

- **IDCODE**  
Presents the contents of the Device Identification register in serial format.
- **CLAMP**  
Ensures that the Bypass register is connected between TDI and TDO, and then drives data that was loaded into the Boundary Scan register (e.g., via SAMPLE-PRELOAD instruction) to output signals. These signals do not change while the CLAMP instruction is selected.
- **HiZ**  
Puts all chip outputs in inactive (floating) state (including all pins that do not require a TRI-STATE output for normal functionality). Note that not all pull-up resistors are disabled in this state.

### 8.1.3 JTAG Chain

Balls that are not part of the JTAG chain:

- USB I/Os

**Table 8-1. JTAG Mode Instruction Support**

| Code | Instruction    | Activity   |
|------|----------------|--|
| 000  | EXTEST         | Drives shifted data to output pins.                  |
| 001  | SAMPLE/PRELOAD | Captures inputs and system outputs.                  |
| 010  | IDCODE         | Scans out device identifier.                         |
| 011  | HIZ            | Puts all output and bidirectional pins in TRI-STATE. |
| 100  | CLAMP          | Drives fixed data from Boundary Scan register.       |
| 101  | Reserved       |  |
| 110  | Reserved       |  |
| 111  | BYPASS         | Presents shortest external path through device.      |





# Electrical Specifications



This chapter provides information about:

- General electrical specifications
- DC characteristics
- AC characteristics

All voltage values in this chapter are with respect to  $V_{SS}$  unless otherwise noted.

## 9.1 General Specifications

### 9.1.1 Electro Static Discharge (ESD)

This device is a high performance integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations. Table 9-1 lists the ESD ratings of the SC3200.

**Table 9-1. Electro Static Discharge (ESD)**

| Parameter              | Units     |
|------------------------|-----------|
| Human Body Model (HBM) | 2000V ESD |
| Machine Model (MM)     | 200V ESD  |

### 9.1.2 Power/Ground Connections and Decoupling

When testing and operating the SC3200, use standard high frequency techniques to reduce parasitic effects. For example:

- Filter the DC power leads with low-inductance decoupling capacitors.
- Use low-impedance wiring.
- Utilizing the PWR and GND pins.

### 9.1.3 Absolute Maximum Ratings

Stresses beyond those indicated in the following table may cause permanent damage to the SC3200, reduce device reliability and result in premature failure, even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced device life span and reduced reliability.

**Note:** The values in the following table are stress ratings only. They do not imply that operation under other conditions is impossible.

**Table 9-2. Absolute Maximum Ratings**

| Symbol        | Parameter                  | Min  | Max           | Unit        | Comments       |
|---------------|----------------------------|------|---------------|-------------|----------------|
| $T_{CASE}$    | Operating case temperature | -10  | 110           | $^{\circ}C$ | Note 1         |
| $T_{STORAGE}$ | Storage temperature        | -45  | 125           | $^{\circ}C$ | Note 2         |
| $V_{CC}$      | Supply voltage             |      | See Table 9-3 | V           |                |
| $V_{MAX}$     | Voltage on                 |      |               |             |                |
|               | 5V tolerant balls          | -0.5 | 6.0           | V           | Note 3         |
|               | Others                     | -0.5 | 3.6           | V           | Note 3, Note 4 |
| $I_{IK}$      | Input clamp current        | -0.5 | 10            | mA          | Note 1         |
| $I_{OK}$      | Output clamp current       |      | 25            | mA          | Note 1         |

Note 1. Power applied - no clocks.

Note 2. No bias.

Note 3. Voltage min is -0.8V with a transient voltage of 20 ns or less.

Note 4. Voltage max is 4.0V with a transient voltage of 20 ns or less.

### 9.1.4 Operating Conditions

Table 9-3 lists the various power supplies of the SC3200 and provides the device operating conditions.

**Table 9-3. Operating Conditions**

| Symbol (Note 1)          | Parameter  | Min  | Typ | Max  | Unit               | Comments |
|--------------------------|--|------|-----|------|--------------------|----------|
| $T_C$                    | Operating case temperature   | 0    | -   | 85   | $^{\circ}\text{C}$ |          |
| $V_{CCUSB}$              | Analog power supply. Powers internal analog circuits and some external signals (see Table 9-4).  | 3.14 | 3.3 | 3.46 | V                  |          |
| $V_{BAT}$                | Battery supply voltage. Powers RTC and ACPI when $V_{BAT}$ is greater than $V_{SB}$ (by at least 0.5V), and some external signals (see Table 9-4).     | 2.4  | 3.0 | 3.46 | V                  |          |
| $V_{IO}$                 | I/O buffer power supply. Powers most of the external signals (see Table 9-4); certain signals within this power plane are 5V tolerant.                 | 3.14 | 3.3 | 3.46 | V                  |          |
| $V_{CORE}$               | Core processor and internal digital power supply. Powers internal digital logic, including internal frequency multipliers.                             | 1.71 | 1.8 | 1.89 | V                  |          |
| $V_{PLL2}$<br>$V_{PLL3}$ | PLL. Internal Phase Locked Loops (PLL) power supply.   | 3.14 | 3.3 | 3.46 | V                  |          |
| $V_{SB}$                 | Standby power supply. Powers RTC and ACPI when $V_{SB}$ is greater than $V_{BAT}-0.5\text{V}$ , and some external signals (see Table 9-4).             | 3.14 | 3.3 | 3.46 | V                  |          |
| $V_{SBL}$                | Standby logic. Powers internal logic needed to support Standby $V_{SB}$ .<br><br>$V_{SBL}$ requires a 0.1 $\mu\text{F}$ bypass capacitor to $V_{SS}$ . | 1.71 | 1.8 | 1.89 | V                  |          |

Note 1. For  $V_{IH}$  (Input High Voltage),  $V_{IL}$  (Input Low Voltage),  $I_{OH}$  (Output High Current), and  $I_{OL}$  (Output Low Current) operating conditions refer to Section 9.2 "DC Characteristics" on page 375.

#### Notes:

- All power sources except  $V_{BAT}$  must be connected, even if the function is not used.
- $V_{SB}$ , and  $V_{SBL}$  must be on if any other voltage is applied.  $V_{SB}$  and  $V_{BAT}$  voltages can be applied separately. See Section 9.3.15 "Power-Up Sequencing" on page 434.
- The power planes of the SC3200 can be turned on or off. For more information, see Section 6.2.9 "Power Management Logic" on page 174.
- It is recommended that the voltage difference between  $V_{CORE}$  and  $V_{SBL}$  be less than 0.25V, in order to reduce leakage current. If the voltage difference exceeds 0.25V, excessive leakage current is used in gates that are connected on the boundary between voltage domains.
- It is recommended that the voltage difference between  $V_{IO}$  and  $V_{SB}$  be less than 0.25V, in order to reduce leakage current. If the voltage difference exceeds 0.25V, excessive leakage current is used in gates that are connected on the boundary between voltage domains.

Table 9-4 indicates which power rails are used for each signal of the SC3200 external interface. Power planes not listed in this table are internal, and are not related to signals of the external interface.

**Table 9-4. Power Planes of External Interface Signals**

| Power Plane | Signal Names   | V <sub>CC</sub> Balls | V <sub>SS</sub> Balls |
|-------------|--|-----------------------|-----------------------|
| Standby     | GPWIO[0:2], LED#, ONCTL#, PWRBTN#, PWRCNT[1:2], THRM#, CLK32, IRRX1, RI2#, SDATA_IN2 | V <sub>SB</sub>       | V <sub>SS</sub>       |
| Battery     | X32I, X32O   | V <sub>BAT</sub>      | V <sub>SS</sub>       |
| USB         | DPOS_PORT1, DNEG_PORT1, DPOS_PORT2, DNEG_PORT2, DPOS_PORT3, DNEG_PORT3               | AV <sub>CCUSB</sub>   | AV <sub>SSUSB</sub>   |
| I/O         | All other external interface signals   | V <sub>IO</sub>       | V <sub>SS</sub>       |

### 9.1.5 DC Current

DC current is not a simple measurement. Three of the SC3200 power states (On, Active Idle, Sleep) were selected for measurement. For each power state measured, two functional characteristics (Typical Average, Absolute Maximum) are used to determine how much current the SC3200 uses.

#### 9.1.5.1 Power State Parameter Definitions

The DC characteristics tables in this section list Core and I/O current for three of the power states. For more explanation on the SC3200 power states see Section 6.2.9 "Power Management Logic" on page 174.

- **On (C0):** All internal and external clocks with respect to the SC3200 are running and all functional blocks inside the GX1 module (CPU Core, Memory Controller, Display Controller, etc.) are actively generating cycles. This is equivalent to the ACPI specification's "S0,C0" state.
- **Active Idle (C1):** The CPU Core has been halted, all other functional blocks (including the Display Controller for refreshing the display) are actively generating cycles. This state is entered when a HLT instruction is executed by the CPU Core. From a user's perspective, this state is indistinguishable from the On state and is equivalent to the ACPI specification's "S0,C1" state.
- **Sleep (SL2):** This is the lowest power state the SC3200 can be in with voltage still applied to the device's core and I/O supply pins. This is equivalent to the ACPI specification's "S1" state.

#### 9.1.5.2 Definition and Measurement Techniques of SC3200 Current Parameters

These parameters describe the current while the SC3200 is in the On state:

- **Typical Average:** Indicates the average current used by the SC3200 while in the On state. This is measured by running typical Windows applications in a typical display mode. In this case, 800x600x8 bpp at 75 Hz, 50 MHz DCLK using a background image of vertical stripes (4-pixel wide) alternating between black and white with power management disabled (to guarantee that the SC3200 never goes into the Active Idle state). This number is provided for reference only since it can vary greatly depending on the usage model of the system.
- **Note:** This typical average should not be confused with the typical power numbers. Typical power is based on a combination of On (Typical Average) and Active Idle states.
- **Absolute Maximum:** Indicates the maximum instantaneous current used by the SC3200. CPU Core current is measured by running the Landmark Speed 200 benchmark test (with power management disabled) and measuring the peak current at any given instant during the test. I/O current is measured by running Microsoft Windows 98® and using a background image of vertical stripes (1-pixel wide) alternating between black and white at the maximum display resolution.

### 9.1.5.3 Definition of System Conditions for Measuring On Parameters

The SC3200's current is highly dependent on two functional characteristics, DCLK (DOT clock) and SDRAM frequency. Table 9-5 shows how these factors are controlled when measuring the typical average and absolute maximum processor current parameters.

### 9.1.5.4 DC Current Measurements

Table 9-6 and Table 9-7 show the DC current measurements of the SC3200.

**Table 9-5. System Conditions Used to Measure SC3200 Current During On State**

| CPU Current Measurement | System Conditions             |                             |                   |                    |
|-------------------------|-------------------------------|-----------------------------|-------------------|--------------------|
|                         | V <sub>CORE</sub><br>(Note 1) | V <sub>IO</sub><br>(Note 1) | DCLK<br>Frequency | SDRAM<br>Frequency |
| Typical Average         | Nominal                       | Nominal                     | 50 MHz (Note 2)   | Nominal            |
| Absolute Maximum        | Max                           | Max                         | 135 MHz (Note 3)  | Max                |

Note 1. See Table 9-3 on page 370 for nominal and maximum voltages.

Note 2. A DCLK frequency of 50 MHz is derived by setting the display mode to 800x600x8 bpp at 75 Hz, using a display image of vertical stripes (4-pixel wide) alternating between black and white with power management disabled.

Note 3. A DCLK frequency of 135 MHz is derived by setting the display mode to 1280x1024x8 bpp at 75 Hz, using a display image of vertical stripes (1-pixel wide) alternating between black and white with power management disabled.

**Table 9-6. DC Characteristics for On State**

| Symbol              | Parameter (Note 1)  | Typ Avg | Abs Max | Unit | Comments                              |
|---------------------|---|---------|---------|------|---------------------------------------|
| I <sub>CC3ON</sub>  | f <sub>CLK</sub> = 233 MHz, I/O Current @ V <sub>IO</sub> = 3.3V (Nominal); CPU state = On    | 260     | 300     | mA   | I <sub>CC</sub> for V <sub>IO</sub>   |
|                     | f <sub>CLK</sub> = 266 MHz, I/O Current @ V <sub>IO</sub> = 3.3V (Nominal); CPU state = On    | 270     | 310     |      |                                       |
| I <sub>COREON</sub> | f <sub>CLK</sub> = 233 MHz, Core Current @ V <sub>CORE</sub> = 1.8V (Nominal); CPU state = On | 820     | 990     | mA   | I <sub>CC</sub> for V <sub>CORE</sub> |
|                     | f <sub>CLK</sub> = 266 MHz, Core Current @ V <sub>CORE</sub> = 1.8V (Nominal); CPU state = On | 900     | 1090    |      |                                       |
| I <sub>SBON</sub>   | SB Current @ V <sub>SB</sub> = 3.3V (Nominal); CPU state = On                                 | 1       | 2       | mA   |                                       |
| I <sub>SBLON</sub>  | SBL Current @ V <sub>SBL</sub> = 1.8V (Nominal); CPU state = On                               | 10      | 20      | mA   |                                       |
|                     | SBL Current @ V <sub>SBL</sub> = 2.0V (Nominal); CPU state = On                               | 10      | 20      |      |                                       |

Note 1. f<sub>CLK</sub> ratings refer to internal clock frequency.

**Table 9-7. DC Characteristics for Active Idle, Sleep, and Off States**

| Symbol                | Parameter <sup>Note 1</sup>  | Min | Typ | Max | Unit | Comments                                       |
|-----------------------|--|-----|-----|-----|------|--|
| I <sub>CC3IDLE</sub>  | f <sub>CLK</sub> = 233 MHz, I/O Current @ V <sub>IO</sub> = 3.3V (Nominal); CPU state = Active Idle    |     | 260 |     | mA   | I <sub>CC</sub> for V <sub>IO</sub>            |
|                       | f <sub>CLK</sub> = 266 MHz, I/O Current @ V <sub>IO</sub> = 3.3V (Nominal); CPU state = Active Idle    |     | 270 |     |      |  |
| I <sub>CC3SLP</sub>   | I/O Current @ V <sub>IO</sub> = 3.3V (Nominal); CPU state = Sleep                                      |     | 20  | 30  | mA   | I <sub>CC</sub> for V <sub>IO</sub> , Note 2   |
| I <sub>COREIDLE</sub> | f <sub>CLK</sub> = 233 MHz, Core Current @ V <sub>CORE</sub> = 1.8V (Nominal); CPU state = Active Idle |     | 360 |     | mA   | I <sub>CC</sub> for V <sub>CORE</sub>          |
|                       | f <sub>CLK</sub> = 266 MHz, Core Current @ V <sub>CORE</sub> = 1.8V (Nominal); CPU state = Active Idle |     | 380 |     |      |  |
| I <sub>CORESLEP</sub> | Core Current @ V <sub>CORE</sub> = 1.8V (Nominal); CPU state = Sleep                                   |     | 20  | 30  | mA   | I <sub>CC</sub> for V <sub>CORE</sub> , Note 2 |
| I <sub>SBOFF</sub>    | SB Current @ V <sub>SB</sub> = 3.3V (Nominal); CPU state = Off   |     | <1  |     | mA   |  |
| I <sub>SBLOFF</sub>   | SBL Current @ V <sub>SBL</sub> = 1.8V (Nominal); CPU state = Off                                       |     | <1  |     | mA   | I <sub>CC</sub> for V <sub>SBL</sub> , Note 3  |
| I <sub>BAT</sub>      | BAT Current @ V <sub>BAT</sub> = 3.0 (Nominal); CPU state = Off  |     | 7   | 50  | μA   |  |

Note 1. f<sub>CLK</sub> ratings refer to internal clock frequency.

Note 2. All inputs are at 0.2V or V<sub>IO</sub> – 0.2 (CMOS levels). All inputs are held static, and all outputs are unloaded (static I<sub>OUT</sub> = 0 mA).

Note 3. All V<sub>SBL</sub> supplied inputs are at 0.2V or V<sub>SBL</sub> – 0.2 (CMOS levels). All inputs are held static, and all outputs are unloaded (static I<sub>OUT</sub> = 0 mA).

### 9.1.6 Ball Capacitance and Inductance

Table 9-8 gives ball capacitance and inductance values.

**Table 9-8. Ball Capacitance and Inductance**

| Symbol           | Parameter               | Min | Typ | Max | Unit | Comments |
|------------------|-------------------------|-----|-----|-----|------|----------|
| C <sub>IN</sub>  | Input Pin Capacitance   |     | 4   | 7   | pF   | Note 1   |
| C <sub>IN</sub>  | Clock Input Capacitance | 5   | 8   | 12  | pF   | Note 1   |
| C <sub>IO</sub>  | I/O Pin Capacitance     |     | 10  | 12  | pF   | Note 1   |
| C <sub>O</sub>   | Output Pin Capacitance  |     | 6   | 8   | pF   | Note 1   |
| L <sub>PIN</sub> | Pin Inductance          |     |     | 20  | nH   | Note 2   |

Note 1. T<sub>A</sub> = 25°C, f = 1 MHz. All capacitances are not 100% tested.

Note 2. Not 100% tested.

### 9.1.7 Pull-Up and Pull-Down Resistors

The following table lists input balls that are internally connected to a pull-up (PU) or pull-down (PD) resistor. If these balls are not used, they do not require connection to an external PU or PD resistor.

**Note:** The resistors described in this table are implemented as transistors. The resistance for PUs assumes  $V_{IN} = V_{SS}$  and for PDs assumes  $V_{IN} = V_{IO}$ .

**Table 9-9. Balls with PU/PD Resistors**

| Signal Name                | Ball No.                  |                       | PU/<br>PD    | Typ<br>(Note 1)<br>Value [ $\Omega$ ] |
|----------------------------|---------------------------|-----------------------|--------------|---------------------------------------|
|                            | EBGA                      | TEPBGA                |              |                                       |
| <b>PCI</b>                 |                           |                       |              |                                       |
| FRAME#                     | E1                        | D8                    | PU           | 22.5K                                 |
| C/BE[3:0]#                 | A8, D8,<br>A10, A13       | H4, F3, J2,<br>L1     | PU           | 22.5K                                 |
| PAR                        | C10                       | J4                    | PU           | 22.5K                                 |
| IRDY#                      | C8                        | F2                    | PU           | 22.5K                                 |
| TRDY#                      | B8                        | F1                    | PU           | 22.5K                                 |
| STOP#                      | D9                        | G1                    | PU           | 22.5K                                 |
| LOCK#                      | C9                        | H3                    | PU           | 22.5K                                 |
| DEVSEL#                    | B5                        | E4                    | PU           | 22.5K                                 |
| PERR#                      | B9                        | H2                    | PU           | 22.5K                                 |
| SERR#                      | A9                        | H1                    | PU           | 22.5K                                 |
| REQ[1:0]#                  | E3, C1                    | A5, B5                | PU           | 22.5K                                 |
| INTA#                      | AE3                       | D26                   | PU           | 22.5K                                 |
| INTB#                      | AF1                       | C26                   | PU           | 22.5K                                 |
| INTC#                      | H4                        | C9                    | PU           | 22.5K                                 |
| INTD#                      | B22                       | AA2                   | PU           | 22.5K                                 |
| <b>Low Pin Count (LPC)</b> |                           |                       |              |                                       |
| LAD[3:0]                   | AJ10, AK10,<br>AL10, AJ11 | L29, L30,<br>L31, M28 | PU           | 22.5K                                 |
| LDRQ                       | AL9                       | L28                   | PU           | 22.5K                                 |
| SERIRQ                     | AL8                       | J31                   | PU           | 22.5K                                 |
| <b>System (Straps)</b>     |                           |                       |              |                                       |
| CLKSEL[3:0]                | AL13, AK3,<br>B27, F3     | P30, D29,<br>AF3, B8  | PD           | 100K                                  |
| BOOT16                     | G4                        | C8                    | PD           | 100K                                  |
| TFT_PRSENT                 | AK13                      | P29                   | PD           | 100K                                  |
| LPC_ROM                    | E4                        | D6                    | PD           | 100K                                  |
| FPCI_MON                   | D3                        | A4                    | PD           | 100K                                  |
| DID[1:0]                   | D2, D4                    | C6, C5                | PD           | 100K                                  |
| <b>ACCESS.bus (Note 2)</b> |                           |                       |              |                                       |
| AB1C                       | AJ13                      | N31                   | PU           | 22.5K                                 |
| AB1D                       | AL12                      | N30                   | PU           | 22.5K                                 |
| AB2C                       | AJ12                      | N29                   | PU           | 22.5K                                 |
| AB2D                       | AL11                      | M29                   | PU           | 22.5K                                 |
| <b>Parallel Port</b>       |                           |                       |              |                                       |
| AFD#/DSTRB#                | AB2                       | D22                   | PU           | 22.5K                                 |
| PE                         | T3                        | D17                   | PUNot<br>e 2 | 22.5K                                 |
|                            |                           |                       | PDNot<br>e 2 | 22.5K                                 |
| SLIN#/ASTRB#               | W1                        | B20                   | PU           | 22.5K                                 |
| STB#/WRITE#                | AB1                       | A22                   | PU           | 22.5K                                 |

| Signal Name                 | Ball No.         |                  | PU/<br>PD | Typ<br>(Note 1)<br>Value [ $\Omega$ ] |
|-----------------------------|------------------|------------------|-----------|---------------------------------------|
|                             | EBGA             | TEPBGA           |           |                                       |
| INIT#                       | Y3               | B21              | PU        | 22.5K                                 |
| <b>JTAG</b>                 |                  |                  |           |                                       |
| TCK                         | AL4              | E31              | PU        | 22.5K                                 |
| TMS                         | AJ5              | F28              | PU        | 22.5K                                 |
| TDI                         | AK5              | F29              | PU        | 22.5K                                 |
| TRST#                       | AK4              | E29              | PU        | 22.5K                                 |
| <b>GPIO (Note 2)</b>        |                  |                  |           |                                       |
| GPIO1                       | H2, AL12         | D10, N30         | PU        | 22.5K                                 |
| GPIO6                       | AH3              | D28              | PU        | 22.5K                                 |
| GPIO7                       | AH4              | C30              | PU        | 22.5K                                 |
| GPIO8                       | AJ2              | C31              | PU        | 22.5K                                 |
| GPIO9                       | AG4              | C28              | PU        | 22.5K                                 |
| GPIO10                      | AJ1              | B29              | PU        | 22.5K                                 |
| GPIO11                      | H30              | AJ8              | PU        | 22.5K                                 |
| GPIO12                      | AJ12             | N29              | PU        | 22.5K                                 |
| GPIO13                      | AL11             | M29              | PU        | 22.5K                                 |
| GPIO14                      | F1               | D9               | PU        | 22.5K                                 |
| GPIO15                      | G3               | A8               | PU        | 22.5K                                 |
| GPIO16                      | AL15             | V31              | PU        | 22.5K                                 |
| GPIO17                      | J4               | A10              | PU        | 22.5K                                 |
| GPIO18                      | A28              | AG1              | PU        | 22.5K                                 |
| GPIO19                      | H4               | C9               | PU        | 22.5K                                 |
| GPIO20                      | H3, AJ13         | A9, N31          | PU        | 22.5K                                 |
| GPIO32                      | AJ11             | M28              | PU        | 22.5K                                 |
| GPIO33                      | AL10             | L31              | PU        | 22.5K                                 |
| GPIO34                      | AK10             | L30              | PU        | 22.5K                                 |
| GPIO35                      | AJ10             | L29              | PU        | 22.5K                                 |
| GPIO36                      | AL9              | L28              | PU        | 22.5K                                 |
| GPIO37                      | AK9              | K31              | PU        | 22.5K                                 |
| GPIO38                      | AJ9              | K28              | PU        | 22.5K                                 |
| GPIO39                      | AL8              | J31              | PU        | 22.5K                                 |
| <b>Power Management</b>     |                  |                  |           |                                       |
| PWRBTN#                     | E29              | AH5              | PU        | 100K                                  |
| GPWIO[2:0]                  | G29, G28,<br>E31 | AJ6, AK5,<br>AH6 | PU        | 100K                                  |
| <b>Test and Measurement</b> |                  |                  |           |                                       |
| GTEST                       | AL5              | F30              | PD        | 22.5K                                 |

Note 1. Accuracy is: 22.5 K $\Omega$  resistors are within a range of 20 K $\Omega$  to 50 K $\Omega$ . 100 K $\Omega$  resistors are within a range of 90 K $\Omega$  to 250 K $\Omega$ .

Note 2. Controlled by software.

## 9.2 DC Characteristics

Table 9-10 describes the signal buffer types of the SC3200. (See Table 3-2 "432-EBGA Ball Assignment - Sorted by Ball Number" on page 29 and Table 3-4 "481-TEPBGA Ball Assignment - Sorted by Ball Number" on page 43) for each signal's buffer type.)

The subsections that follows provide detailed DC characteristics according to buffer type.

**Table 9-10. Buffer Types**

| Symbol             | Description  | Reference      |
|--------------------|--|----------------|
| Diode              | Diodes only, no buffer   | ---            |
| IN <sub>AB</sub>   | Input, ACCESS.bus compatible with Schmitt Trigger                                  | Section 9.2.1  |
| IN <sub>BTN</sub>  | Input, TTL compatible with Schmitt Trigger, low leakage                            | Section 9.2.2  |
| IN <sub>PCI</sub>  | Input, PCI compatible  | Section 9.2.3  |
| IN <sub>STRP</sub> | Input, Strap ball (min V <sub>IH</sub> is 0.6V <sub>IO</sub> ) with weak pull-down | Section 9.2.4  |
| IN <sub>T</sub>    | Input, TTL compatible  | Section 9.2.5  |
| IN <sub>TS</sub>   | Input, TTL compatible with Schmitt Trigger type 200 mV                             | Section 9.2.6  |
| IN <sub>TS1</sub>  | Input, with Schmitt Trigger type 200 mV  | Section 9.2.7  |
| IN <sub>USB</sub>  | Input, USB compatible  | Section 9.2.8  |
| O <sub>AC97</sub>  | Output, Totem-Pole, AC97 compatible  | Section 9.2.9  |
| OD <sub>n</sub>    | Output, Open-Drain, capable of sinking <i>n</i> mA. Note 1                         | Section 9.2.10 |
| OD <sub>PCI</sub>  | Output, Open-Drain, PCI compatible   | Section 9.2.11 |
| O <sub>p/n</sub>   | Output, Totem-Pole, capable of sourcing <i>p</i> mA and sinking <i>n</i> mA        | Section 9.2.12 |
| O <sub>PCI</sub>   | Output, PCI compatible, TRI-STATE  | Section 9.2.13 |
| O <sub>USB</sub>   | Output, USB compatible   | Section 9.2.14 |
| TS <sub>p/n</sub>  | Output, TRI-STATE, capable of sourcing <i>p</i> mA and sinking <i>n</i> mA         | Section 9.2.15 |
| WIRE               | Wire, no buffer  | ---            |

Note 1. Output from these signals is open-drain and cannot be forced high.

### 9.2.1 $IN_{AB}$ DC Characteristics

| Symbol    | Parameter             | Min              | Max | Unit    | Comments          |
|-----------|-----------------------|------------------|-----|---------|-------------------|
| $V_{IH}$  | Input High Voltage    | 1.4              |     | V       |                   |
| $V_{IL}$  | Input Low Voltage     | -0.5<br>(Note 1) | 0.8 | V       |                   |
| $I_{IL}$  | Input Leakage Current |                  | 10  | $\mu A$ | $V_{IN} = V_{IO}$ |
|           |                       |                  | -10 | $\mu A$ | $V_{IN} = V_{SS}$ |
| $V_{HIS}$ | Input hysteresis      | 150              |     | mV      |                   |

Note 1. Not 100% tested.

### 9.2.2 $IN_{BTN}$ DC Characteristics

| Symbol    | Parameter              | Min              | Max                      | Unit    | Comments          |
|-----------|------------------------|------------------|--------------------------|---------|-------------------|
| $V_{IH}$  | Input High Voltage     | 2.0              | $V_{SB}+0.3$<br>(Note 1) | V       |                   |
| $V_{IL}$  | Input Low Voltage      | -0.5<br>(Note 1) | 0.8                      | V       |                   |
| $I_{IL}$  | Input Leakage Current  |                  | 5                        | $\mu A$ | $V_{IN} = V_{SB}$ |
|           |                        |                  | -36                      | $\mu A$ | $V_{IN} = V_{SS}$ |
| $V_{HIS}$ | Input HysteresisNote 1 | 250              |                          | mV      |                   |

Note 1. Not 100% tested.

### 9.2.3 $IN_{PCI}$ DC Characteristics

Note that the buffer type for PCICLK (EBGA ball E2 / TEPBGA ball A7) is  $IN_T$  - not  $IN_{PCI}$ .

| Symbol    | Parameter             | Min              | Max                      | Unit    | Comments                               |
|-----------|-----------------------|------------------|--------------------------|---------|--|
| $V_{IH}$  | Input High Voltage    | $0.5V_{IO}$      | $V_{IO}+0.3$<br>(Note 1) | V       |  |
| $V_{IL}$  | Input Low Voltage     | -0.5<br>(Note 1) | $0.3V_{IO}$              | V       |  |
| $V_{IPU}$ | Input Pull-up Voltage | $0.7V_{IO}$      |                          | V       | Note 2                                 |
| $I_{IL}$  | Input Leakage Current |                  | +/-10                    | $\mu A$ | $0 < V_{IN} < V_{IO}$ , Note 3, Note 4 |

Note 1. Not 100% tested.

Note 2. Not 100% tested. This parameter indicates the minimum voltage to which pull-up resistors are calculated in order to pull a floated network.

Note 3. Input leakage currents include HiZ output leakage for all bidirectional buffers with TRI-STATE outputs.

Note 4. See Exceptions 2 and 3 in Section 9.2.15.1 on page 379.



### 9.2.4 $IN_{STRP}$ DC Characteristics

| Symbol   | Parameter             | Min         | Max                      | Unit    | Comments                        |
|----------|-----------------------|-------------|--------------------------|---------|---------------------------------|
| $V_{IH}$ | Input High Voltage    | $0.6V_{IO}$ | $V_{IO}+0.3$<br>(Note 1) | V       |                                 |
| $V_{IL}$ | Input Low Voltage     |             | $0.3V_{IO}$              | V       |                                 |
| $I_{IL}$ | Input Leakage Current |             | 36                       | $\mu A$ | During Reset: $V_{IN} = V_{IO}$ |
|          |                       |             | -10                      | $\mu A$ | $V_{IN} = V_{SS}$               |

Note 1. Not 100% tested.

### 9.2.5 $IN_T$ DC Characteristics

| Symbol   | Parameter             | Min              | Max                      | Unit    | Comments          |
|----------|-----------------------|------------------|--------------------------|---------|-------------------|
| $V_{IH}$ | Input High Voltage    | 2.0              | $V_{IO}+0.3$<br>(Note 1) | V       |                   |
| $V_{IL}$ | Input Low Voltage     | -0.5<br>(Note 1) | 0.8                      | V       |                   |
| $I_{IL}$ | Input Leakage Current |                  | 10                       | $\mu A$ | $V_{IN} = V_{IO}$ |
|          |                       |                  | -10                      | $\mu A$ | $V_{IN} = V_{SS}$ |

Note 1. Not 100% tested.

### 9.2.6 $IN_{TS}$ DC Characteristics

| Symbol   | Parameter             | Min              | Max                      | Unit    | Comments          |
|----------|-----------------------|------------------|--------------------------|---------|-------------------|
| $V_{IH}$ | Input High Voltage    | 2.0              | $V_{IO}+0.3$<br>(Note 1) | V       |                   |
| $V_{IL}$ | Input Low Voltage     | -0.5<br>(Note 1) | 0.8                      | V       |                   |
| $I_{IL}$ | Input Leakage Current |                  | 10                       | $\mu A$ | $V_{IN} = V_{IO}$ |
|          |                       |                  | -10                      | $\mu A$ | $V_{IN} = V_{SS}$ |
| $V_H$    | Input Hysteresis      | 200              |                          | mV      |                   |

Note 1. Not 100% tested.

### 9.2.7 $IN_{TS1}$ DC Characteristics

| Symbol    | Parameter             | Min              | Max                      | Unit    | Comments          |
|-----------|-----------------------|------------------|--------------------------|---------|-------------------|
| $V_{IH}$  | Input High Voltage    | $0.5V_{IO}$      | $V_{IO}+0.3$<br>(Note 1) | V       |                   |
| $V_{IL}$  | Input Low Voltage     | -0.5<br>(Note 1) | $0.3V_{IO}$              | V       |                   |
| $I_{IL}$  | Input Leakage Current |                  | 10                       | $\mu A$ | $V_{IN} = V_{IO}$ |
|           |                       |                  | -10                      | $\mu A$ | $V_{IN} = V_{SS}$ |
| $V_{HIS}$ | Input Hysteresis      | 200              |                          | mV      | Note 1            |

Note 1. Not 100% tested.

9.2.8 IN<sub>USB</sub> DC Characteristics

| Symbol          | Parameter                       | Min              | Max                              | Unit | Comments                          |
|-----------------|---------------------------------|------------------|----------------------------------|------|-----------------------------------|
| V <sub>IH</sub> | Input High Voltage              | 2.0              | V <sub>IO</sub> +0.3<br>(Note 1) | V    |                                   |
| V <sub>IL</sub> | Input Low Voltage               | -0.5<br>(Note 1) | 0.8                              | V    |                                   |
| I <sub>IL</sub> | Input Leakage Current           |                  | 10                               | μA   | V <sub>IN</sub> = V <sub>IO</sub> |
|                 |                                 |                  | -10                              | μA   | V <sub>IN</sub> = V <sub>SS</sub> |
| V <sub>DI</sub> | Differential Input Sensitivity  | 0.2              |                                  | V    | (D+)-(D-)  and Figure 9-1         |
| V <sub>CM</sub> | Differential Common Mode Range  | 0.8              | 2.5                              | V    | Includes V <sub>DI</sub> Range    |
| V <sub>SE</sub> | Single Ended Receiver Threshold | 0.8              | 2.0                              | V    |                                   |

Note 1. Not 100% tested.

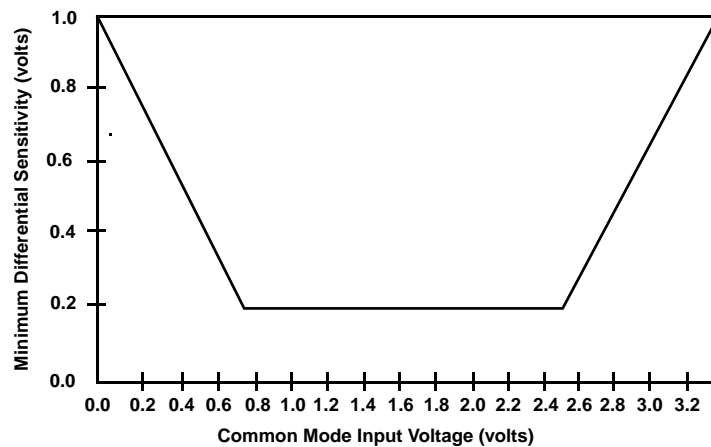


Figure 9-1. Differential Input Sensitivity for Common Mode Range

9.2.9 O<sub>AC97</sub> DC Characteristics

| Symbol          | Parameter           | Min                | Max                | Unit | Comments                |
|-----------------|---------------------|--------------------|--------------------|------|-------------------------|
| V <sub>OH</sub> | Output High Voltage | 0.9V <sub>IO</sub> |                    | V    | I <sub>OH</sub> = -5 mA |
| V <sub>OL</sub> | Output Low Voltage  |                    | 0.1V <sub>IO</sub> | V    | I <sub>OL</sub> = 5 mA  |

9.2.10 OD<sub>n</sub> DC Characteristics

| Symbol          | Parameter          | Min | Max | Unit | Comments               |
|-----------------|--------------------|-----|-----|------|------------------------|
| V <sub>OL</sub> | Output Low Voltage |     | 0.4 | V    | I <sub>OL</sub> = n mA |

**9.2.11 OD<sub>PCI</sub> DC Characteristics**

| Symbol          | Parameter          | Min | Max                | Unit | Comments                  |
|-----------------|--------------------|-----|--------------------|------|---------------------------|
| V <sub>OL</sub> | Output Low Voltage |     | 0.1V <sub>IO</sub> | V    | I <sub>OL</sub> = 1500 μA |

**9.2.12 O<sub>p/n</sub> DC Characteristics**

| Symbol          | Parameter           | Min | Max | Unit | Comments                |
|-----------------|---------------------|-----|-----|------|-------------------------|
| V <sub>OH</sub> | Output High Voltage | 2.4 |     | V    | I <sub>OH</sub> = -p mA |
| V <sub>OL</sub> | Output Low Voltage  |     | 0.4 | V    | I <sub>OL</sub> = n mA  |

**9.2.13 O<sub>PCI</sub> DC Characteristics**

| Symbol          | Parameter           | Min                | Max                | Unit | Comments                  |
|-----------------|---------------------|--------------------|--------------------|------|---------------------------|
| V <sub>OH</sub> | Output High Voltage | 0.9V <sub>IO</sub> |                    | V    | I <sub>OH</sub> = -500 μA |
| V <sub>OL</sub> | Output Low Voltage  |                    | 0.1V <sub>IO</sub> | V    | I <sub>OL</sub> = 1500 μA |

**9.2.14 O<sub>USB</sub> DC Characteristics**

| Symbol               | Parameter                       | Min | Max             | Unit | Comments  |
|----------------------|---------------------------------|-----|-----------------|------|---|
| V <sub>USB_OH</sub>  | High-level Output Voltage       | 2.8 | 3.6<br>(Note 1) | V    | I <sub>OH</sub> = -0.25 mA<br>R <sub>L</sub> = 15 KΩ to GND |
| V <sub>USB_OL</sub>  | Low-level Output Voltage        |     | 0.3             | V    | I <sub>OL</sub> = 2.5 mA<br>R <sub>L</sub> = 1.5 KΩ to 3.6V |
| t <sub>USB_CRS</sub> | Output Signal Crossover Voltage | 1.3 | 2.0             | V    |   |

Note 1. Tested by characterization.

**9.2.15 TS<sub>p/n</sub> DC Characteristics**

| Symbol          | Parameter           | Min | Max | Unit | Comments                |
|-----------------|---------------------|-----|-----|------|-------------------------|
| V <sub>OH</sub> | Output High Voltage | 2.4 |     | V    | I <sub>OH</sub> = -p mA |
| V <sub>OL</sub> | Output Low Voltage  |     | 0.4 | V    | I <sub>OL</sub> = n mA  |

**9.2.15.1 Exceptions**

- I<sub>OH</sub> is valid for a GPIO pin only when it is not configured as open-drain.
- Signals with internal pull-ups have a maximum input leakage current of:  $-\left(\frac{V_{\text{power}} - V_{\text{IN}}}{R(\text{pull-up})}\right)$   
Where V<sub>power</sub> is V<sub>IO</sub> or V<sub>SB</sub>.
- Signals with internal pull-downs have a maximum input leakage current of:  $+\left(\frac{V_{\text{IN}} - V_{\text{SS}}}{R(\text{pull-down})}\right)$

### 9.3 AC Characteristics

The tables in this section list the following AC characteristics:

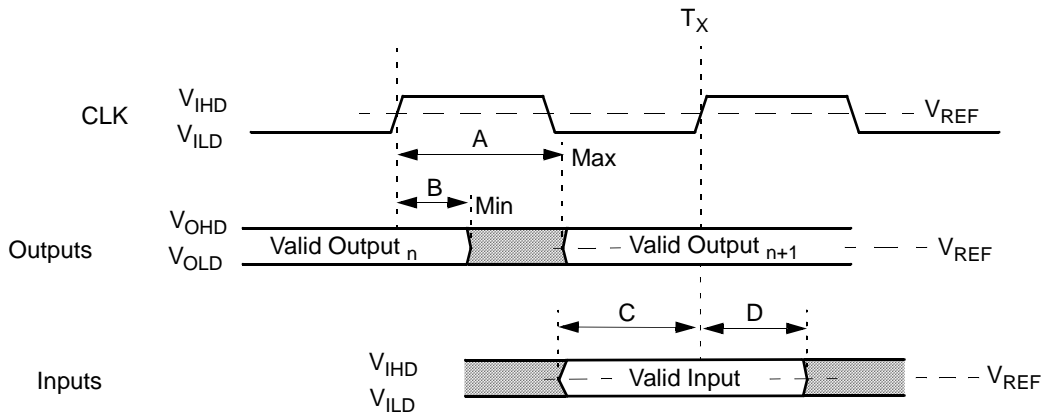
- Output delays
- Input setup requirements
- Input hold requirements
- Output float delays
- Power-up sequencing requirements

The default levels for measurement of the rising clock edge reference voltage ( $V_{REF}$ ), and other voltages are shown in Table 9-11. Input or output signals must cross these levels during testing. Unless otherwise specified, all measurement points in this section conform to these default levels.

**Table 9-11. Default Levels for Measurement of Switching Parameters**

| Symbol    | Parameter                 | Value (V) |
|-----------|---------------------------|-----------|
| $V_{REF}$ | Reference Voltage         | 1.5       |
| $V_{IHD}$ | Input High Drive Voltage  | 2.0       |
| $V_{ILD}$ | Input Low Drive Voltage   | 0.8       |
| $V_{OHD}$ | Output High Drive Voltage | 2.4       |
| $V_{OLD}$ | Output Low Drive Voltage  | 0.4       |

All AC tests are at  $V_{IO} = 3.14V$  to  $3.46V$  (3.3V nominal),  $T_C = 0^\circ C$  to  $85^\circ C$ ,  $C_L = 50$  pF, unless otherwise specified.

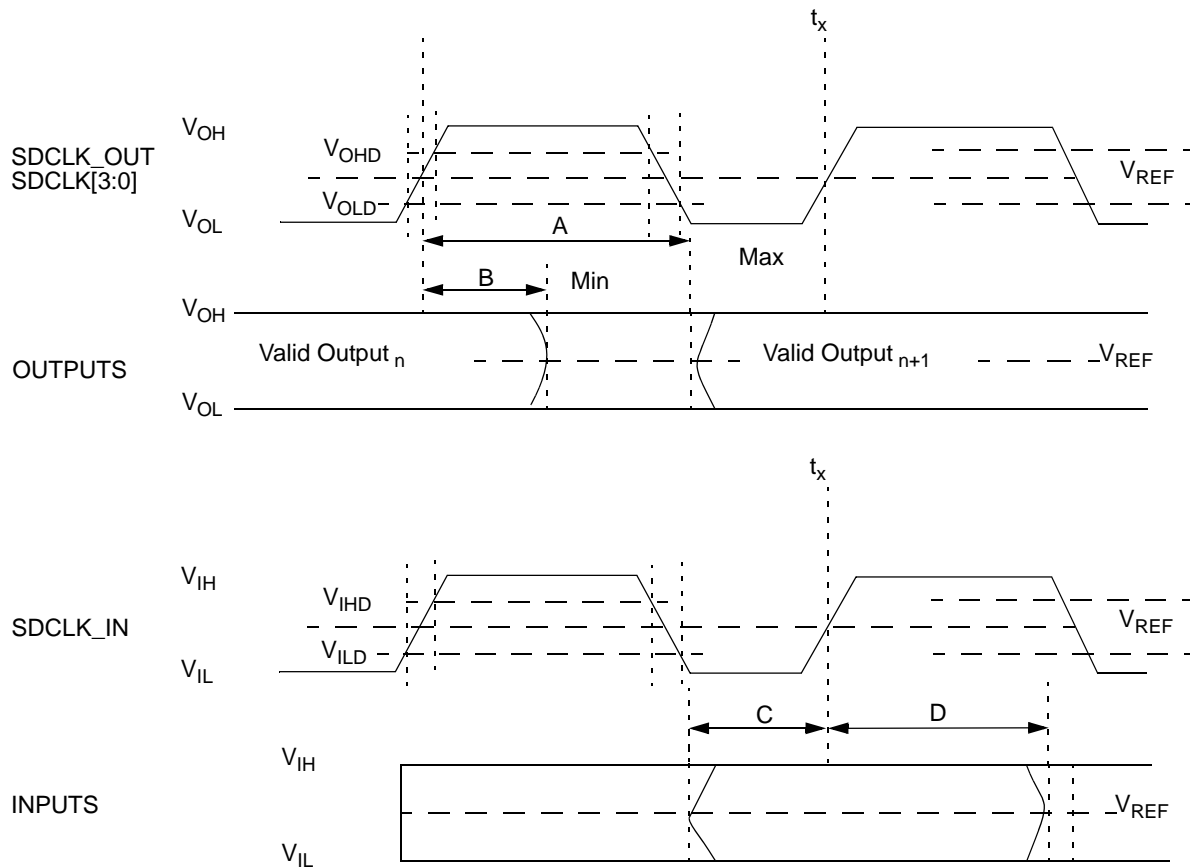


**Legend:** A = Maximum Output or Float Delay Specification  
 B = Minimum Output or Float Delay Specification  
 C = Minimum Input Setup Specification  
 D = Minimum Input Hold Specification

**Figure 9-2. Drive level and Measurement Points**

### 9.3.1 Memory Controller Interface

The minimum input setup and hold times described in Figure 9-3 (legend C and D) define the smallest acceptable sampling window during which a synchronous input signal must be stable to ensure correct operation.



- Legend: A = Maximum Output Delay  
 B = Minimum Output Delay  
 C = Minimum Input Setup  
 D = Minimum Input Hold

**Figure 9-3. Memory Controller Drive Level and Measurement Points**

Table 9-12. Memory Controller Timing Parameters

| Symbol          | Parameter  | Min              | Max             | Unit | Comments       |
|-----------------|--|------------------|-----------------|------|----------------|
| t <sub>1</sub>  | Control output valid from SDCLK[3:0]   | $-3.0 + (x * y)$ | $0.1 + (x * y)$ | ns   | Note 1, Note 2 |
| t <sub>2</sub>  | MA[12:0], BA[1:0] output valid from SDCLK[3:0]                                     | $-3.2 + (x * y)$ | $0.1 + (x * y)$ | ns   | Note 2         |
| t <sub>3</sub>  | MD[63:0] output valid from SDCLK[3:0]  | $-2.2 + (x * y)$ | $0.7 + (x * y)$ | ns   | Note 2         |
| t <sub>4</sub>  | MD[63:0] read data in setup to SDCLK_IN  | 1.3              |                 | ns   |                |
| t <sub>5</sub>  | MD[63:0] read data hold to SDCLK_IN  | 2.0              |                 | ns   |                |
| t <sub>6</sub>  | SDCLK[3:0], SDCLK_OUT cycle time   |                  |                 |      |                |
|                 | 233 MHz  | 10               | 14              | ns   |                |
|                 | 266 MHz  | 8.3              | 13.5            |      |                |
| t <sub>7</sub>  | SDCLK[3:0], SDCLK_OUT fall/rise time between (V <sub>OLD</sub> -V <sub>OHD</sub> ) |                  | 2               | ns   |                |
| t <sub>9</sub>  | SDCLK_IN fall/rise time between (V <sub>ILD</sub> -V <sub>IHD</sub> )              |                  | 2               | ns   |                |
| t <sub>10</sub> | SDCLK[3:0], SDCLK_OUT high time  |                  |                 |      |                |
|                 | 233 MHz  | 4.0              |                 | ns   |                |
|                 | 266 MHz  | 3.0              |                 |      |                |
| t <sub>11</sub> | SDCLK[3:0], SDCLK_OUT low time   |                  |                 |      |                |
|                 | 233 MHz  | 4.0              |                 | ns   |                |
|                 | 266 MHz  | 2.5              |                 |      |                |

Note 1. Control output includes all the following signals: RASA#, CASA#, WEA#, CKEA, DQM[7:0], and CS[1:0]#. Load = 50 pF, V<sub>CORE</sub> = 1.8V@ 233/266 MHz, V<sub>IO</sub> = 3.3V, @25°C.

Note 2. Use the Min/Max equations [value+(x \* y)] to calculate the actual output value.

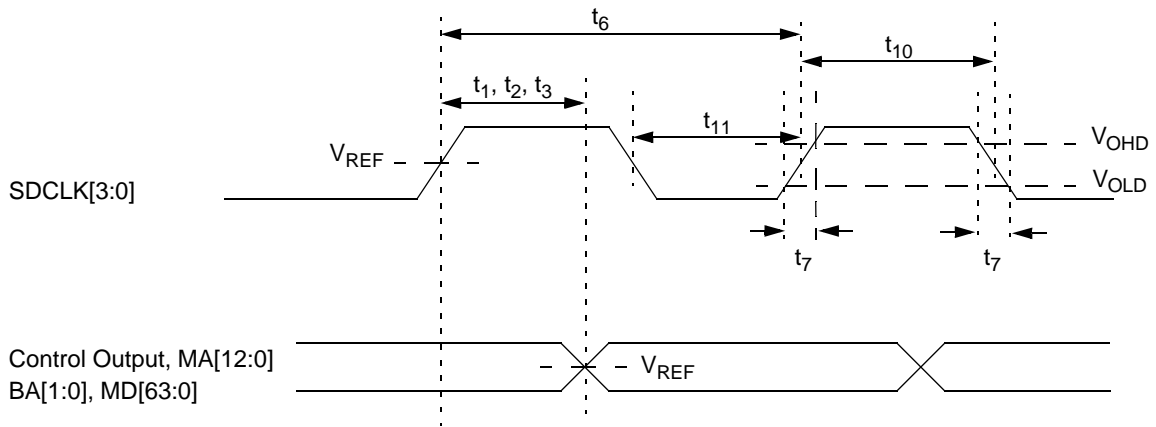
x is the shift value which is applied to the SHFTSDCLK field, and y is 0.45 the core clock period.

Note that the SHFTSDCLK field = GX\_BASE+Memory Offset 8404h[5:3]. Refer to the *AMD Geode™ GX1 Processor Data Book* for more information.

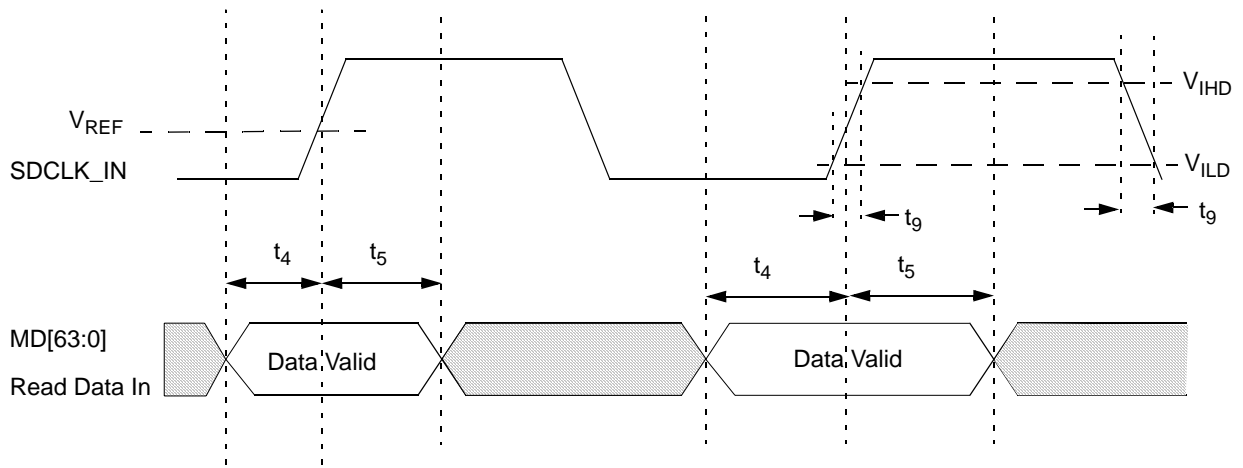
For example, for a 266 MHz SC3200 running a 88.7 MHz SDRAM clock, with a shift value of 3:

t<sub>1</sub> Min =  $-3 + (3 * (3.76 * 0.45)) = 2.08$  ns

t<sub>1</sub> Max =  $0.1 + (3 * (3.76 * 0.45)) = 5.18$  ns



**Figure 9-4. Memory Controller Output Valid Timing Diagram**



**Figure 9-5. Read Data In Setup and Hold Timing Diagram**

9.3.2 Video Port

Table 9-13. Video Input Port Timing Parameters

| Symbol         | Parameter   | Min   | Max | Unit | Comments |
|----------------|---|-------|-----|------|----------|
| $t_{VP\_C}$    | VPCKIN cycle time                                     | 18    |     | ns   |          |
| $t_{VP\_S}$    | Video Port input setup time before VPCKIN rising edge | 6     |     | ns   |          |
| $t_{VP\_H}$    | Video Port input hold time after VPCKIN rising edge   | 0     |     | ns   |          |
| $t_{VPCK\_FR}$ | VPCKIN fall/rise time                                 | -     | 2   | ns   | Note 1   |
| $t_{VPCK\_D}$  | VPCKIN duty cycle                                     | 35/65 |     | %    |          |

Note 1. Guaranteed by characterization.

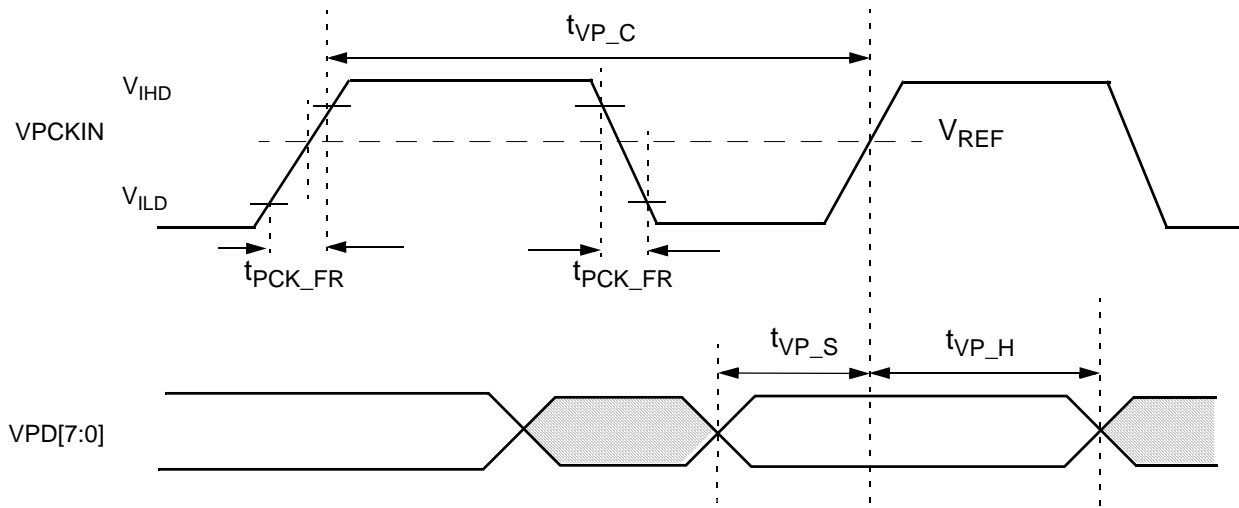


Figure 9-6. Video Input Port Timing Diagram



9.3.3 TFT Interface

Table 9-14. TFT Timing Parameters

| Symbol        | Parameter  | Min   | Max | Unit | Comments |
|---------------|--|-------|-----|------|----------|
| $t_{OV}$      | TFTD[17:0], TFTDE valid time after TFTDCK rising edge (multiplexed on IDE)           | 0     | 8   | ns   |          |
| $t_{OV}$      | TFTD[17:0], TFTDE valid time after TFTDCK rising edge (multiplexed on Parallel Port) | 0     | 4   | ns   |          |
| $t_{CLK\_RF}$ | TFTDCK rise/fall time between 0.8V and 2.0V  |       | 3   | ns   | Note 1   |
| $t_{CLK\_P}$  | TFTDCK period time (multiplexed on IDE)  | 25    |     | ns   |          |
| $t_{CLK\_P}$  | TFTDCK period time (multiplexed on Parallel Port)                                    | 12.5  |     | ns   |          |
| $t_{CLK\_D}$  | TFTDCK duty cycle  | 40/60 |     | %    |          |

Note 1. Guaranteed by characterization

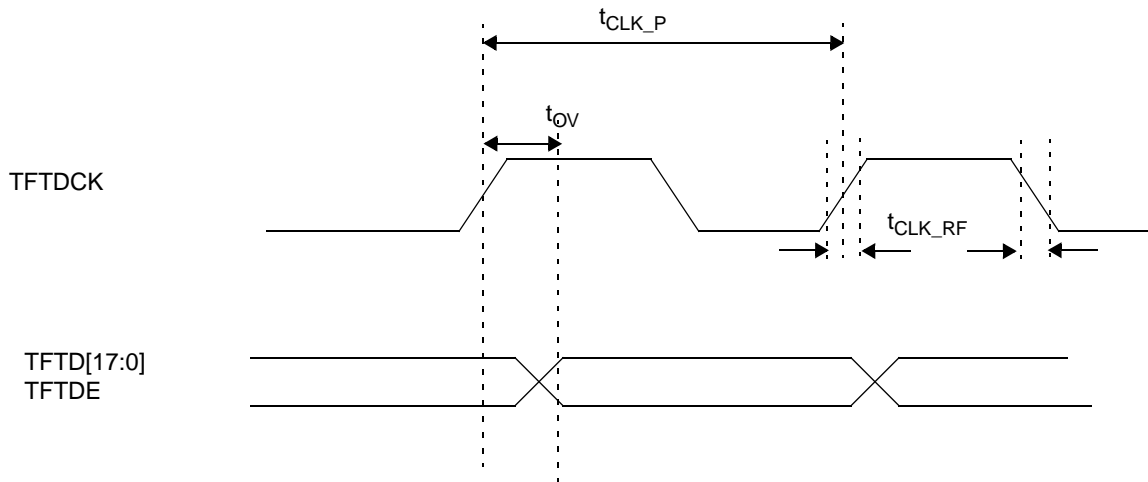


Figure 9-7. TFT Timing Diagram

### 9.3.4 ACCESS.bus Interface

The following tables describe the timing for the ACCESS.bus signals.

**Notes:** 1) All ACCESS.bus timing is not 100% tested.

2) In this table  $t_{CLK} = 1/24\text{MHz} = 41.7 \text{ ns}$ .

**Table 9-15. ACCESS.bus Input Timing Parameters**

| Symbol         | Parameter                                      | Min                           | Max | Unit          | Comments                     |
|----------------|--|-------------------------------|-----|---------------|------------------------------|
| $t_{BUFi}$     | Bus free time between Stop and Start condition | $t_{SCLhigho}$                |     |               |                              |
| $t_{CSTOsi}$   | AB1C/AB2C setup time                           | $8 \cdot t_{CLK} - t_{SCLri}$ |     |               | Before Stop condition        |
| $t_{CSTRhi}$   | AB1C/AB2C hold time                            | $8 \cdot t_{CLK} - t_{SCLri}$ |     |               | After Start condition        |
| $t_{CSTRsi}$   | AB1C/AB2C setup time                           | $8 \cdot t_{CLK} - t_{SCLri}$ |     |               | Before Start condition       |
| $t_{DHCsi}$    | Data high setup time                           | $2 \cdot t_{CLK}$             |     |               | Before AB1C/AB2C rising edge |
| $t_{DLCsi}$    | Data low setup time                            | $2 \cdot t_{CLK}$             |     |               | Before AB1C/AB2C rising edge |
| $t_{SCLfi}$    | AB1D/AB2D fall time                            |                               | 300 | ns            |                              |
| $t_{SCLri}$    | AB1D/AB2D rise time                            |                               | 1   | $\mu\text{s}$ |                              |
| $t_{SCLlowi}$  | AB1C/AB2C low time                             | $16 \cdot t_{CLK}$            |     |               | After AB1C/AB2C falling edge |
| $t_{SCLhighi}$ | AB1C/AB2C high time                            | $16 \cdot t_{CLK}$            |     |               | After AB1C/AB2C rising edge  |
| $t_{SDAfi}$    | AB1D/AB2D fall time                            |                               | 300 | ns            |                              |
| $t_{SDAri}$    | AB1D/AB2D rise time                            |                               | 1   | $\mu\text{s}$ |                              |
| $t_{SDAhi}$    | AB1D/AB2D hold time                            | 0                             |     |               | After AB1C/AB2C falling edge |
| $t_{SDAsi}$    | AB1D/AB2D setup time                           | $2 \cdot t_{CLK}$             |     |               | Before AB1C/AB2C rising edge |

**Table 9-16. ACCESS.bus Output Timing Parameters**

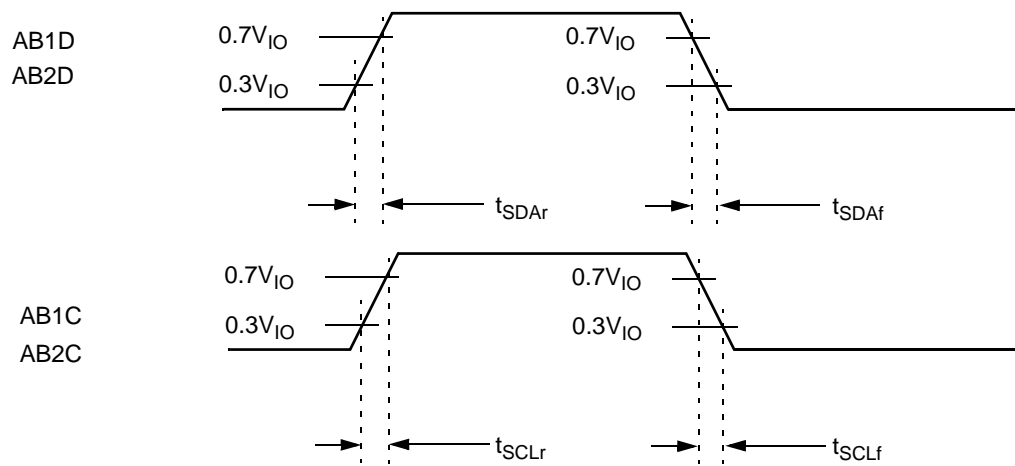
| Symbol         | Parameter                                      | Min                               | Max | Unit          | Comments                             |
|----------------|--|-----------------------------------|-----|---------------|--------------------------------------|
| $t_{SCLhigho}$ | AB1C/AB2C high time                            | $K \cdot t_{CLK} - 1 \mu\text{s}$ |     |               | After AB1C/AB2C rising edge, Note 1  |
| $t_{SCLlowo}$  | AB1C/AB2C low time                             | $K \cdot t_{CLK} - 1 \mu\text{s}$ |     |               | After AB1C/AB2C falling edge         |
| $t_{BUFo}$     | Bus free time between Stop and Start condition | $t_{SCLhigho}$                    | 1   | $\mu\text{s}$ | Note 2                               |
| $t_{CSTOso}$   | AB1C/AB2C setup time                           | $t_{SCLhigho}$                    | 1   | $\mu\text{s}$ | Before Stop condition, Note 2        |
| $t_{CSTRho}$   | AB1C/AB2C hold time                            | $t_{SCLhigho}$                    | 1   | $\mu\text{s}$ | After Start condition, Note 2        |
| $t_{CSTRso}$   | AB1C/AB2C setup time                           | $t_{SCLhigho}$                    | 1   | $\mu\text{s}$ | Before Start condition, Note 2       |
| $t_{DHCso}$    | Data high setup time                           | $t_{SCLhigho} - t_{SDAro}$        | 1   | $\mu\text{s}$ | Before AB1C/AB2C rising edge, Note 2 |
| $t_{DLCso}$    | Data low setup time                            | $t_{SCLhigho} - t_{SDAfo}$        | 1   | $\mu\text{s}$ | Before AB1C/AB2C rising edge, Note 2 |
| $t_{SCLfo}$    | AB1D/AB2D signal fall time                     |                                   | 300 | ns            |                                      |
| $t_{SCLro}$    | AB1D/AB2D signal rise time                     |                                   | 1   | $\mu\text{s}$ |                                      |

**Table 9-16. ACCESS.bus Output Timing Parameters (Continued)**

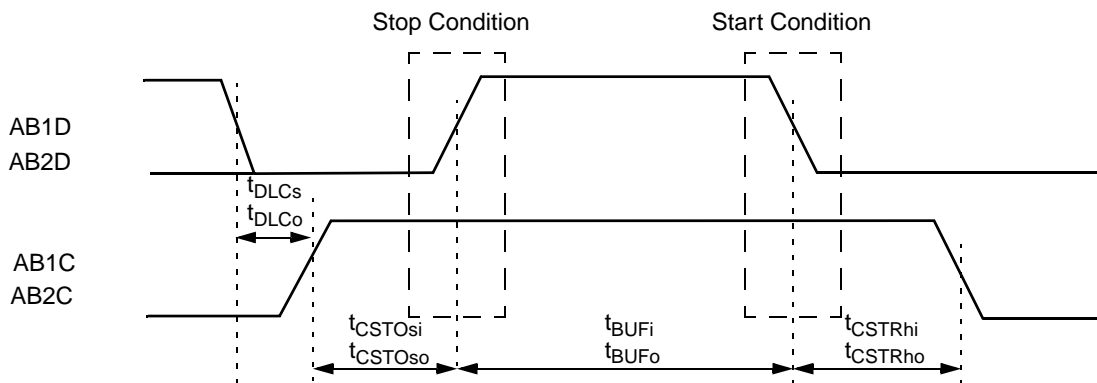
| Symbol      | Parameter                  | Min                       | Max                    | Unit    | Comments                     |
|-------------|----------------------------|---------------------------|------------------------|---------|------------------------------|
| $t_{SDAfo}$ | AB1D/AB2D signal fall time |                           | 300                    | ns      |                              |
| $t_{SDAro}$ | AB1D/AB2D signal rise time |                           | 1                      | $\mu$ s |                              |
| $t_{SDAho}$ | AB1D/AB2D hold time        | $7 * t_{CLK} - t_{SCLfo}$ |                        |         | After AB1C/AB2C falling edge |
| $t_{SDAvo}$ | AB1D/AB2D valid time       |                           | $7 * t_{CLK} + t_{RD}$ |         | After AB1C/AB2C falling edge |

Note 1. K is determined by bits [7:1] of the ACBCTL2 register (LDN 05h/06h, Offset 05h).

Note 2.  $t_{SCLhigho}$  value depends on the signal capacitance and the pull-up value of the relevant pin.



**Figure 9-8. ACB Signals: Rising Time and Falling Timing Diagram**



**Figure 9-9. ACB Start and Stop Condition Timing Diagram**

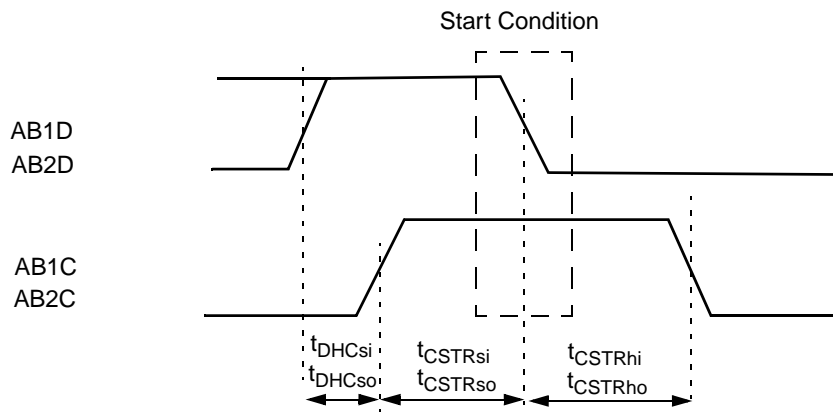


Figure 9-10. ACB Start Condition Timing Diagram

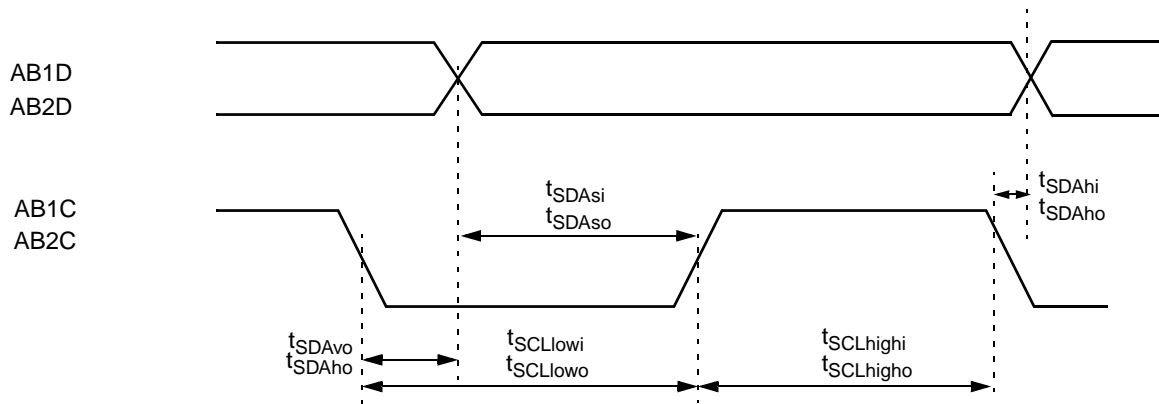


Figure 9-11. ACB Data Bit Timing Diagram

### 9.3.5 PCI Bus Interface

The SC3200 is compliant with PCI Bus Rev. 2.1 specifications. Relevant information from the PCI Bus specifications is provided below.

All parameters in Table 9-17 are not 100% tested. The parameters in this table are further described in Figure 9-13.

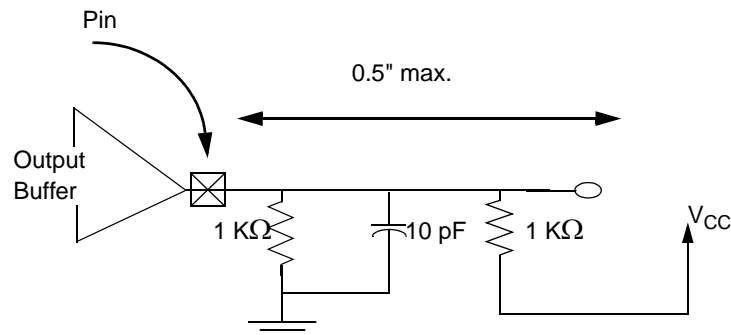
**Table 9-17. PCI AC Specifications**

| Symbol                           | Parameter              | Min  | Max                         | Unit | Comments   |
|----------------------------------|------------------------|--|-----------------------------|------|--|
| I <sub>OH</sub> (AC)<br>(Note 1) | Switching current high | -12V <sub>IO</sub>                             |                             | mA   | 0 < V <sub>OUT</sub> ≤ 0.3V <sub>IO</sub> ,                |
|                                  |                        | -17.1(V <sub>IO</sub> -V <sub>OUT</sub> )      |                             | mA   | 0.3V <sub>IO</sub> < V <sub>OUT</sub> < 0.9V <sub>IO</sub> |
|                                  |                        |  | Equation A<br>(Figure 9-13) |      | 0.7V <sub>IO</sub> < V <sub>OUT</sub> < V <sub>IO</sub>    |
|                                  | Test point (Note 2)    |  | -32V <sub>IO</sub>          | mA   | V <sub>OUT</sub> = 0.7V <sub>IO</sub>                      |
| I <sub>OL</sub> (AC)<br>(Note 1) | Switching current low  | 16V <sub>IO</sub>                              |                             | mA   | V <sub>IO</sub> > V <sub>OUT</sub> ≥ 0.6V <sub>IO</sub>    |
|                                  |                        | 26.7V <sub>OUT</sub>                           |                             | mA   | 0.6V <sub>IO</sub> > V <sub>OUT</sub> > 0.1V <sub>IO</sub> |
|                                  |                        |  | Equation B<br>(Figure 9-13) |      | 0.18V <sub>IO</sub> > V <sub>OUT</sub> > 0                 |
|                                  | Test point (Note 2)    |  | 38V <sub>IO</sub>           | mA   | V <sub>OUT</sub> = 0.18V <sub>IO</sub>                     |
| I <sub>CL</sub>                  | Low clamp current      | -25+(V <sub>IN</sub> +1)/0.015                 |                             | mA   | -3 < V <sub>IN</sub> ≤ -1                                  |
| I <sub>CH</sub>                  | High clamp current     | 25+(V <sub>IN</sub> -V <sub>IO</sub> -1)/0.015 |                             | mA   | V <sub>IO</sub> +4 > V <sub>IN</sub> > V <sub>IO</sub> +1  |
| SLEW <sub>R</sub><br>(Note 3)    | Output rise slew rate  | 1  | 4                           | V/ns | 0.2V <sub>IO</sub> - 0.6V <sub>IO</sub> Load               |
| SLEW <sub>F</sub>                | Output fall slew rate  | 1  | 4                           | V/ns | 0.6V <sub>IO</sub> - 0.2V <sub>IO</sub> Load               |

Note 1. Refer to the V/I curves in Figure 9-13. This specification does not apply to PCICLK0, PCICLK1, and PCIRST# which are system outputs.

Note 2. Maximum current requirements are met when drivers pull beyond the first step voltage. Equations which define these maximum values (A and B) are provided with relevant diagrams in Figure 9-13. These maximum values are guaranteed by design.

Note 3. Rise slew rate does not apply to open-drain outputs. This parameter is interpreted as the cumulative edge rate across the specified range, according to the test circuit in Figure 9-12.



**Figure 9-12. Testing Setup for Slew Rate and Minimum Timing**

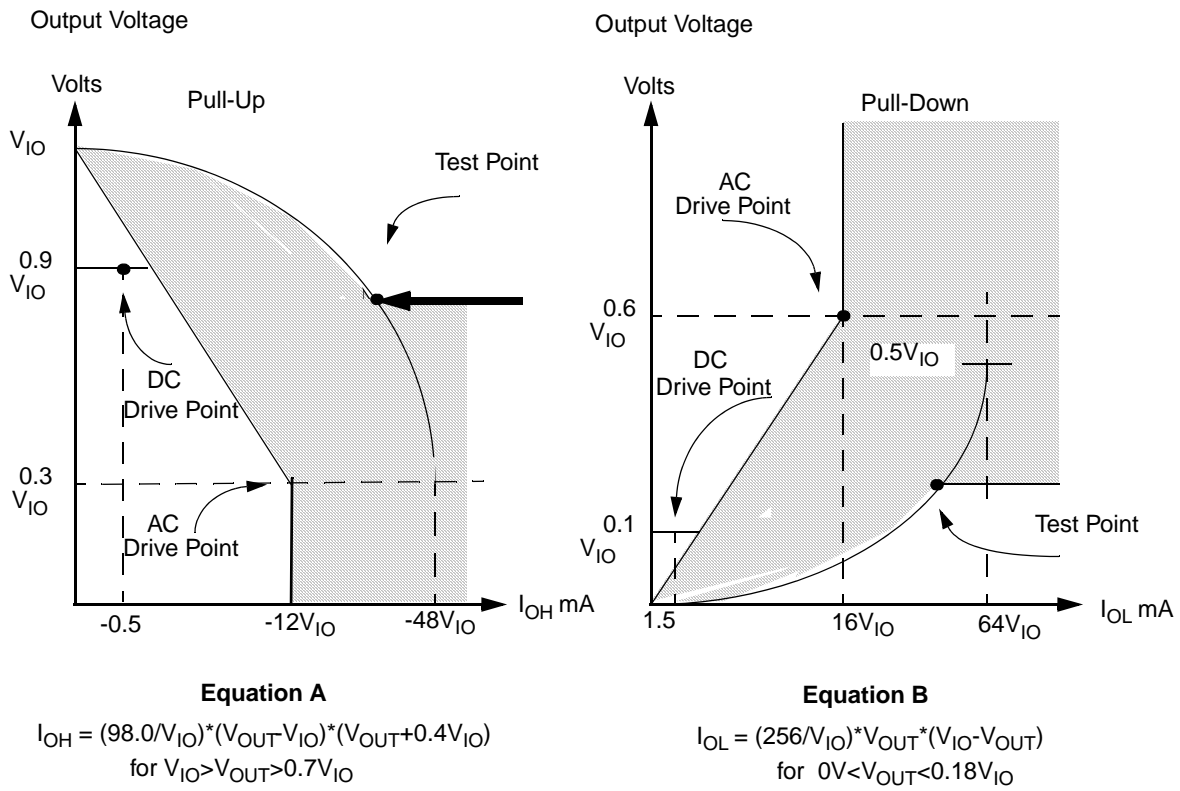


Figure 9-13. V/I Curves for PCI Output Signals

**Table 9-18. PCI Clock Parameters**

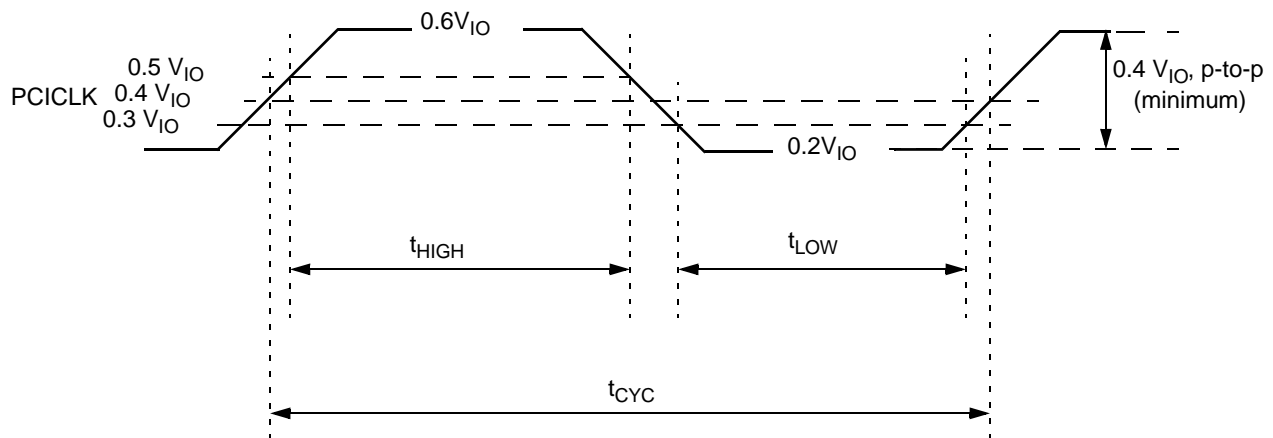
| Symbol        | Parameter         | Min | Max | Unit  | Comments |
|---------------|-------------------|-----|-----|-------|----------|
| $t_{CYC}$     | PCICLK cycle time | 30  |     | ns    | Note 1   |
| $t_{HIGH}$    | PCICLK high time  | 11  |     | ns    | Note 2   |
| $t_{LOW}$     | PCICLK low time   | 11  |     | ns    | Note 2   |
| $PCICLK_{sr}$ | PCICLK slew Rate  | 1   | 4   | V/ns  | Note 3   |
| $PCIRST_{sr}$ | PCIRST# slew Rate | 50  | -   | mV/ns | Note 4   |

Note 1. Clock frequency is between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are not 100% tested. The clock can only be stopped in a low state.

Note 2. Guaranteed by characterization.

Note 3. Slew rate must be met across the minimum peak-to-peak portion of the clock waveform (see Figure 9-14).

Note 4. The minimum PCIRST# slew rate applies only to the rising (de-assertion) edge of the reset signal. See Figure 9-18 for PCIRST# timing.



**Figure 9-14. PCICLK Timing and Measurement Points**

Table 9-19. PCI Timing Parameters

| Symbol         | Parameter                                 | Min | Max | Unit    | Comments                  |
|----------------|---|-----|-----|---------|---------------------------|
| $t_{VAL}$      | PCICLK to signal valid delay (on the bus) | 2   | 11  | ns      | Note 1, Note 2            |
| $t_{VAL}(ptp)$ | PCICLK to signal valid delay (GNT#)       | 2   | 9   | ns      | Note 1, Note 2            |
| $t_{ON}$       | Float to active delay                     | 2   |     | ns      | Note 1, Note 3,           |
| $t_{OFF}$      | Active to float delay                     |     | 28  | ns      | Note 1, Note 3,           |
| $t_{SU}$       | Input setup time to PCICLK (on the bus)   | 7   |     | ns      | Note 4                    |
| $t_{SU}(ptp)$  | Input setup time to PCICLK (REQ#)         | 6   |     | ns      | Note 4                    |
| $t_H$          | Input hold time from PCICLK               | 0   |     | ns      | Note 4                    |
| $t_{RST}$      | PCIRST# active time after power stable    | 1   |     | ms      | Note 3, Note 5            |
| $t_{RST-CLK}$  | PCIRST# active time after PCICLK stable   | 100 |     | $\mu$ s | Note 3, Note 5            |
| $t_{RST-OFF}$  | PCIRST# active to output float delay      |     | 40  | ns      | Note 3, Note 5,<br>Note 6 |

Note 1. See the timing measurement conditions in Figure 9-16.

Note 2. Minimum times are evaluated with same load used for slew rate measurement (as shown in note 3 of Table ); maximum times are evaluated with the load circuits shown in Figure 9-15, for high-going and low-going edges respectively.

Note 3. Not 100% tested.

Note 4. See the timing measurement conditions in Figure 9-17.

Note 5. PCIRST# is asserted and de-asserted asynchronously with respect to PCICLK (see Figure 9-18).

Note 6. All output drivers are asynchronously floated when PCIRST# is active.

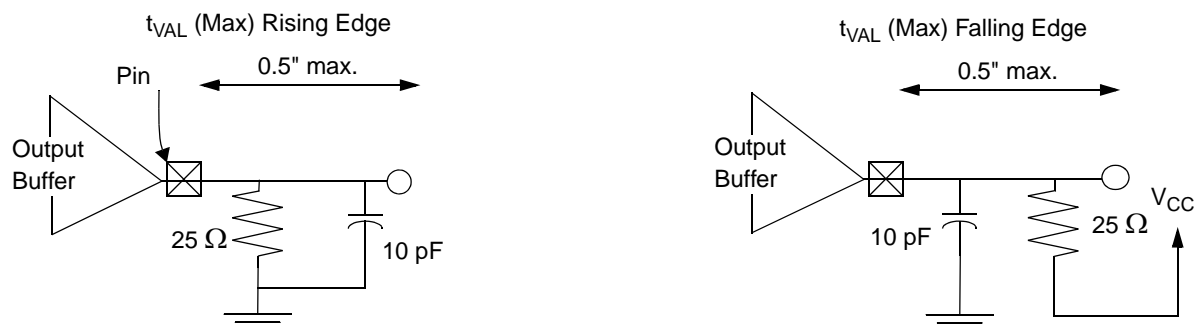


Figure 9-15. Load Circuits for Maximum Time Measurements



9.3.5.1 Measurement and Test Conditions

Table 9-20. Measurement Condition Parameters

| Symbol                    | Value          | Unit | Comments |
|---------------------------|----------------|------|----------|
| $V_{TH}$                  | $0.6 V_{IO}$   | V    | Note 1   |
| $V_{TL}$                  | $0.2 V_{IO}$   | V    | Note 1   |
| $V_{TEST}$                | $0.4 V_{IO}$   | V    |          |
| $V_{STEP}$ (rising edge)  | $0.285 V_{IO}$ | V    |          |
| $V_{STEP}$ (falling edge) | $0.615 V_{IO}$ | V    |          |
| $V_{MAX}$                 | $0.4 V_{IO}$   | V    | Note 2   |
| Input signal edge rate    | 1              | V/ns |          |

Note 1. The input test is performed with  $0.1 V_{IO}$  of overdrive. Timing parameters must not exceed this overdrive.

Note 2.  $V_{MAX}$  specifies the maximum peak-to-peak waveform allowed for measuring input timing.

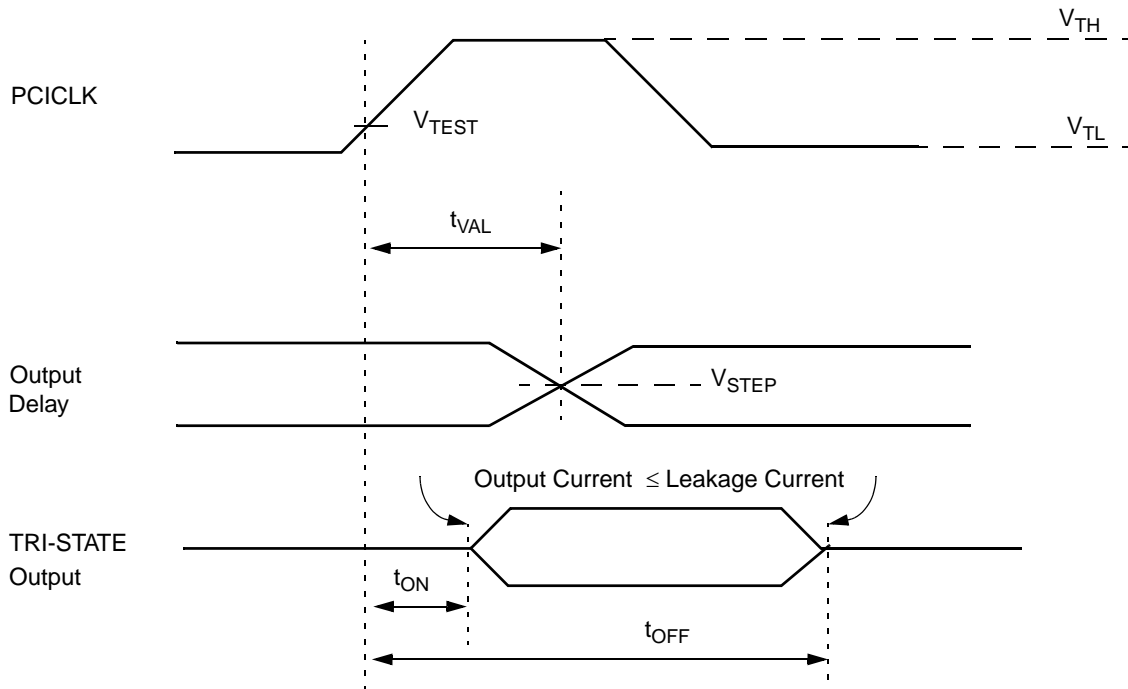


Figure 9-16. Output Timing Measurement Conditions

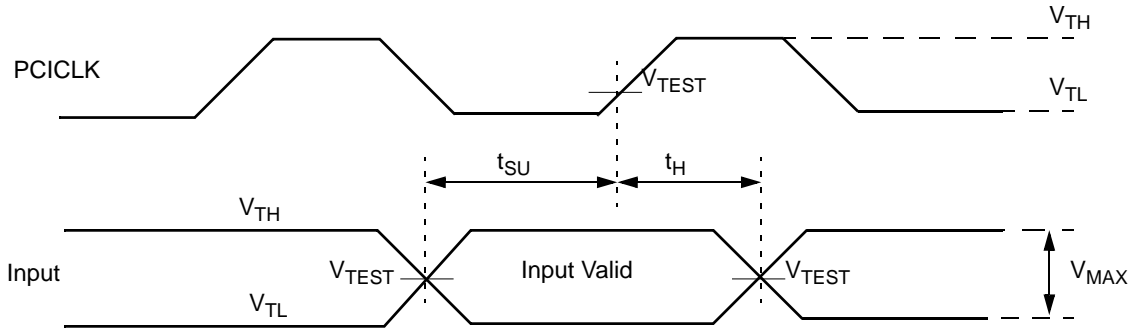
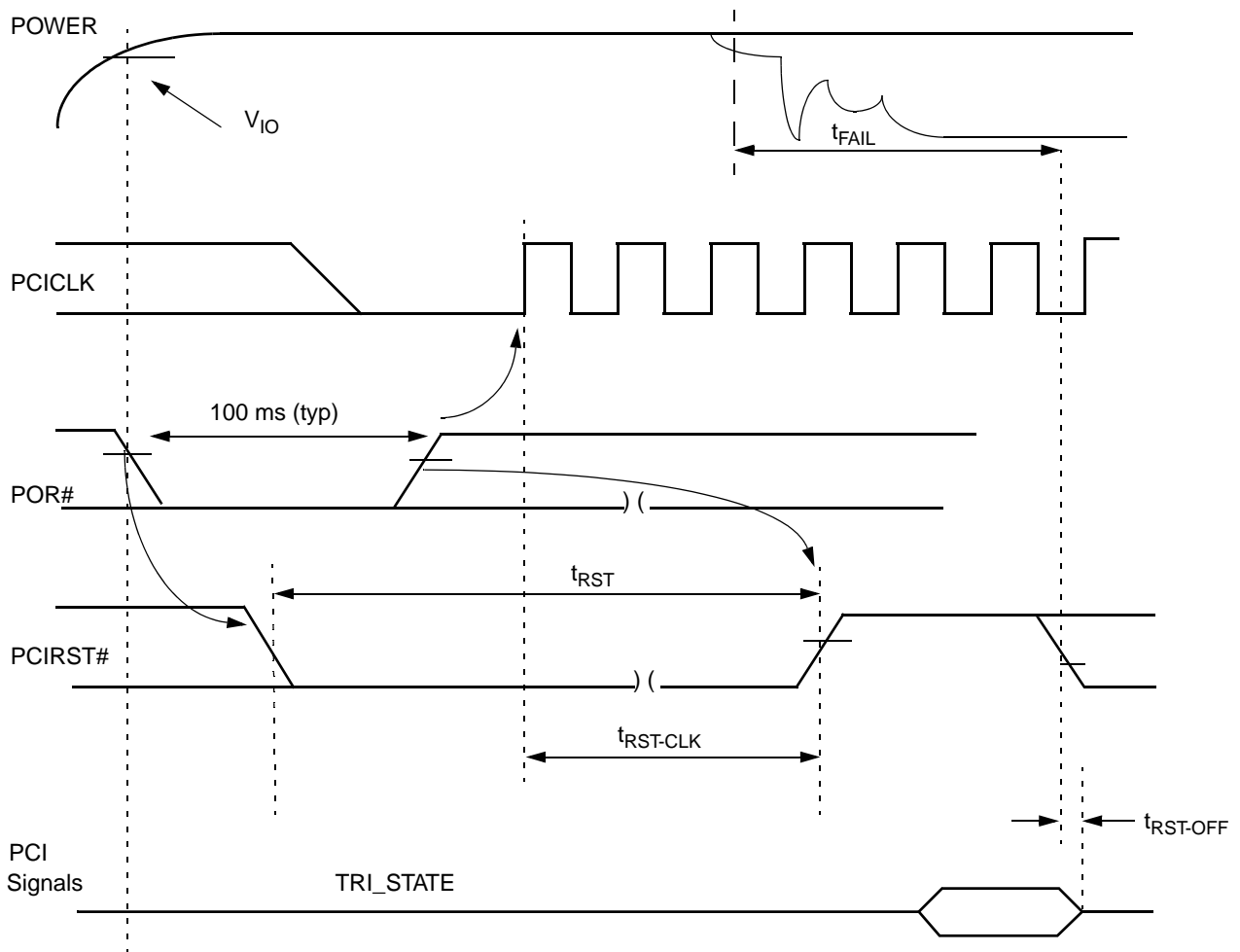


Figure 9-17. Input Timing Measurement Conditions



**Note:** The value of  $t_{FAIL}$  is 500 ns (maximum) from the power rail which exceeds specified tolerance by more than 500 mV.

Figure 9-18. PCI Reset Timing

### 9.3.6 Sub-ISA Interface

All output timing is guaranteed for 50 pF load, unless otherwise specified.

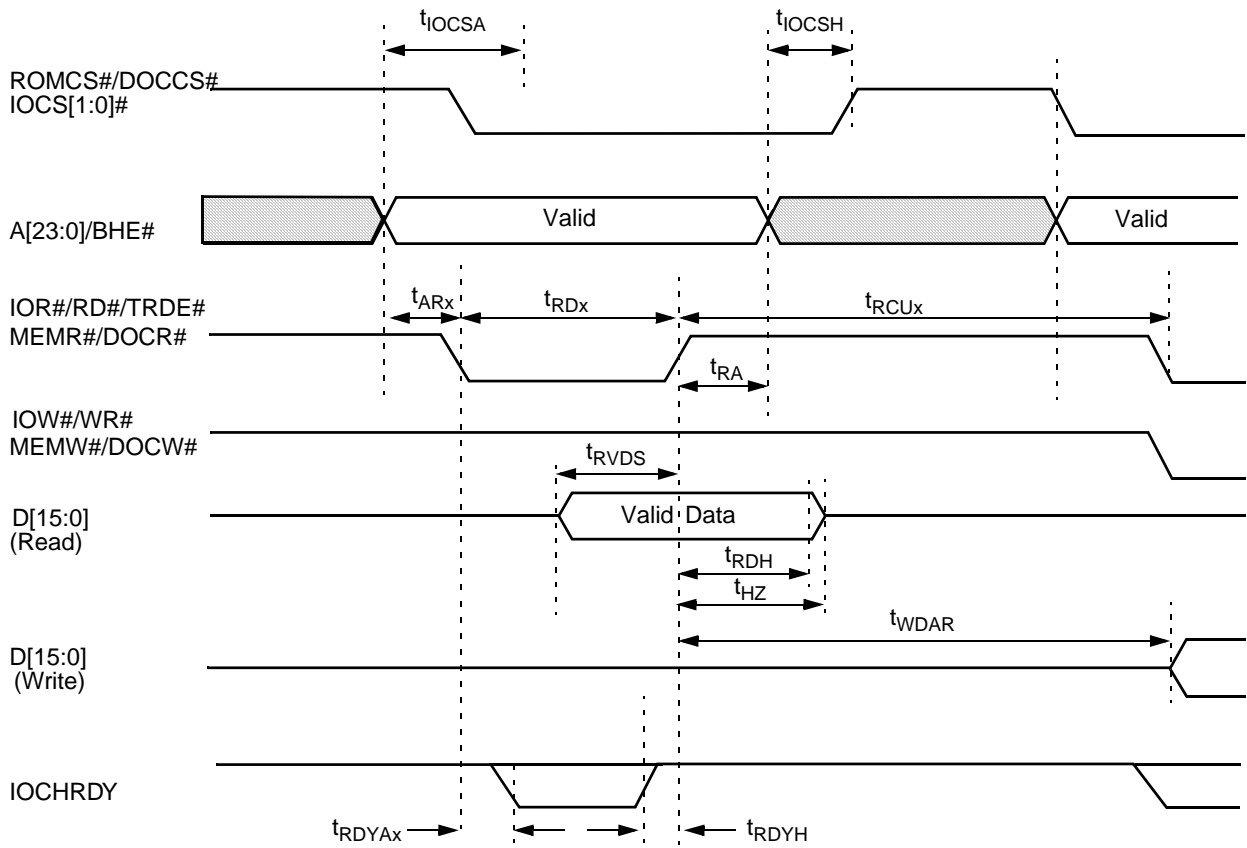
The ISA Clock divisor (defined in F0 Index 50h[2:0] of the Core Logic module) is 011.

**Table 9-21. Sub-ISA Timing Parameters**

| Symbol             | Parameter  | Bus Width (Bits) | Type   | Min (ns) | Max (ns) | Figure       | Comments        |
|--------------------|--|------------------|--------|----------|----------|--------------|-----------------|
| t <sub>RD1</sub>   | MEMR#/DOCR#/RD#/TRDE# read active pulse width FE to RE           | 16               | M      | 225      |          | 9-19         | Standard        |
| t <sub>RD2</sub>   | MEMR#/DOCR#/RD#/TRDE# read active pulse width FE to RE           | 16               | M      | 105      |          | 9-19         | Zero wait state |
| t <sub>RD3</sub>   | IOR#/RD#/TRDE# read active pulse width FE to RE                  | 16               | I/O    | 160      |          | 9-19         | Standard        |
| t <sub>RD4</sub>   | IOR#/MEMR#/DOCR#/RD#/TRDE# read active pulse width FE to RE      | 8                | M, I/O | 520      |          | 9-19         | Standard        |
| t <sub>RD5</sub>   | IOR#/MEMR#/DOCR#/RD#/TRDE# read active pulse width FE to RE      | 8                | M, I/O | 160      |          | 9-19         | Zero wait state |
| t <sub>RCU1</sub>  | MEMR#/DOCR#/RD#/TRDE# inactive pulse width                       | 16               | M      | 103      |          | 9-19         |                 |
| t <sub>RCU2</sub>  | MEMR#/DOCR#/RD#/TRDE# inactive pulse width                       | 8                | M      | 163      |          | 9-19         |                 |
| t <sub>RCU3</sub>  | IOR#/RD#/TRDE# inactive pulse width                              | 8, 16            | I/O    | 163      |          | 9-19         |                 |
| t <sub>WR1</sub>   | MEMW#/WR# write active pulse width FE to RE                      | 16               | M      | 225      |          | 9-20         | Standard        |
| t <sub>WR2</sub>   | MEMW#/DOCW#/WR# write active pulse width FE to RE                | 16               | M      | 105      |          | 9-20         | Zero wait state |
| t <sub>WR3</sub>   | IOW#/WR# write active pulse width FE to RE                       | 16               | I/O    | 160      |          | 9-20         | Standard        |
| t <sub>WR4</sub>   | IOW#/MEMW#/DOCW#/WR# write active pulse width FE to RE           | 8                | M, I/O | 520      |          | 9-20         | Standard        |
| t <sub>WR5</sub>   | IOW#/MEMW#/DOCW#/WR# write active pulse width FE to RE           | 8                | M, I/O | 160      |          | 9-20         | Zero wait state |
| t <sub>WCU1</sub>  | MEMW#/WR#/DOCW# inactive pulse width                             | 16               | M      | 103      |          | 9-20         |                 |
| t <sub>WCU2</sub>  | MEMW#/WR#/DOCW# inactive pulse width                             | 8                | M      | 163      |          | 9-20         |                 |
| t <sub>WCU3</sub>  | IOW#/WR# inactive pulse width                                    | 8, 16            | I/O    | 163      |          | 9-20         |                 |
| t <sub>RDYH</sub>  | IOR#/MEMR#/RD#/DOCR#/IOW#/MEMW#/WR#/DOCW# hold after IOCHRDY RE  | 8, 16            | M, I/O | 120      |          | 9-19<br>9-20 |                 |
| t <sub>RDYA1</sub> | IOCHRDY valid after IOR#/MEMR#/RD#/DOCR#/IOW#/MEMW#/WR#/DOCW# FE | 16               | M, I/O |          | 78       | 9-19<br>9-20 |                 |

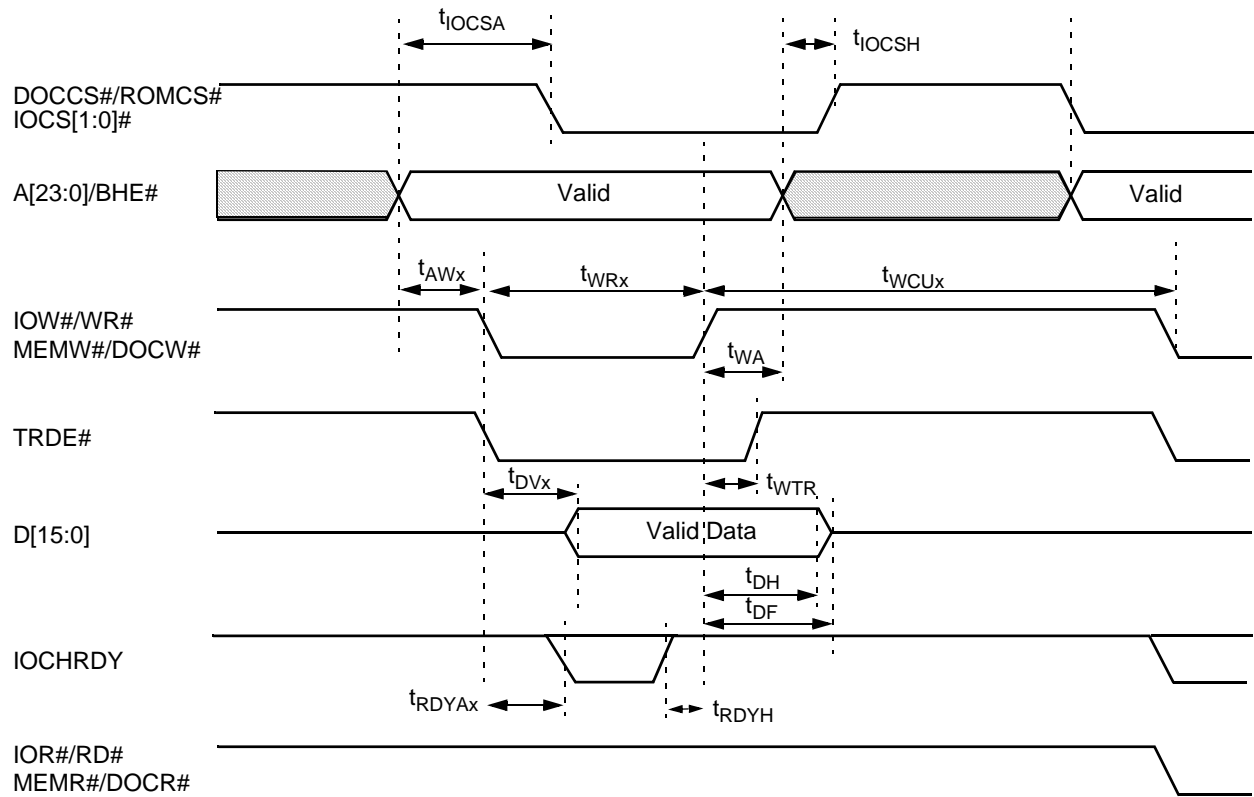
Table 9-21. Sub-ISA Timing Parameters (Continued)

| Symbol             | Parameter   | Bus Width (Bits) | Type   | Min (ns) | Max (ns) | Figure       | Comments |
|--------------------|---|------------------|--------|----------|----------|--------------|----------|
| t <sub>RDYA2</sub> | IOCHRDY valid after IOR#/MEMR#/RD#/DOCR#/IOW#/MEMW#/WR#/DOCW# FE  | 8                | M, I/O |          | 366      | 9-19<br>9-20 |          |
| t <sub>IOCSA</sub> | IOCS[1:0]#/DOCS#/ROMCS# driven active from A[23:0] valid          | 8, 16            | M, I/O |          | 34       | 9-19<br>9-20 |          |
| t <sub>IOCSH</sub> | IOCS[1:0]#/DOCS#/ROMCS# valid hold after A[23:0] invalid          | 8, 16            | M, I/O | 0        |          | 9-19<br>9-20 |          |
| t <sub>AR1</sub>   | A[23:0]/BHE# valid before MEMR#/DOCR# active                      | 16               | M      | 34       |          | 9-19         |          |
| t <sub>AR2</sub>   | A[23:0]/BHE# valid before IOR# active                             | 16               | I/O    | 100      |          | 9-19         |          |
| t <sub>AR3</sub>   | A[23:0]/BHE# valid before MEMR#/DOCR#/IOR# active                 | 8                | M, I/O | 100      |          | 9-19         |          |
| t <sub>RA</sub>    | A[23:0]/BHE# valid hold after MEMR#/DOCR#/IOR# inactive           | 8, 16            | M, I/O | 25       |          | 9-19         |          |
| t <sub>RVDS</sub>  | Read data D[15:0] valid setup before MEMR#/DOCR#/IOR# inactive    | 8, 16            | M, I/O | 24       |          | 9-19         |          |
| t <sub>RDH</sub>   | Read data D[15:0] valid hold after MEMR#/DOCR#/IOR# inactive      | 8, 16            | M, I/O | 0        |          | 9-19         |          |
| t <sub>HZ</sub>    | Read data floating after MEMR#/DOCR#/IOR# inactive                | 8, 16            | M, I/O |          | 41       | 9-19         |          |
| t <sub>AW1</sub>   | A[23:0]/BHE# valid before MEMW#/DOCW# active                      | 16               | M      | 34       |          | 9-20         |          |
| t <sub>AW2</sub>   | A[23:0]/BHE# valid before IOW# active                             | 16               | I/O    | 100      |          | 9-20         |          |
| t <sub>AW3</sub>   | A[23:0]/BHE# valid before MEMW#/DOCW#/IOW# active                 | 8                | M, I/O | 100      |          | 9-20         |          |
| t <sub>WA</sub>    | A[23:0]/BHE# valid hold after MEMW#/DOCW#/IOW# invalid            | 8, 16            | M, I/O | 25       |          | 9-20         |          |
| t <sub>DV1</sub>   | Write data D[15:0] valid after MEMW#/DOCW# active                 | 8, 16            | M      | 40       |          | 9-20         |          |
| t <sub>DV2</sub>   | Write data D[15:0] valid after IOW# active                        | 8                | I/O    | 40       |          | 9-20         |          |
| t <sub>DV3</sub>   | Write data D[15:0] valid after IOW# active                        | 16               | I/O    | -23      |          | 9-20         |          |
| t <sub>WTR</sub>   | TRDE# inactive after MEMW#/DOCW#/IOW# inactive                    | 8, 16            | M, I/O | 20       |          | 9-20         |          |
| t <sub>DH</sub>    | Write data D[15:0] after MEMW#/DOCW#/IOW# inactive                | 8, 16            | M, I/O | 45       |          | 9-20         |          |
| t <sub>DF</sub>    | Write data D[15:0] goes TRI-STATE after MEMW#/DOCW#/IOW# inactive | 8, 16            | M, I/O |          | 105      | 9-20         |          |
| t <sub>WDAR</sub>  | Write data D[15:0] after read MEMR#/DOCR#/IOR#                    | 8, 16            | M, I/O | 41       |          | 9-19         |          |



**Note:** x indicates a numeric index for the relevant symbol.

**Figure 9-19. Sub-ISA Read Operation Timing Diagram**



**Note:** x indicates a numeric index for the relevant symbol.

**Figure 9-20. Sub-ISA Write Operation Timing Diagram**

9.3.7 LPC Interface

Table 9-22. LPC and SERIRQ Timing Parameters

| Symbol    | Parameter             | Min | Max | Unit | Comments                  |
|-----------|-----------------------|-----|-----|------|---------------------------|
| $t_{VAL}$ | Output Valid delay    | 0   | 17  | ns   | After PCICLK rising edge  |
| $t_{ON}$  | Float to Active delay | 2   |     | ns   | After PCICLK rising edge  |
| $t_{OFF}$ | Active to Float delay |     | 28  | ns   | After PCICLK rising edge  |
| $t_{SU}$  | Input Setup time      | 7   |     | ns   | Before PCICLK rising edge |
| $t_{HI}$  | Input Hold time       | 0   |     | ns   | After PCICLK rising edge  |

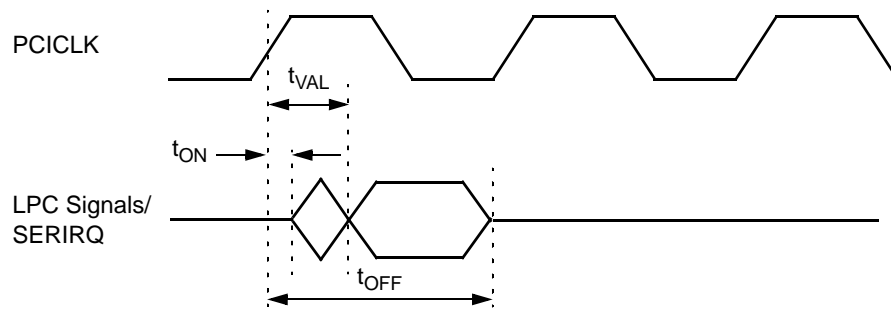


Figure 9-21. LPC Output Timing Diagram

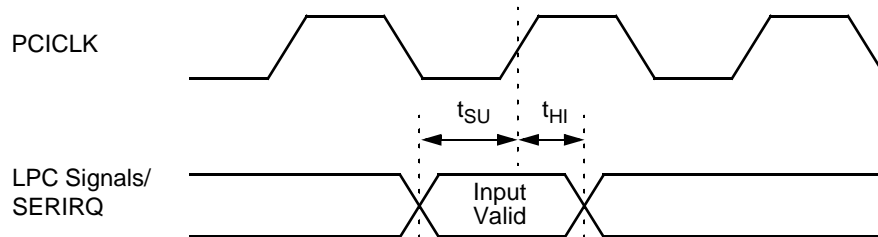


Figure 9-22. LPC Input Timing Diagram

## 9.3.8 IDE Interface

Table 9-23. IDE General Timing Parameters

| Symbol                    | Parameter  | Min | Max | Unit          | Comments              |
|---------------------------|--|-----|-----|---------------|-----------------------|
| $t_{\text{IDE\_FALL}}$    | IDE signals fall time (from $0.9V_{\text{IO}}$ to $0.1V_{\text{IO}}$ ) | 5   |     | ns            | $C_L = 40 \text{ pF}$ |
| $t_{\text{IDE\_RISE}}$    | IDE signals rise time (from $0.1V_{\text{IO}}$ to $0.9V_{\text{IO}}$ ) | 5   |     | ns            | $C_L = 40 \text{ pF}$ |
| $t_{\text{IDE\_RST\_PW}}$ | IDE_RST# pulse width   | 25  |     | $\mu\text{s}$ |                       |

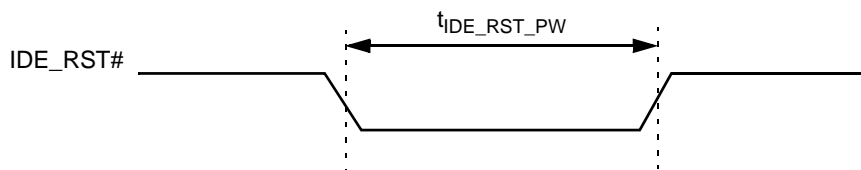


Figure 9-23. IDE Reset Timing Diagram



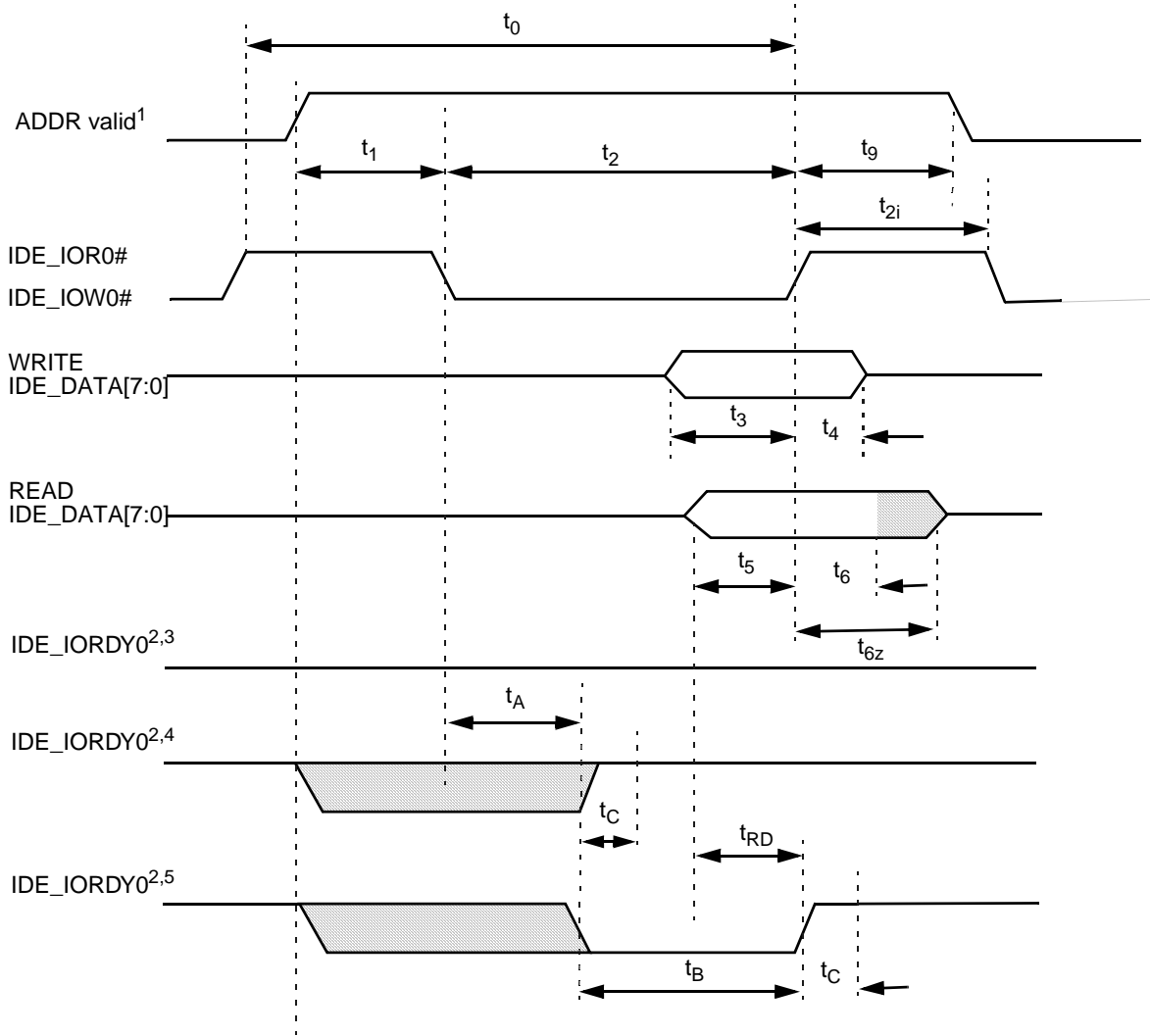
Table 9-24. IDE Register Transfer to/from Device Timing Parameters

| Symbol   | Parameter  | Mode |      |      |      |      | Unit | Comments |
|----------|--|------|------|------|------|------|------|----------|
|          |  | 0    | 1    | 2    | 3    | 5    |      |          |
| $t_0$    | Cycle time (min)   | 600  | 383  | 240  | 180  | 120  | ns   | Note 1   |
| $t_1$    | Address valid to IDE_IOR[0:1]#/IDE_IOW[0:1]# setup (min)                                     | 70   | 50   | 30   | 30   | 25   | ns   |          |
| $t_2$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# pulse width 8-bit (min)  | 290  | 290  | 290  | 80   | 70   | ns   | Note 1   |
| $t_{2i}$ | IDE_IOR[0:1]#/IDE_IOW[0:1]# recovery time (min)  | -    | -    | -    | 70   | 25   | ns   | Note 1   |
| $t_3$    | IDE_IOW[0:1]# data setup (min)   | 60   | 45   | 30   | 30   | 20   | ns   |          |
| $t_4$    | IDE_IOW[0:1]# data hold (min)  | 30   | 20   | 15   | 10   | 10   | ns   |          |
| $t_5$    | IDE_IOR[0:1]# data setup (min)   | 50   | 35   | 20   | 20   | 20   | ns   |          |
| $t_6$    | IDE_IOR[0:1]# data hold (min)  | 5    | 5    | 5    | 5    | 5    | ns   |          |
| $t_{6Z}$ | IDE_IOR[0:1]# data TRI-STATE (max)   | 30   | 30   | 30   | 30   | 30   | ns   | Note 2   |
| $t_9$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# to address valid hold (min)                                      | 20   | 15   | 10   | 10   | 10   | ns   |          |
| $t_{RD}$ | Read data valid to IDE_IORDY[0:1] active (if IDE_IORDY[0:1] initially low after $t_A$ (min)) | 0    | 0    | 0    | 0    | 0    | ns   |          |
| $t_A$    | IDE_IORDY[0:1] setup time  | 35   | 35   | 35   | 35   | 35   | ns   | Note 3   |
| $t_B$    | IDE_IORDY[0:1] pulse width (max)   | 1250 | 1250 | 1250 | 1250 | 1250 | ns   |          |
| $t_C$    | IDE_IORDY[0:1] assertion to release (max)  | 5    | 5    | 5    | 5    | 5    | ns   |          |

Note 1.  $t_0$  is the minimum total cycle time,  $t_2$  is the minimum command active time, and  $t_{2i}$  is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the command active time and the command inactive time. The three timing requirements of  $t_0$ ,  $t_2$ , and  $t_{2i}$  are met. The minimum total cycle time requirements is greater than the sum of  $t_2$  and  $t_{2i}$ . (This means that a host implementation can lengthen  $t_2$  and/or  $t_{2i}$  to ensure that  $t_0$  is equal to or greater than the value reported in the device's IDENTIFY DEVICE data.)

Note 2. This parameter specifies the time from the rising edge of IDE\_IOR[0:1]# to the time that the data bus is no longer driven by the device (TRI-STATE).

Note 3. The delay from the activation of IDE\_IOR[0:1]# or IDE\_IOW[0:1]# until the state of IDE\_IORDY[0,1] is first sampled. If IDE\_IORDY[0:1] is inactive, then the host waits until IDE\_IORDY[0:1] is active before the PIO cycle is completed. If the device is not driving IDE\_IORDY[0:1] negated after activation ( $t_A$ ) of IDE\_IOR[0:1]# or IDE\_IOW[0:1]#, then  $t_5$  is met and  $t_{RD}$  is not applicable. If the device is driving IDE\_IORDY[0:1] negated after activation ( $t_A$ ) of IDE\_IOR[0:1]# or IDE\_IOW[0:1]#, then  $t_{RD}$  is met and  $t_5$  is not applicable.



**Notes:**

- 1) Device address consists of signals IDE\_CS[0:1]# and IDE\_ADDR[2:0].
- 2) Negation of IDE\_IORDY0,1 is used to extend the PIO cycle. The determination of whether or not the cycle is to be extended is made by the host after  $t_A$  from the assertion of IDE\_IOR[0:1]# or IDE\_IOW[0:1]#.
- 3) Device never negates IDE\_IORDY[0:1]. Device keeps IDE\_IORDY[0:1] released, and no wait is generated.
- 4) Device negates IDE\_IORDY[0:1] before  $t_A$  but causes IDE\_IORDY[0:1] to be asserted before  $t_A$ . IDE\_IORDY[0:1] is released, and no wait is generated.
- 5) Device negates IDE\_IORDY[0:1] before  $t_A$ . IDE\_IORDY[0:1] is released prior to negation and may be asserted for no more than 5 ns before release. A wait is generated.
- 6) The cycle completes after IDE\_IORDY[0:1] is reasserted. For cycles where a wait is generated and IDE\_IOR[0:1] is asserted, the device places read data on IDE\_DATA[15:0] for  $t_{RD}$  before asserting IDE\_IORDY[0:1].

**Figure 9-24. Register Transfer to/from Device Timing Diagram**

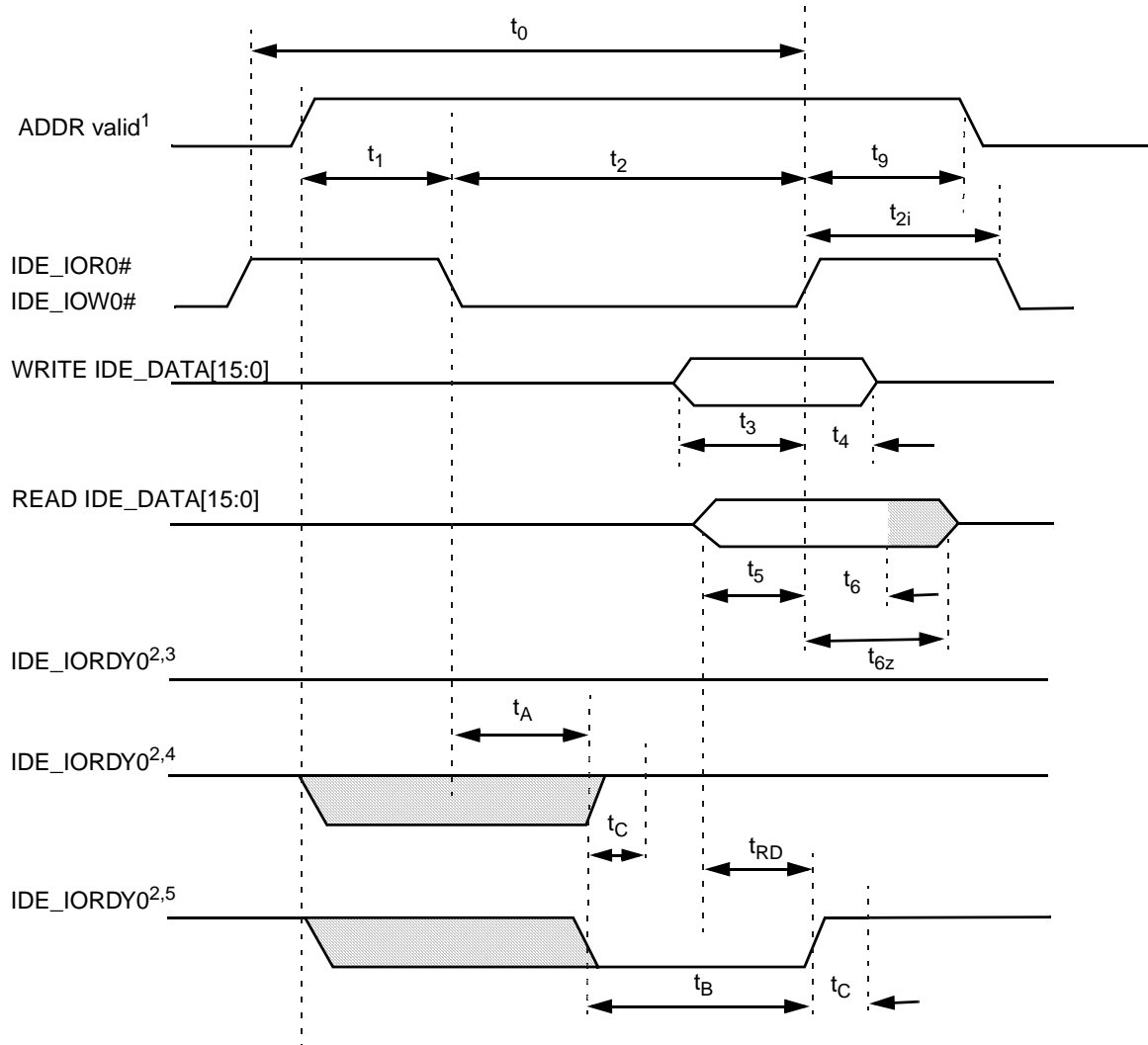
Table 9-25. IDE PIO Data Transfer to/from Device Timing Parameters

| Symbol   | Parameter   | Mode |      |      |      |      | Unit | Comments |
|----------|---|------|------|------|------|------|------|----------|
|          |   | 0    | 1    | 2    | 3    | 4    |      |          |
| $t_0$    | Cycle time (min)  | 600  | 383  | 240  | 180  | 120  | ns   | Note 1   |
| $t_1$    | Address valid to IDE_IOR[0:1]#/IDE_IOW[0:1]# setup (min)                                      | 70   | 50   | 30   | 30   | 25   | ns   |          |
| $t_2$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# 16-bit (min)  | 165  | 125  | 100  | 80   | 70   | ns   | Note 1   |
| $t_{2i}$ | IDE_IOR[0:1]#/IDE_IOW[0:1]# recovery time (min)   | -    | -    | -    | 70   | 25   | ns   | Note 1   |
| $t_3$    | IDE_IOW[0:1]# data setup (min)  | 60   | 45   | 30   | 30   | 20   | ns   |          |
| $t_4$    | IDE_IOW[0:1]# data hold (min)   | 30   | 20   | 15   | 10   | 10   | ns   |          |
| $t_5$    | IDE_IOR[0:1]# data setup (min)  | 50   | 35   | 20   | 20   | 20   | ns   |          |
| $t_6$    | IDE_IOR[0:1]# data hold (min)   | 5    | 5    | 5    | 5    | 5    | ns   |          |
| $t_{6Z}$ | IDE_IOR[0:1]# data TRI-STATE (max)  | 30   | 30   | 30   | 30   | 30   | ns   | Note 2   |
| $t_9$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# to address valid hold (min)                                       | 20   | 15   | 10   | 10   | 10   | ns   |          |
| $t_{RD}$ | Read Data Valid to IDE_IORDY[0,1] active (if IDE_IORDY[0:1] initially low after $t_A$ ) (min) | 0    | 0    | 0    | 0    | 0    | ns   |          |
| $t_A$    | IDE_IORDY[0:1] Setup time   | 35   | 35   | 35   | 35   | 35   | ns   | Note 3   |
| $t_B$    | IDE_IORDY[0:1] Pulse Width (max)  | 1250 | 1250 | 1250 | 1250 | 1250 | ns   |          |
| $t_C$    | IDE_IORDY[0:1] assertion to release (max)   | 5    | 5    | 5    | 5    | 5    | ns   |          |

Note 1.  $t_0$  is the minimum total cycle time,  $t_2$  is the minimum command active time, and  $t_{2i}$  is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the command active time and the command inactive time. The three timing requirements of  $t_0$ ,  $t_2$ , and  $t_{2i}$  are met. The minimum total cycle time requirement is greater than the sum of  $t_2$  and  $t_{2i}$ . (This means that a host implementation may lengthen  $t_2$  and/or  $t_{2i}$  to ensure that  $t_0$  is equal to or greater than the value reported in the device's IDENTIFY DEVICE data.)

Note 2. This parameter specifies the time from the rising edge of IDE\_IOR[0:1]# to the time that the data bus is no longer driven by the device (TRI-STATE).

Note 3. The delay from the activation of IDE\_IOR[0:1]# or IDE\_IOW[0:1]# until the state of IDE\_IORDY[0:1] is first sampled. If IDE\_IORDY[0:1] is inactive, then the host waits until IDE\_IORDY[0:1] is active before the PIO cycle is completed. If the device is not driving IDE\_IORDY[0:1] negated after the activation ( $t_A$ ) of IDE\_IOR[0:1]# or IDE\_IOW[0:1]#, then  $t_5$  is met and  $t_{RD}$  is not applicable. If the device is driving IDE\_IORDY[0:1] negated after the activation ( $t_A$ ) of IDE\_IOR[0:1]# or IDE\_IOW[0:1]#, then  $t_{RD}$  is met and  $t_5$  is not applicable.

**Notes:**

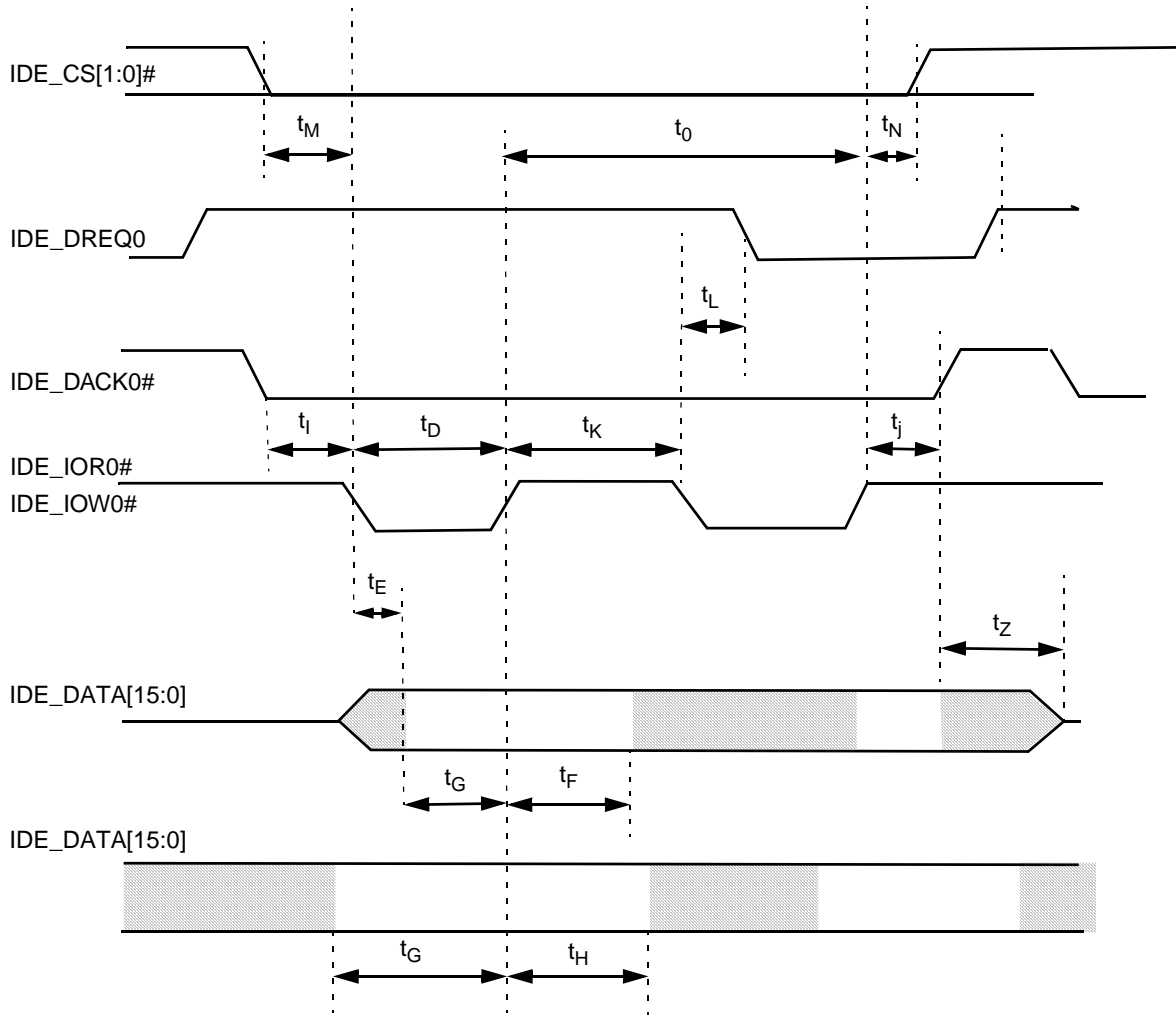
- 1) Device address consists of signals  $\bar{\text{IDE\_CS}}[0:1]\#$  and  $\text{IDE\_ADDR}[2:0]$ .
- 2) Negation of  $\text{IDE\_IORDY}[0:1]$  is used to extend the PIO cycle. The determination of whether or not the cycle is to be extended is made by the host after  $t_A$  from the assertion of  $\text{IDE\_IOR}[0:1]\#$  or  $\text{IDE\_IOW}[0:1]\#$ .
- 3) Device never negates  $\text{IDE\_IORDY}[0:1]$ . Devices keep  $\text{IDE\_IORDY}[0:1]$  released, and no wait is generated.
- 4) Device negates  $\text{IDE\_IORDY}[0:1]$  before  $t_A$  but causes  $\text{IDE\_IORDY}[0:1]$  to be asserted before  $t_A$ .  $\text{IDE\_IORDY}[0:1]$  is released, and no wait is generated.
- 5) Device negates  $\text{IDE\_IORDY}[0:1]$  before  $t_A$ .  $\text{IDE\_IORDY}[0:1]$  is released prior to negation and may be asserted for no more than 5 ns before release. A wait is generated.
- 6) The cycle completes after  $\text{IDE\_IORDY}[0:1]$  is reasserted. For cycles where a wait is generated and  $\text{IDE\_IOR}[0:1]\#$  is asserted, the device places read data on  $\text{IDE\_DATA}[15:0]$  for  $t_{RD}$  before asserting  $\text{IDE\_IORDY}[0:1]$ .

**Figure 9-25. PIO Data Transfer to/from Device Timing Diagram**

Table 9-26. IDE Multiword DMA Data Transfer Timing Parameters

| Symbol   | Parameter   | Mode |     |     | Unit | Comments |
|----------|---|------|-----|-----|------|----------|
|          |   | 0    | 1   | 2   |      |          |
| $t_0$    | Cycle time (min)  | 480  | 150 | 120 | ns   | Note 1   |
| $t_D$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# (min)                         | 215  | 80  | 70  | ns   |          |
| $t_E$    | IDE_IOR[0:1]# data access (max)                           | 150  | 60  | 50  | ns   |          |
| $t_F$    | IDE_IOR[0:1]# data hold (min)                             | 5    | 5   | 5   | ns   |          |
| $t_G$    | IDE_IOW[0:1]#/IDE_IOW[0:1]# data setup (min)              | 100  | 30  | 20  | ns   |          |
| $t_H$    | IDE_IOW[0:1]# data hold (min)                             | 20   | 15  | 10  | ns   |          |
| $t_I$    | IDE_DACK[0:1]# to IDE_IOR[0:1]#/IDE_IOW[0:1]# setup (min) | 0    | 0   | 0   | ns   |          |
| $t_J$    | IDE_IOR[0:1]#/IDE_IOW[0:1]# to IDE_DACK[0:1]# hold (min)  | 20   | 5   | 5   | ns   |          |
| $t_{KR}$ | IDE_IOR[0:1]# negated pulse width (min)                   | 50   | 50  | 25  | ns   |          |
| $t_{KW}$ | IDE_IOW[0:1]# negated pulse width (min)                   | 215  | 50  | 25  | ns   |          |
| $t_{LR}$ | IDE_IOR[0:1]# to IDE_DREQ[0:1] delay (max)                | 120  | 40  | 35  | ns   |          |
| $t_{LW}$ | IDE_IOW[0:1]# to IDE_DREQ0,1 delay (max)                  | 40   | 40  | 35  | ns   |          |
| $t_M$    | IDE_CS[0:1]# valid to IDE_IOR[0:1]#/IDE_IOW[0:1]# (min)   | 50   | 30  | 25  | ns   |          |
| $t_N$    | IDE_CS[0:1]# hold   | 15   | 10  | 10  | ns   |          |
| $t_Z$    | IDE_DACK[0:1]# to TRI-STATE                               | 20   | 25  | 25  | ns   |          |

Note 1.  $t_0$  is the minimum total cycle time,  $t_D$  is the minimum command active time, and  $t_{KR}$  or  $t_{KW}$  is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the command active time and the command inactive time. The three timing requirements of  $t_0$ ,  $t_D$  and  $t_{KR/KW}$ , are met. The minimum total cycle time requirement  $t_0$  is greater than the sum of  $t_D$  and  $t_{KR/KW}$ . (This means that a host implementation can lengthen  $t_D$  and/or  $t_{KR/KW}$  to ensure that  $t_0$  is equal to or greater than the value reported in the device's IDENTIFY DEVICE data.)



**Notes:**

- 1) For Multiword DMA transfers, the Device may negate IDE\_DREQ[0:1] within the  $t_L$  specified time once IDE\_DACK[0:1] is asserted, and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave IDE\_DREQ[0:1] asserted and wait for the host to reassert IDE\_DACK[0:1]#.
- 2) This signal can be negated by the host to Suspend the DMA transfer in process.

**Figure 9-26. Multiword DMA Data Transfer Timing Diagram**

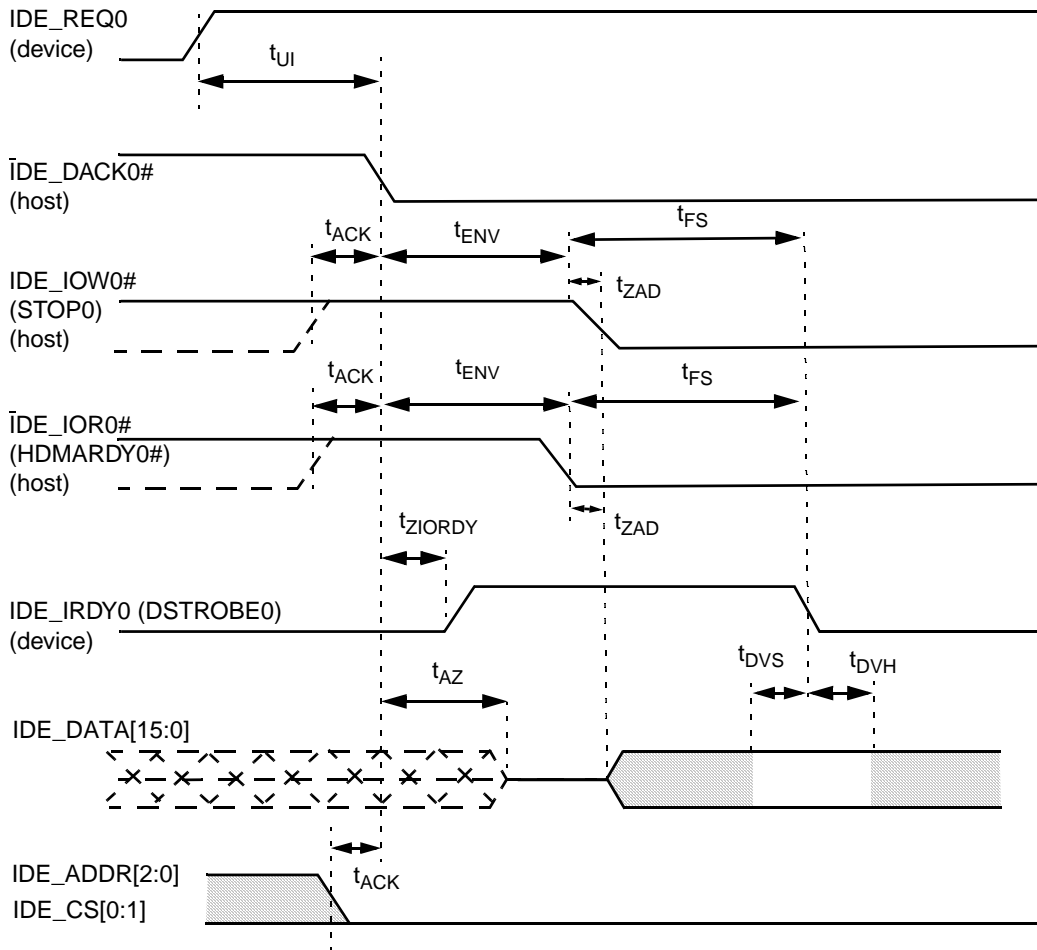
Table 9-27. IDE UltraDMA Data Burst Timing Parameters

| Symbol       | Parameter  | Mode 0 |     | Mode 1 |     | Mode 2 |     | Unit | Comments |
|--------------|--|--------|-----|--------|-----|--------|-----|------|----------|
|              |  | Min    | Max | Min    | Max | Min    | Max |      |          |
| $t_{2CYC}$   | Typical sustained average two cycle time   | 240    |     | 160    |     | 120    |     | ns   |          |
|              | Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)        | 235    |     | 156    |     | 117    |     | ns   |          |
| $t_{CYC}$    | Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)   | 114    |     | 75     |     | 55     |     | ns   |          |
| $t_{DS}$     | Data setup time (at recipient)   | 15     |     | 10     |     | 7      |     | ns   |          |
| $t_{DH}$     | Data hold time (at recipient)  | 5      |     | 5      |     | 5      |     | ns   |          |
| $t_{DVS}$    | Data valid setup time at sender (from data bus being valid until STROBE edge)  | 70     |     | 48     |     | 34     |     | ns   |          |
| $t_{DVH}$    | Data valid hold time at sender (from STROBE edge until data may become invalid)  | 6      |     | 6      |     | 6      |     | ns   |          |
| $t_{FS}$     | First STROBE time (for device to first negate IDE_IRDY[0:1] (DSTROBE[0:1]) from IDE_IOW[0:1]# (STOP[0:1]) during a data in burst)              | 0      | 230 | 0      | 200 | 0      | 170 | ns   |          |
| $t_{LI}$     | Limited interlock time   | 0      | 150 | 0      | 150 | 0      | 150 | ns   | Note 1   |
| $t_{MLI}$    | Interlock time with minimum  | 20     |     | 20     |     | 20     |     | ns   | Note 1   |
| $t_{UI}$     | Unlimited interlock time   | 0      |     | 0      |     | 0      |     | ns   | Note 1   |
| $t_{AZ}$     | Maximum time allowed for output drivers to release (from being asserted or negated)  |        | 10  |        | 10  |        | 10  | ns   |          |
| $t_{ZAH}$    | Minimum delay time required for output drivers to assert or negate (from released state)   | 20     |     | 20     |     | 20     |     | ns   |          |
| $t_{ZAD}$    |  | 0      |     | 0      |     | 0      |     | ns   |          |
| $t_{ENV}$    | Envelope time (from IDE_DACK[0:1]# to IDE_IOW[0:1]# (STOP[0:1]) and IDE_IOR[0:1]# (HDMARDY[0:1]#) during data out burst initiation)            | 20     | 70  | 20     | 70  | 20     | 70  | ns   |          |
| $t_{SR}$     | STROBE to DMARDY time (if DMARDY# is negated before this long after STROBE edge, the recipient receives no more than one additional data WORD) |        | 50  |        | 30  |        | 20  | ns   |          |
| $t_{RFS}$    | Ready-to-final-STROBE time (no STROBE edges are sent this long after negation of DMARDY#)  |        | 75  |        | 60  |        | 50  | ns   |          |
| $t_{RP}$     | Ready-to-pause time (time that recipient waits to initiate pause after negating DMARDY#)   | 160    |     | 125    |     | 100    |     | ns   |          |
| $t_{IORDYZ}$ | Pull-up time before allowing IDE_IORDY[0:1] to be released   |        | 20  |        | 20  |        | 20  | ns   |          |
| $t_{ZIORDY}$ | Minimum time device waits before driving IDE_IORDY[0:1]  | 0      |     | 0      |     | 0      |     | ns   |          |
| $t_{ACK}$    | Setup and hold times for IDE_DACK[0:1]# (before assertion or negation)   | 20     |     | 20     |     | 20     |     | ns   |          |
| $t_{SS}$     | Time from STROBE edge to negation of IDE_DREQ[0:1] or assertion of IDE_IOW[0:1]# (STOP[0:1]) (when sender terminates a burst)                  | 50     |     | 50     |     | 50     |     | ns   |          |

Note 1.  $t_{UI}$ ,  $t_{MLI}$ , and  $t_{LI}$  indicate sender-to-recipient or recipient-to-sender interlocks, that is, one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.  $t_{UI}$  is an unlimited interlock with no maximum time value.  $t_{MLI}$  is a limited timeout with a defined minimum.  $t_{LI}$  is a limited time-out with a defined maximum.

All timing parameters are measured at the connector of the device to which the parameter applies. For example, the sender stops generating STROBE edges  $t_{RFS}$  after the

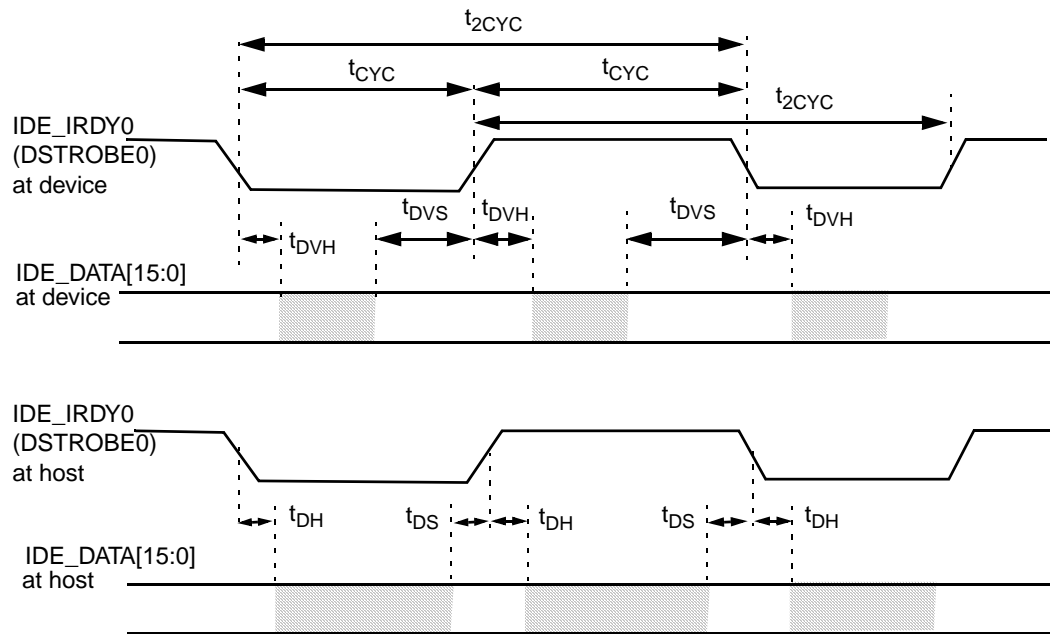
negation of DMARDY. Both STROBE and DMARDY timing measurements are taken at the connector of the sender.



**Note:** The definitions for the IDE\_IOW[0:1]# (STOP[0:1]), IDE\_IOR[0:1]# (HDMARDY[0:1]#) and IDE\_IRDY[0:1] (DSTROBE[0:1]) signal lines are not in effect until IDE\_REQ[0:1] and IDE\_DACK[0:1]# are asserted.

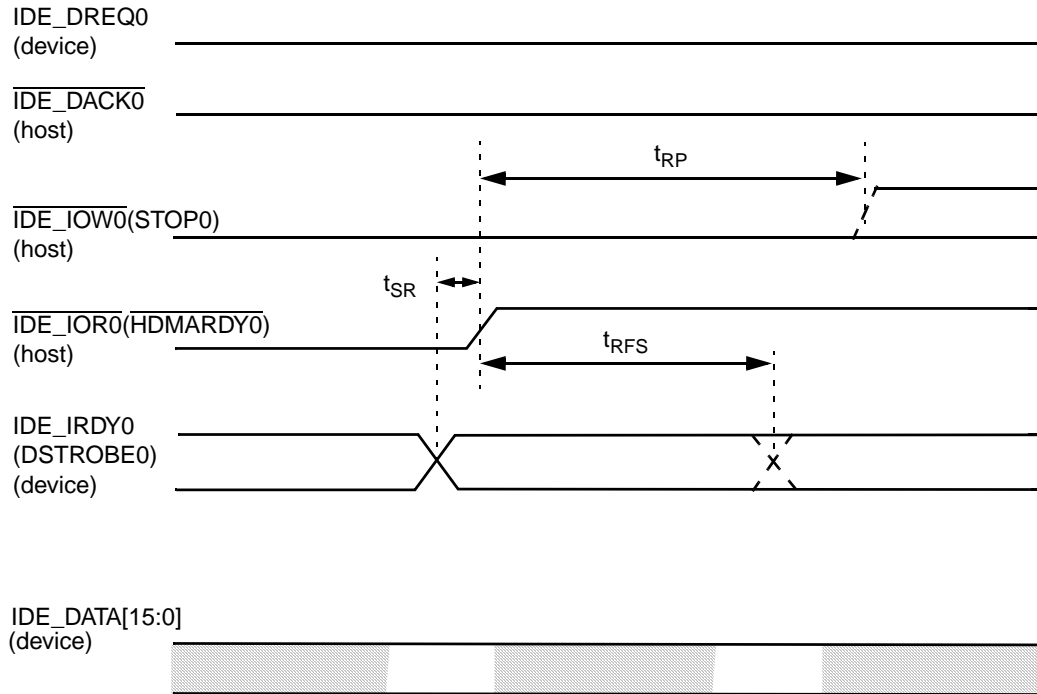
Figure 9-27. Initiating an UltraDMA Data in Burst Timing Diagram





**Note:** IDE\_DATA[15:0] and IDE\_IRDY[0:1] (DSTROBE[0:1]) signals are shown at both the host and the device to emphasize that cable settling time and cable propagation delay do not allow the data signals to be considered stable at the host until a certain amount of time after they are driven by the device.

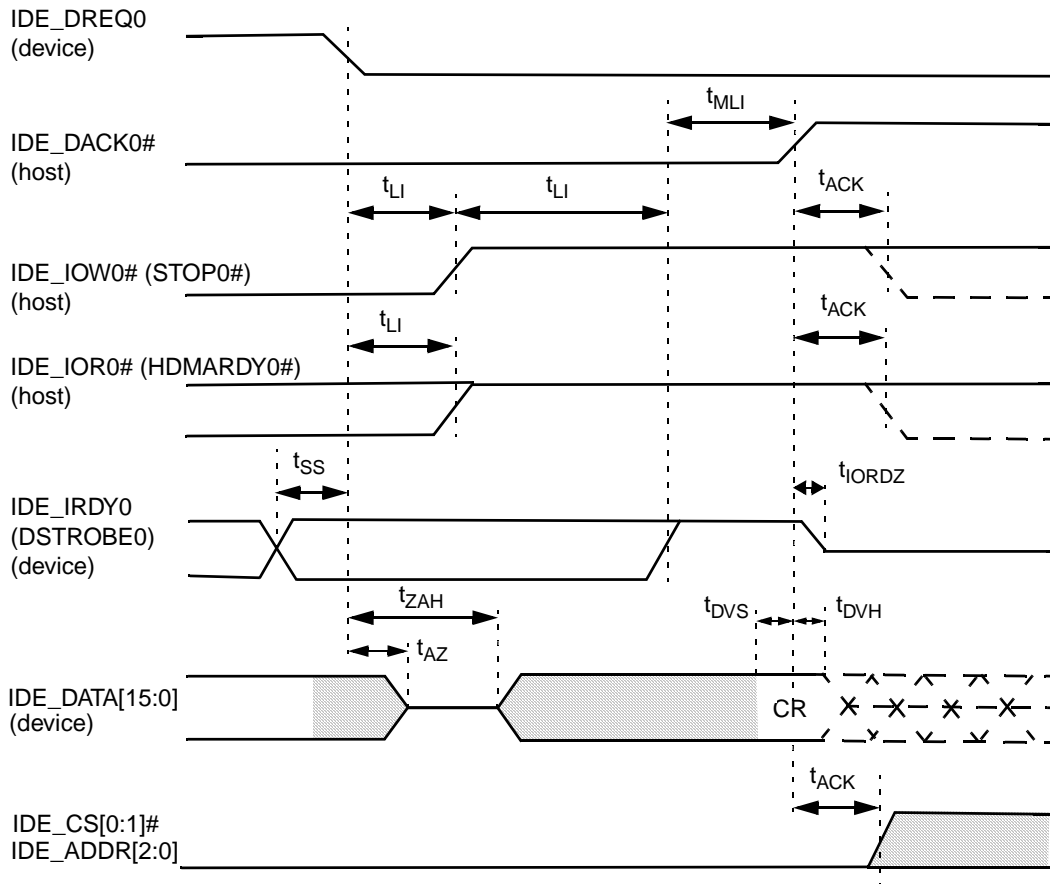
**Figure 9-28. Sustained UltraDMA Data In Burst Timing Diagram**



**Notes:**

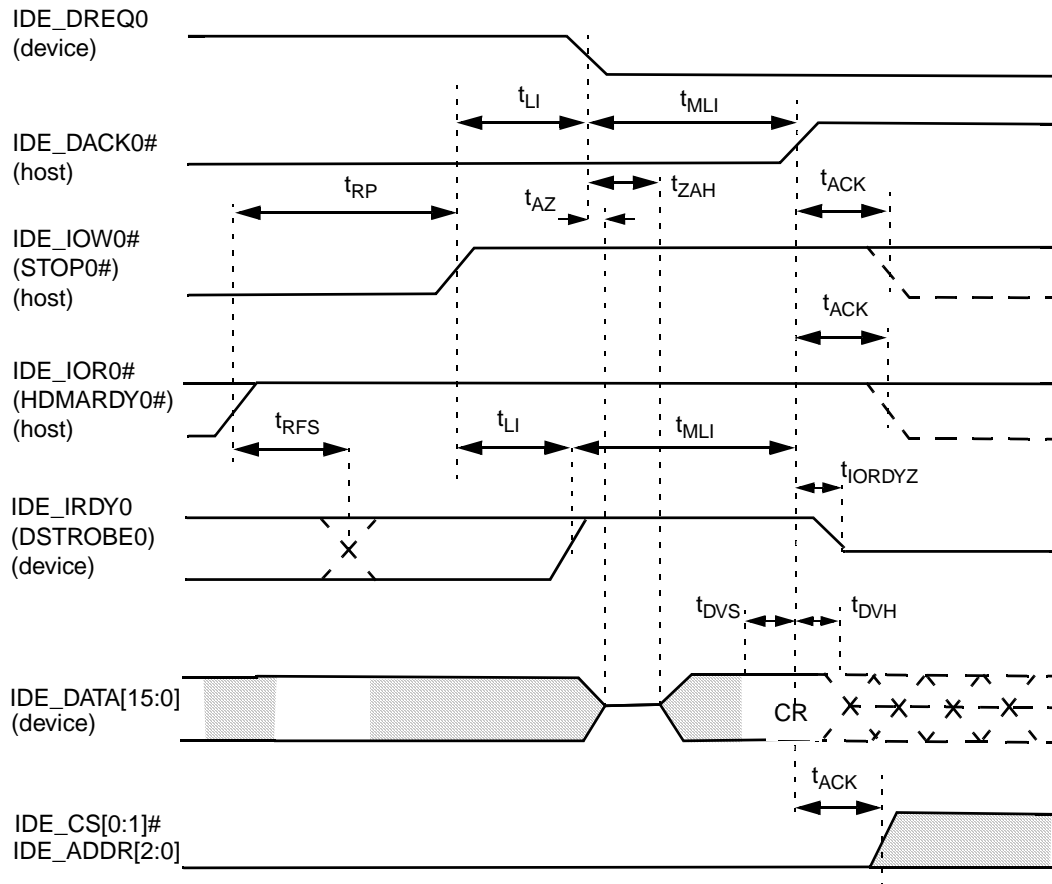
- 1) The host can assert IDE\_IOW[0:1]# (STOP[0:1]#) to request termination of the UltraDMA burst no sooner than  $t_{RP}$  after IDE\_IOR[0:1]# (HDMARDY[0:1]#) is de-asserted.
- 2) If the  $t_{SR}$  timing is not satisfied, the host may receive up to two additional data WORDs from the device.

**Figure 9-29. Host Pausing an UltraDMA Data In Burst Timing Diagram**



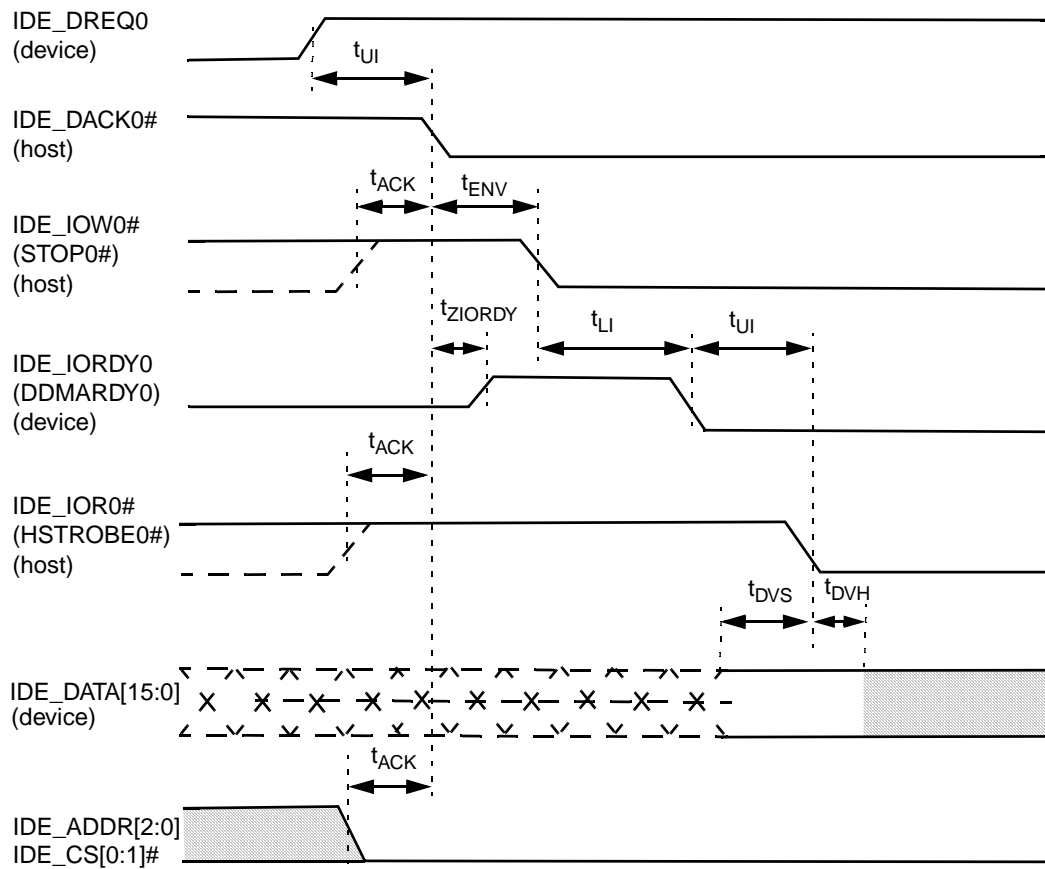
**Note:** The definitions for the IDE\_IOW[0:1]# (STOP[0:1]#), IDE\_IOR[0:1]# (HDMARDY[0:1]#), and IDE\_IRDY[0:1] (DSTROBE[0:1]) signal lines are no longer in effect after IDE\_DREQ[0:1] and IDE\_DACK[0:1]# are de-asserted.

**Figure 9-30. Device Terminating an UltraDMA Data In Burst Timing Diagram**



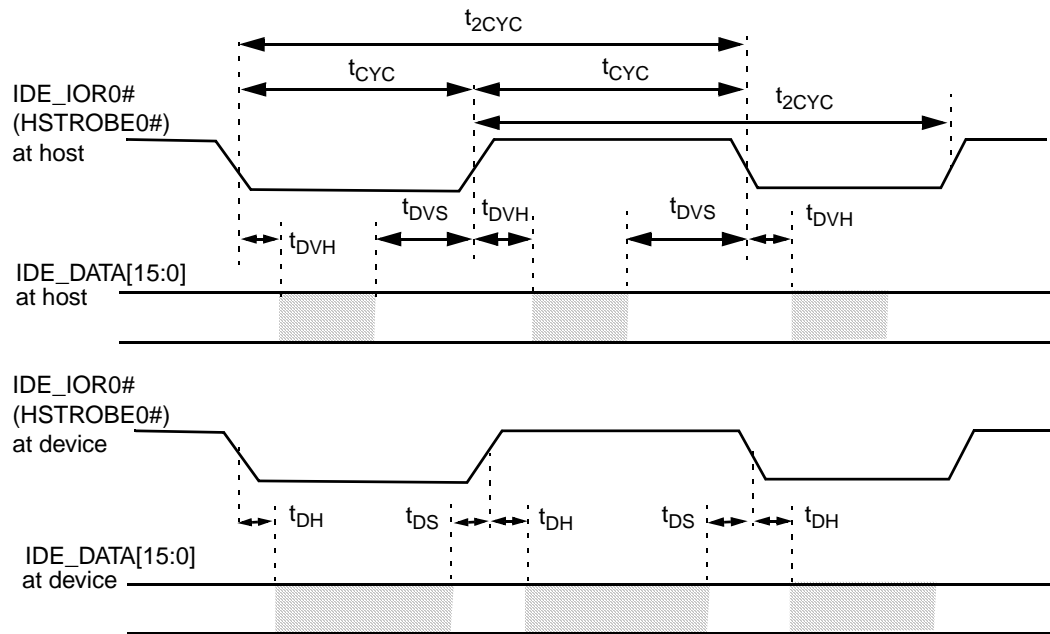
**Note:** The definitions for the  $IDE\_IOW[0:1]\#$  (STOP[0:1]#),  $IDE\_IOR[0:1]\#$  (HDMARDY[0:1]#), and  $IDE\_IRDY[0:1]$  (DSTROBE[0:1]) signal lines are no longer in effect after  $IDE\_DREQ[0:1]$  and  $IDE\_DACK[0:1]$  are de-asserted.

**Figure 9-31. Host Terminating an UltraDMA Data In Burst Timing Diagram**



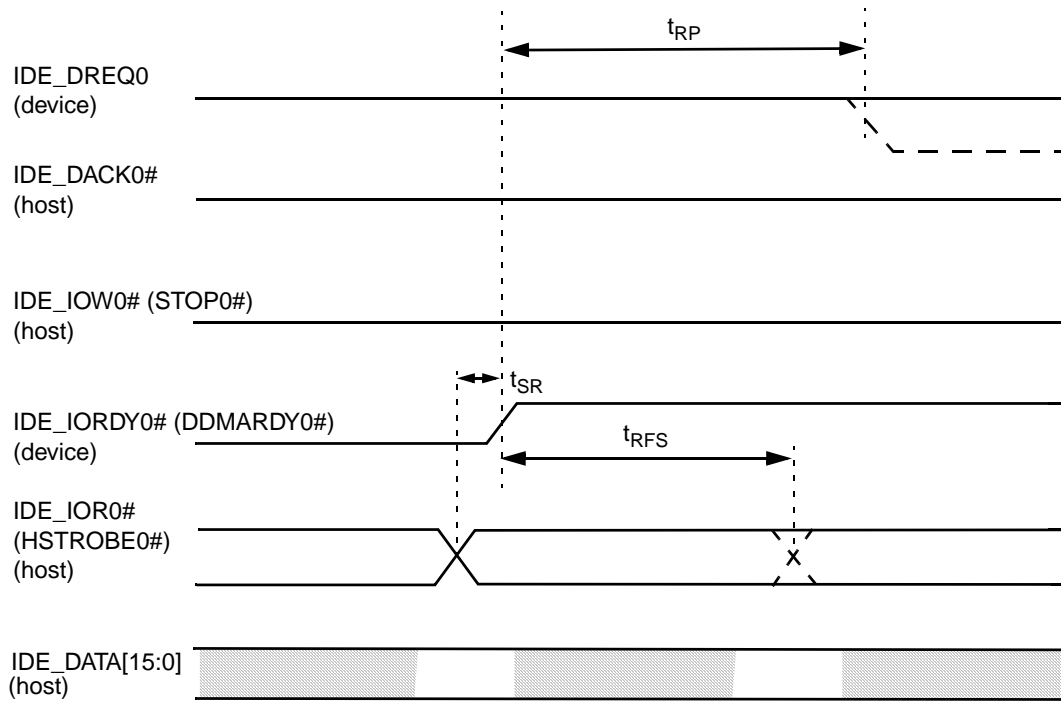
**Note:** The definitions for the IDE\_IOW[0:1]# (STOP[0:1]#), IDE\_IORDY[0:1]# (DDMARDY[0:1]) and IDE\_IOR[0:1]# (HSTROBE[0:1]#) signal lines are not in effect until IDE\_DREQ[0:1] and IDE\_DACK[0:1]# are asserted.

**Figure 9-32. Initiating an UltraDMA Data Out Burst Timing Diagram**



**Note:** IDE\_DATA[15:0] and IDE\_IOR[0:1]# (HSTROBE[0:1]#) signals are shown at both the device and the host to emphasize that cable settling time and cable propagation delay do not allow the data signals to be considered stable at the device until a certain amount of time after they are driven by the device.

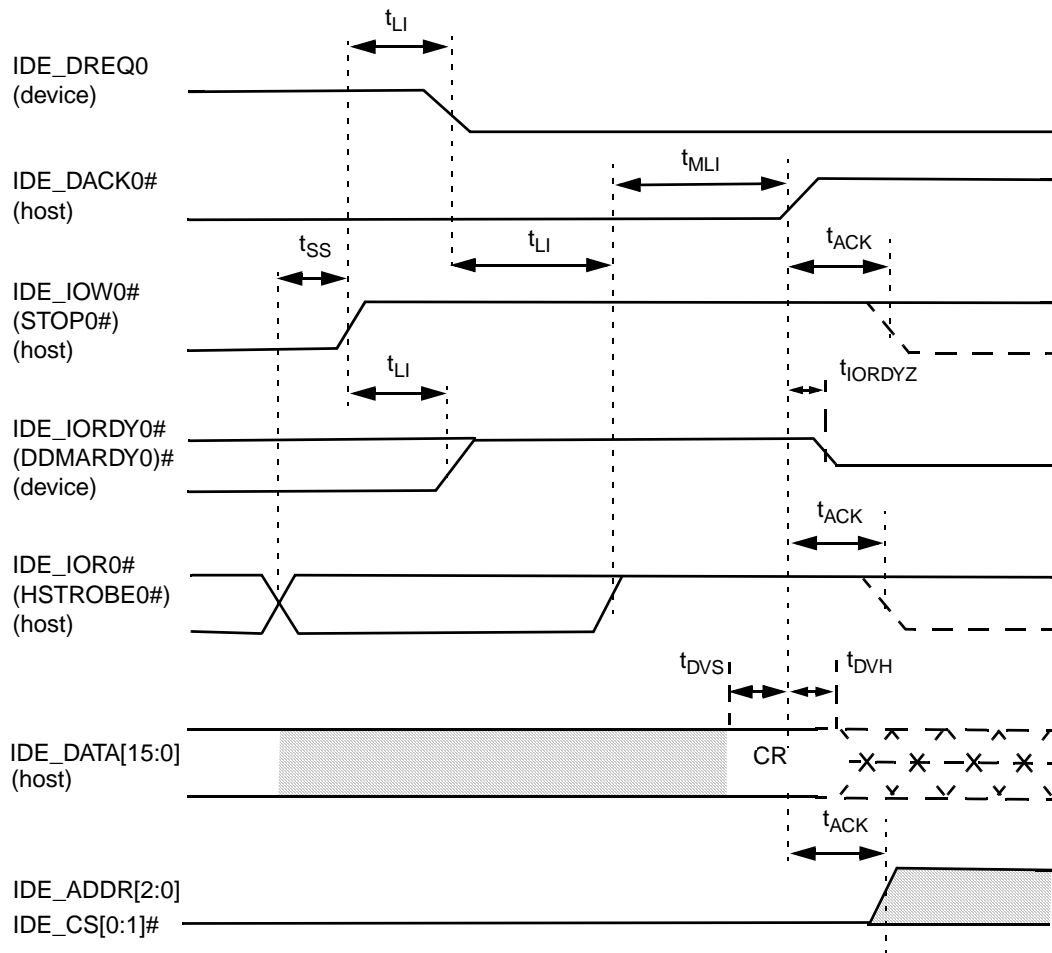
**Figure 9-33. Sustained UltraDMA Data Out Burst Timing Diagram**



**Notes:**

- 1) The device can de-assert IDE\_DREQ[0:1] to request termination of the UltraDMA burst no sooner than  $t_{RP}$  after IDE\_IORDY[0:1]# (DDMARDY[0:1]#) is de-asserted.
- 2) If the  $t_{SR}$  timing is not satisfied, the device may receive up to two additional datawords from the host.

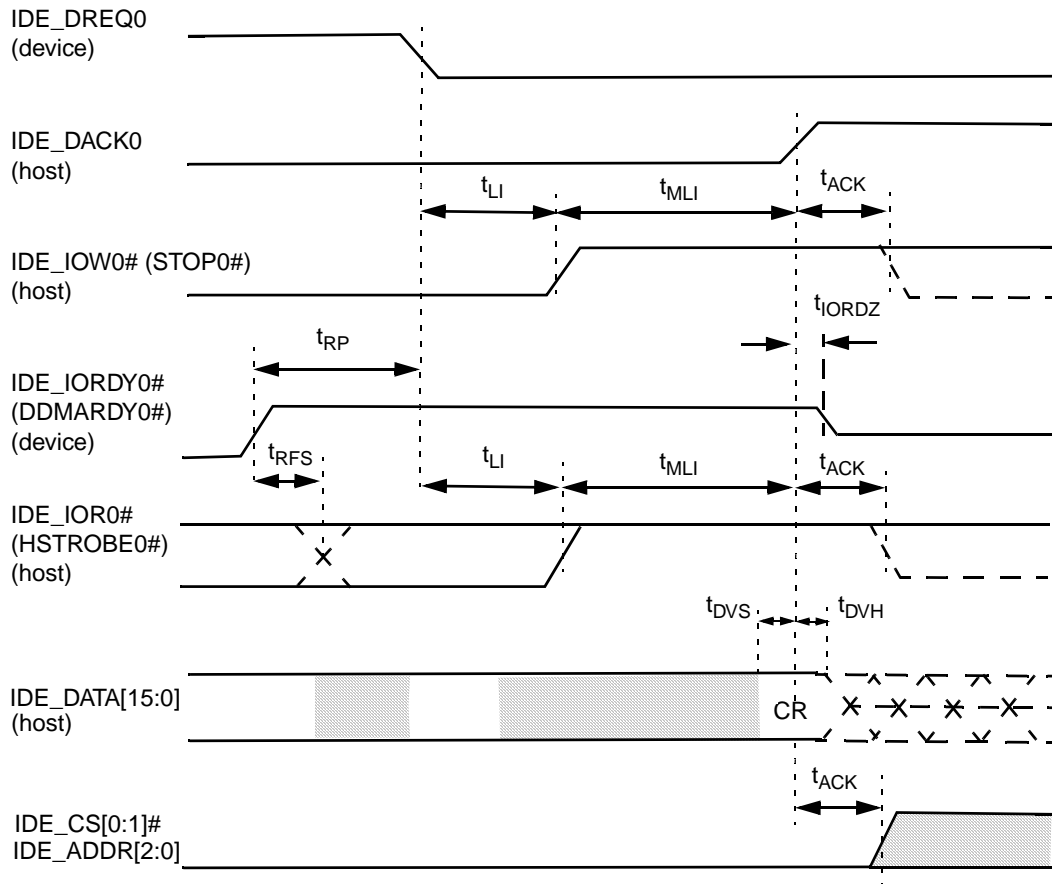
**Figure 9-34. Device Pausing an UltraDMA Data Out Burst Timing Diagram**



**Note:** The definitions for the IDE\_IOW[0:1]# (STOP[0:1]#), IDE\_IORDY[0,1]# (DDMARDY[0:1]#) and IDE\_IOR[0:1]# (HSTROBE[0:1]#) signal lines are no longer in effect after IDE\_DREQ[0:1] and IDE\_DACK[0:1]# are de-asserted.

**Figure 9-35. Host Terminating an UltraDMA Data Out Burst Timing Diagram**





**Note:** The definitions for the  $IDE\_IOW[0:1]\#$  ( $STOP[0:1]\#$ ),  $IDE\_IORDY[0:1]\#$  ( $DDMARDY[0:1]\#$ ) and  $IDE\_IOR[0:1]\#$  ( $HSTROBE[0:1]\#$ ) signal lines are no longer in effect after  $IDE\_DREQ[0:1]$  and  $IDE\_DACK[0:1]\#$  are de-asserted.

**Figure 9-36. Device Terminating an UltraDMA Data Out Burst Timing Diagram**

## 9.3.9 Universal Serial Bus (USB) Interface

Table 9-28. USB Timing Parameters

| Symbol  | Parameter  | Min    | Max             | Unit | Figure | Comments  |
|---|--|--------|-----------------|------|--------|---|
| <b>Full Speed Source (Note 1, Note 2)</b>     |  |        |                 |      |        |   |
| t <sub>USB_R1</sub>                           | DPOS_Port1,2,3, DNEG_Port1,2,3<br>Driver Rise Time             | 4      | 20              | ns   | 9-37   | (Monotonic) from 10% to 90% of the D_Port lines |
| t <sub>USB_F1</sub>                           | DPOS_Port1,2,3, DNEG_Port1,2,3<br>Driver Fall Time             | 4      | 20              | ns   | 9-37   | (Monotonic) from 90% to 10% of the D_Port lines |
| t <sub>USB_FRFM</sub>                         | Rise/Fall time matching  | 90     | 110             | %    |        |   |
| t <sub>USB_FSDR</sub>                         | Full-speed data rate   | 11.97  | 12.03           | Mbps |        | Average bit rate 12 Mbps<br>± 0.25%             |
| t <sub>USB_FSF</sub>                          | Full-speed frame interval                                      | 0.9995 | 1.0005          | ms   |        | 1.0 ms ± 0.05%                                  |
| t <sub>period_F</sub>                         | Full-speed period between data bits                            | 83.1   | 83.5            | ns   |        | Average bit rate 12 Mbps                        |
| t <sub>USB_DOR</sub>                          | Driver-output resistance                                       | 28     | 43              | W    |        | Steady-state drive                              |
| t <sub>USB_DJ11</sub>                         | Source differential driver jitter for consecutive transition   | -3.5   | 3.5             | ns   | 9-38   | Note 3, Note 4                                  |
| t <sub>USB_DJ12</sub>                         | Source differential driver jitter for paired transitions       | -4.0   | 4.0             | ns   | 9-38   | Note 3, Note 4                                  |
| t <sub>USB_SE1</sub>                          | Source EOP width   | 160    | 175             | ns   | 9-38   | Note 4, Note 5                                  |
| t <sub>USB_DE1</sub>                          | Differential to EOP transition skew                            | -2     | 5               | ns   | 9-39   | Note 4, Note 5                                  |
| t <sub>USB_RJ11</sub>                         | Receiver data jitter tolerance for consecutive transition      | -18.5  | 18.5            | ns   | 9-40   | Note 4  |
| t <sub>USB_RJ12</sub>                         | Receiver data jitter tolerance for paired transitions          | -9     | 9               | ns   | 9-40   | Note 4  |
| <b>Full Speed Receiver EOP Width (Note 4)</b> |  |        |                 |      |        |   |
| t <sub>USB_RE11</sub>                         | Must reject as EOP   |        | 40              | ns   | 9-39   | Note 5  |
| t <sub>USB_RE12</sub>                         | Must accept as EOP   | 82     |                 | ns   | 9-39   | Note 5  |
| <b>Low Speed Source (Note 1)</b>              |  |        |                 |      |        |   |
| t <sub>USB_R2</sub>                           | DPOS_Port1,2,3, DNEG_Port1,2,3<br>Driver Rise Time             | 75     | 300<br>(Note 6) | ns   | 9-37   | (Monotonic) from 10% to 90% of the D_Port lines |
| t <sub>USB_F2</sub>                           | DPOS_Port1,2,3, DNEG_Port1,2,3<br>Driver Fall Time             | 75     | 300<br>(Note 6) | ns   | 9-37   | (Monotonic) from 90% to 10% of the D_Port lines |
| t <sub>USB_LRFM</sub>                         | Low-speed Rise/Fall time matching                              | 80     | 120             | %    |        |   |
| t <sub>USB_LSDR</sub>                         | Low-speed data rate  | 1.4775 | 1.5225          | Mbps |        | Average bit rate 1.5 Mbps<br>± 1.5%             |
| t <sub>PERIOD_L</sub>                         | Low-speed period   | 0.657  | 0.677           | μs   |        | at 1.5 Mbps                                     |
| t <sub>USB_DJD21</sub>                        | Source differential driver jitter for consecutive transactions | -75    | 75              | ns   |        | Host (downstream),<br>Note 4                    |
| t <sub>USB_DJD22</sub>                        | Source differential driver jitter for paired transactions      | -45    | 45              | ns   | 9-38   | Host (downstream),<br>Note 4                    |
| t <sub>USB_DJU21</sub>                        | Source differential driver jitter for consecutive transaction  | -95    | 95              | ns   | 9-38   | Function (downstream),<br>Note 4                |

Table 9-28. USB Timing Parameters (Continued)

| Symbol                                       | Parameter   | Min  | Max | Unit | Figure | Comments                      |
|--|---|------|-----|------|--------|-------------------------------|
| t <sub>USB_DJU22</sub>                       | Source differential driver jitter for paired transactions   | -150 | 150 | ns   | 9-38   | Function (downstream), Note 4 |
| t <sub>USB_SE2</sub>                         | Source EOP width  | 1.25 | 1.5 | μs   | 9-39   | Note 4, Note 5                |
| t <sub>USB_DE2</sub>                         | Differential to EOP transition skew                         | -40  | 100 | ns   | 9-39   | Note 5                        |
| t <sub>USB_RJD21</sub>                       | Receiver data jitter tolerance for consecutive transactions | -152 | 152 | ns   | 9-40   | Host (upstream), Note 4       |
| t <sub>USB_RJD22</sub>                       | Receiver data jitter tolerance for paired transactions      | -200 | 200 | ns   | 9-40   | Host (upstream), Note 4       |
| t <sub>USB_RJU21</sub>                       | Receiver data jitter tolerance for consecutive transactions | -75  | 75  | ns   | 9-40   | Function (downstream), Note 4 |
| t <sub>USB_RJU22</sub>                       | Receiver data jitter tolerance for paired transactions      | -45  | 45  | ns   | 9-40   | Function (downstream), Note 4 |
| <b>Low Speed Receiver EOP Width (Note 5)</b> |   |      |     |      |        |                               |
| t <sub>USB_RE21</sub>                        | Must reject as EOP  |      | 330 | ns   | 9-38   |                               |
| t <sub>USB_RE22</sub>                        | Must accept as EOP  | 675  |     | ns   | 9-38   |                               |

Note 1. Unless otherwise specified, all timings use a 50 pF capacitive load (C<sub>L</sub>) to ground.

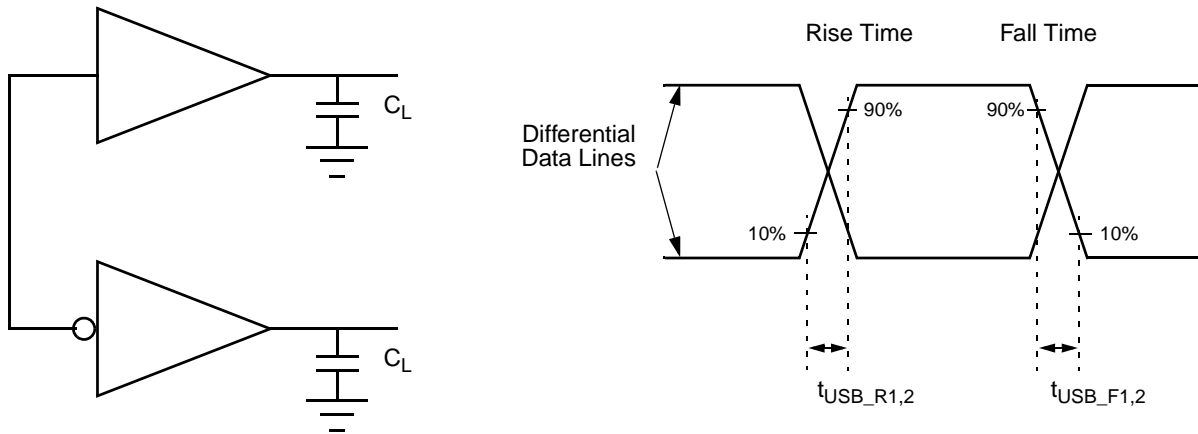
Note 2. Full-speed timing has a 1.5 KΩ pull-up to 2.8 V on the DPOS\_Port1,2,3 lines.

Note 3. Timing difference between the differential data signals (DPOS\_PORT1,2,3 and DNEG\_PORT1,2,3).

Note 4. Measured at the crossover point of differential data signals (DPOS\_PORT1,2,3 and DNEG\_PORT1,2,3).

Note 5. EOP is the End of Packet where DPOS\_PORT<sup>t</sup> = DNEG\_PORT = SE0. SE0 occurs when output level voltage ≤ V<sub>SE</sub> (Min).

Note 6. C<sub>L</sub> = 350 pF.



Full Speed: 4 to 20 ns at  $C_L = 50$  pF  
 Low Speed: 75 ns at  $C_L = 50$  pF, 300 ns at  $C_L = 350$  pF

Figure 9-37. Data Signal Rise and Fall Timing Diagram

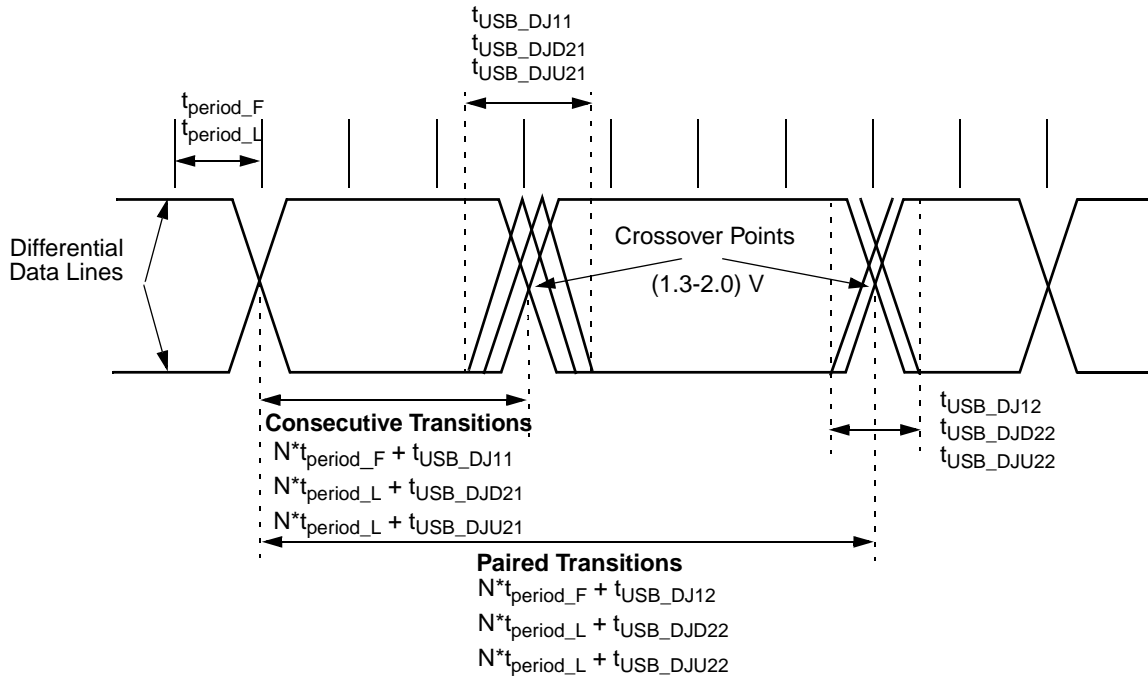


Figure 9-38. Source Differential Data Jitter Timing Diagram

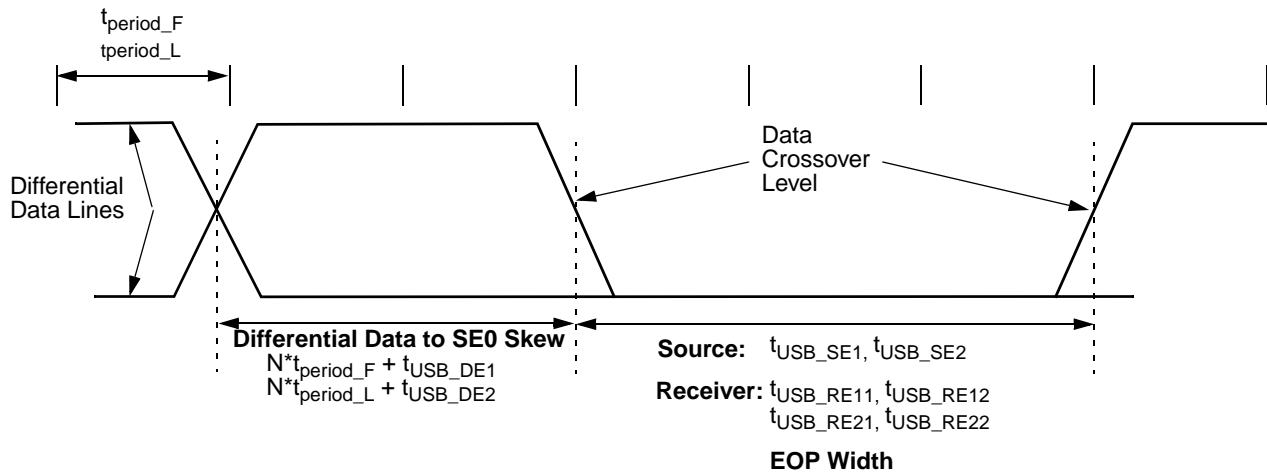


Figure 9-39. EOP Width Timing Diagram

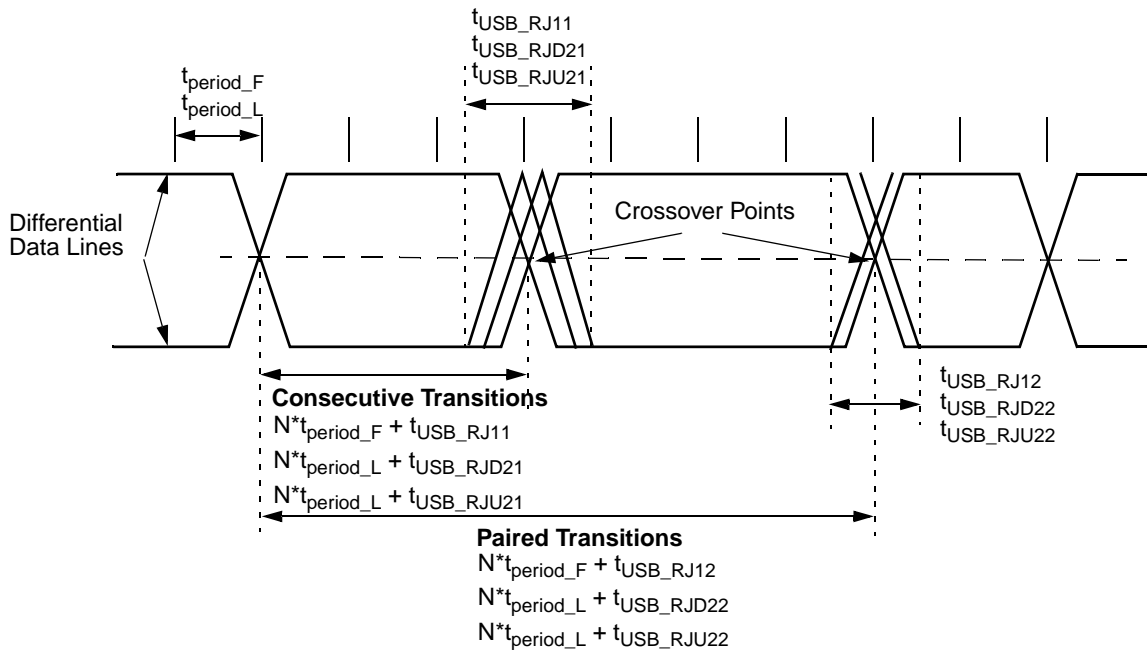


Figure 9-40. Receiver Jitter Tolerance Timing Diagram

9.3.10 Serial Port (UART)

Table 9-29. UART, Sharp-IR, SIR, and Consumer Remote Control Timing Parameters

| Symbol           | Parameter   | Min   | Max   | Unit | Comments              |
|------------------|---|---|---|------|-----------------------|
| t <sub>BT</sub>  | Single bit time in UART and Sharp-IR                                  | t <sub>BTN</sub> - 25<br>(Note 1)                     | t <sub>BTN</sub> + 25                                 | ns   | Transmitter           |
|                  |   | t <sub>BTN</sub> - 2%                                 | t <sub>BTN</sub> + 2%                                 | ns   | Receiver              |
| t <sub>CMW</sub> | Modulation signal pulse width in Sharp-IR and Consumer Remote Control | t <sub>CWN</sub> - 25<br>(Note 2)                     | t <sub>CWN</sub> + 25                                 | ns   | Transmitter           |
|                  |   | 500   |   | ns   | Receiver              |
| t <sub>CMP</sub> | Modulation signal period in Sharp-IR and Consumer Remote Control      | t <sub>CPN</sub> - 25<br>(Note 3)                     | t <sub>CPN</sub> + 25                                 | ns   | Transmitter           |
|                  |   | t <sub>MMIN</sub><br>(Note 4)                         | t <sub>MMAX</sub><br>(Note 4)                         | ns   | Receiver              |
| t <sub>SPW</sub> | SIR signal pulse width  | <sup>(3/16)</sup> × t <sub>BTN</sub> - 15<br>(Note 1) | <sup>(3/16)</sup> × t <sub>BTN</sub> + 15<br>(Note 1) | ns   | Transmitter, Variable |
|                  |   | 1.48  | 1.78  | µs   | Transmitter, Fixed    |
|                  |   | 1   |   | µs   | Receiver              |
| S <sub>DRT</sub> | SIR data rate tolerance % of nominal data rate                        |   | ± 0.87%   |      | Transmitter           |
|                  |   |   | ± 2.0%  |      | Receiver              |
| t <sub>SJT</sub> | SIR leading edge jitter % of nominal bit duration                     |   | ± 2.5%  |      | Transmitter           |
|                  |   |   | ± 6.5%  |      | Receiver              |

- Note 1. t<sub>BTN</sub> is the nominal bit time in UART, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers.
- Note 2. t<sub>CWN</sub> is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits [7:5]) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
- Note 3. t<sub>CPN</sub> is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFR field (bits [4:0]) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
- Note 4. t<sub>MMIN</sub> and t<sub>MMAX</sub> define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of register IRRXDC and the setting of the RXHSC bit (bit 5) of the RCCFG register.

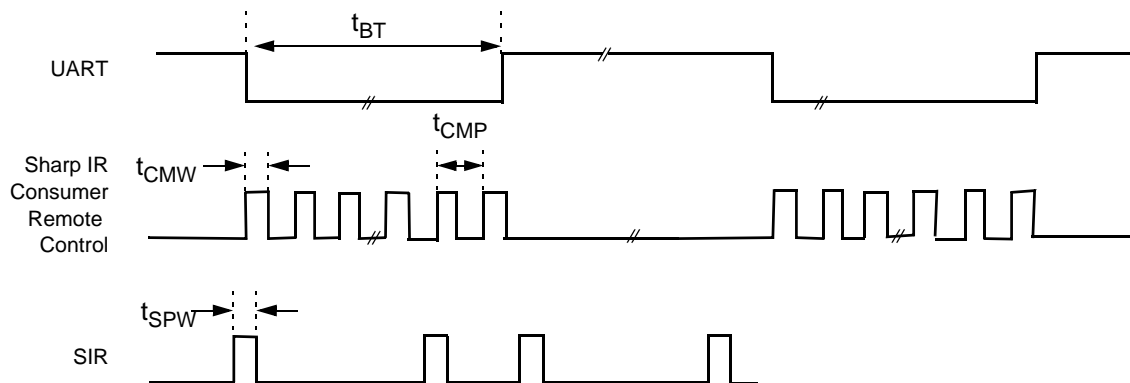


Figure 9-41. UART, Sharp-IR, SIR, and Consumer Remote Control Timing Diagram

9.3.11 Fast IR Port

Table 9-30. Fast IR Port Timing Parameters

| Symbol     | Parameter   | Min                      | Max          | Unit | Comments    |
|------------|---|--------------------------|--------------|------|-------------|
| $t_{MPW}$  | MIR signal pulse width                              | $t_{MWN}-25$<br>(Note 1) | $t_{MWN}+25$ | ns   | Transmitter |
|            |   | 60                       |              | ns   | Receiver    |
| $M_{DRT}$  | MIR transmitter data rate tolerance                 |                          | $\pm 0.1\%$  |      |             |
| $t_{MJT}$  | MIR receiver edge jitter, % of nominal bit duration |                          | $\pm 2.9\%$  |      |             |
| $t_{FPW}$  | FIR signal pulse width                              | 120                      | 130          | ns   | Transmitter |
|            |   | 90                       | 160          | ns   | Receiver    |
| $t_{FDPW}$ | FIR signal double pulse width                       | 245                      | 255          | ns   | Transmitter |
|            |   | 215                      | 285          | ns   | Receiver    |
| $F_{DRT}$  | FIR transmitter data rate tolerance                 |                          | $\pm 0.01\%$ |      |             |
| $t_{FJT}$  | FIR receiver edge jitter, % of nominal bit duration |                          | $\pm 4.0\%$  |      |             |

Note 1.  $t_{MWN}$  is the nominal pulse width for MIR mode. It is determined by the M\_PWID field (bits [4:0]) in the MIR\_PW register at offset 01h in bank 6 of logical device 5.

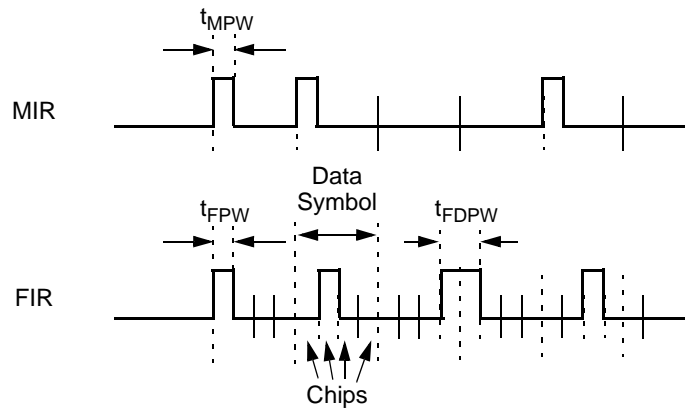


Figure 9-42. Fast IR (MIR and FIR) Timing Diagram

9.3.12 Parallel Port Interface

Table 9-31. Standard Parallel Port Timing Parameters

| Symbol    | Parameter       | Min | Typ | Max | Unit | Comments |
|-----------|-----------------|-----|-----|-----|------|----------|
| $t_{PDH}$ | Port data hold  |     | 500 |     | ns   | Note 1   |
| $t_{PDS}$ | Port data setup |     | 500 |     | ns   | Note 1   |
| $t_{SW}$  | Strobe width    |     | 500 |     | ns   | Note 1   |

Note 1. Times are system dependent and are therefore not tested.

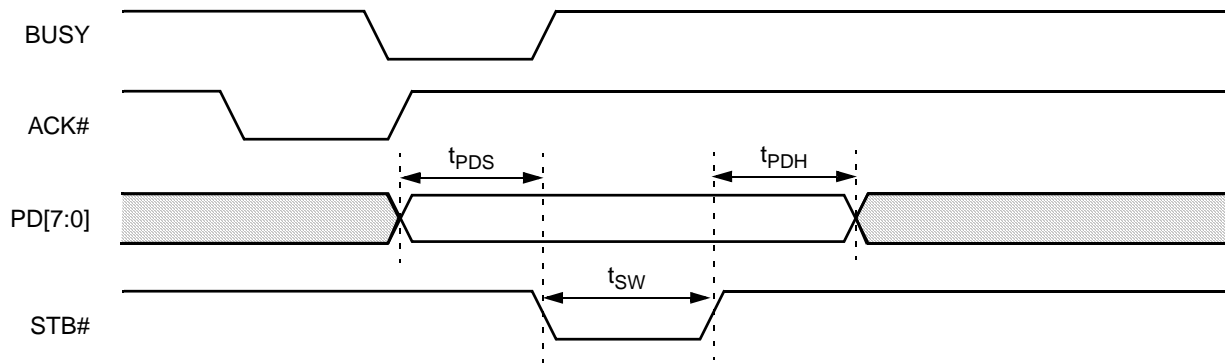
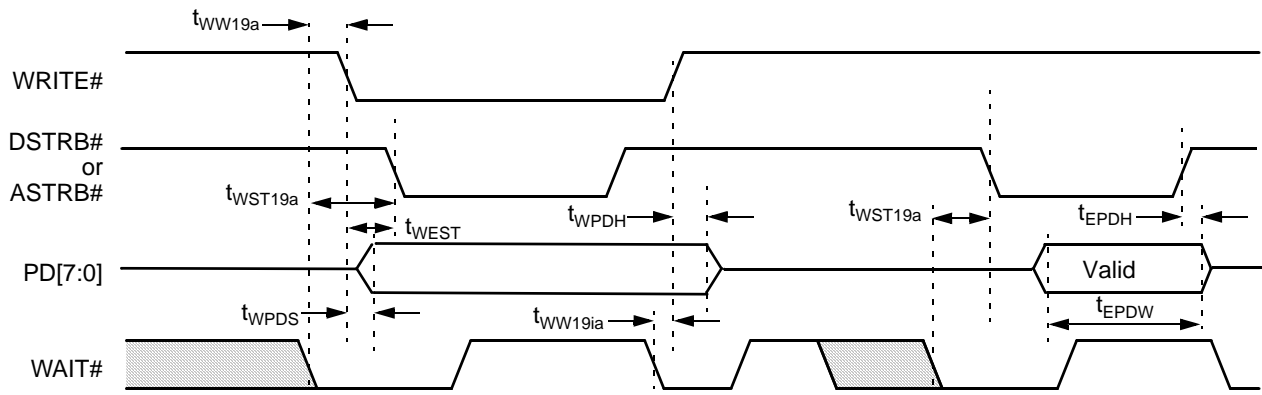


Figure 9-43. Standard Parallel Port Typical Data Exchange Timing Diagram



**Table 9-32. Enhanced Parallel Port Timing Parameters**

| Symbol       | Parameter                                    | Min | Max | EPP 1.7 | EPP 1.9 | Unit | Comments |
|--------------|--|-----|-----|---------|---------|------|----------|
| $t_{WW19a}$  | WRITE# active from WAIT# low                 |     | 45  |         | x       | ns   |          |
| $t_{WW19ia}$ | WRITE# inactive from WAIT# low               |     | 45  |         | x       | ns   |          |
| $t_{WST19a}$ | DSTRB# or ASTRB# active from WAIT# low       |     | 65  |         | x       | ns   |          |
| $t_{WEST}$   | DSTRB# or ASTRB# active after WRITE# active  | 10  |     | x       | x       | ns   |          |
| $t_{WPDH}$   | PD[7:0] hold after WRITE# inactive           | 0   |     | x       | x       | ns   |          |
| $t_{WPDS}$   | PD[7:0] valid after WRITE# active            |     | 15  | x       | x       | ns   |          |
| $t_{EPDW}$   | PD[7:0] valid width                          | 80  |     | x       | x       | ns   |          |
| $t_{EPDH}$   | PD[7:0] hold after DSTRB# or ASTRB# inactive | 0   |     | x       | x       | ns   |          |



**Figure 9-44. Enhanced Parallel Port Timing Diagram**

9.3.12.1 Extended Capabilities Port (ECP)

Table 9-33. ECP Forward Mode Timing Parameters

| Symbol      | Parameter                       | Min | Max | Unit | Comments |
|-------------|---------------------------------|-----|-----|------|----------|
| $t_{ECDSF}$ | Data setup before STB# active   | 0   |     | ns   |          |
| $t_{ECDHF}$ | Data hold after BUSY inactive   | 0   |     | ns   |          |
| $t_{ECLHF}$ | BUSY active after STB# active   | 75  |     | ns   |          |
| $t_{ECHHF}$ | STB# inactive after BUSY active | 0   | 1   | s    |          |
| $t_{ECHLF}$ | BUSY inactive after STB# active | 0   | 35  | ms   |          |
| $t_{ECLLF}$ | STB# active after BUSY inactive | 0   |     | ns   |          |

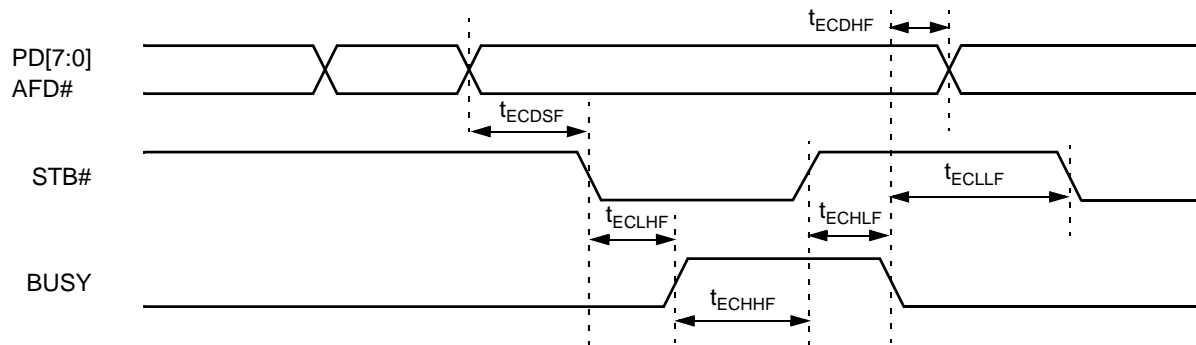
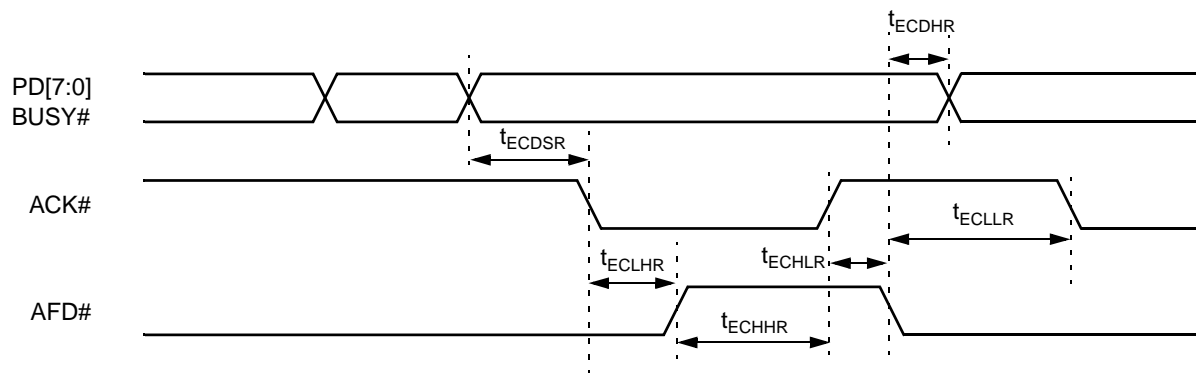


Figure 9-45. ECP Forward Mode Timing Diagram

**Table 9-34. ECP Reverse Mode Timing Parameters**

| Symbol      | Parameter                         | Min | Max | Unit | Comments |
|-------------|-----------------------------------|-----|-----|------|----------|
| $t_{ECDSR}$ | Data setup before ACK# active     | 0   |     | ns   |          |
| $t_{ECDHR}$ | Data hold after AFD# active       | 0   |     | ns   |          |
| $t_{ECLHR}$ | AFD# inactive after ACK# active   | 75  |     | ns   |          |
| $t_{ECHHR}$ | ACK# inactive after AFD# inactive | 0   | 35  | ms   |          |
| $t_{ECHLR}$ | AFD# active after ACK# inactive   | 0   | 1   | s    |          |
| $t_{ECLLR}$ | ACK# active after AFD# active     | 0   |     | ns   |          |



**Figure 9-46. ECP Reverse Mode Timing Diagram**

9.3.13 Audio Interface (AC97)

Table 9-35. AC Reset Timing Parameters

| Symbol         | Parameter                                   | Min   | Typ | Max | Unit    | Comments |
|----------------|---|-------|-----|-----|---------|----------|
| $t_{RST\_LOW}$ | AC97_RST# active low pulse width            | 1.0   |     |     | $\mu s$ |          |
| $t_{RST2CLK}$  | AC97_RST# inactive to BIT_CLK startup delay | 162.8 |     |     | ns      |          |

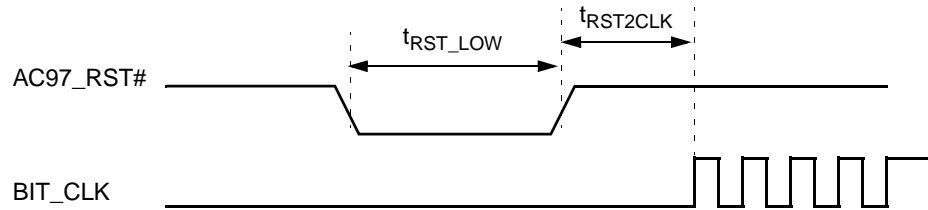


Figure 9-47. AC97 Reset Timing Diagram

Table 9-36. AC97 Sync Timing Parameters

| Symbol           | Parameter                              | Min   | Typ | Max | Unit    | Comments |
|------------------|--|-------|-----|-----|---------|----------|
| $t_{SYNC\_HIGH}$ | SYNC active high pulse width           |       | 1.3 |     | $\mu s$ |          |
| $t_{SYNC\_IA}$   | SYNC inactive to BIT_CLK startup delay | 162.8 |     |     | ns      |          |

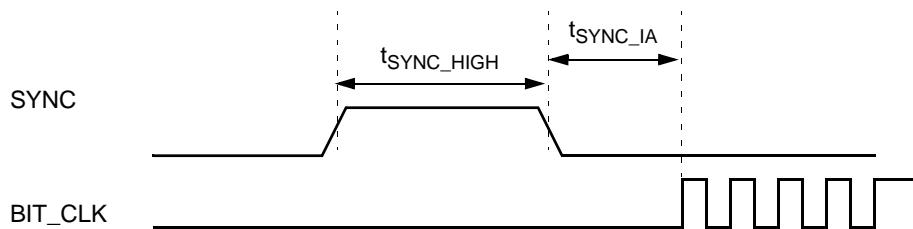
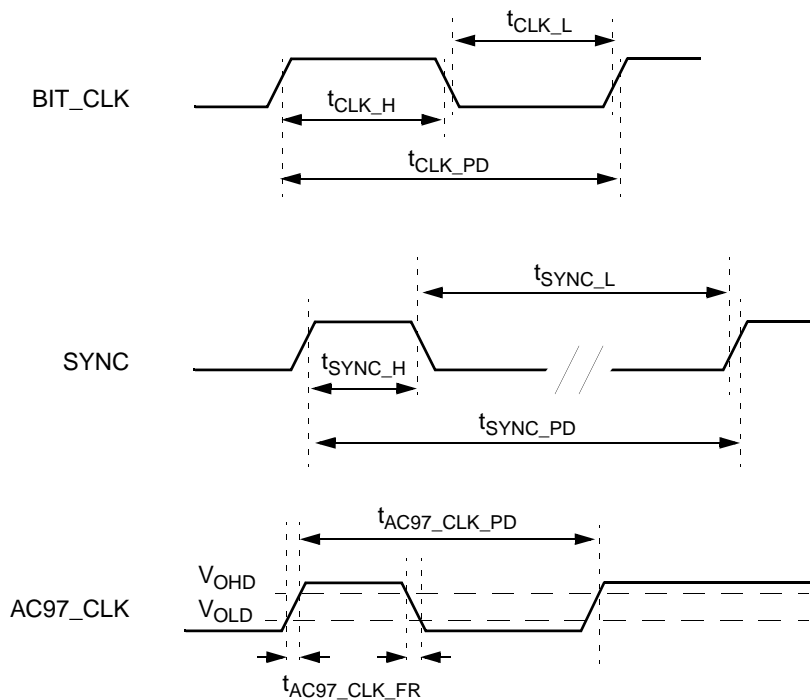


Figure 9-48. AC97 Sync Timing Diagram

**Table 9-37. AC97 Clocks Parameters**

| Symbol                     | Parameter                           | Min   | Typ    | Max   | Unit          | Comments                   |
|----------------------------|-------------------------------------|-------|--------|-------|---------------|----------------------------|
| $F_{\text{BIT\_CLK}}$      | BIT_CLK frequency                   |       | 12.288 |       | MHz           |                            |
| $t_{\text{CLK\_PD}}$       | BIT_CLK period                      |       | 81.4   |       | ns            |                            |
| $t_{\text{CLK\_J}}$        | BIT_CLK output jitter               |       |        | 750   | ps            |                            |
| $t_{\text{CLK\_H}}$        | BIT_CLK high pulse width            | 32.56 | 40.7   | 48.84 | ns            | Note 1                     |
| $t_{\text{CLK\_L}}$        | BIT_CLK low pulse width             | 32.56 | 40.7   | 48.84 | ns            | Note 1                     |
| $F_{\text{SYNC}}$          | SYNC frequency                      |       | 48.0   |       | KHz           |                            |
| $t_{\text{SYNC\_PD}}$      | SYNC period                         |       | 20.8   |       | $\mu\text{s}$ |                            |
| $t_{\text{SYNC\_H}}$       | SYNC high pulse width               |       | 1.3    |       | $\mu\text{s}$ |                            |
| $t_{\text{SYNC\_L}}$       | SYNC low pulse width                |       | 19.5   |       | $\mu\text{s}$ |                            |
| $F_{\text{AC97\_CLK}}$     | AC97_CLK frequency                  |       | 24.576 |       | MHz           |                            |
| $t_{\text{AC97\_CLK\_PD}}$ | AC97_CLK period                     |       | 40.7   |       | ns            |                            |
| $t_{\text{AC97\_CLK\_D}}$  | AC97_CLK duty cycle                 | 45    |        | 55    | %             |                            |
| $t_{\text{AC97\_CLK\_FR}}$ | AC97_CLK fall/rise time             | 2     |        | 5     | ns            |                            |
| $t_{\text{AC97\_CLK\_J}}$  | AC97_CLK output edge-to-edge jitter |       |        | 100   | ps            | Measured from edge to edge |

Note 1. Worst case duty cycle restricted to 40/60.



**Figure 9-49. AC97 Clocks Diagram**

Table 9-38. AC97 I/O Timing Parameters

| Symbol         | Parameter   | Min  | Typ | Max | Unit | Comments |
|----------------|---|------|-----|-----|------|----------|
| $t_{AC97\_S}$  | Input setup to falling edge of BIT_CLK                    | 15.0 |     |     | ns   |          |
| $t_{AC97\_H}$  | Hold from falling edge of BIT_CLK                         | 10.0 |     |     | ns   |          |
| $t_{AC97\_OV}$ | SDATA_OUT or SYNC valid after rising edge of BIT_CLK      |      |     | 15  | ns   |          |
| $t_{AC97\_OH}$ | SDATA_OUT or SYNC hold time after falling edge of BIT_CLK | 5    |     |     | ns   |          |
| $t_{AC97\_SV}$ | Sync out valid after rising edge of BIT_CLK               |      |     | 15  | ns   |          |
| $t_{AC97\_SH}$ | Sync out hold after falling edge of BIT_CLK               | 5    |     |     | ns   |          |

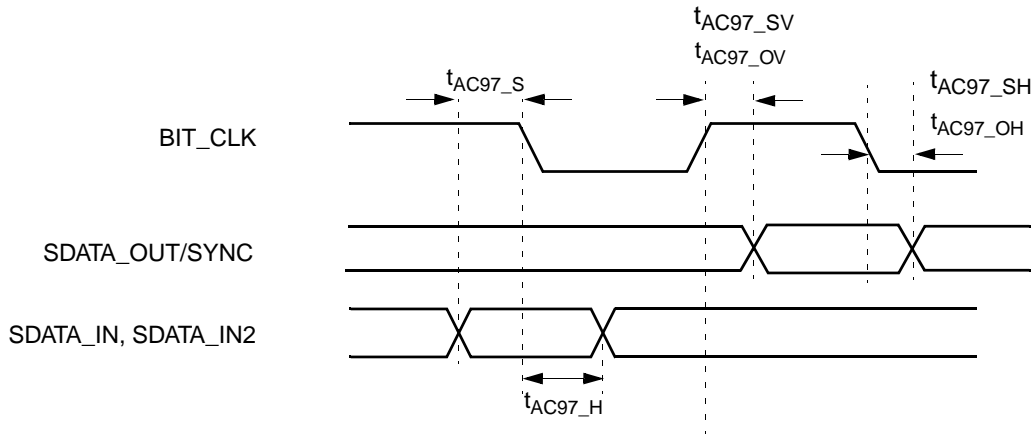
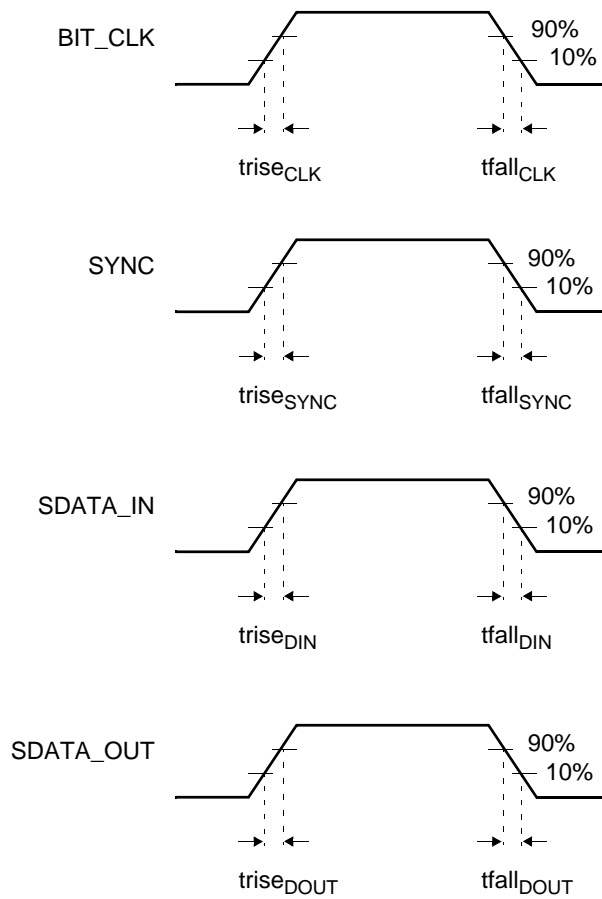


Figure 9-50. AC97 Data Timing Diagram

**Table 9-39. AC97 Signal Rise and Fall Timing Parameters**

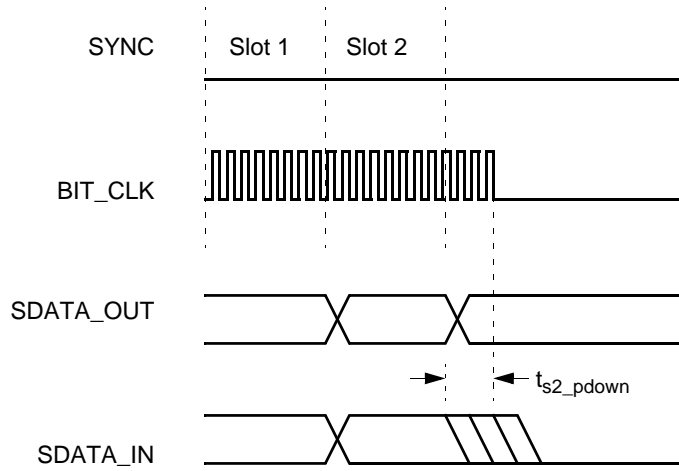
| Symbol            | Parameter           | Min | Typ | Max | Unit | Comments             |
|-------------------|---------------------|-----|-----|-----|------|----------------------|
| $t_{rise_{CLK}}$  | BIT_CLK rise time   | 2   |     | 6   | ns   |                      |
| $t_{fall_{CLK}}$  | BIT_CLK fall time   | 2   |     | 6   | ns   |                      |
| $t_{rise_{SYNC}}$ | SYNC rise time      | 2   |     | 6   | ns   | $C_L = 50\text{ pF}$ |
| $t_{fall_{SYNC}}$ | SYNC fall time      | 2   |     | 6   | ns   | $C_L = 50\text{ pF}$ |
| $t_{rise_{DIN}}$  | SDATA_IN rise time  | 2   |     | 6   | ns   |                      |
| $t_{fall_{DIN}}$  | SDATA_IN fall time  | 2   |     | 6   | ns   |                      |
| $t_{rise_{DOUT}}$ | SDATA_OUT rise time | 2   |     | 6   | ns   | $C_L = 50\text{ pF}$ |
| $t_{fall_{DOUT}}$ | SDATA_OUT fall time | 2   |     | 6   | ns   | $C_L = 50\text{ pF}$ |



**Figure 9-51. AC97 Rise and Fall Timing Diagram**

**Table 9-40. AC97 Low Power Mode Timing Parameters**

| Symbol          | Parameter                              | Min | Typ | Max | Unit    | Comments |
|-----------------|--|-----|-----|-----|---------|----------|
| $t_{s2\_pdown}$ | End of Slot 2 to BIT_CLK, SDATA_IN low |     |     | 1.0 | $\mu s$ |          |



**Note:** BIT\_CLK is not to scale

**Figure 9-52. AC97 Low Power Mode Timing Diagram**



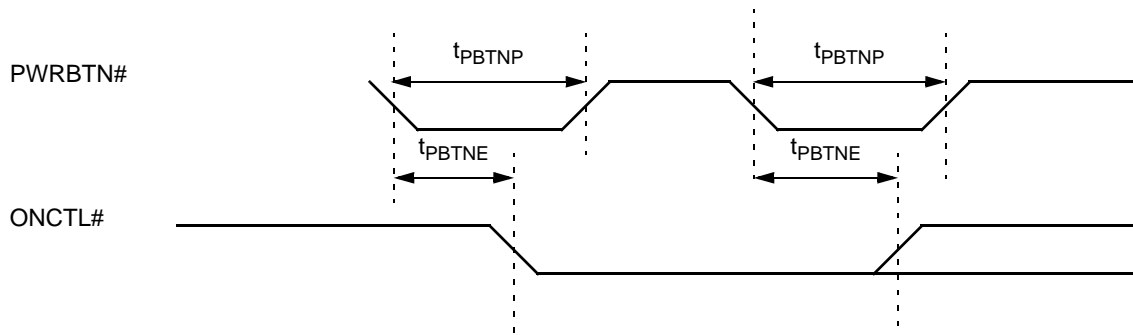
### 9.3.14 Power Management Interface

LED# Cycle time: 1 s ± 0.1 s, 40%-60% duty cycle.

**Table 9-41. PWRBTN# Timing Parameters**

| Symbol      | Parameter                           | Min | Max | Unit | Comments |
|-------------|-------------------------------------|-----|-----|------|----------|
| $t_{PBTNP}$ | PWRBTN# pulse width                 | 16  |     | ms   | Note 1   |
| $t_{PBTNE}$ | Delay from PWRBTN# events to ONCTL# | 14  | 16  | ms   |          |

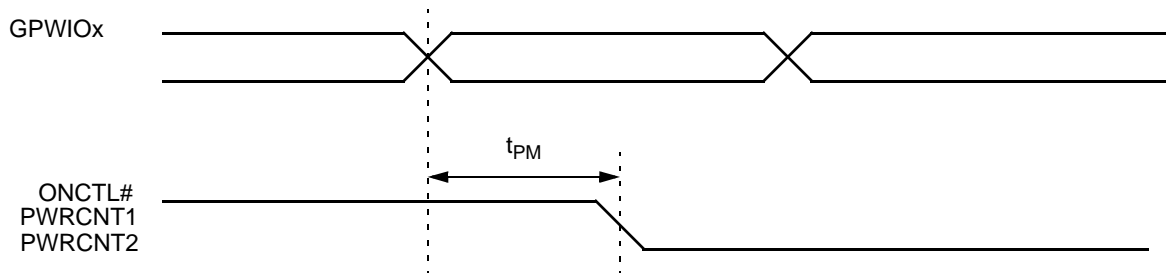
Note 1. Not 100% tested.



**Figure 9-53. PWRBTN# Trigger and ONCTL# Timing Diagram**

**Table 9-42. Power Management Event (GPWIO) and ONCTL# Timing Parameters**

| Symbol   | Parameter                                  | Min | Max | Unit | Comments |
|----------|--|-----|-----|------|----------|
| $t_{PM}$ | Power management event to ONCTL# assertion |     | 45  | ns   |          |



**Figure 9-54. GPWIO and ONCTL# Timing Diagram**

9.3.15 Power-Up Sequencing

Table 9-43. Power-Up Sequence Using the Power Button Timing Parameters

| Symbol | Parameter   | Min  | Max  | Unit    | Comments  |
|--------|---|------|------|---------|---|
| $t_1$  | Voltage sequence  | -100 | 100  | ms      | Optimum power-up results with $t_1 = 0$ .   |
| $t_2$  | PWRBTN# inactive after $V_{SB}$ or $V_{SBL}$ applied, whichever is applied last | 0    | 1    | $\mu$ s | PWRBTN# is an input and must be powered by $V_{SB}$ .   |
| $t_3$  | PWRBTN# active pulse width  | 16   | 4000 | ms      | If PWRBTN# max is exceeded, ONCTL# will go inactive.  |
| $t_4$  | ONCTL# inactive after $V_{SB}$ applied  | 0    | 1    | ms      |   |
| $t_5$  | Signal active after PWRBTN active   | 14   | 16   | ms      |   |
| $t_6$  | $V_{CORE}$ and $V_{IO}$ applied after ONCTL# active                             | 0    |      | ms      | System determines when $V_{CORE}$ and $V_{IO}$ are applied, hence there is no maximum constraint. |
| $t_7$  | POR# inactive after $V_{CORE}$ and $V_{IO}$ applied                             | 50   |      | ms      | POR# must not glitch during active time.  |

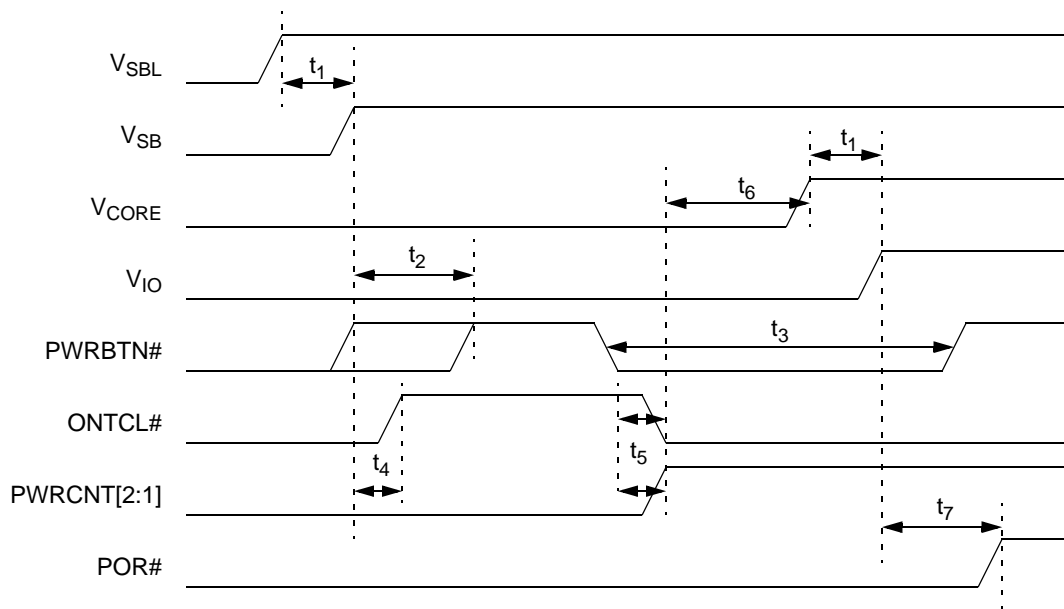
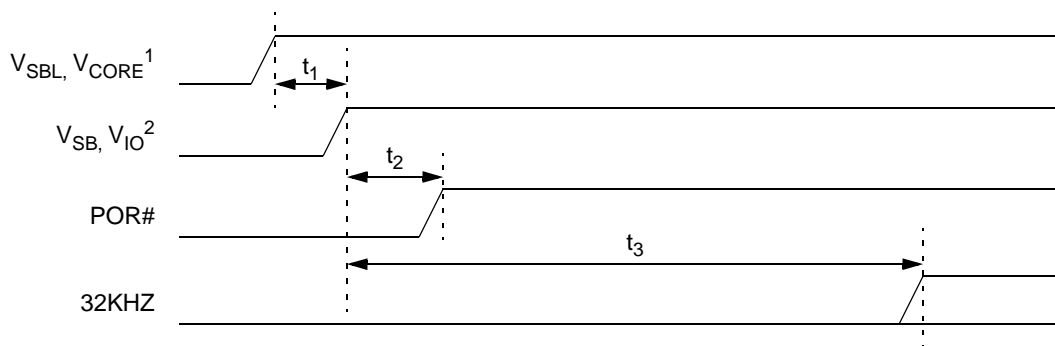


Figure 9-55. Power-Up Sequencing With PWRBTN# Timing Diagram

**Table 9-44. Power-Up Sequence Not Using the Power Button Timing Parameters**

| Symbol | Parameter  | Min  | Max | Unit | Comments  |
|--------|--|------|-----|------|---|
| $t_1$  | Voltage sequence   | -100 | 100 | ms   | Optimum power-up results with $t_1 = 0$ .   |
| $t_2$  | POR# inactive after $V_{SBL}$ , $V_{CORE}$ , $V_{SB}$ , and $V_{IO}$ applied | 50   |     | ms   | POR# must not glitch during active time.  |
| $t_3$  | 32KHZ startup time   |      | 1   | s    | Time required for 32 KHz oscillator and 14.318 MHz derived from PLL6 to become stable at which time the RTC can reliably count. |



- 1)  $V_{SBL}$  and  $V_{CORE}$  should be tied together.
- 2)  $V_{SB}$  and  $V_{IO}$  should be tied together.

**Figure 9-56. Power-Up Sequencing Without PWRBTN# Timing Diagram**

ACPI is non-functional and all ACPI outputs are undefined when the power-up sequence does not include using the power button. SUSP# is an internal signal generated from the ACPI block. Without an ACPI reset, SUSP# can be permanently asserted. If the USE\_SUSP bit in CCR2 of GX1 module is enabled (Index C2h[7] = 1), the CPU will stop.

If ACPI functionality is desired, or the situation described above avoided, the power button must be toggled. This can be done externally or internally. GPIO63 is internally connected to PWRBTN#. To toggle the power button with software, GPIO63 must be programmed as an output using the normal GPIO programming protocol (see Section 6.4.1.1 "GPIO Support Registers" on page 240). GPIO63 must be pulsed low for at least 16 ms and not more than 4 sec.

Asserting POR# has no effect on ACPI. If POR# is asserted and ACPI was active prior to POR#, then ACPI will remain active after POR#. Therefore, BIOS must ensure that ACPI is inactive before GPIO63 is pulsed low.

9.3.16 JTAG Interface

Table 9-45. JTAG Timing Parameters

| Symbol   | Parameter                    | Min | Max | Unit | Comments   |
|----------|------------------------------|-----|-----|------|------------|
|          | TCK frequency                |     | 25  | MHz  |            |
| $t_1$    | TCK period                   | 40  |     | ns   |            |
| $t_2$    | TCK high time                | 10  |     | ns   |            |
| $t_3$    | TCK low time                 | 10  |     | ns   |            |
| $t_4$    | TCK rise time                |     | 4   | ns   |            |
| $t_5$    | TCK fall time                |     | 4   | ns   |            |
| $t_6$    | TDO valid delay              | 3   | 25  | ns   |            |
| $t_7$    | Non-test outputs valid delay | 3   | 25  | ns   | 50 pF load |
| $t_8$    | TDO float delay              |     | 30  | ns   |            |
| $t_9$    | Non-test outputs float delay |     | 36  | ns   |            |
| $t_{10}$ | TDI, TMS setup time          | 8   |     | ns   |            |
| $t_{11}$ | Non-test inputs setup time   | 8   |     | ns   |            |
| $t_{12}$ | TDI, TMS hold time           | 7   |     | ns   |            |
| $t_{13}$ | Non-test inputs hold time    | 7   |     | ns   |            |

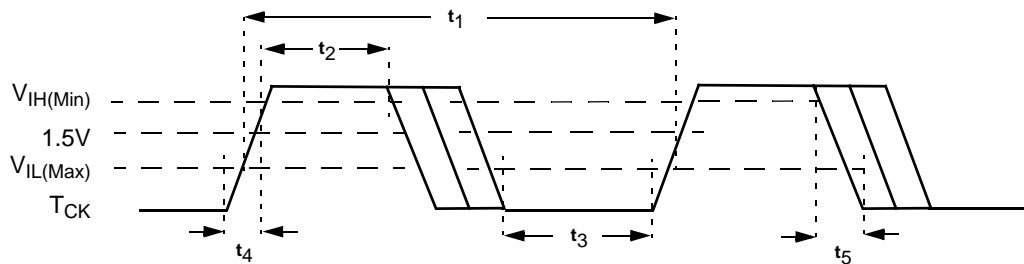


Figure 9-57. TCK Measurement Points and Timing Diagram

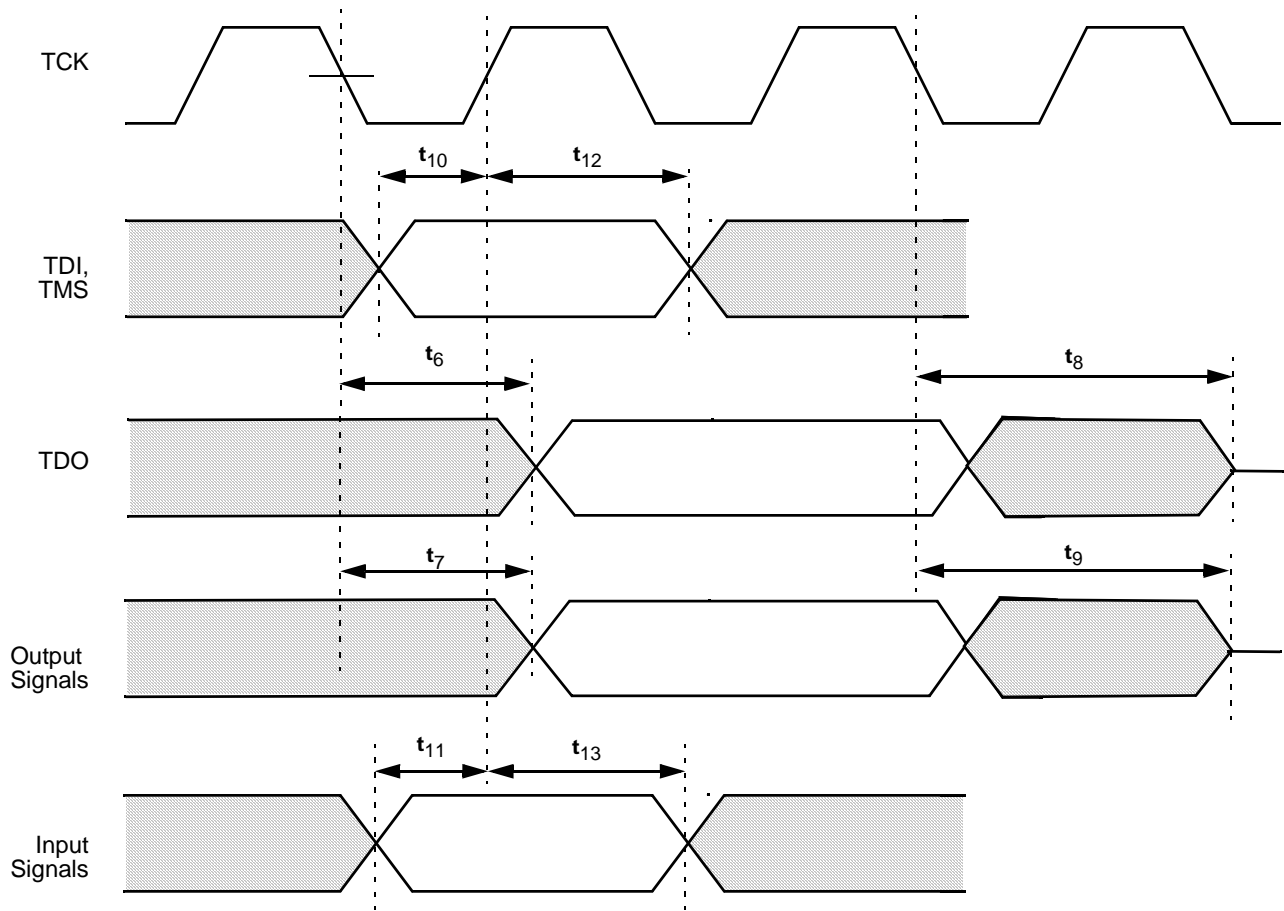


Figure 9-58. JTAG Test Timing Diagram



# 10 Package Specifications

## 10.1 Thermal Characteristics

The junction-to-case thermal resistance ( $\theta_{JC}$ ) of the packages shown in Table 10-1 can be used to calculate the junction (die) temperature under any given circumstance.

**Table 10-1.  $\theta_{JC}$  ( $\times C/W$ )**

| Package | Max ( $^{\circ}C/W$ ) |
|---------|-----------------------|
| EBGA    | 1                     |
| TEPBGA  | 5                     |

Note that there is no specification for maximum junction temperature given since the operation of the device is guaranteed to a case temperature range of  $0^{\circ}C$  to  $85^{\circ}C$  (see Table 9-3 on page 370). As long as the case temperature of the device is maintained within this range, the junction temperature of the die will also be maintained within its allowable operating range. However, the die (junction) temperature under a given operating condition can be calculated by using the following equation:

$$T_J = T_C + (P * \theta_{JC})$$

where:

$T_J$  = Junction temperature ( $^{\circ}C$ )

$T_C$  = Case temperature at top center of package ( $^{\circ}C$ )

$P$  = Maximum power dissipation (W)

$\theta_{JC}$  = Junction-to-case thermal resistance ( $^{\circ}C/W$ )

These examples are given for reference only. The actual value used for maximum power ( $P$ ) and ambient temperature ( $T_A$ ) is determined by the system designer based on system configuration, extremes of the operating environment, and whether active thermal management (via Suspend Modulation) of the GX1 module is employed.

A maximum junction temperature is not specified since a maximum case temperature is. Therefore, the following equation can be used to calculate the maximum thermal resistance required of the thermal solution for a given maximum ambient temperature:

$$\theta_{CS} + \theta_{SA} = \frac{T_C - T_A}{P}$$

where:

$\theta_{CS}$  = Max case-to-heatsink thermal resistance ( $^{\circ}C/W$ ) allowed for thermal solution

$\theta_{SA}$  = Max heatsink-to-ambient thermal resistance ( $^{\circ}C/W$ ) allowed for thermal solution

$T_A$  = Max ambient temperature ( $^{\circ}C$ )

$T_C$  = Max case temperature at top center of package ( $^{\circ}C$ )

$P$  = Maximum power dissipation (W)

If thermal grease is used between the case and heatsink,  $\theta_{CS}$  will reduce to about  $0.01^{\circ}C/W$ . Therefore, the above equation can be simplified to:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

where:

$\theta_{CA} = \theta_{SA}$  = Max heatsink-to-ambient thermal resistance ( $^{\circ}C/W$ ) allowed for thermal solution

The calculated  $\theta_{CA}$  value (examples shown in Table 10-2) represents the maximum allowed thermal resistance of the selected cooling solution which is required to maintain the maximum  $T_{CASE}$  (shown in Table 9-3 on page 370) for the application in which the device is used.

**Table 10-2. Case-to-Ambient Thermal Resistance Example @  $85^{\circ}C$**

| Core Voltage ( $V_{CORE}$ ) (Nominal) | Core Frequency | Maximum Power (W) | $\theta_{CA}$ for Different Ambient Temperatures ( $^{\circ}C/W$ ) |               |               |               |               |
|---------------------------------------|----------------|-------------------|--|---------------|---------------|---------------|---------------|
|                                       |                |                   | $20^{\circ}C$  | $25^{\circ}C$ | $30^{\circ}C$ | $35^{\circ}C$ | $40^{\circ}C$ |
| 1.8V                                  | 266 MHz        | 3.32              | 19.58  | 18.07         | 16.57         | 15.06         | 13.55         |

### 10.1.1 Heatsink Considerations

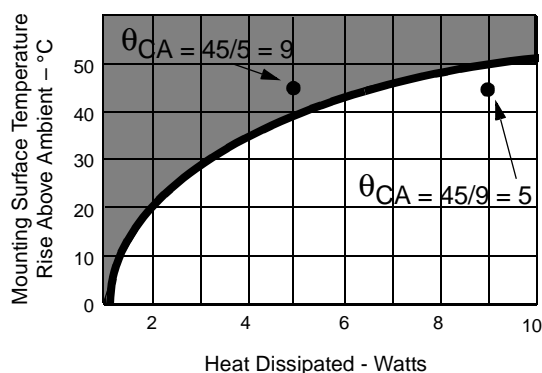
Table 10-2 on page 439 shows the maximum allowed thermal resistance of a heatsink for particular operating environments. The calculated values, defined as  $\theta_{CA}$ , represent the required ability of a particular heatsink to transfer heat generated by the SC3200 processor from its case into the air, thereby maintaining the case temperature at or below 85°C. Because  $\theta_{CA}$  is a measure of thermal resistivity, it is inversely proportional to the heatsinks ability to dissipate heat or its thermal conductivity.

**Note:** A “perfect” heatsink would be able to maintain a case temperature equal to that of the ambient air inside the system chassis.

Looking at Table 10-2, it can be seen that as ambient temperature ( $T_A$ ) increases,  $\theta_{CA}$  decreases, and that as power consumption of the processor ( $P$ ) increases,  $\theta_{CA}$  decreases. Thus, the ability of the heatsink to dissipate thermal energy must increase as the processor power increases and as the temperature inside the enclosure increases.

While  $\theta_{CA}$  is a useful parameter to calculate, heatsinks are not typically specified in terms of a single  $\theta_{CA}$ . This is because the thermal resistivity of a heatsink is not constant across power or temperature. In fact, heatsinks become slightly less efficient as the amount of heat they are trying to dissipate increases. For this reason, heatsinks are typically specified by graphs that plot heat dissipation (in watts) vs. mounting surface (case) temperature rise above ambient (in °C). This method is necessary because ambient and case temperatures fluctuate constantly during normal operation of the system. The system designer must be careful to choose the proper heatsink by matching the required  $\theta_{CA}$  with the thermal dissipation curve of the device under the entire range of operating conditions in order to make sure that the maximum case temperature (from Table 9-3 on page 370) is never exceeded. To choose the proper heatsink, the system designer must make sure that the calculated  $\theta_{CA}$  falls above the curve (shaded area). The curve itself defines the minimum temperature rise above ambient that the heatsink can maintain.

Figure 10-1 is an example of a particular heatsink under consideration



**Figure 10-1. Heatsink Example**

#### Example 1

Assume  $P$  (max) = 5W and  $T_A$  (max) = 40°C.

Therefore:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

$$\theta_{CA} = \frac{85 - 40}{5}$$

$$\theta_{CA} = 9$$

The heatsink must provide a thermal resistance below 9°C/W. In this case, the heatsink under consideration is more than adequate since at 5W worst case, it can limit the case temperature rise above ambient to 40°C ( $\theta_{CA} = 8$ ).

#### Example 2

Assume  $P$  (max) = 9W and  $T_A$  (max) = 40°C.

Therefore:

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

$$\theta_{CA} = \frac{85 - 40}{9}$$

$$\theta_{CA} = 5$$

In this case, the heatsink under consideration is NOT adequate to limit the case temperature rise above ambient to 45°C for a 9W processor.

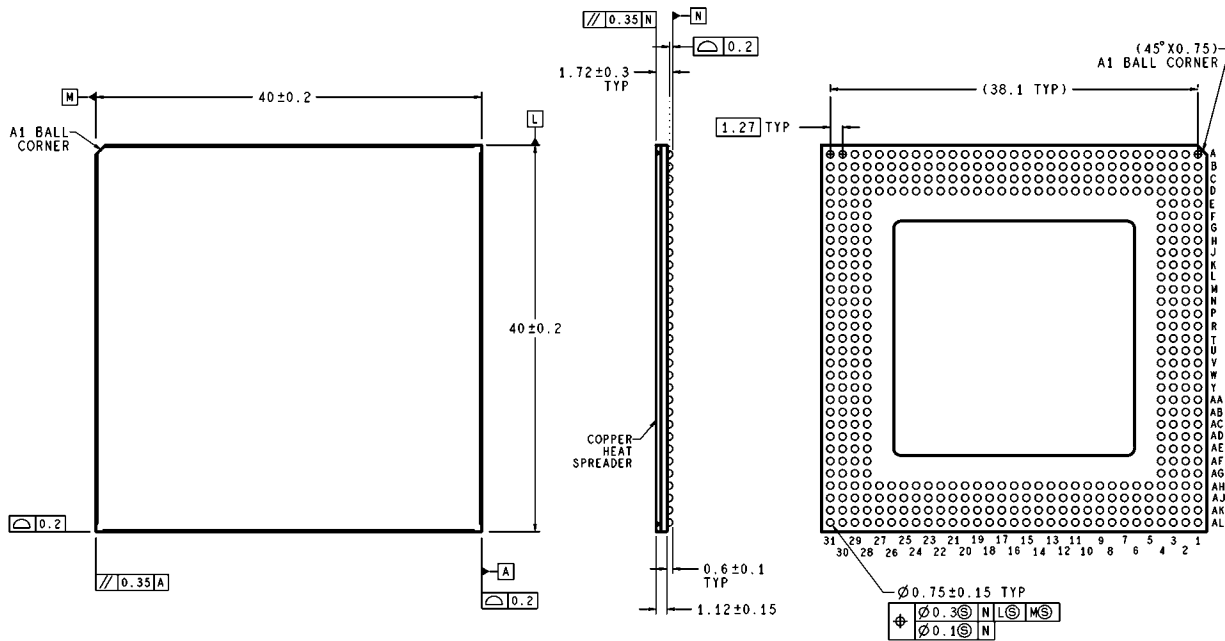
For more information on thermal design considerations or heatsink properties, refer to the Product Selection Guide of any leading vendor of thermal engineering solutions.

**Note:** The power dissipations  $P$  used in these examples are not representative of the power dissipation of the SC3200 processor, which is always less than 4 Watts.



## 10.2 Physical Dimensions

The figures in this section provide the mechanical package outlines for the 432-Terminal EBGA (Enhanced Ball Grid Array) and 481-Terminal TEPBGA (Thermally Enhanced Ball Grid Array) packages.



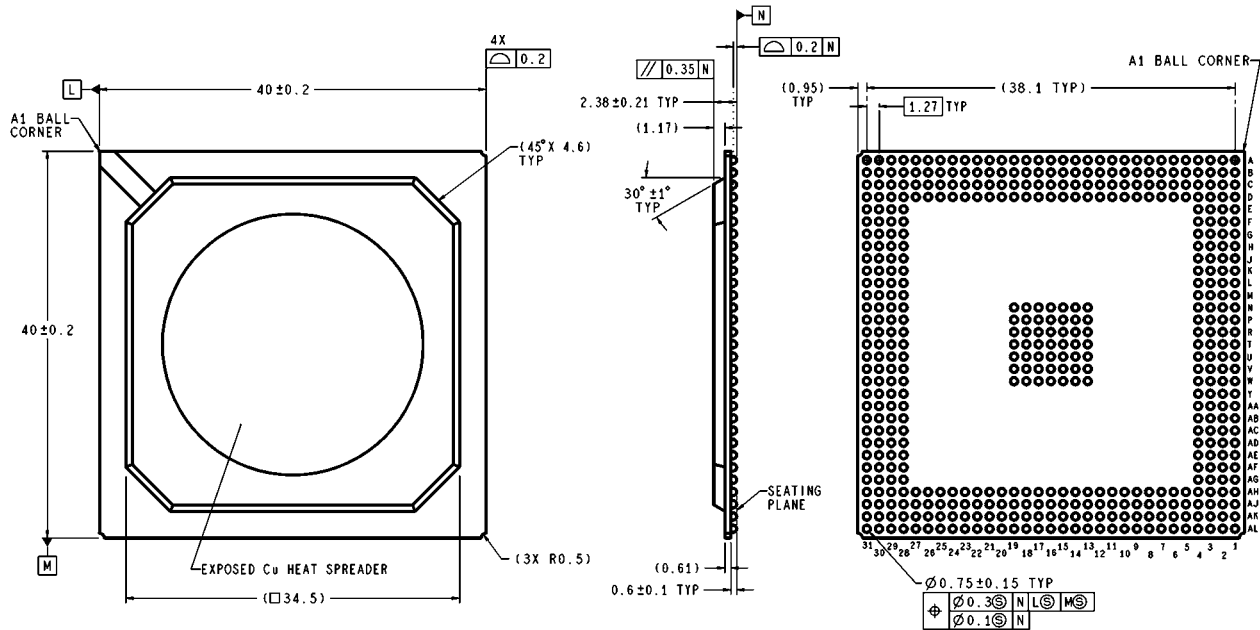
DIMENSIONS ARE IN MILLIMETERS

LCL432A (Rev B)

**NOTES:** UNLESS OTHERWISE SPECIFIED.

- 1) EBGA WITH LEAD (PB):
  - a) SOLDER BALL COMPOSITION: SN 63%, PB 37%.
  - b) SOLDERING PROFILE:  $220^\circ$  C.
- 2) EBGA LEAD (PB) FREE:
  - a) SOLDER BALL COMPOSITION: SN 96.5%, AG 3.5%.
  - b) SOLDERING PROFILE:  $260^\circ$  C
- 3) DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM N.
- 4) REFERENCE JEDEC REGISTRATION MO-151, VARIATION -1.00, DATED JUNE 1997.
- 5) THETA JUNCTION TO CASE ( $T_{JC}$ ) =  $1^\circ$ C/WATT.

**Figure 10-2. 432-Terminal EBGA Package (Body Size: 40x40x1.72 mm; Pitch: 1.27 mm)**



DIMENSIONS ARE IN MILLIMETERS

UFH481A (Rev A)

**NOTES:** UNLESS OTHERWISE SPECIFIED.

- 1) TEPBGA WITH LEAD (PB):
  - a) SOLDER BALL COMPOSITION: SN 63%, PB 37%.
  - b) SOLDERING PROFILE:  $220^\circ$  C.
- 2) TEPBGA LEAD (PB) FREE:
  - a) SOLDER BALL COMPOSITION: SN 96.5%, AG 3.5%.
  - b) SOLDERING PROFILE:  $260^\circ$  C
- 3) DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM N.
- 4) THE MOLD SURFACE AREA MAY INCLUDE DIMPLE FOR A1 BALL CORNER IDENTIFICATION.
- 5) REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAU-1.
- 6) THETA JUNCTION TO CASE ( $T_{JC}$ ) =  $5^\circ$ C/WATT.

**Figure 10-3. 481-Terminal TEPBGA Package (Body Size: 40x40x2.38 mm; Pitch: 1.27 mm)**

# Support Documentation

## A.1 Order Information

| Order Number (AMD OPN) <sup>1</sup> | Core Frequency (MHz) | Core Voltage (V <sub>CORE</sub> ) | Temp. (Degree C) | Package <sup>2</sup> |
|-------------------------------------|----------------------|-----------------------------------|------------------|----------------------|
| SC3200UCL-266                       | 266                  | 1.8V                              | 0 - 85           | EBGA                 |
| SC3200UCL-266F                      |                      |                                   |                  | Lead Free EBGA       |
| SC3200UFH-233                       | 233                  | 1.8V                              | 0 - 85           | TEPBGA               |
| SC3200UFH-233F                      |                      |                                   |                  | Lead Free TEPBGA     |
| SC3200UFH-266                       | 266                  | 1.8V                              | 0 - 85           | TEPBGA               |
| SC3200UFH-266F                      |                      |                                   |                  | Lead Free TEPBGA     |

1. The "F" suffix denotes the lead free package.
2. As of this publication date, a lead free package version may not be available. Check with your local AMD Sales Representative for availability. See Section 10.0 "Package Specifications" on page 439 for details on the lead free part.

## A.2 Data Book Revision History

This document is a report of the revision/creation process of the data book for the Geode SC3200. Any revisions (i.e., additions, deletions, parameter corrections, etc.) are recorded in the table below.

**Table A-1. Revision History**

| Revision # (PDF Date)   | Revisions / Comments  |
|-------------------------|---|
| 0.1<br>(August 1999)    | First draft of data book. (For internal review only)  |
| 0.2<br>(October 1999)   | Second draft.   |
| 0.5<br>(January 2000)   | Draft.  |
| 0.8<br>(March 2000)     | Draft   |
| 1.0<br>(July 2000)      | Preliminary data book.  |
| 1.1<br>(August 2000)    | Corrected typos, removed unimplemented features.  |
| 1.32<br>(February 2001) | Preliminary data book. GNT[1:0]# strapping functions changed. Minor modifications and corrections. Video Input Port (VIP) added.  |
| 2.0<br>(April 2002)     | The entire data book has been reformatted and several sections re-written. Strap information and TEPBGA ball assignments have been added. Additionally, internal test signals and multiplexing have been included. This data book should be viewed as a new document. |

**Table A-1. Revision History (Continued)**

| <b>Revision #<br/>(PDF Date)</b> | <b>Revisions / Comments</b>  |
|----------------------------------|--|
| 2.1<br>(June 2002)               | Release for posting on external web site. Changes made to the Architecture Overview, Signal Definitions, Core Logic Module, Video Processor Module, Electrical Specifications, and Package Specifications chapters. See Revision 2.1 for details.  |
| 2.2<br>(July 2002)               | Corrected pin definitions for ball K3 on EBGA package and ball D12 on TEPBGA package. Were incorrectly called out as VIO, changed to VCORE. Effected:<br>Figure 2-2 "432-EBGA Ball Assignment Diagram"<br>Table 2-2 "432-EBGA Ball Assignment - Sorted by Ball Number"<br>Table 2-3 "432-EBGA Ball Assignment - Sorted Alphabetically by Signal Name"<br>Figure 2-3 "481-TEPBGA Ball Assignment Diagram"<br>Table 2-4 "481-TEPBGA Ball Assignment - Sorted by Ball Number"<br>Table 2-5 "481-TEPBGA Ball Assignment - Sorted Alphabetically by Signal Name"<br>Section 2.4.20 "Power, Ground and No Connections" |
| 3.0<br>(August 2002)             | Major corrections include fixing TEPBGA ball numbers in "Two-Signal/Group Multiplexing" table (Table 2-7) and GPIO signal descriptions (Table 2.4.16).   |
| 3.1<br>(February 2002)           | Many minor changes mostly to the Video Processor and Electrical sections. Expounded on the notes in the Mechanical section.  |
| 4.0<br>(March 2003)              | Many changes. Changed all references to XpressAUDIO to audio. See revision 4.0 for details.  |
| 5.0<br>(November 2003)           | Numerous minor changes/corrections made based upon user inputs. See revision 5.0 for details.  |
| 5.1<br>(March 2004)              | Minor changes/corrections made based upon user inputs. See Table A-2 "Edits to Current Revision" for details.  |

Table A-2. Edits to Current Revision

| Section   | Revision   |
|---|--|
| <b>Section 1.0</b><br>"AMD Geode™<br>SC3200<br>Processor" | <ul style="list-style-type: none"> <li>Section 1.2 "Features" on page 14: <ul style="list-style-type: none"> <li>Other Features: Modified Voltages sub-bullets for clarification purposes.</li> </ul> </li> </ul>  |
| <b>Section 2.0</b><br>"Architecture<br>Overview"          | <ul style="list-style-type: none"> <li>No changes.</li> </ul>  |
| <b>Section 3.0</b><br>"Signal<br>Definitions"             | <ul style="list-style-type: none"> <li>Section 3.4.6 "PCI Bus Interface Signals" on page 68: <ul style="list-style-type: none"> <li>Rewrote SERR# description, was wrong.</li> </ul> </li> <li>Section 3.4.10 "Universal Serial Bus (USB) Interface Signals" on page 76: <ul style="list-style-type: none"> <li>Changed footnote to say "A 15 KΩ pull-down resistor is required on all ports (even if unused)."</li> </ul> </li> </ul>   |
| <b>Section 4.0</b><br>"General<br>Configuration<br>Block" | <ul style="list-style-type: none"> <li>Table 4-7 "Strapped Core Clock Frequency" on page 101: <ul style="list-style-type: none"> <li>Added note: <b>Note:</b> Not all speeds are supported. For information on supported speeds, see Section A.1 "Order Information" on page 443."</li> </ul> </li> </ul>  |
| <b>Section 5.0</b><br>"SuperI/O<br>Module"                | <ul style="list-style-type: none"> <li>No changes.</li> </ul>  |
| <b>Section 6.0</b><br>"Core Logic<br>Module"              | <ul style="list-style-type: none"> <li>Section 6.2.6.1 "DMA Controller" on page 168: <ul style="list-style-type: none"> <li>Added text in parenthesis to first bullet. Now reads as "Standard seven-channel DMA support (Channels 5 through 7 are not supported)."</li> <li>DMA Channels subsection: Added last sentence to last paragraph "DMA Channels 5 through 7 are not supported."</li> </ul> </li> <li>Section 6.2.6.3 "Programmable Interrupt Controller" on page 171: <ul style="list-style-type: none"> <li>Added second sentence to first paragraph, "The PIC devices support all x86 modes of operation except Special Fully Nested mode."</li> </ul> </li> <li>Section 6.4.1 "Bridge, GPIO, and LPC Registers - Function 0" on page 206: <ul style="list-style-type: none"> <li>F0 Index 6Ch (ROM Mask Register): Corrected reset value to 0000FFF0h (was listed as FFF0h). Added note, <b>Note:</b> Register must be read/written as a DWORD." Also corrected reset value and "Width" column in Table 6-14 on page 192 (register summary table).</li> <li>F0BAR1+I/O Offset 00h: Rewrote bit descriptions and added note for clarification purposes.</li> <li>F0BAR1+Offset 0Ch: Rewrote bit descriptions and added note for clarification purposes.</li> <li>F0BAR1+Offset 10h[13]: Changed note. Did say "This bit should not be enabled when using the internal SuperI/O module and if IO_SIOCFG_IN (F5BAR0+I/O Offset 00h[26:25]) = 11." Now says "This bit should not be routed to LPC when using the internal SuperI/O module and if IO_SIOCFG_IN (F5BAR0+I/O Offset 00h[26:25]) = 10."</li> </ul> </li> <li>Section 6.4.2 "SMI Status and ACPI Registers - Function 1" on page 252: <ul style="list-style-type: none"> <li>F1BAR0+I/O Offset 00h[11] and Offset 02h[11]: Clarified that the IRQ2 is from the SIO module and not an external SIO.</li> </ul> </li> <li>Section 6.4.3 "IDE Controller Registers - Function 2" on page 273: <ul style="list-style-type: none"> <li>F2 Index 40h and 44h: Removed Format 0 and Format 1 settings for a Fast-PCI clock frequency of 48 MHz since it is not supported.</li> </ul> </li> <li>Section 6.4.7 "ISA Legacy Register Space" on page 313: <ul style="list-style-type: none"> <li>Changed register descriptions in Table 6-43 and Table 6-44 to emphasize that DMA Channels 5 through 7 are not supported.</li> </ul> </li> </ul> |
| <b>Section 7.0</b><br>"Video<br>Processor<br>Module"      | <ul style="list-style-type: none"> <li>No changes.</li> </ul>  |

Table A-2. Edits to Current Revision (Continued)

| Section   | Revision  |
|---|---|
| <b>Section 8.0</b><br>“Debugging and Monitoring”  | <ul style="list-style-type: none"> <li>No changes.</li> </ul>   |
| <b>Section 9.0</b><br>“Electrical Specifications” | <ul style="list-style-type: none"> <li>Table 9-2 "Absolute Maximum Ratings" on page 369: <ul style="list-style-type: none"> <li>— Changed T<sub>CASE</sub> Min value from -45°C to -10°C.</li> </ul> </li> </ul>  |
| <b>Section 10.0</b><br>“Package Specifications”   | <ul style="list-style-type: none"> <li>Section 10.1 "Thermal Characteristics" on page 439: <ul style="list-style-type: none"> <li>— New section.</li> </ul> </li> <li>Figure 10-3 "481-Terminal TEPBGA Package (Body Size: 40x40x2.38 mm; Pitch: 1.27 mm)" on page 442: <ul style="list-style-type: none"> <li>— Removed lot code example from figure.</li> </ul> </li> </ul> |
| <b>Appendix A</b><br>“Support Documentation”      | <ul style="list-style-type: none"> <li>Updated edits to reflect current revision.</li> </ul>  |



**www.amd.com**

One AMD Place  
P.O. Box 3453  
Sunnyvale, CA 94088-3453 USA  
Tel: 408-732-2400 or 800-538-8450  
TWX: 910-339-9280  
TELEX: 34-6306

**TECHNICAL SUPPORT**

USA & Canada: 800-222-9323 or 408-749-5703  
USA & Canada: PC Microprocessor: 408-749-3060  
USA & Canada Email: pcs.support@amd.com  
Latin America Email: spanish.support@amd.com  
Argentina: 001-800-200-1111, after tone 800-859-4478  
Chile: 800-532-853  
Mexico: 95-800-222-9323

Europe & UK: +44-0-1276-803299  
Fax: +44-0-1276-803298  
France: 0800-908-621  
Germany: +49-89-450-53199  
Italy: 800-877224  
Europe Email: euro.tech@amd.com  
Far East Fax: 852-2956-0588  
Japan Fax: 81-3-3346-7848