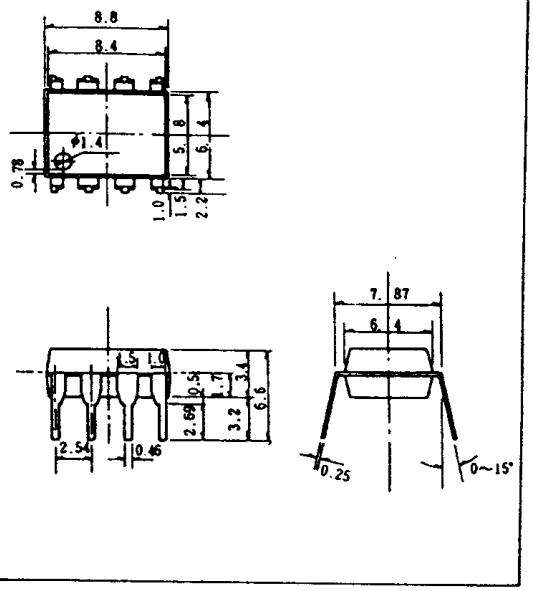
DBL 3842

CURRENT MODE PWM CONTROLLER

The DBL3842, high performance current mode controller, provides the necessary features to off-line and DC-DC fixed frequency current control applications offering the designer a cost effective solution with minimal external components.

Internally protection circurity includes built-in input and reference under-voltage lockout and current limiting with hysteresis. Also other characteristics of internal circuit provide improved line regulation, enhanced load response, trimmed oscillation for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator and totempole output designed to source and sink high peak current from a capacitive load such as the gate of a power MOSFET.

8DIP Unit : mm



☐ FEATURES

- o Optimized for off-line control
- o Low start up and operating current
- o Pulse by pulse current limiting
- o Enhanced load response characteristic
- o Current mode operation to 500KHz
- o Undervoltage lockout with 6V hysteresis
- o Internally trimmed bandgap reference about 5V
- o Automatic feed forward compensation
- o High current totem-pole output

☐ MAXIMUM RATINGS(T_a=25℃)

Characteristics	Symbol	Rating	Unit
Supply Voltage	Vcc	30	V
Current Sense and Vfb Input	Vin	−0.3 to Vcc	V
Total Power Supply and Zener Current	Icc + Iz	30	mA
Output Sink of Source Current	Io	1	A
Error Amp Output Sink Current	Ieo	10	mA
Operating Ambient Temperature	Ta	0 to 70	℃
Storage Temperature Range	Tstg	−65 to 150	℃
Power Dissipation at Ta≤50℃	Pd	1	W

* note) All voltages are with respect to PIN5, and current are positive into the specified pin.

☐ PIN DESCRIPTION

PIN NO	FUNCTION	DESCRIPTION
1	Compensation	Error amplifier output and is made available for loop compensation.
2	Voltage feedback	Inverting input of error amplifier, normally connected to the switching power supply output through a resister driver.
3	Current sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output.
4	Rt/Ct	The oscillator frequency and maximum output duty cycle are programmed by connecting resister Rt to Vref and capacitor Ct to ground.
5	Ground	This pin is the combined control circuitry and power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0A are sourced and sinked by this pin.
7	Vcc	This pin is the positive supply of the control IC.
8	Vref	This is the reference output, it provides charging current for capacitor Ct through resistor Rt.

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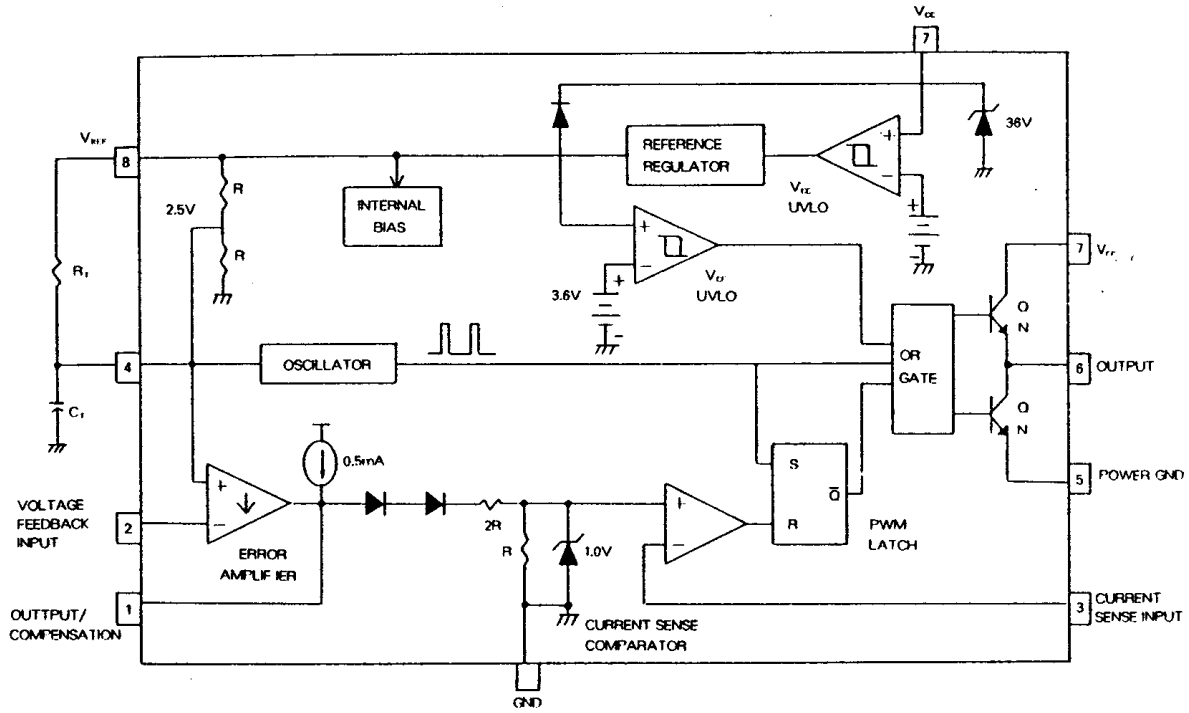
☐ BLOCK DIAGRAM



☐ ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for $0 \leq T_a \leq 70℃$; $V_{CC}=15V$(Note 4), $R_t=10K\Omega$, $C_t=3.3nF$)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1. Reference Section						
Output Voltage	V_{ref}	$T_a=25℃$, $I_o=1mA$	4.90	5.00	5.10	V
Line Regulation	ΔV_{ref}	$12V \leq V_{CC} \leq 25V$		6	20	mV
Load Regulation	ΔV_{ref}	$1 \leq I_o \leq 20mA$		6	25	mV
Temperature Stability	$\Delta V_r/\Delta T$	(Note 1)		0.2	0.4	mV/℃
Output Noise Voltage	Vn	$10Hz \leq f \leq 10KHz$ $T_a=25℃$ (Note 1)		50		μV
Long Term Stability	S	$T_a=125℃$, 1000Hrs(Note 1)		5		mV
Output Short Circuit	I_{sc}		−30	−100	−180	mA

☐ ELECTRICAL CHARACTERISTICS(continued)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
2. Oscillator Section						
Initial Accuracy	f_{sc}	T_a=25℃	47	52	57	KHz
Voltage Stability	$\Delta f/\Delta V$	$12 \le V_a \le 25V$		0.2	1.0	%
Temperature Stability	$\Delta f/\Delta T$	$T_{min} \le T_a \le T_{max}$(Note 1)		5		%
Amplitude	V_4	V_{pin4} Peak to Peak		1.7		V
3. Error Amp Section						
Input Voltage	V_2	V_{pin1}=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_b			−0.3	−2.0	μA
Open loop Voltage Gain	A_{vol}	$2 \le V_0 \le 4V$	65	90		dB
Supply Voltage Rejection	SVR	$12 \le V_a \le 25V$	60	70		dB
Output Sink Current	I_o	V_{pin2}=2.7V, V_{pin1}=1.1V	2	6		mA
Output Source Current	I_o	V_{pin2}=2.3V, V_{pin1}=5V	−0.5	−0.8		mA
V_{out} High	V_{oh}	V_{pin2}=2.3V; R_L=15KΩ to Ground	5	6		V
V_{out} LOW	V_{ol}	V_{pin2}=2.7V; R_L=15KΩ to Pin8		0.7	1.1	V
4. Current Sense Section						
Gain	G_V	(Note 2 & 3)	2.8	3.0	3.2	V/V
Maximum Input Signal	V_3	V_{pin1}=5V(Note 2)	0.9	3.0	1.1	V
Supply Volt Rejection	SVR	$12 \le V_a \le 25V$(Note 2)		70		dB
Input Bias Current	I_b			−2	−10	μA
5. Output Section						
Output Low Level	V_{ol}	I_{sink}=20mA		0.1	0.4	V
		I_{sink}=200mA		1.5	2.2	V
Output High Level	V_{oh}	I_{source}=20mA	13.0	13.5		V
		I_{source}=200mA	12.0	13.5		V
Rise time	t_r	T_a=25℃ Cl=1nF(Note 1)		50	150	ns
Fall time	t_f	T_a=25℃ Cl=1nF(Note 1)		50	150	ns

☐ ELECTRICAL CHARACTERISTICS(continued)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
6. Under-Voltage Lockout Section						
Start Threshold	Vth	Vpin7 where Vpin8≥4.9V	14.5	16.0	17.5	V
Min. Operation Voltage After Turn-on	Vcc(min)	Vpin7 where Vpin8≤1V	8.5	10.0	11.5	V
7. PWM Section						
Maximum Duty Cycle	DC max		93	97	100	ns
8. Total Standby Section						
Start-up Current	Ist	Vcc=14V after turn on		0.5	1.0	mA
Operating Supply Current	Icc	Vpin2=Vpin3=0V		11	20	mA
Zener Voltage	Vz	Icc=25mA		36		V

NOTE : 1. These parameters, although guaranteed, are not 100% tested in production

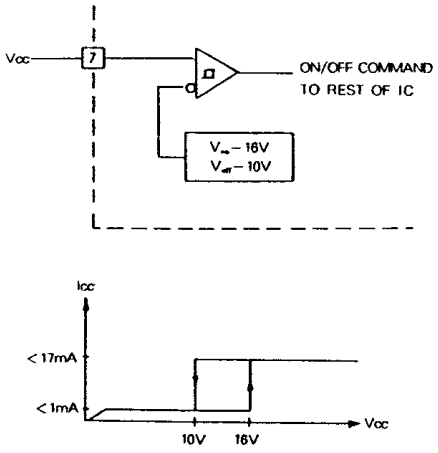
2. Parameter measured at trip point of latch with Vpin2=0

3. Gain defined as : $A=\Delta Vpin1/\Delta Vpin3$; $0\leq Vpin3\leq 0.8V$

4. Adjust Vcc above the start threshould before setting at 15V

☐ INFORMATION IN USING IC

1. UNDERVOLTAGE LOCKOUT

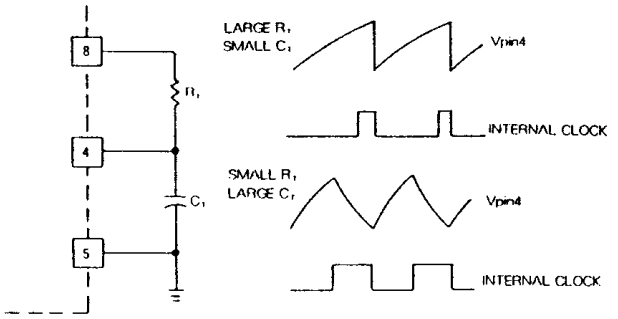


To prevent erratic output behavior which activating the power switch with extraneous leakage currents, during under voltage lock-out. Output(pin6) should be shunted to ground with a bleeder resister.

The Vcc comparator upper and lower threshold are 16V/10V. The large hysteresis and low start up currents makes it ideally suited in off-line converter application where efficient bootstrap start-up techniques are required.

☐ INFORMATION IN USING IC(continued)

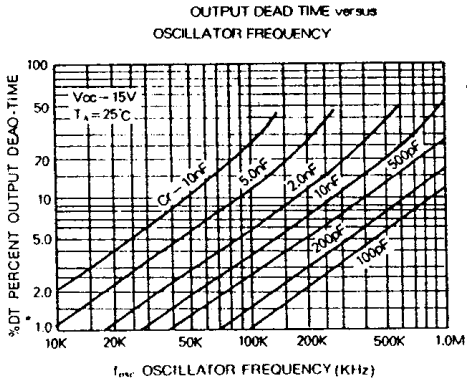
2. OSCILLATOR WAVEFORMS AND MAXIMUM DUTY CYCL

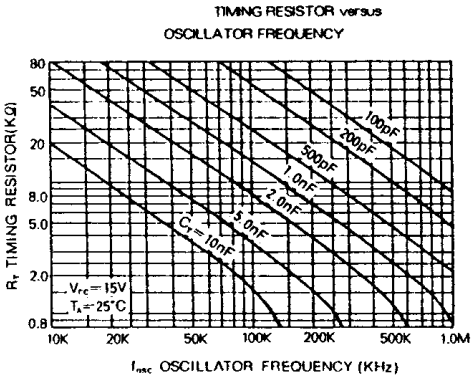


The oscillator frequency is programmed by the values selected for the timing components Rt and Ct. Ct is charged from 5V, Vref, through resistor Rt to approximately 2.8V and discharged to 1.2V by an internal current sink.

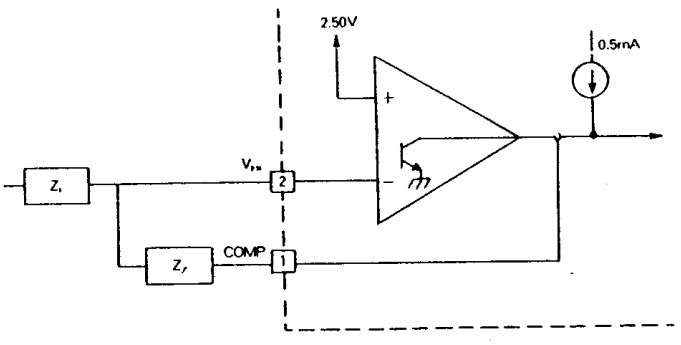
During the dischare of Ct, the oscillator generates an internal blanking pulse and the center input NOR gate high.

This makes output to be in a low state and control the amount of output dead time.





3. ERROR AMP CONFIGURATION



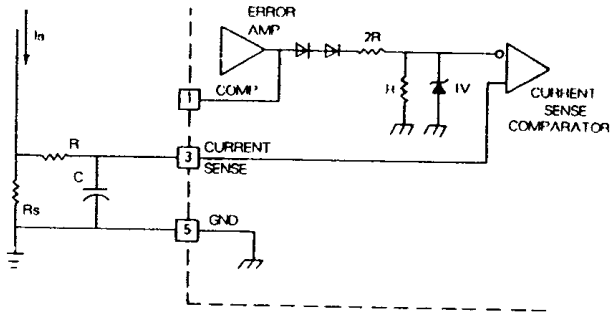
Error amp output(Pin1) is provided for external loop compensation and error amp can source or sink up to 0.5mA. The non-inverting input is internally biased at 2.5V and is not pinned out.

The converter output voltage is typically divided down and monitored by the inverting input(pin2).

☐ INFORMATION IN USING IC(continued)

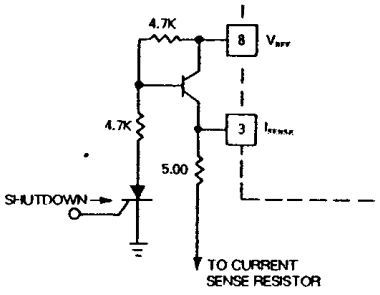
4. CURRENT SENSE CIRCUIT

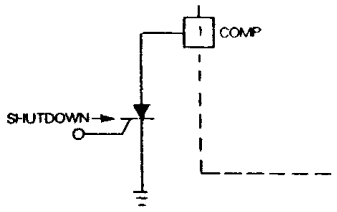
$$Ipeak = \frac{R(Vpin1 - 2Vbe)}{3R \times Rs}$$



A normal operating conditions occurs when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the current sense comparator threshold will be internally clamped to 1.0V Therefore the maximum peak switch current is Ipk(max) = 1.0V/Rs, and under the normal operating conditious the peak inductor current controlled by the voltage at pin1.

5. SHUTDOWN TECHNIQUES



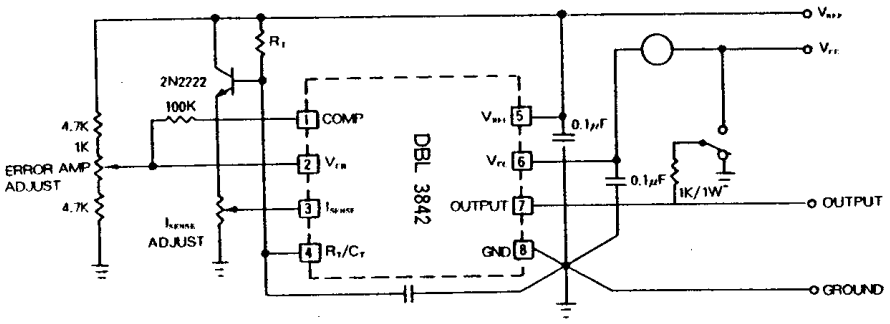


Shutdown of the DBL3842 can be accomplished by two methods; either raise pin3 above 1V or pull pin1 below a voltage two diodes drops above ground. Either method causes the output of the PWM comparator to be high(refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed.

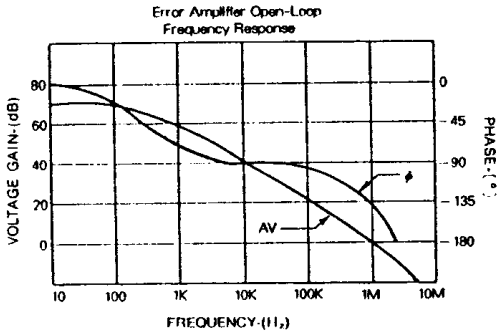
In one example, an externally latched shutdown may be accomplished by adding an SCR which turn off, allowing the SCR to reset.

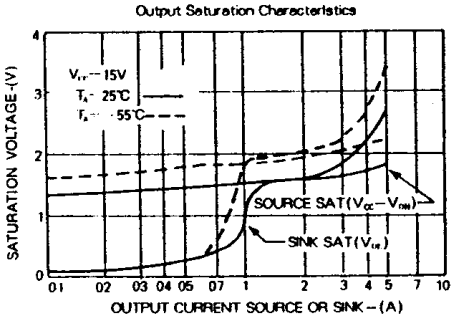
☐ INFORMATION IN USING IC(continued)

6. OPEN LOOP TEST

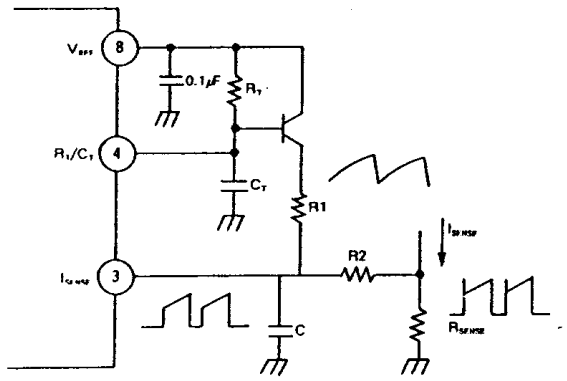


High peak currents associated with capacitive leads necessitate careful grounding techniques. Timing and by-pass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.





7. SLOPE COMPENSATION



A fration of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for coverters requiring duty cycle over 50%. Note that capacitor C, forms a filter with R2 to supress the leading edge switch spikes.