

HD100155

Quad. Multiplexers/Latches

The HD100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (\overline{E}_n) inputs are low, the data that appears at an outputs is controlled by the Select (S_n) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1 , the Select inputs can force the outputs low for the case where the latch is transparent (both Enables are low) and can steer a

high signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1 .

A positive-going signal on either Enable input latches the outputs. A high signal on the Master Reset (MS) input overrides all the other inputs and forces the Q outputs low.

OPERATING MODE TABLE

CONTROLS				OUTPUT
\overline{E}_1	\overline{E}_2	\overline{S}_0	S_1	Q_n
H	x	x	x	latched*
x	H	x	x	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n} + D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

H = High Level
 L = Low Level
 x = Immaterial
 * = Stores data present before E_n went high.

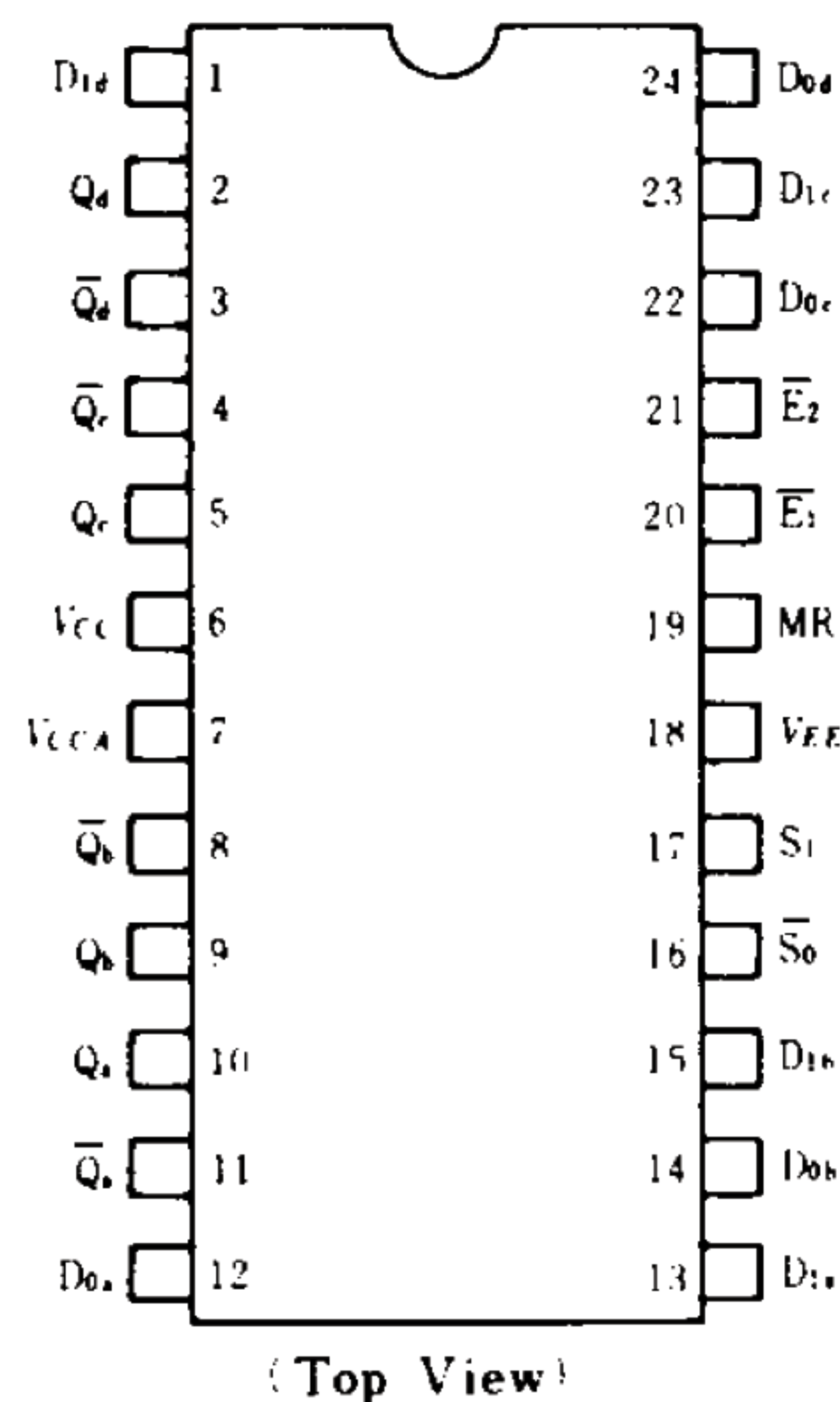
TRUTH TABLE

MR	Input						Output	
	\overline{E}_1	\overline{E}_2	S_1	\overline{S}_0	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	Q_a Q_b Q_c Q_d	Q_a Q_b Q_c Q_d
H	x	x	x	x	x	x	H	L
L	L	L	H	H	H	x	L	H
L	L	L	H	H	L	x	H	L
L	L	L	L	L	x	H	L	H
L	L	L	L	L	x	L	H	L
L	L	L	L	H	x	x	H	L
L	L	L	H	L	H	x	L	H
L	L	L	H	L	x	H	L	H
L	L	L	H	L	L	L	H	L
L	H	x	x	x	x	x	No Change	
L	x	H	x	x	x	x	No Change	

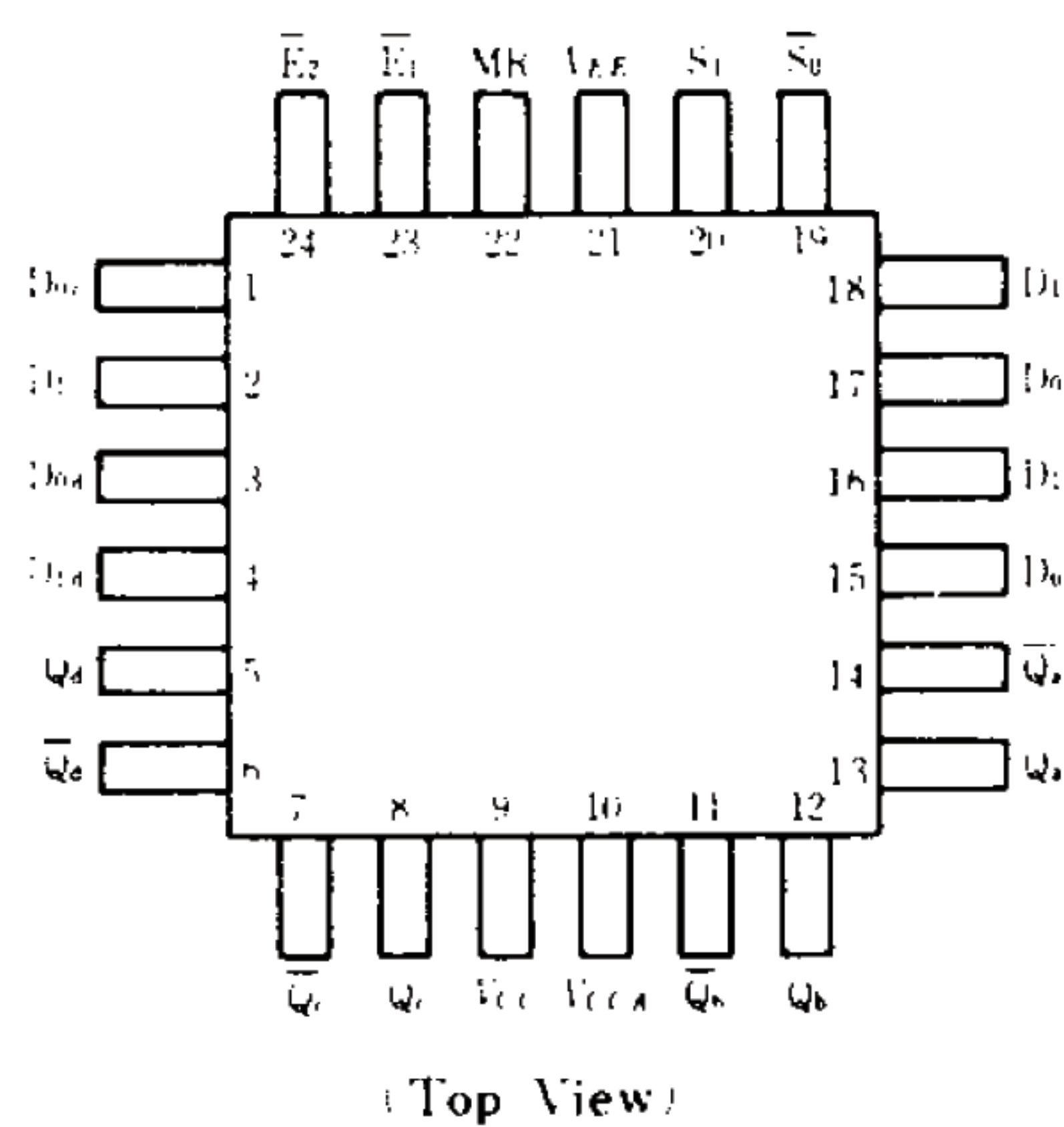
H = High Level
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PIN ARRANGEMENT

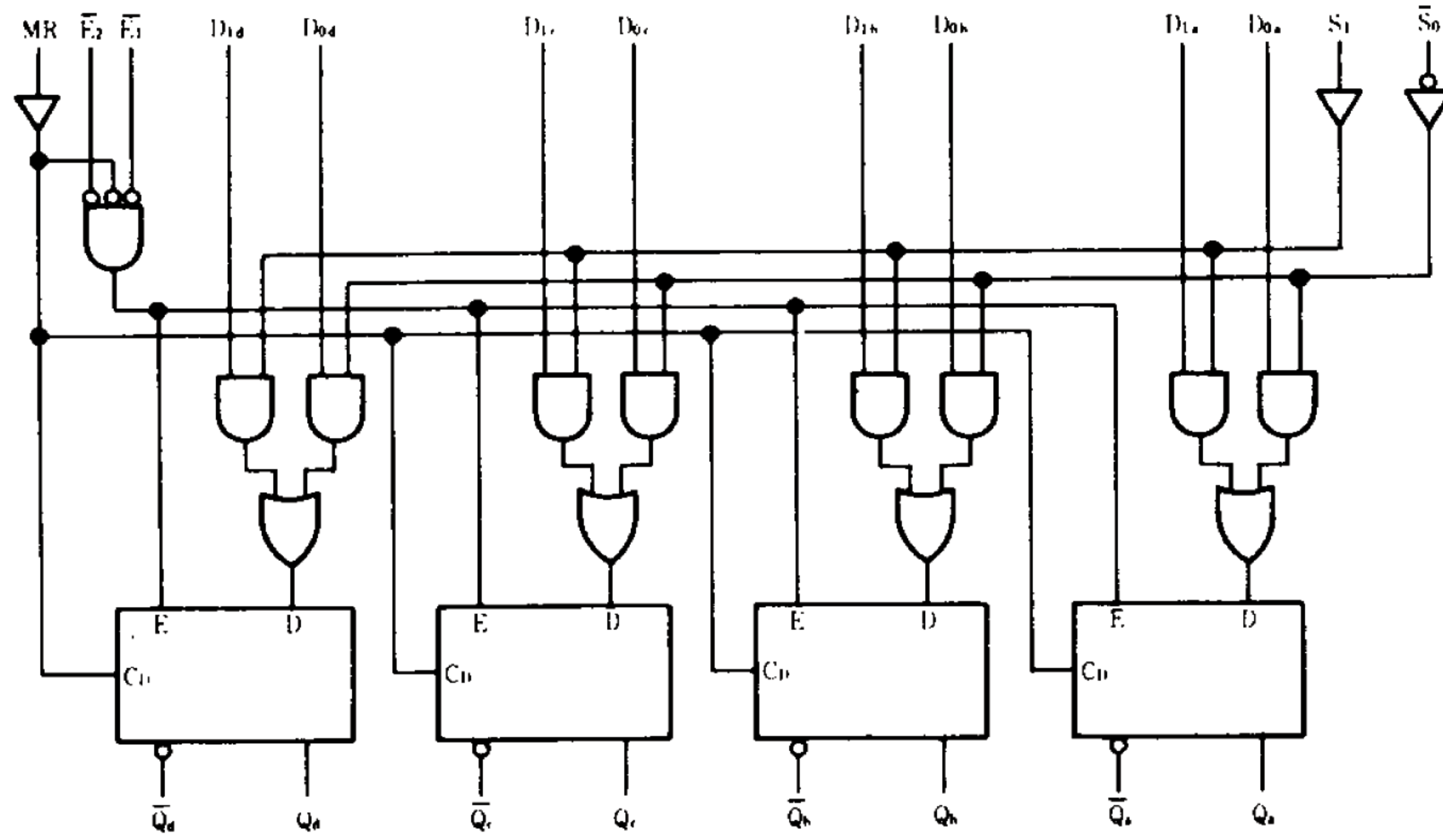
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HD100155F



■ LOGIC DIAGRAM



■ DC CHARACTERISTICS ($V_{EE} = -4.2$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $T_a = 0$ to $+85^\circ C$)

Item	Symbol	Test Condition	min	typ	max	Unit	
Supply Current	I_{EE}	All input open	60	95	133	mA	
Input Current	I_{IH}	$V_{IS} = V_{IH \max}$	S_n input			220	μA
			\bar{E}_n input			350	
			Data input			340	
			MR input			430	

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS ($V_{EE} = -2.2$ to -2.8 V, $V_{CC} = V_{CCA} = 2.0$ V)

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Item	Symbol	Test Condition	0°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	Data input	0.55	1.50	0.60	1.00	1.55	0.60	1.55	ns
			S input	1.40	3.00	1.50	1.80	3.10	1.50	3.10	
			\bar{E} input	0.90	1.90	1.00	1.40	2.00	1.00	2.00	
			MR input	0.95	1.65	1.00	1.70	2.50	1.00	2.50	
Transition Time	t_{TLH}, t_{THL}		0.55	1.75	0.50	1.10	1.65	0.50	1.65	ns	
Setup Time	t_{SU}	See test circuit and waveform	Data input	0.60	—	0.60	—	—	0.60	—	ns
			S input	2.30	—	2.30	—	—	2.30	—	
			MR input (Release Time)	1.30	—	1.50	—	—	1.50	—	
Hold Time	t_H	See test circuit and waveform	Data input	0.50	—	0.40	—	—	0.40	—	ns
			S input	-0.45	—	-0.50	—	—	-0.50	—	
Pulse Width	t_W	See test circuit and waveform	\bar{E}_1, \bar{E}_2 (L)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

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Item	Symbol	Test Condition	0°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	Data input	0.60	1.45	0.70	0.95	1.55	0.70	1.55	ns
			S input	1.50	3.00	1.50	1.80	3.20	1.50	3.20	
			\bar{E} input	0.90	2.10	1.00	1.50	2.20	1.00	2.20	
			MR input	1.00	2.50	1.00	1.60	2.70	1.00	2.70	
Transition Time	t_{TLH}, t_{THL}		0.50	1.65	0.50	1.00	1.65	0.50	1.65	ns	
Setup Time	t_{SU}	See test circuit and waveform	Data input	0.50	—	0.60	—	—	0.60	—	ns
			S input	2.10	—	2.30	—	—	2.30	—	
			MR input (Release Time)	1.20	—	1.40	—	—	1.40	—	
Hold Time	t_H	See test circuit and waveform	Data input	0.30	—	0.30	—	—	0.30	—	ns
			S input	-0.70	—	-0.70	—	—	-0.80	—	
Pulse Width	t_W	See test circuit and waveform	\bar{E}_1, \bar{E}_2 (L)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 m/s (500 linear fpm) is maintained.