

MC145407

Advance Information 5 Volt Only Driver/Receiver EIA-232-E and CCITT V.28

The MC145407 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-E and CCITT V.28 while operating from a single + 5 V power supply. A voltage doubler and inverter convert the + 5 V to ± 10 V. This is accomplished through an on-board 20 kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the MC145407 are virtually identical to those of the MC145406. Therefore, for applications requiring more than three drivers and/or three receivers, an MC145406 can be powered from an MC145407, since the MC145407 charge pumps have been designed to guarantee ± 5 V at the output of up to six drivers. Thus, the MC145407 provides a high-performance, low-power, stand-alone solution or, with the MC145406, a + 5 V only, high-performance two-chip solution.

Drivers

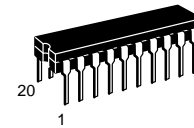
- ± 7.5 V Output Swing
- 300 Ω Power-Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/ μ s to 30 V/ μ s

Receivers

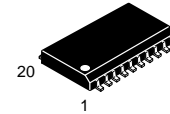
- + 25 V Input Range
- 3 to 7 k Ω Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity

Charge Pumps

- + 5 V to ± 10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On-Chip Drivers and Three Drivers on the MC145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On-Chip 20 kHz Oscillator



P SUFFIX
PLASTIC DIP
CASE 738

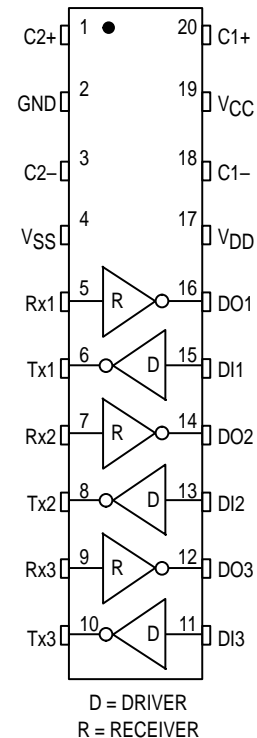


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

| | |
|------------|-------------|
| MC145407P | Plastic DIP |
| MC145407DW | SOG Package |

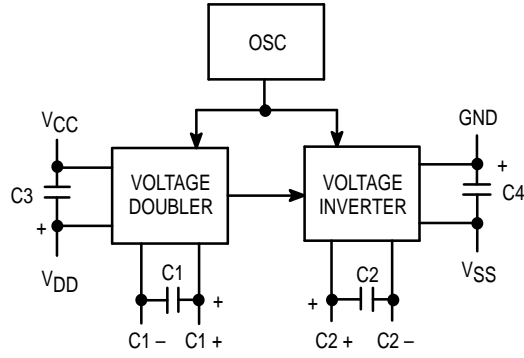
PIN ASSIGNMENT



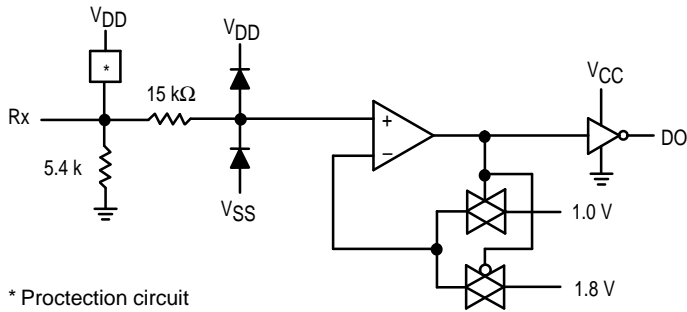
This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTION DIAGRAM

CHARGE PUMPS

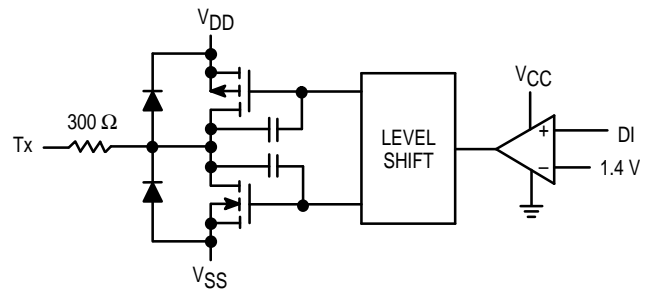


RECEIVER



* Protection circuit

DRIVER



MAXIMUM RATINGS (Voltage polarities referenced to GND)

| Rating | Symbol | Value | Unit |
|---|-----------|---|------|
| DC Supply Voltages | V_{CC} | - 0.5 to + 6.0 | V |
| Input Voltage Range Rx1 – Rx3 Inputs DI1 – DI3 Inputs | V_{IR} | $V_{SS} - 15$ to $V_{DD} + 15$ - 0.5 to $(V_{CC} + 0.5)$ | V |
| DC Current per Pin | I | ± 100 | mA |
| Power Dissipation | P_D | 1 | W |
| Operating Temperature Range | T_A | - 40 to + 85 | °C |
| Storage Temperature Range | T_{stg} | - 85 to + 150 | °C |

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{CC}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15 V) \leq V_{Rx1} - Rx3 \leq (V_{DD} + 15 V)$, and Tx should be constrained to $V_{SS} \leq V_{Tx1} - Tx3 \leq V_{DD}$.

Unused inputs must always be tied to appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; C1, C2, C3, C4 = 10 μ F; T_A = - 40 to + 85°C)

| Parameter | Symbol | Min | Typ | Max | Unit | |
|--|----------|--------------------|-------|-------|------|---|
| DC Supply Voltage | V_{CC} | 4.5 | 5 | 5.5 | V | |
| Quiescent Supply Current (Outputs unloaded, inputs low) | I_{CC} | — | 1.2 | 3.0 | mA | |
| Output Voltage | V_{DD} | $I_{load} = 0$ mA | 8.5 | 10 | 11 | V |
| | | $I_{load} = 5$ mA | 7.5 | 9.5 | — | |
| | | $I_{load} = 10$ mA | 6 | 9 | — | |
| | V_{SS} | $I_{load} = 0$ mA | - 8.5 | - 10 | - 11 | |
| | | $I_{load} = 5$ mA | - 7.5 | - 9.2 | — | |
| | | $I_{load} = 10$ mA | - 6 | - 8.6 | — | |

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; $V_{CC} = + 5 V \pm 10\%$; C1, C2, C3, C4 = 10 μ F; T_A = - 40 to + 85°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|------------------------|----------------------------------|-------------|------------|------------|
| Input Turn-on Threshold $V_{DO1} - DO3 = V_{OL}$ | Rx1 – Rx3 V_{on} | 1.35 | 1.8 | 2.35 | V |
| Input Turn-off Threshold $V_{DO1} - DO3 = V_{OH}$ | Rx1 – Rx3 V_{off} | 0.75 | 1.0 | 1.25 | V |
| Input Threshold Hysteresis ($V_{on} - V_{off}$) | Rx1 – Rx3 V_{hys} | 0.6 | 0.8 | — | V |
| Input Resistance | Rx1 – Rx3 R_{in} | 3.0 | 5.4 | 7.0 | k Ω |
| High-Level Output Voltage $V_{Rx1} - Rx3 = - 3 V$ to $- 25 V$ $I_{OH} = - 20 \mu A$ $I_{OH} = - 1 mA$ | DO1 – DO3 V_{OH} | $V_{CC} - 0.1$ $V_{CC} - 0.7$ | — 4.3 | — — | V |
| Low-Level Output Voltage $V_{Rx1} - Rx3 = + 3 V$ to $+ 25 V$ $I_{OL} = + 20 \mu A$ $I_{OL} = + 1.6 mA$ | DO1 – DO3 V_{OL} | — — | 0.01 0.5 | 0.1 0.7 | V |

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V: $V_{CC} = +5\text{ V} \pm 10\%$; C1, C2, C3, C4 = 10 μF ; $T_A = -40$ to $+85^\circ\text{C}$)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|----------|--------------|-----------------------|---------------|
| Digital Input Voltage Logic 0 Logic 1 | DI1 – DI3 V_{IL} V_{IH} | — 2.0 | — — | 0.8 — | V |
| Input Current $GND \leq V_{DI1} - DI3 \leq V_{CC}$ | DI1 – DI3 I_{in} | — | — | ± 1.0 | μA |
| Output High Voltage $V_{DI1} - DI3 = \text{Logic 0}, R_L = 3.0\text{ k}\Omega$ | Tx1 – Tx3 Tx1 – Tx6* | 6 5 | 7.5 6.5 | — — | V |
| Output Low Voltage $V_{DI1} - DI3 = \text{Logic 1}, R_L = 3.0\text{ k}\Omega$ | Tx1 – Tx3 Tx1 – Tx6* | -6 -5 | -7.5 -6.5 | — — | V |
| Off Source Impedance (Figure 1) | Tx1 – Tx3 Z_{off} | 300 | — | — | Ω |
| Output Short-Circuit Current $V_{CC} = +5.5\text{ V}$ | Tx1 – Tx3 Tx1 – Tx3 shorted to GND** Tx1 – Tx3 shorted to $\pm 15\text{ V}$ *** | — — | — — | ± 60 ± 100 | mA |

* Specifications for an MC145407 powering an MC145406 with three additional drivers/receivers.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS ($V_{CC} = +5\text{ V} \pm 10\%$; C1, C2, C3, C4 = 10 μF ; $T_A = -40$ to $+85^\circ\text{C}$; See Figures 2 and 3)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Drivers

| | | | | | |
|--|------------------------|----------|----------|---------------|------------------|
| Propagation Delay Time Low-to-High $R_L = 3\text{ k}\Omega, C_L = 50\text{ pF}$ or 2500 pF High-to-Low $R_L = 3\text{ k}\Omega, C_L = 50\text{ pF}$ or 2500 pF | Tx1 – Tx3 t_{PLH} | — | 0.5 | 1 | μs |
| | t_{PHL} | — | 0.5 | 1 | |
| Output Slew Rate Minimum Load: $R_L = 7\text{ k}\Omega, C_L = 0\text{ pF}$ Maximum Load: $R_L = 3\text{ k}\Omega, C_L = 2500\text{ pF}$ | Tx1 – Tx3 SR | — 4.0 | 9.0 — | ± 30 — | V/ μs |

Receivers ($C_L = 50\text{ pF}$)

| | | | | | |
|--|------------------------|---|-----|-----|---------------|
| Propagation Delay Time Low-to-High High-to-Low | DO1 – DO3 t_{PLH} | — | — | 1 | μs |
| | t_{PHL} | — | — | 1 | |
| Output Rise Time | DO1 – DO3 t_r | — | 250 | 400 | ns |
| Output Fall Time | DO1 – DO3 t_f | — | 40 | 100 | ns |

PIN DESCRIPTIONS

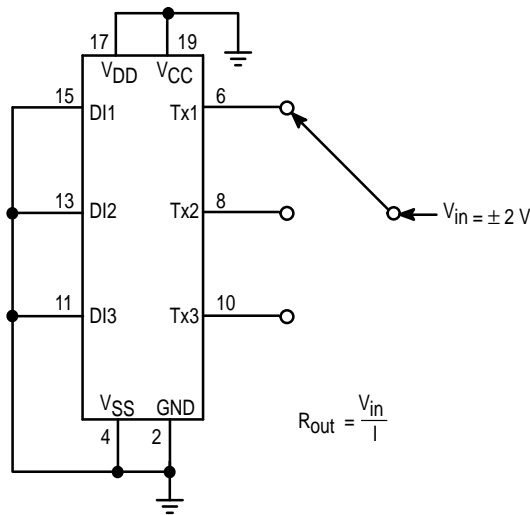


Figure 1. Power-Off Source Resistance

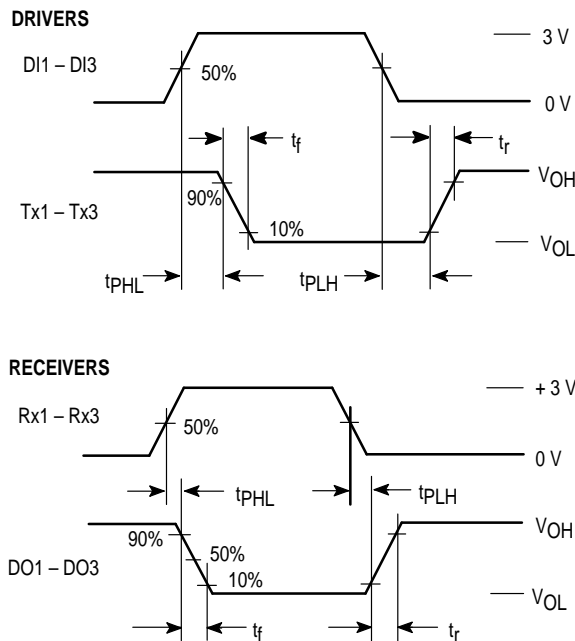


Figure 2. Switching Characteristics

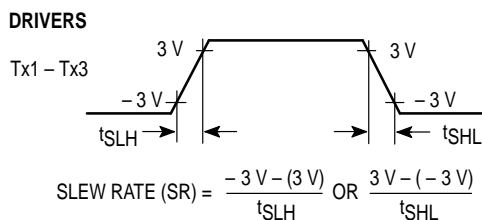


Figure 3. Slew Rate Characterization

VCC Digital Power Supply (Pin 19)

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA-232-E connector (Pin 7) as well as to the logic power supply ground.

VDD Positive Power Supply (Pin 17)

This is the positive output of the on-chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

VSS Negative Power Supply (Pin 4)

This is the negative output of the on-chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2-, C1-, C1+ Voltage Doubler and Inverter (Pins 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the VDD and VSS voltages.

Rx1, Rx2, Rx3 Receive Data Input (Pins 5, 7, 9)

These are the EIA-232-E receive signal inputs. A voltage between +3 and +25 V is decoded as a space and causes the corresponding DO pin to swing to ground (0 V). A voltage between -3 and -25 V is decoded as a mark, and causes the DO pin to swing up to VCC.

DO1, DO2, DO3 Data Output (Pins 16, 14, 12)

These are the receiver digital output pins, which swing from VCC to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3 Data Input (Pins 15, 13, 11)

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between VCC and GND.

Tx1, Tx2, Tx3 Transmit Data Output (Pins 6, 8, 10)

These are the EIA-232-E transmit signal output pins, which swing toward VDD and VSS. A logic 1 at a DI input causes the corresponding Tx output to swing toward VSS. A logic 0 causes the output to swing toward VDD. The actual levels and slew rate achieved will depend on the output loading ($R_L \parallel C_L$).

APPLICATIONS INFORMATION

ESD CONSIDERATIONS

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply busses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 7 shows a technique which will clamp the ESD voltage at approximately + 15 V using the MMBZ15V DLT1. Any residual voltage which appears on the supply pins is shunted to ground through the 0.1 μ F capacitors.

OPERATION WITH SMALLER VALUE CHARGE PUMP CAPS

The MC145407 is characterized in the electrical tables

using 10 μ F charge pump caps to illustrate its capability in driving a companion MC145406 or MC145403. If there is no requirement to support a second interface device and/or the charge pump is not being used to power any other components, the MC145407 is capable of complying with EIA-232-E and V.28 with smaller value charge pump caps. Table 1 summarizes driver performance with both 2.2 μ F and 1.0 μ F charge pump caps.

Table 1. Typical Performance

| Parameter | 2.2 μ F | 1.0 μ F |
|---------------------------|----------------|----------------|
| Tx V _{OH} @ 25°C | 7.3 | 7.2 |
| Tx V _{OH} @ 85°C | 7.2 | 7.1 |
| Tx V _{OL} @ 25°C | -6.5 | -6.4 |
| Tx V _{OL} @ 85°C | -6.1 | -6.0 |
| Tx Slew Rate @ 25°C | 8.0 V/ μ s | 8.0 V/ μ s |
| Tx Slew Rate @ 85°C | 7.0 V/ μ s | 7.0 V/ μ s |

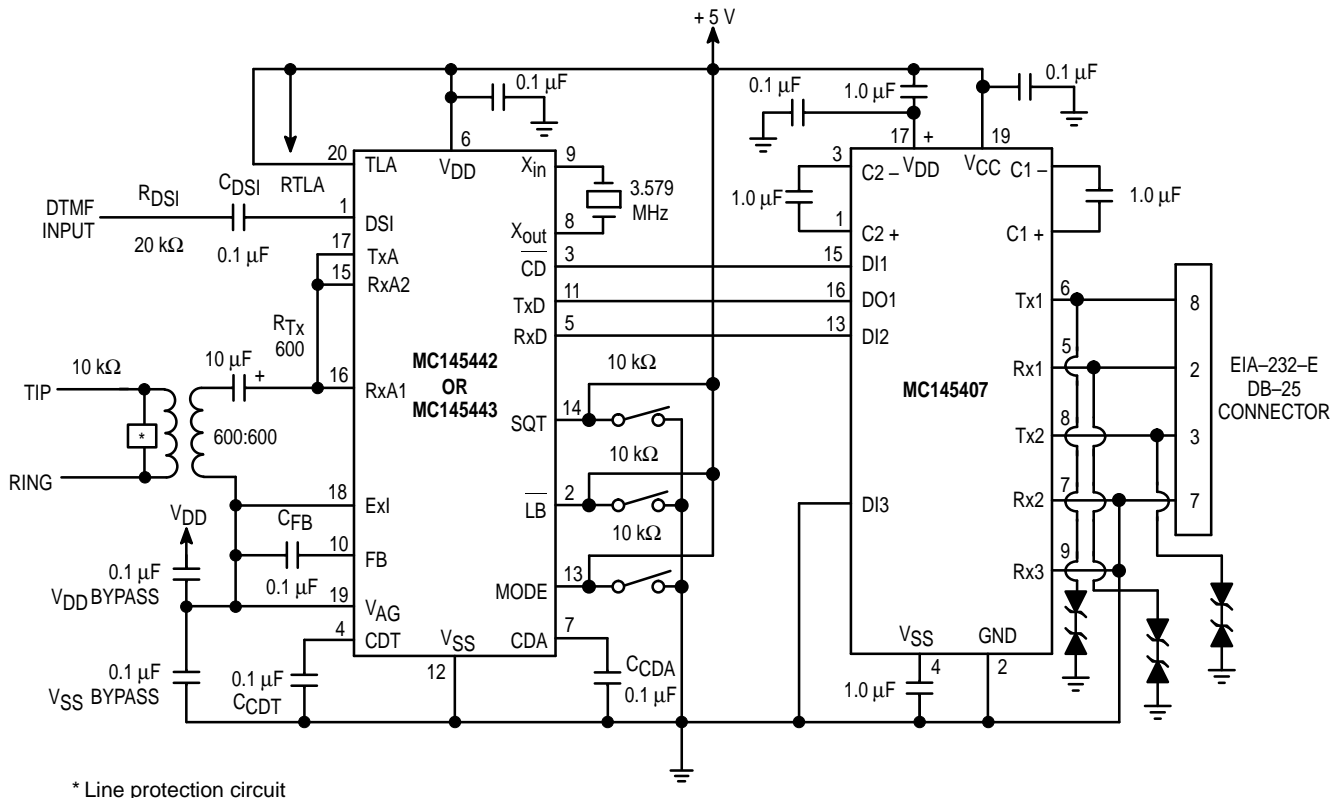


Figure 4. 5 V, 300 Baud Modem with EIA-232-E Interface

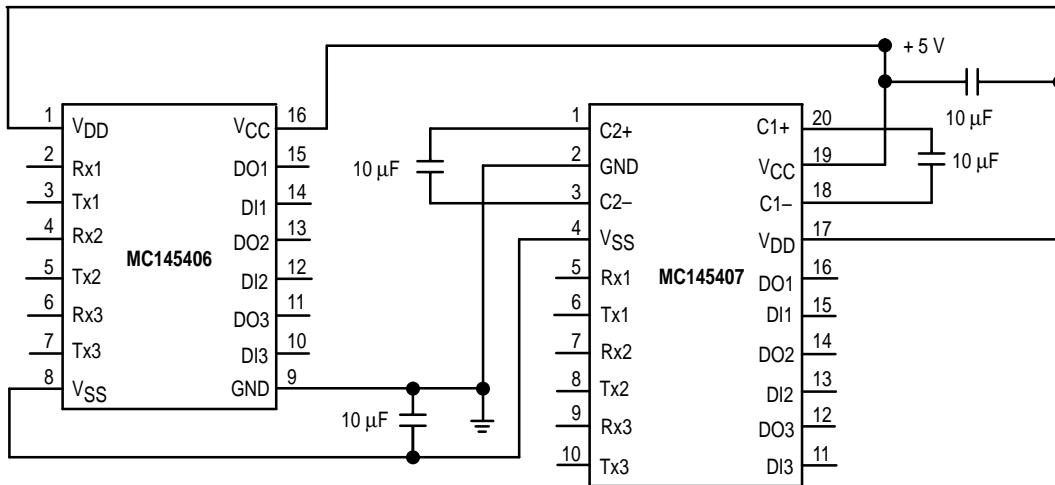


Figure 5. MC145406/MC145407 5 V Only Solution for up to Six EIA-232-E Drivers and Receivers

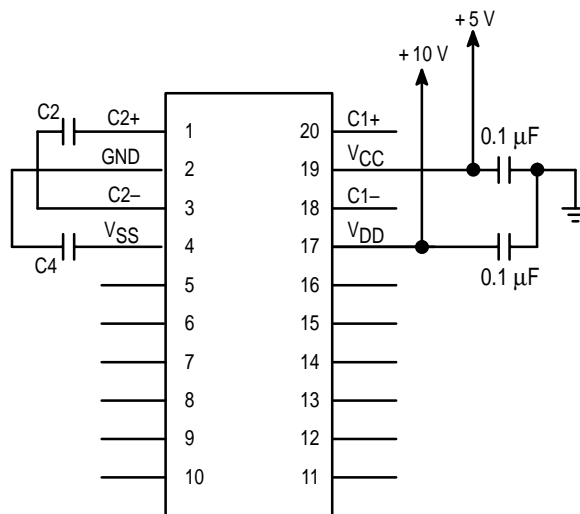


Figure 6. Two Supply Configuration (MC145407 Generates VSS Only)

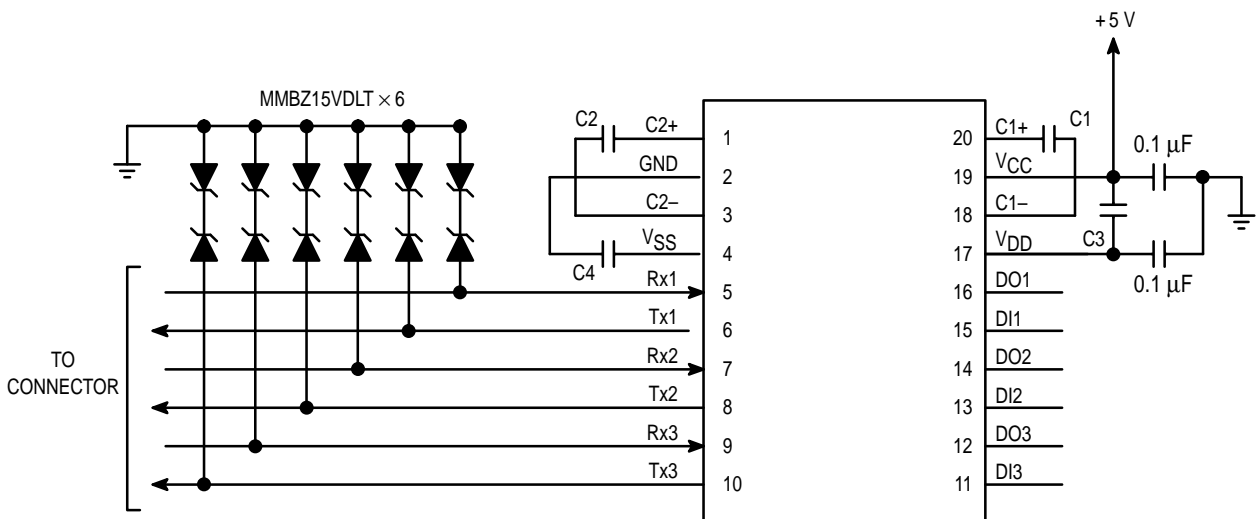
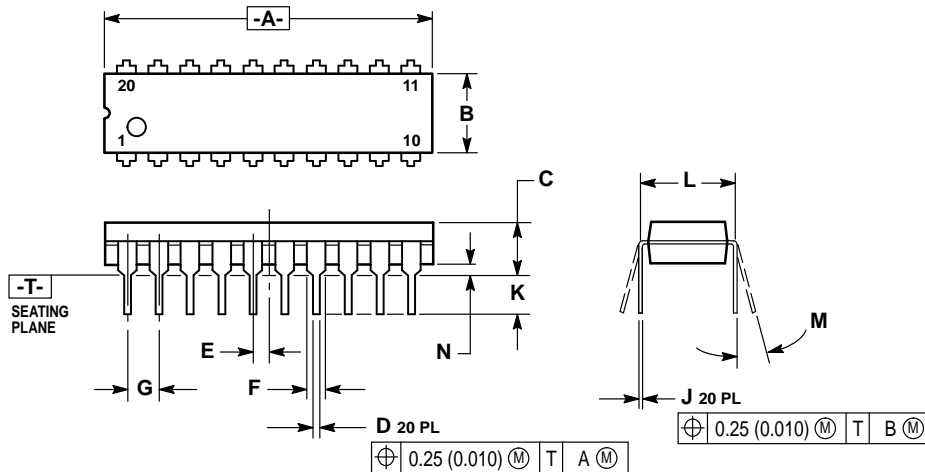


Figure 7. ESD Protection Scheme

PACKAGE DIMENSIONS

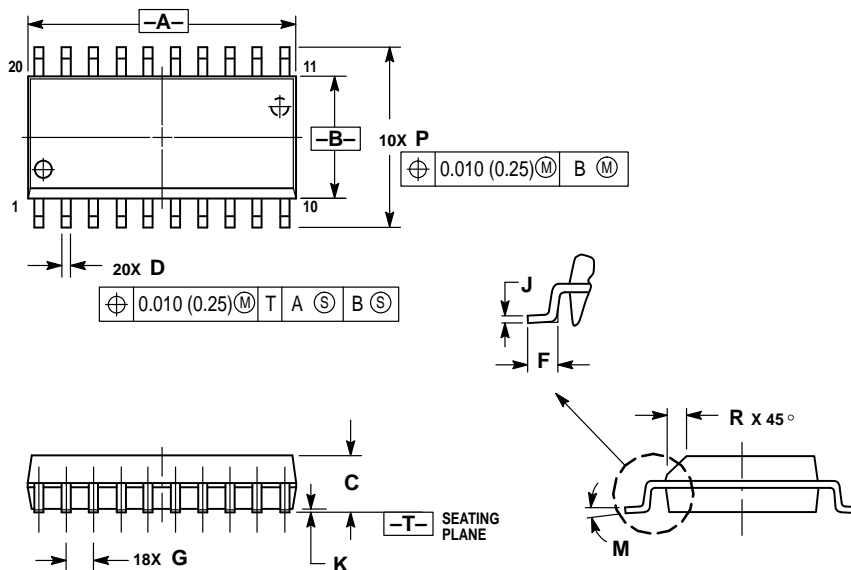
P SUFFIX PLASTIC DIP CASE 738-03



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

DW SUFFIX SOG PACKAGE CASE 751D-04



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.
 - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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MC145407/D

