PRELIMINARY **CY62148**

512K x 8 Static RAM

Features

- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 660 mW (max.)**
- **Low standby power (L version)**
  - **— 2.75 mW (max.)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with CE and OE options**

Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 99% when deselected.

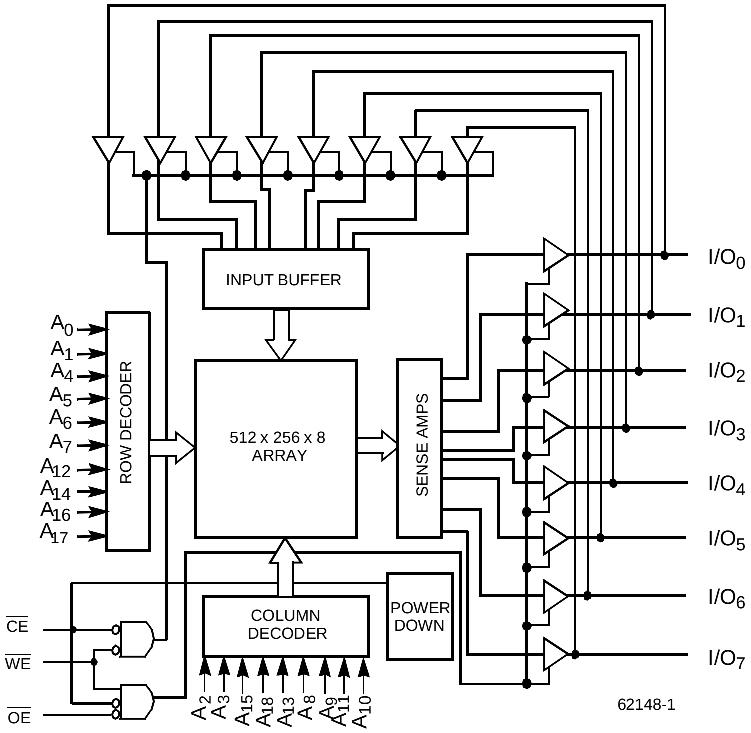
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A$_0$ through A$_{18}$).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY62148 is available in a standard 32 pin 450-mil-wide body width SOIC and 32 pin TSOP II packages.

Logic Block Diagram



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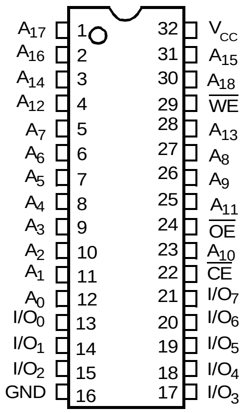
Pin Configuration

Top View
SOIC
TSOP II



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June 30, 1998

Selection Guide

			CY62148–55	CY62148–70	CY62148–100
Maximum Access Time (ns)			55	70	100
Maximum Operating Current			120	120	120
		L	90	90	90
		LL	90	90	90
Maximum CMOS Standby Current			2 mA	2 mA	2 mA
		L	100 µA	100 µA	100 µA
	Commercial	LL	20 µA	20 µA	20 µA
	Industrial	LL	40 µA	40 µA	40 µA

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied ....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND........ –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State[1]....................................–0.5V to V_{CC} +0.5V

DC Input Voltage[1].................................–0.5V to V_{CC} +0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage...2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Typ.[3]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 1mA			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1mA					0.4	V
V_{IH}	Input HIGH Voltage				2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]				–0.3		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} + 0 mA, f = f_{MAX} = 1/t_{RC}					120	mA
				L			90	mA
				LL			90	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}					15	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0				1.6 µA	2	mA
				L		1.6	100	µA
			Com'l	LL		1.6	20	µA
			Ind'l	LL		1.6	40	µA

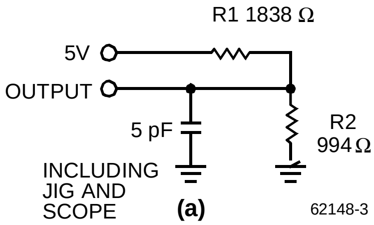
Notes:

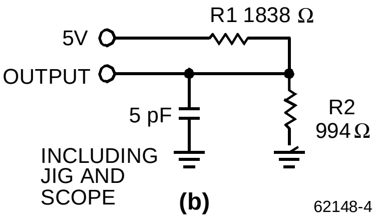
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Typical values are measured at V_{CC} = 5V, T_A = 25°C, and are included for reference only and are not tested or guaranteed.

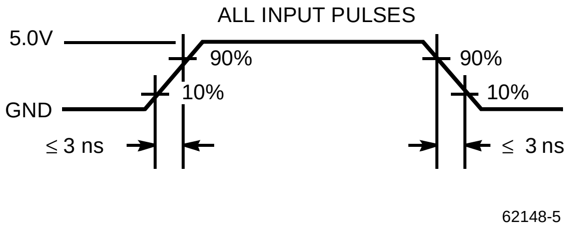
Capacitance[4]

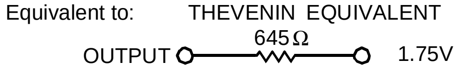
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms









Switching Characteristics[5] Over the Operating Range

Parameter	Description	62148–55		62148–70		62148–100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	55		70		100		ns
t_{AA}	Address to Data Valid		55		70		100	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70		100	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		20		35		50	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z[7]	5		5		5		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[6, 7]		20		25		30	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[7]	10		10		10		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[6, 7]		20		25		30	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70		100	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	55		70		100		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	45		60		80		ns
t_{AW}	Address Set-Up to Write End	45		60		80		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	45		55		60		ns
t_{SD}	Data Set-Up to Write End	25		25		25		ns

Notes:

4. Tested initially and after any design or process changes that may affect these parameters.
5. Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}_1$ LOW, and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

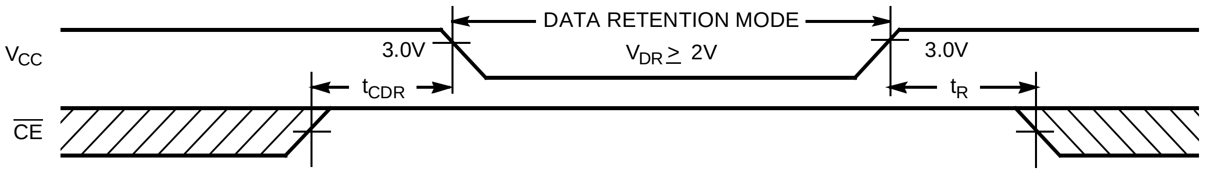
Switching Characteristics[5] Over the Operating Range (continued)

Parameter	Description	62148–55		62148–70		62148–100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		20		25		30	ns

Data Retention Characteristics (Over the Operating Range)

Parameter	Description			Conditions	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention				2.0			V
I_{CCDR}	Data Retention Current	Com'l		No input may exceed V_{CC} + 0.3V $V_{CC} = V_{DR} = 3.0V$ $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} > V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		1.6 µA	1.7	mA
			L				80	µA
			LL				20	µA
		Ind'l	LL				40	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time				0			ns
t_R	Operation Recovery Time				t_{RC}			ns

Data Retention Waveform



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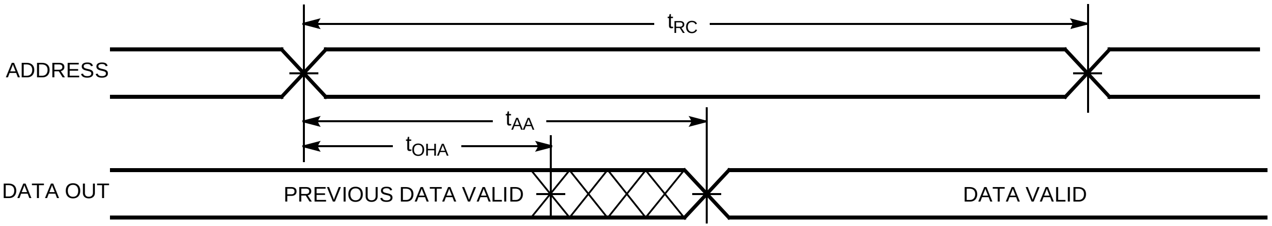
Switching Waveforms

Read Cycle No.1[9, 10]



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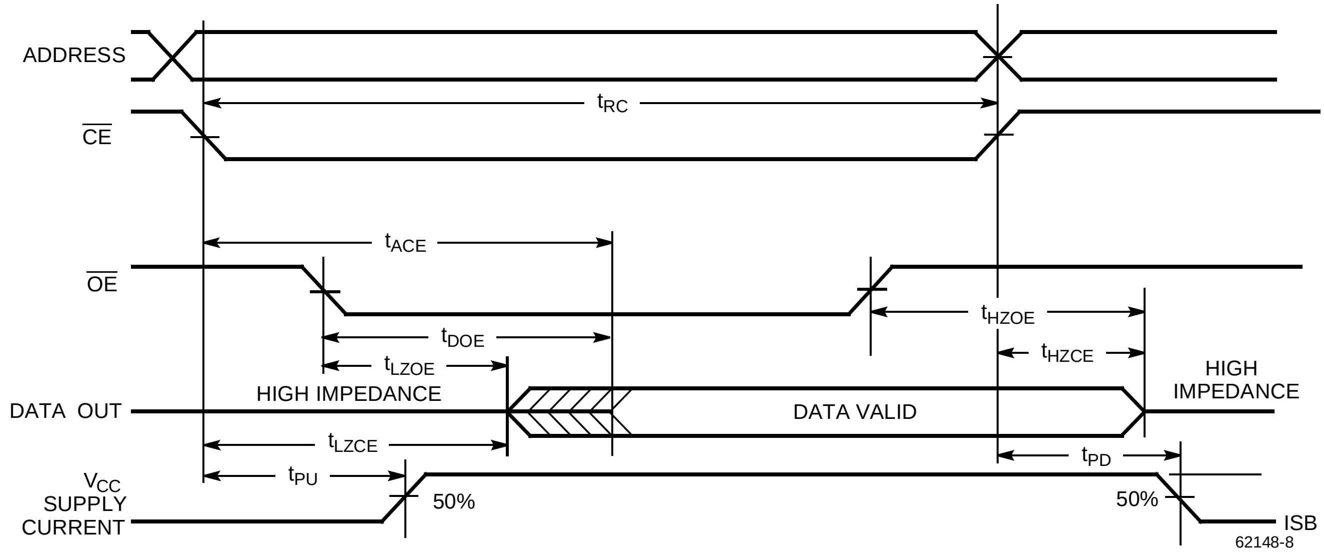
Notes:

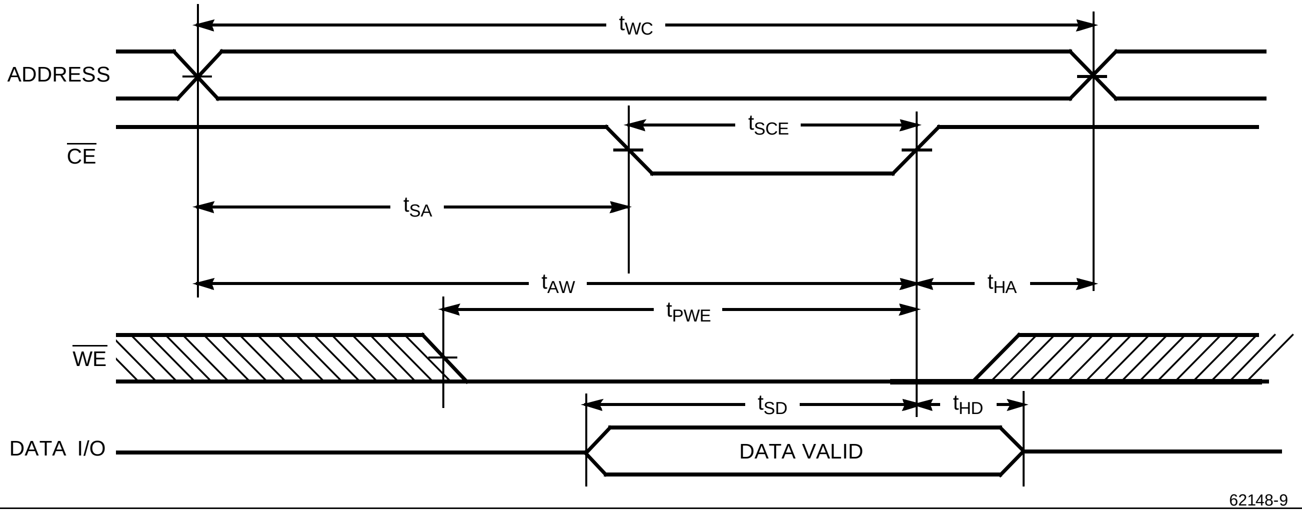
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (OE Controlled)[10, 11]



Write Cycle No. 1 (CE Controlled)[12, 13]

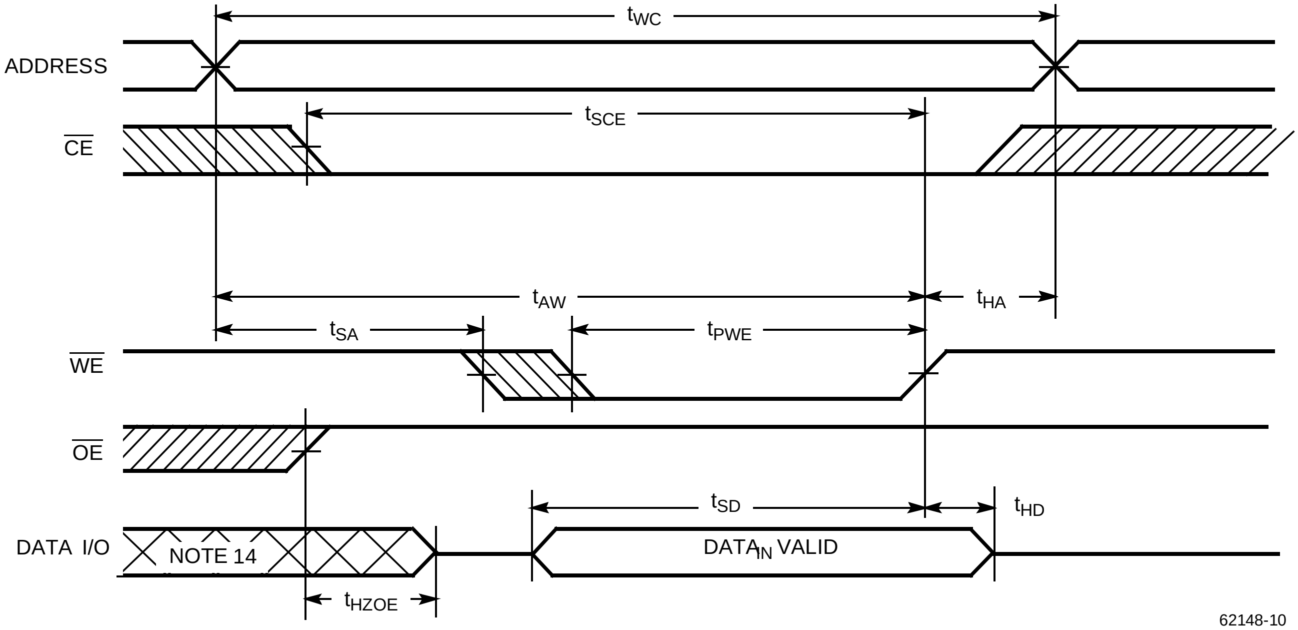


Notes:

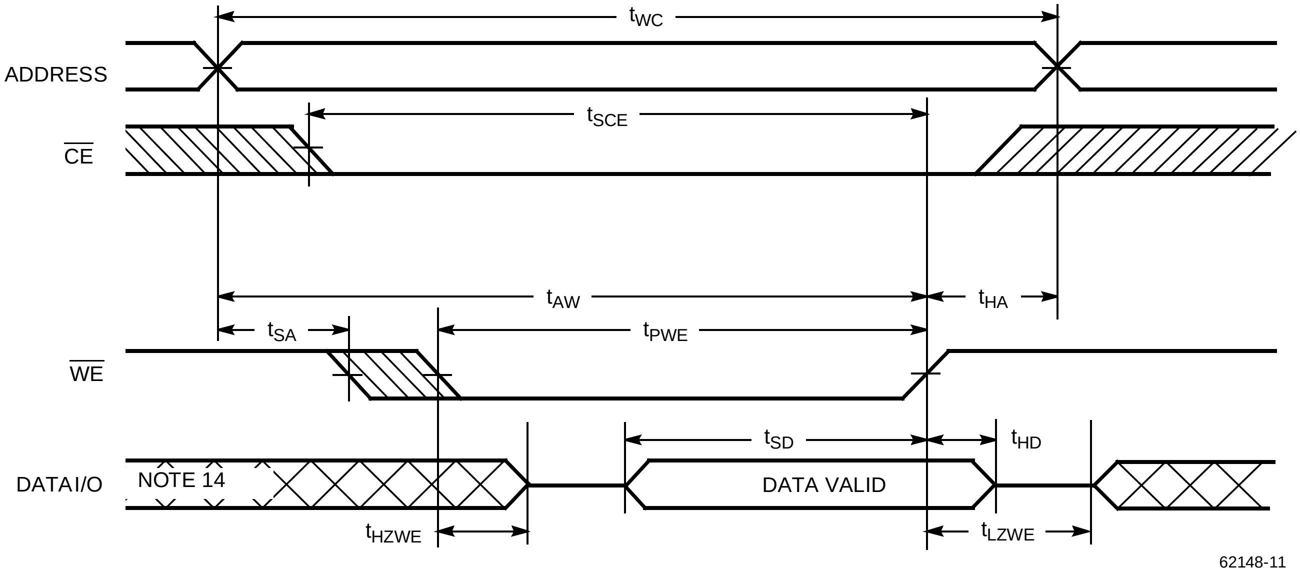
11. Address valid prior to or coincident with CE transition LOW.
12. Data I/O is high-impedance if OE = V_{IH}.
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[12, 13]



Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[12, 13]



Note:

14. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	**$I/O_0 – I/O_7$**	**Mode**	**Power**
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Standby (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	**Ordering Code**	**Package Name**	**Package Type**	**Operating Range**
70	CY62148-70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY62148-70ZSC	ZS32	32-Lead TSOP II	
	CY62148L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSC	ZS32	32-Lead TSOP II	
	CY62148LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSC	ZS32	32-Lead TSOP II	
	CY62148-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
	CY62148-70ZSI	ZS32	32-Lead TSOP II	
	CY62148L-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSI	ZS32	32-Lead TSOP II	
	CY62148LL-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSI	ZS32	32-Lead TSOP II	
100	CY62148-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148-100ZSC	ZS32	32-Lead TSOP II	
	CY62148L-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSC	ZS32	32-Lead TSOP II	
	CY62148LL-100ZSC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSC	ZS32	32-Lead TSOP II	
	CY62148-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148-100ZSI	ZS32	32-Lead TSOP II	
	CY62148L-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSI	ZS32	32-Lead TSOP II	
	CY62148LL-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSI	ZS32	32-Lead TSOP II	

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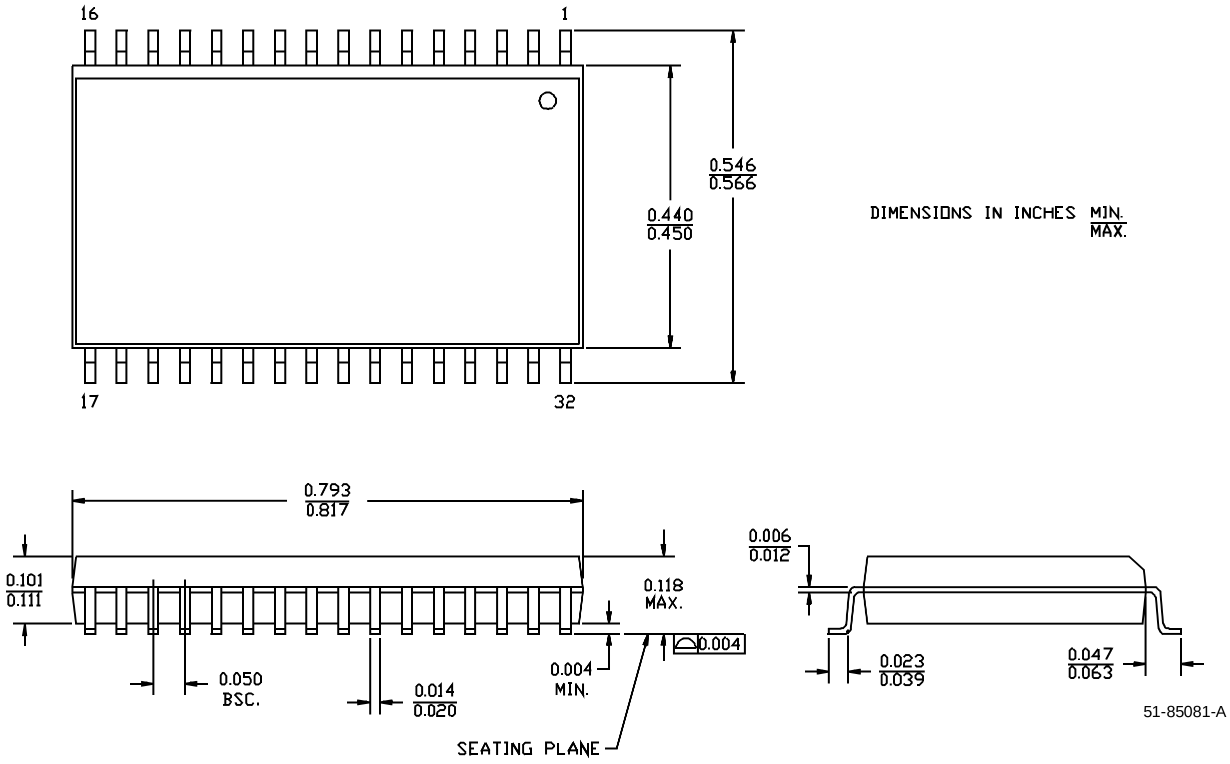
Package Diagrams

32-Lead (450 MIL) Molded SOIC S34



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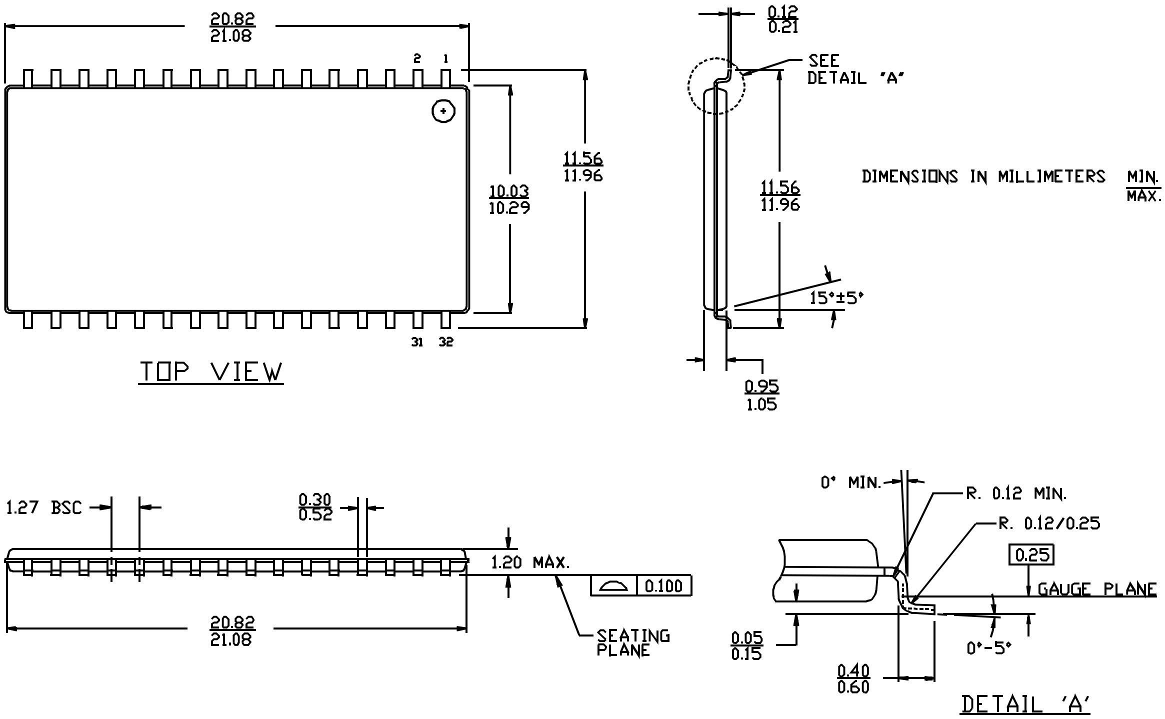
Package Diagrams (continued)

32-Lead TSOP II ZS32



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