

# MPEG Clock Generator with VCXO

## Features

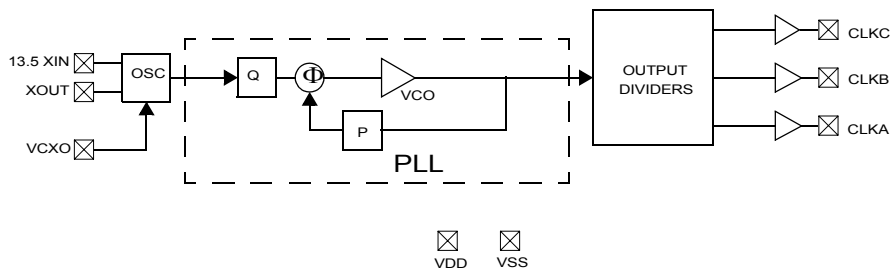
- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation
- 8-pin SOIC package

## Benefits

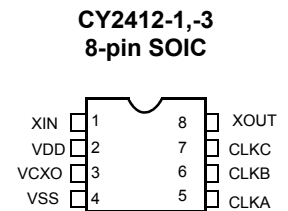
- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large  $\pm 150$ -ppm range, better linearity
- Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Profile
CY2412-1	3	13.5-MHz pullable crystal input per Cypress specification	Two 27 MHz outputs, one 54 MHz (3.3V)	Linear
CY2412-3	3	13.5-MHz pullable crystal input per Cypress specification	27 MHz, 13.5 MHz, 54 MHz (3.3V)	Linear

## Logic Block Diagram



## Pin Configuration



**Pin Summary**

Pin Name	Pin Number	Pin Description
X <sub>IN</sub>	1	Reference Crystal Input
V <sub>DD</sub>	2	Voltage Supply
VCXO	3	Input Analog Control for VCXO
V <sub>SS</sub>	4	Ground
CLKA	5	54-MHz clock output
CLKB	6	13.5-MHz clock output
CLKC	7	27-MHz clock output
X <sub>OUT</sub> <sup>[2]</sup>	8	Reference Crystal Output

**Pullable Crystal Specifications<sup>[1]</sup>**

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
F <sub>NOM</sub>	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C <sub>LNOM</sub>	Nominal load capacitance		–	14	–	pF
R <sub>1</sub>	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R <sub>3</sub> /R <sub>1</sub>	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R <sub>1</sub> values are much less than the maximum spec.	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2.0	mW
F <sub>3SEPHI</sub>	Third overtone separation from 3*F <sub>NOM</sub>	High side	300	–	–	ppm
F <sub>3SEPLO</sub>	Third overtone separation from 3*F <sub>NOM</sub>	Low side	–	–	–150	ppm
C <sub>0</sub>	Crystal shunt capacitance		–	–	7	pF
C <sub>0</sub> /C <sub>1</sub>	Ratio of shunt to motional capacitance		180	–	250	
C <sub>1</sub>	Crystal motional capacitance		14.4	18	21.6	pF

**Note:**

1. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.

**Absolute Maximum Conditions**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[3]</sup>	-65	125	°C
T <sub>J</sub>	Junction Temperature	-	125	°C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electrostatic Discharge	2		kV

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage	3.14	3.3	3.47	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max. Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency		13.5		MHz
t <sub>PU</sub>	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**DC Electrical Characteristics**

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
C <sub>IN</sub>	Input Capacitance				7	pF
I <sub>IZ</sub>	Input Leakage Current			5		μA
f <sub>ΔXO</sub>	VCXO pullability range		±150			ppm
V <sub>VCXO</sub>	VCXO input range		0		V <sub>DD</sub>	V
f <sub>VBW</sub>	VCXO input bandwidth			DC to 200		kHz
I <sub>DD</sub>	Supply Current	Sum of Core and Output Current			35	mA

**AC Electrical Characteristics**

Parameter <sup>[4]</sup>	Description	Test Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V <sub>DD</sub>	45	50	55	%
ER	Rising Edge Rate	Clock Edge Rate, Measured from 20% to 80% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See <i>Figure 2</i> .	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See <i>Figure 2</i> .	0.8	1.4		V/ns
t <sub>g</sub>	Clock Jitter	Peak to Peak period jitter		100	200	ps
t <sub>10</sub>	PLL Lock Time				3	ms

**Notes:**

2. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.
3. Rated for ten years.
4. Not 100% tested.

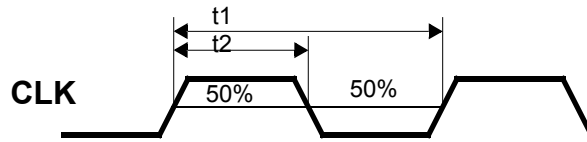


Figure 1. Duty Cycle Definition;  $DC = t2/t1$

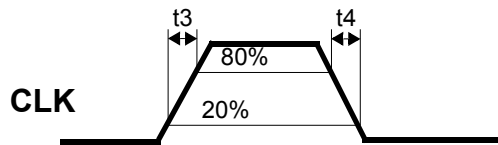
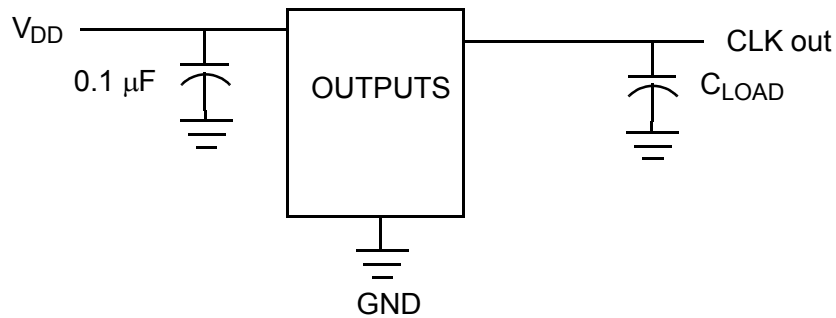


Figure 2. Rise and Fall Time Definitions:  $ER = 0.6 \times VDD / t3$  ,  $EF = 0.6 \times VDD / t4$

### Test Circuit

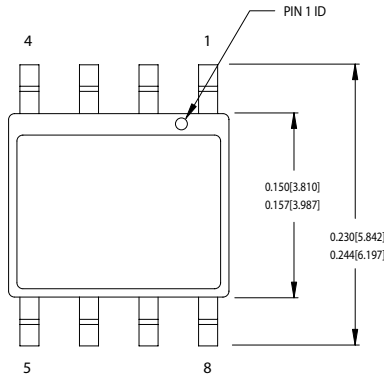


### Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY2412SC-1	8-pin SOIC	Commercial	3.3V
CY2412SC-1T	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412SC-3	8-pin SOIC	Commercial	3.3V
CY2412SC-3T	8-pin SOIC–Tape and Reel	Commercial	3.3V
<b>Lead-free</b>			
CY2412SXC-1	8-pin SOIC	Commercial	3.3V
CY2412SXC-1T	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412SXC-3	8-pin SOIC	Commercial	3.3V
CY2412SXC-3T	8-pin SOIC–Tape and Reel	Commercial	3.3V

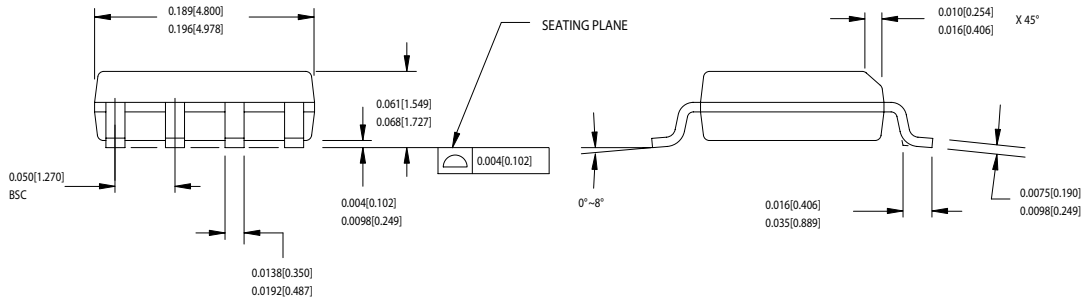
Package Diagram

8-lead (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG.
SZ08.15	LEAD FREE PKG.



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**Document History Page**

<b>Document Title: CY2412 MPEG Clock Generator with VCXO</b>				
<b>Document Number: 38-07227</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	110492	10/28/01	SZV	Change from Spec number: 38-00898 to 38-07227
*A	112457	03/14/02	CKN	Added CY2412-2 to data sheet
*B	116961	08/06/02	CKN	Removed CY2412-2 from the datasheet. Added CY2412-3 to data sheet
*C	121879	12/14/02	RBI	Power-up requirements added to Operating Conditions Information
*D	299735	See ECN	RGL	Added lead-free for CY2412-1 and CY2412-3 devices