



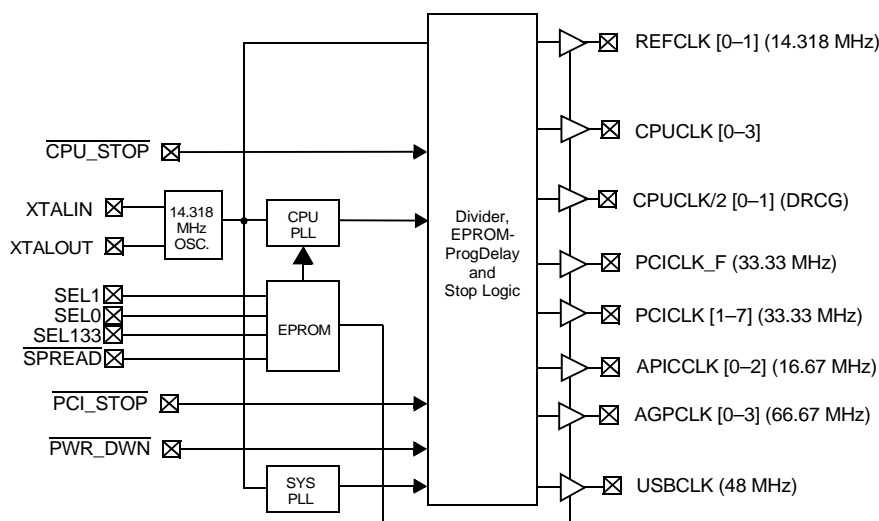
CYPRESS

CY2210

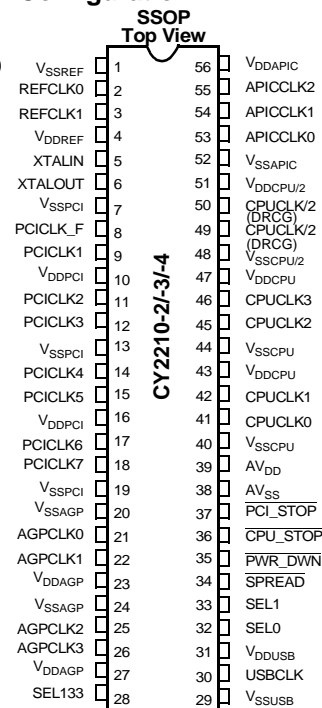
133-MHz Spread Spectrum Clock Synthesizer/Driver with AGP, USB, and DRCG Support

| Features | Benefits |
|---|---|
| <ul style="list-style-type: none"> Mixed 2.5V and 3.3V Operation Compliant to Intel® CK133 (CY2210-3) & CK133W (CY2210-2) synthesizer and driver specification | Usable with Pentium® II and Pentium® III processors |
| <ul style="list-style-type: none"> Multiple output clocks at different frequencies <ul style="list-style-type: none"> Four CPU clocks, up to 133 MHz Eight synchronous PCI clocks, 1 free-running Two CPU/2 clocks, at one-half the CPU frequency Four AGP clocks at 66 MHz Three synchronous APIC clocks, at 16.67 MHz One USB clock at 48 MHz Two reference clocks at 14.318 MHz | Single-chip main motherboard clock generator <ul style="list-style-type: none"> Driven together, support 4 CPUs and a chipset Support for 4 PCI slots and chipset Drives up to two main memory clock generators, including DRCG (CPUCLK/2) Support for multiple AGP slots Support multiprocessing systems Supports USB frequencies and I/O chip |
| <ul style="list-style-type: none"> Spread Spectrum clocking <ul style="list-style-type: none"> 32.5-kHz modulation frequency @ 133 MHz 33.1-kHz modulation frequency @ 100 MHz for CY2210-02/03 33.4-kHz modulation frequency @ 100 MHz for CY2210-04 EPROM programmable percentage of spreading. Default is -0.6%, which is recommended by Intel | Enables reduction of EMI in some systems |
| <ul style="list-style-type: none"> Power-down features | Supports mobile systems |
| <ul style="list-style-type: none"> Three Select inputs | Supports up to eight CPU clock frequencies |
| <ul style="list-style-type: none"> Low-skew and low-jitter outputs | Meets tight system timing requirements at high frequency |
| <ul style="list-style-type: none"> OE and Test Mode support | Enables ATE and "bed of nails" testing |
| <ul style="list-style-type: none"> 56-pin SSOP package | Widely available, standard package enables lower cost |

Logic Block Diagram



Pin Configuration



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Pin Summary

| Name | Pins | Description |
|-------------------------------|---------------------------|---|
| V _{SSREF} | 1 | 3.3V Reference ground |
| V _{DDREF} | 4 | 3.3V Reference voltage supply |
| V _{SSPCI} | 7, 13, 19 | 3.3V PCI ground |
| V _{DDPCI} | 10, 16 | 3.3V PCI voltage supply |
| V _{SSAGP} | 20, 24 | 3.3V AGP ground |
| V _{DDAGP} | 23, 27 | 3.3V AGP voltage supply |
| V _{SSUSB} | 29 | 3.3V USB ground |
| V _{DDUSB} | 31 | 3.3V USB voltage supply |
| V _{SSCPU} | 40, 44 | 2.5V CPU ground |
| V _{DDCPU} | 43, 47 | 2.5V CPU voltage supply |
| V _{SSCPU/2} | 48 | 2.5V CPU/2 ground |
| V _{DDCPU/2} | 51 | 2.5V CPU/2 voltage supply |
| V _{SSAPIC} | 52 | 2.5V APIC ground |
| V _{DDAPIC} | 56 | 2.5V APIC voltage supply |
| A _{VSS} | 38 | Analog ground to PLL and Core |
| A _{VDD} | 39 | Analog voltage supply to PLL and Core |
| XTALIN ^[1] | 5 | Reference crystal input |
| XTALOUT ^[1] | 6 | Reference crystal feedback |
| CPUCLK [0–3] | 41, 42, 45, 46 | CPU clock outputs |
| PCICLK [1–7] | 9, 11, 12, 14, 15, 17, 18 | PCI clock outputs, synchronously running at 33.33 MHz |
| PCICLK_F | 8 | Free running PCI clock |
| CPUCLK/2 | 49, 50 | CPU/2 clock outputs, drive memory clock generator |
| AGPCLK [0–3] | 21, 22, 25, 26 | AGP clock outputs, running at 66.66 MHz |
| APICCLK [0–2] | 53, 54, 55 | APIC clock outputs, running at 16.67 MHz |
| REFCLK [0–1] | 2, 3 | Reference clock outputs, 14.318 MHz |
| USBCLK | 30 | 48-MHz USB clock output |
| $\overline{\text{CPU_STOP}}$ | 36 | Active LOW input, disables CPU and AGP clocks when asserted |
| $\overline{\text{PCI_STOP}}$ | 37 | Active LOW input, disables PCI clocks when asserted |
| $\overline{\text{PWR_DWN}}$ | 35 | Active LOW input, powers down part when asserted |
| $\overline{\text{SPREAD}}$ | 34 | Active LOW input, enables spread spectrum when asserted |
| SEL1 | 33 | CPU frequency select input (See Function Table) |
| SEL0 | 32 | CPU frequency select input (See Function Table) |
| SEL133 | 28 | CPU frequency select input (See Function Table) |

Note:

- For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the application note, "Crystal Oscillator Topics."

Function Table^[2]

| SEL133 | SEL1 | SEL0 | CPUCLK (MHz) | CPUCLK/2 (MHz) | AGPCLK (MHz) | PCICLK (MHz) | USBCLK (MHz) | REFCLK (MHz) | APICCLK (MHz) |
|--------|------|------|------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 0 | 0 | 1 | 100.227 ^[3] | 50.114 ^[3] | 66.818 ^[3] | 33.409 ^[3] | 48.008 ^[3] | 14.318 ^[3] | 16.705 ^[3] |
| 0 | 1 | 0 | 100 | 50 | 66.67 | 33.33 | OFF | 14.318 | 16.67 |
| 0 | 1 | 1 | 100 | 50 | 66.67 | 33.33 | 48 | 14.318 | 16.67 |
| 1 | 0 | 0 | TCLK/2 | TCLK/4 | TCLK/4 | TCLK/8 | TCLK/2 | TCLK | TCLK/16 |
| 1 | 0 | 1 | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| 1 | 1 | 0 | 133.33 | 66.67 | 66.67 | 33.33 | OFF | 14.318 | 16.67 |
| 1 | 1 | 1 | 133.33 | 66.67 | 66.67 | 33.33 | 48 | 14.318 | 16.67 |

Actual Clock Frequency Values

| Clock Output | Target Frequency (MHz) | | | Actual Frequency (MHz) | | | PPM | | |
|--------------|------------------------|--------|--------|------------------------|---------|---------|-------|-------|-------|
| | -2 | -3 | -4 | -2 | -3 | -4 | -2 | -3 | -4 |
| CPUCLK | 100.0 | 100.0 | 100.0 | 99.126 | 99.126 | 100.227 | -8740 | -8740 | +2714 |
| CPUCLK | 133.33 | 133.33 | 133.33 | 132.769 | 132.769 | 132.769 | -4208 | -4208 | -4208 |
| USBCLK | 48.0 | 48.0 | 48.0 | 48.008 | 48.008 | 48.008 | 167 | 167 | 167 |

Clock Enable Configuration

| $\overline{\text{CPU_STOP}}$ | $\overline{\text{PWR_DWN}}$ | $\overline{\text{PCI_STOP}}$ | CPUCLK | CPUCLK/2 | AGP | PCI | PCI_F | REF APIC | OSC. | VCOs |
|-------------------------------|------------------------------|-------------------------------|--------|----------|-----|-----|-------|----------|------|------|
| X | 0 | X | LOW | LOW | LOW | LOW | LOW | LOW | OFF | OFF |
| 0 | 1 | 0 | LOW | ON | LOW | LOW | ON | ON | ON | ON |
| 0 | 1 | 1 | LOW | ON | LOW | ON | ON | ON | ON | ON |
| 1 | 1 | 0 | ON | ON | ON | LOW | ON | ON | ON | ON |
| 1 | 1 | 1 | ON | ON | ON | ON | ON | ON | ON | ON |

Clock Driver Impedances

| Buffer Name | V _{DD} Range | Buffer Type | Impedance | | |
|------------------|-----------------------|-------------|------------------|------------------|------------------|
| | | | Minimum Ω | Typical Ω | Maximum Ω |
| CPU, CPU/2, APIC | 2.375–2.625 | Type 1 | 13.5 | 29 | 45 |
| USB, REF | 3.135–3.465 | Type 3 | 20 | 40 | 60 |
| PCI, AGP | 3.135–3.465 | Type 5 | 12 | 30 | 55 |

Notes:

- TCLK is a test clock driven in on the XTALIN input in test mode.
- Only CY2210-2 supports this option. In CY2210-3, this selection is defined as "N/A" or "Reserved".

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V
 Input Voltage -0.5V to $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C
 Junction Temperature +150°C
 Package Power Dissipation 1W
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) >2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

| Parameter | Description | Min. | Max. | Unit |
|--|---|--------|----------|------|
| V_{DDREF} , V_{DDPCI} , AV_{DD} , V_{DDAGP} , V_{DDUSB} | 3.3V Supply Voltages | 3.135 | 3.465 | V |
| V_{DDCPU} , $V_{DDCPU/2}$ | CPU and CPU/2 Supply Voltage | 2.375 | 2.625 | V |
| V_{DDAPIC} | APIC Supply Voltage | 2.375 | 2.625 | V |
| T_A | Operating Temperature, Ambient | 0 | 70 | °C |
| C_L | Max. Capacitive Load on CPUCLK, CPUCLK/2, USBCLK, REF, APIC PCICLK, AGP | | 20 30 | pF |
| $f_{(REF)}$ | Reference Frequency, Oscillator Nominal Value | 14.318 | 14.318 | MHz |
| t_{PU} | Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-------------|--|---|------------------|------|------|
| V_{IH} | High-level Input Voltage | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$ | 2.0 | | V |
| V_{IL} | Low-level Input Voltage | Except Crystal Pads | | 0.8 | V |
| V_{OH} | High-level Output Voltage ^[4] | CPU, CPU/2, APIC | $I_{OH} = -1$ mA | 2.0 | V |
| | | USB, REF, PCI, AGP | $I_{OH} = -1$ mA | 2.4 | |
| V_{OL} | Low-level Output Voltage ^[4] | CPU, CPU/2, APIC | $I_{OL} = 1$ mA | | 0.4 |
| | | USB, REF, PCI, AGP | $I_{OL} = 1$ mA | | 0.4 |
| I_{IH} | Input High Current | $0 \leq V_{IN} \leq V_{DD}$ | | 10 | μA |
| I_{IL} | Input Low Current | $0 \leq V_{IN} \leq V_{DD}$ | | 10 | μA |
| I_{OH} | High-level Output Current ^[4] | CPU, CPU/2 | $V_{OH} = 2.0V$ | -16 | -60 |
| | | APIC | $V_{OH} = 2.0V$ | -20 | -72 |
| | | USB, REF | $V_{OH} = 2.4V$ | -15 | -51 |
| | | AGP, PCI | $V_{OH} = 2.4V$ | -30 | -100 |
| I_{OL} | Low-level Output Current ^[4] | CPU, CPU/2 | $V_{OL} = 0.4V$ | 19 | 49 |
| | | APIC | $V_{OL} = 0.4V$ | 25 | 58 |
| | | USB, REF | $V_{OL} = 0.4V$ | 10 | 24 |
| | | AGP, PCI | $V_{OL} = 0.4V$ | 20 | 49 |
| I_{OZ} | Output Leakage Current | Three-state | | 10 | μA |
| I_{DD2} | 2.5V Power Supply Current | $AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$, $F_{CPU} = 133$ MHz | | 90 | mA |
| I_{DD3} | 3.3V Power Supply Current | $AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$, $F_{CPU} = 133$ MHz | | 160 | mA |
| I_{DDPD2} | 2.5V Shutdown Current | $AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$ | | 100 | μA |
| I_{DDPD3} | 3.3V Shutdown Current | $AV_{DD}/V_{DDQ3} = 3.465V$, $V_{DD25} = 2.625V$ | | 200 | μA |

Note:

4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics^[4, 5] Over the Operating Range

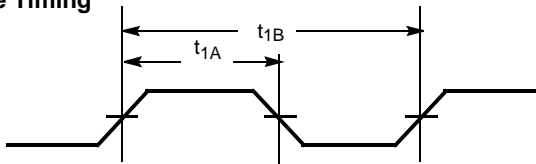
| Parameter | Output | Description | Test Conditions | Min. | Max. | Unit |
|-----------------|------------------|----------------------------------|---|------|------|------|
| t ₁ | All | Output Duty Cycle ^[6] | t _{1A} /t _{1B} | 45 | 55 | % |
| t ₂ | CPU, CPU/2, APIC | Rising Edge Rate | Between 0.4V and 2.0V | 1.0 | 4.0 | V/ns |
| t ₂ | USB, REF | Rising Edge Rate | Between 0.4V and 2.4V | 0.5 | 2.0 | V/ns |
| t ₂ | PCI, AGP | Rising Edge Rate | Between 0.4V and 2.4V | 1.0 | 4.0 | V/ns |
| t ₃ | CPU, CPU/2, APIC | Falling Edge Rate | Between 2.0V and 0.4V | 1.0 | 4.0 | V/ns |
| t ₃ | USB, REF | Falling Edge Rate | Between 2.4V and 0.4V | 0.5 | 2.0 | V/ns |
| t ₃ | PCI, AGP | Falling Edge Rate | Between 2.4V and 0.4V | 1.0 | 4.0 | V/ns |
| t ₆ | CPU | CPU-CPU Skew | Measured at 1.25V | | 175 | ps |
| t ₇ | CPU/2 | CPU/2-CPU/2 Skew | Measured at 1.25V | | 175 | ps |
| t ₈ | APIC | APIC-APIC Skew | Measured at 1.25V | | 250 | ps |
| t ₉ | AGP | AGP-AGP Skew | Measured at 1.5V | | 250 | ps |
| t ₁₀ | PCI | PCI-PCI Skew | Measured at 1.5V | | 500 | ps |
| t ₁₁ | CPU, AGP | CPU-AGP Clock Skew | CPU leads. Measured at 1.25V for 2.5V clocks and 1.5V for 3.3V clocks | 0 | 1.5 | ns |
| t ₁₂ | AGP, PCI | AGP-PCI Clock Skew | AGP leads. Measured at 1.5V | 1.5 | 4.0 | ns |
| t ₁₃ | CPU, APIC | CPU-APIC Clock Skew | CPU leads. Measured at 1.25V | 1.5 | 4 | ns |
| t ₁₄ | CPU, PCI | CPU-PCI Clock Skew | CPU leads. Measured at 1.25V clocks and 1.5V for 3.3V clocks | 1.5 | 4 | ns |
| | CPU | Cycle-Cycle Clock Jitter | With all outputs running (CY2210-2) | | 150 | ps |
| | CPU | Cycle-Cycle Clock Jitter | With all outputs running (CY2210-3/-4) | | 250 | ps |
| | CPU | Cycle-Cycle Clock Jitter | With the USB output turned off (CY2210-3/-4) | | 200 | ps |
| | CPU/2 | Cycle-Cycle Clock Jitter | | | 250 | ps |
| | APIC | Cycle-Cycle Clock Jitter | | | 500 | ps |
| | USB | Cycle-Cycle Clock Jitter | | | 500 | ps |
| | AGP | Cycle-Cycle Clock Jitter | | | 500 | ps |
| | REF | Cycle-Cycle Clock Jitter | | | 1000 | ps |
| | CPU, PCI | Settle Time | CPU and PCI clock stabilization from power-up | | 3 | ms |

Notes:

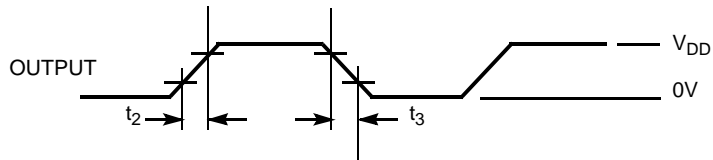
5. All parameters specified with loaded outputs.
6. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.

Switching Waveforms

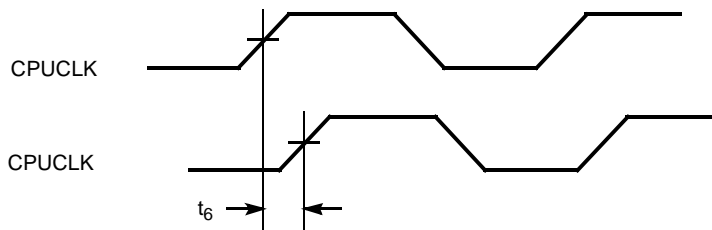
Duty Cycle Timing



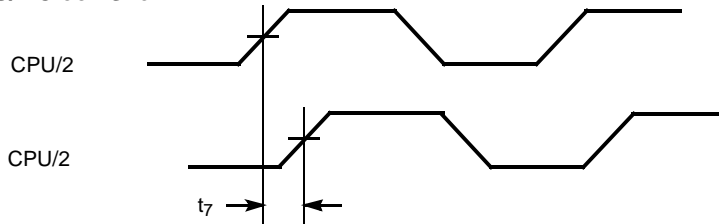
All Outputs Rise/Fall Time



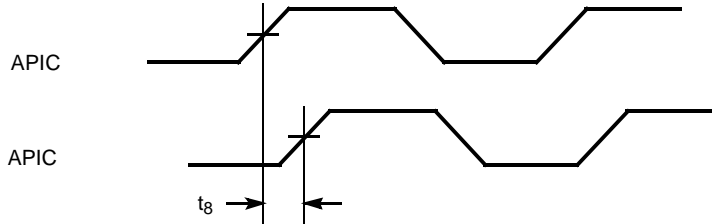
CPU-CPU Clock Skew



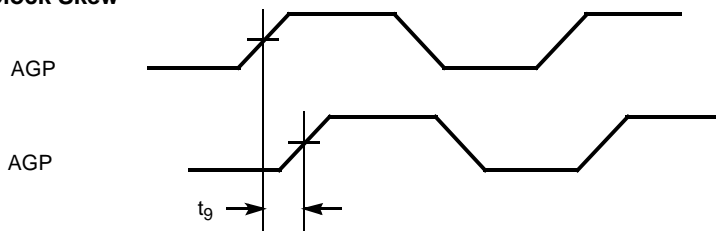
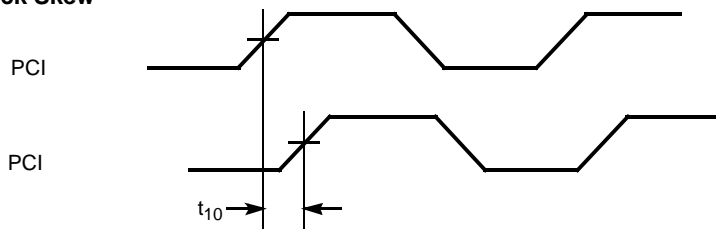
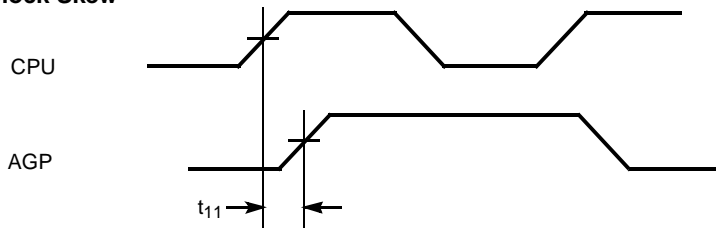
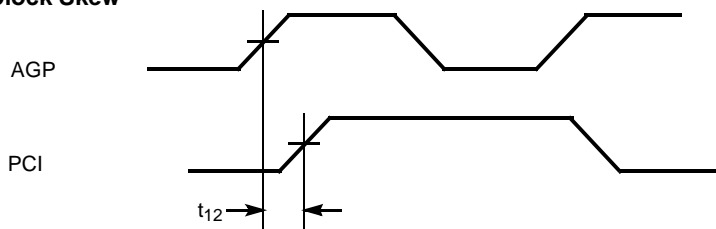
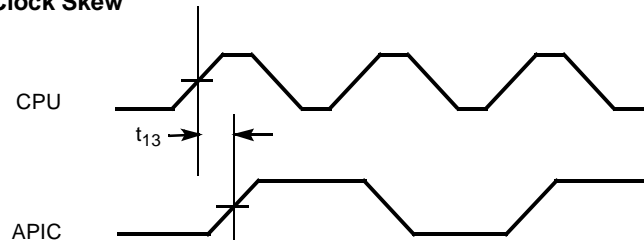
CPU/2 - CPU/2 Clock Skew



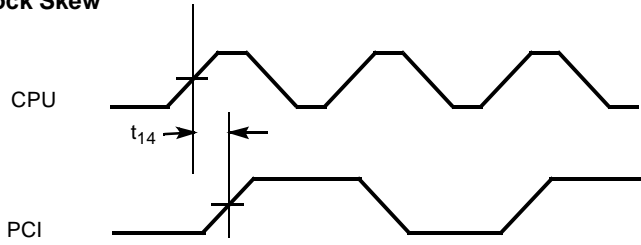
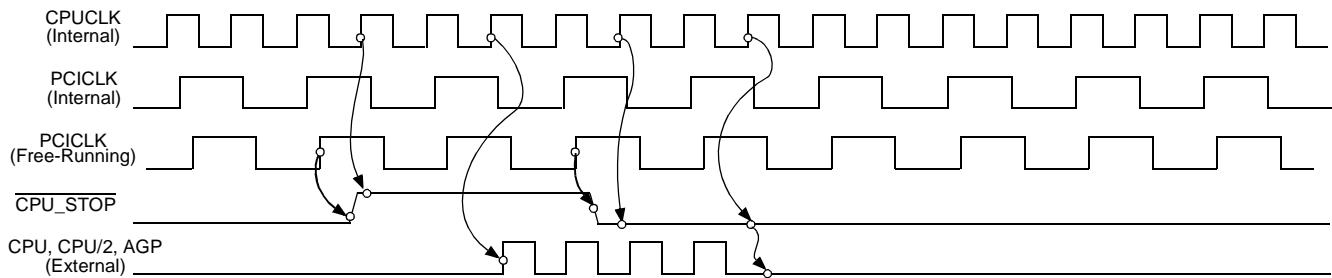
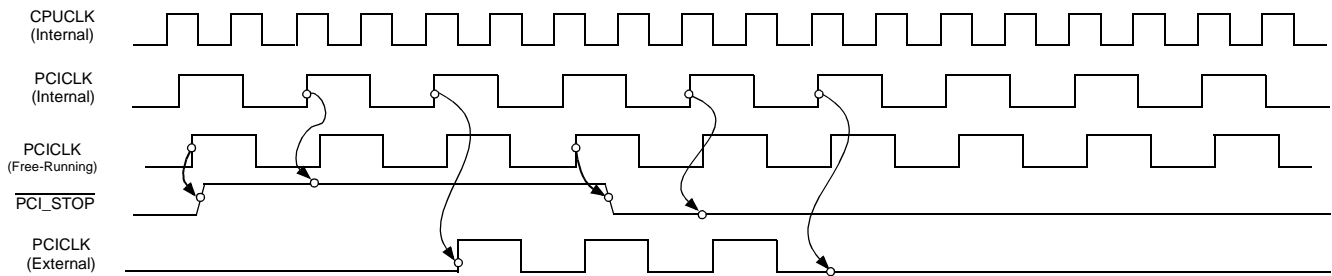
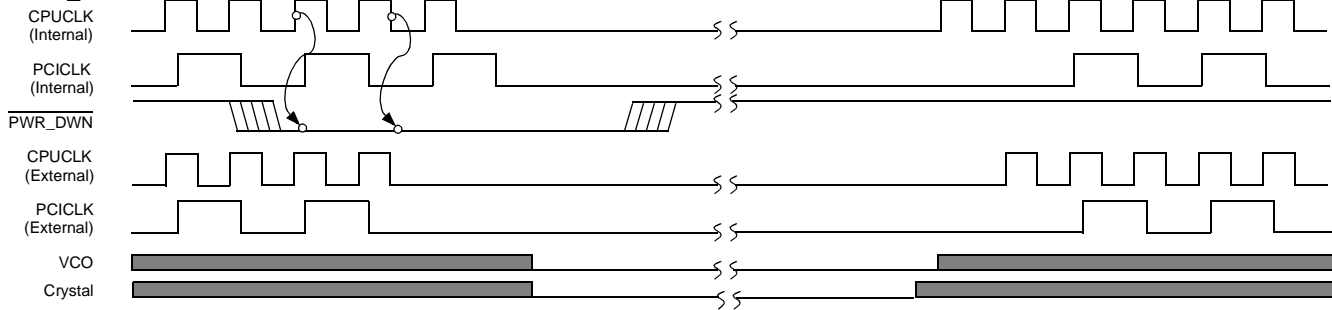
APIC-APIC Clock Skew



Switching Waveforms (continued)

AGP-AGP Clock Skew

PCI-PCI Clock Skew

CPU-AGP Clock Skew

AGP - PCI Clock Skew

CPU-APIC Clock Skew


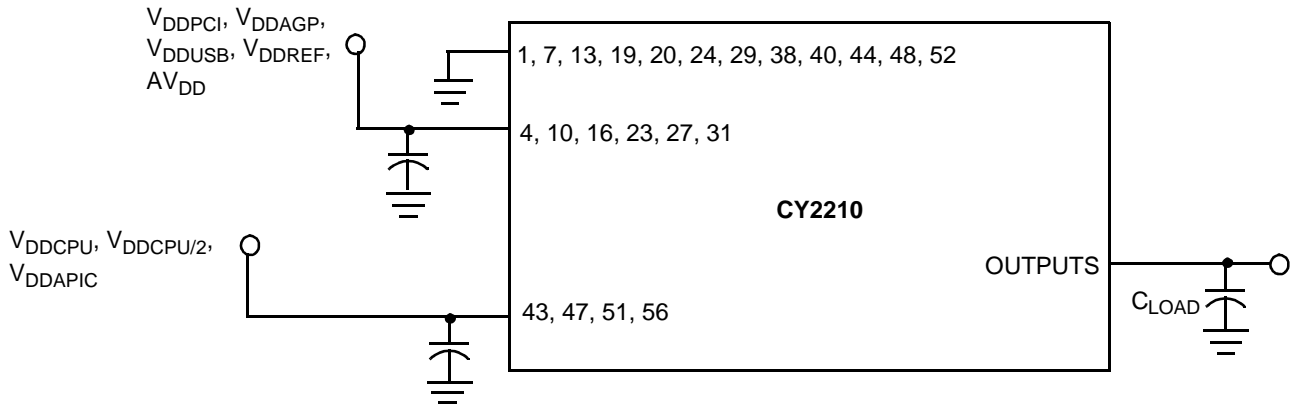
Switching Waveforms (continued)

CPU-PCI Clock Skew

CPU_STOP Timing^[7, 8]

PCI_STOP

PWR_DOWN


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Notes:

7. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
8. CPU_STOP may be applied asynchronously. It is synchronized internally.

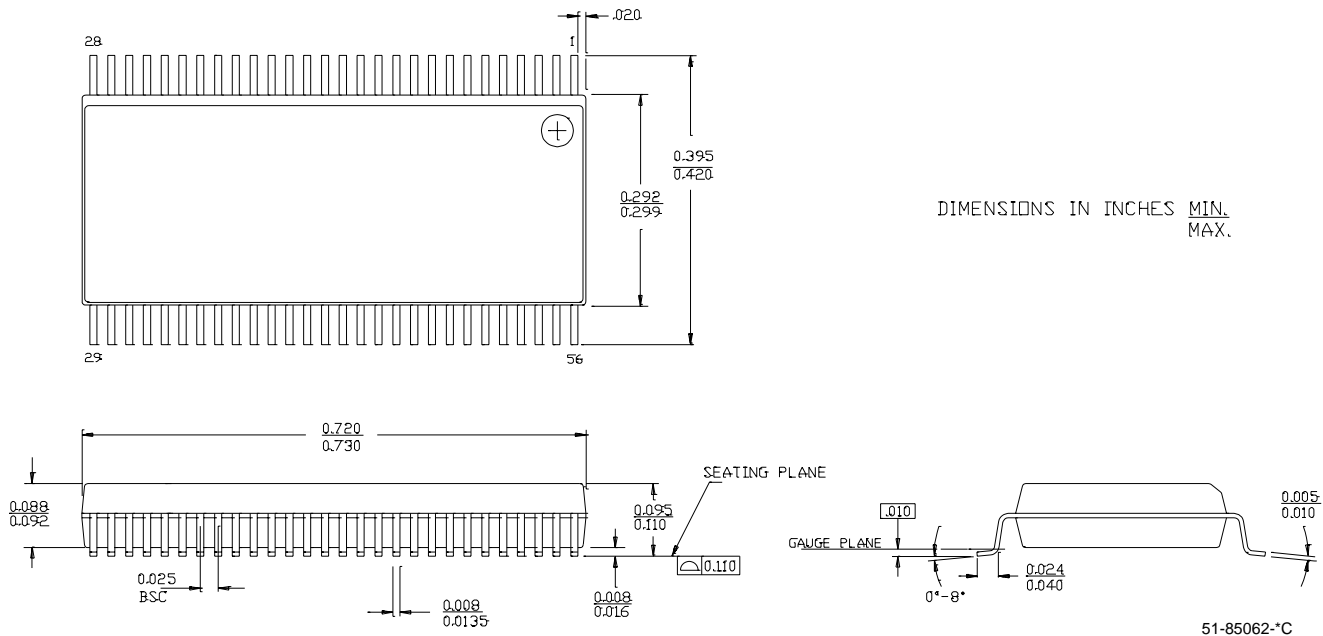
Test Circuit


Note: Each supply pin must have an individual decoupling capacitor.

Note: All capacitors must be placed as close to the pins as is physically possible.

Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|-------------------|--------------|--------------|-----------------|
| CY2210PVC-2/-3/-4 | O56 | 56-Pin SSOP | Commercial |

Package Diagram
56-Lead Shrink Small Outline Package O56


Document Title: CY2210 133-MHz Spread Spectrum Clock Synthesizer/Driver with AGP, USB, and DRCG Support
Document Number: 38-07204

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|-----------------|---|
| ** | 111724 | 01/10/02 | DSG | Change from Spec number: 38-00888 to 38-07204 |
| *A | 121839 | 12/14/02 | RBI | Power up requirements added to Operating Conditions Information |